

Introduction aux Systèmes Numériques

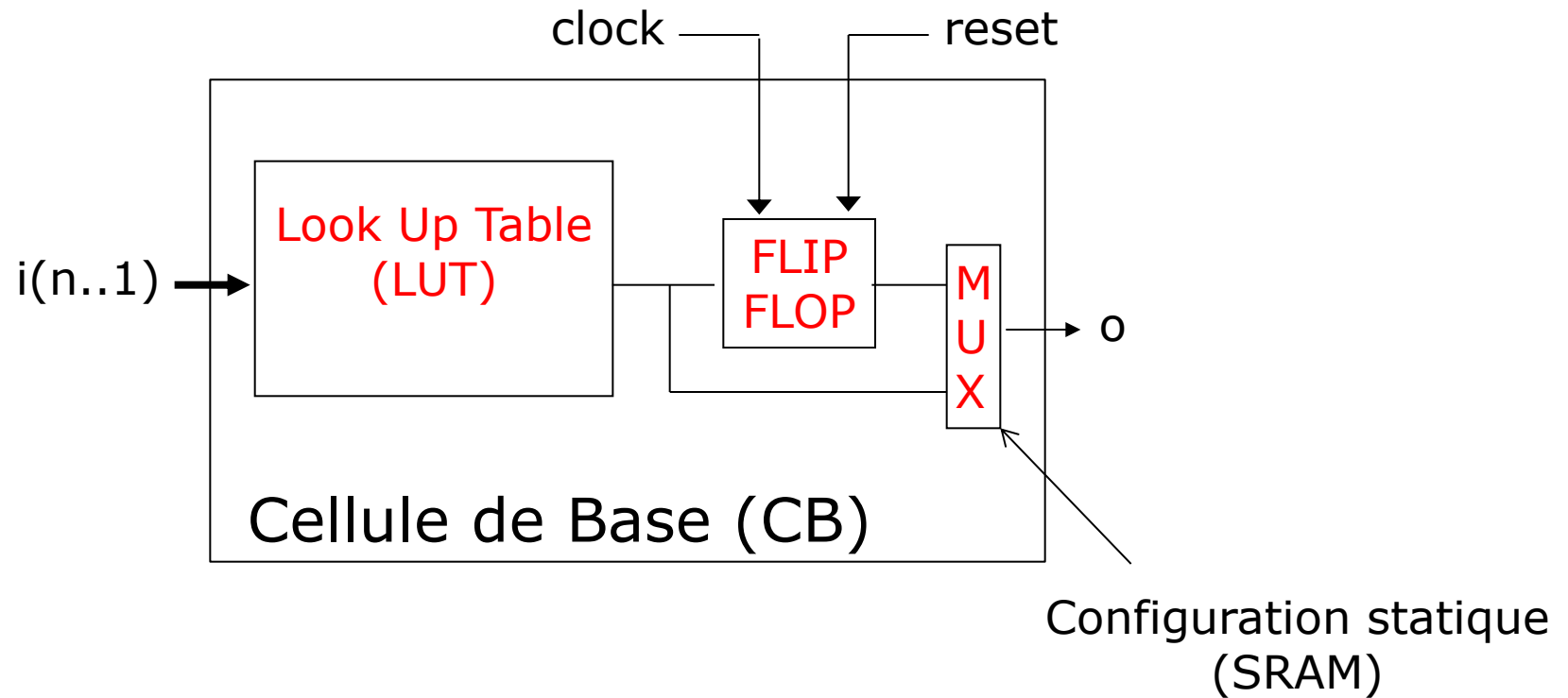
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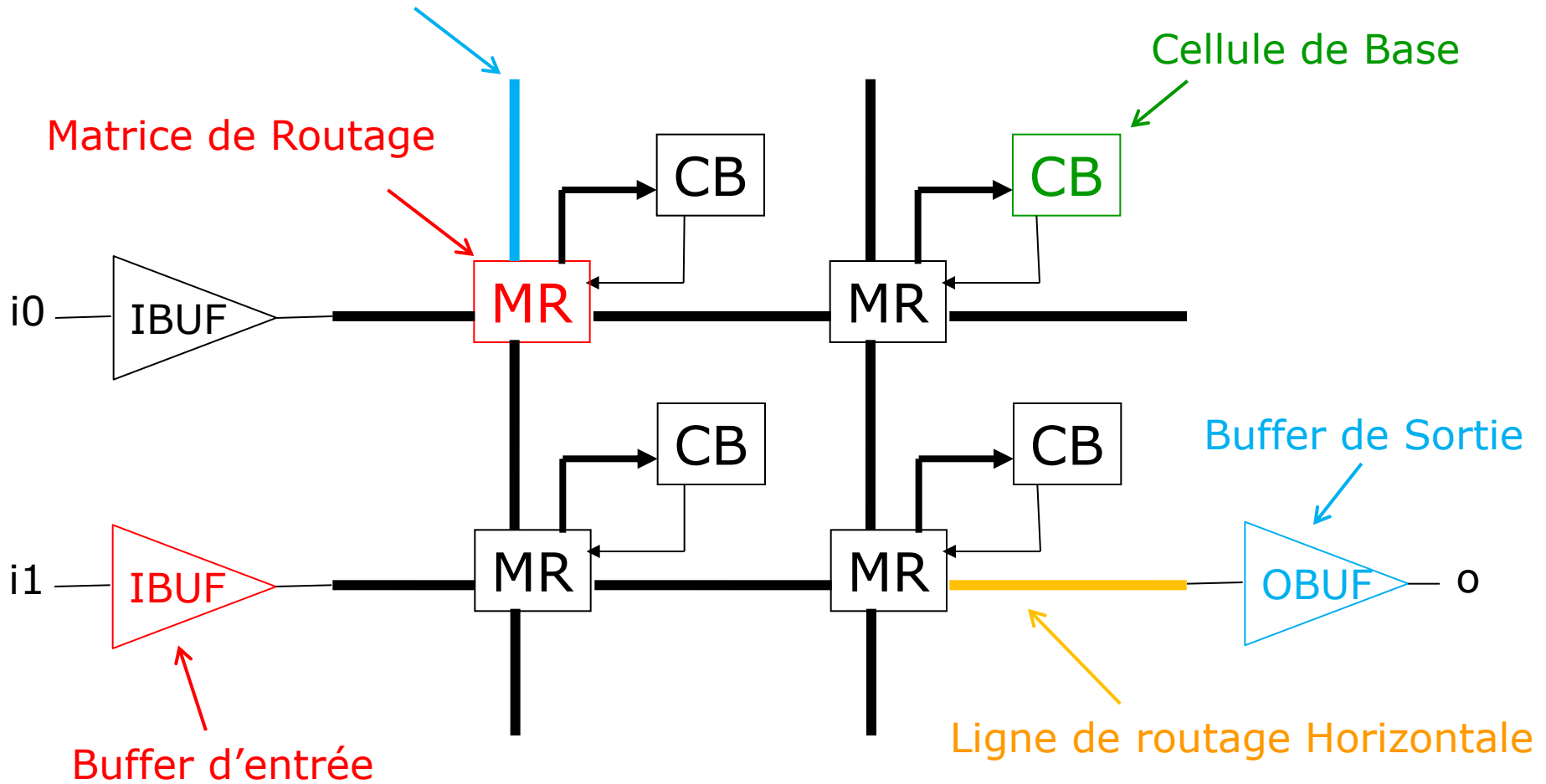
FPGA - Cellule de Base

FPGA : Field Programmable Gate Array



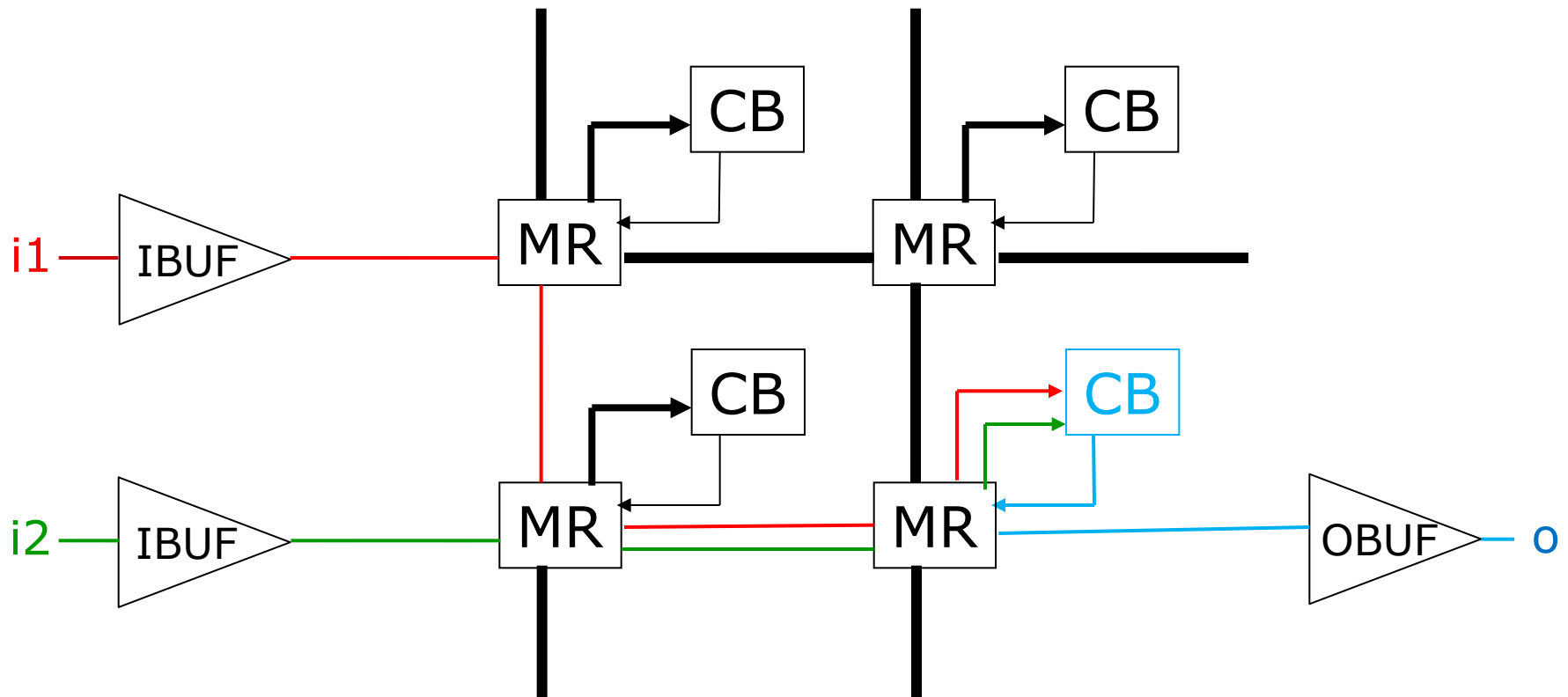
FPGA - Lego

Ligne de routage Verticale

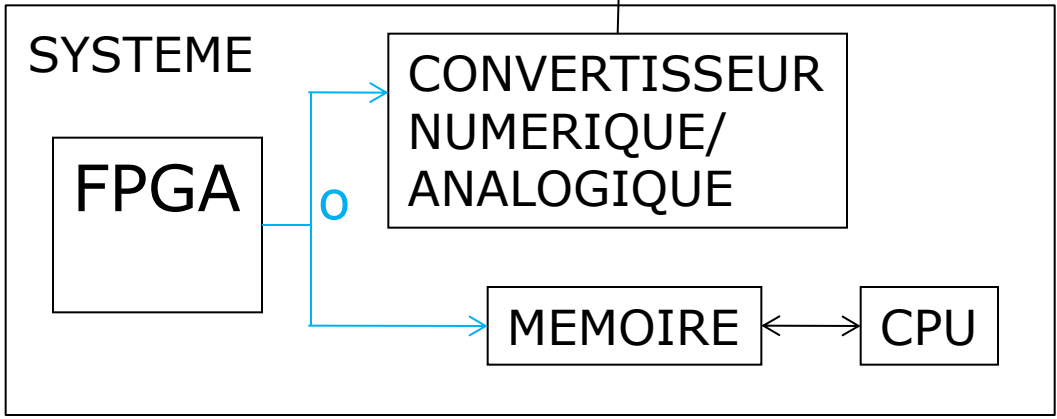
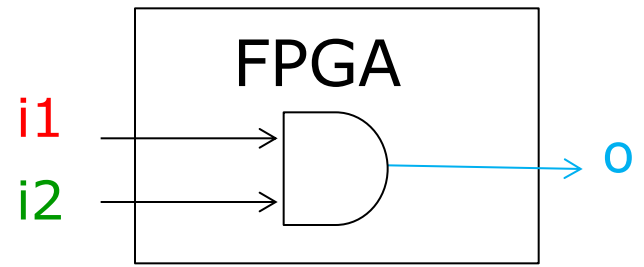
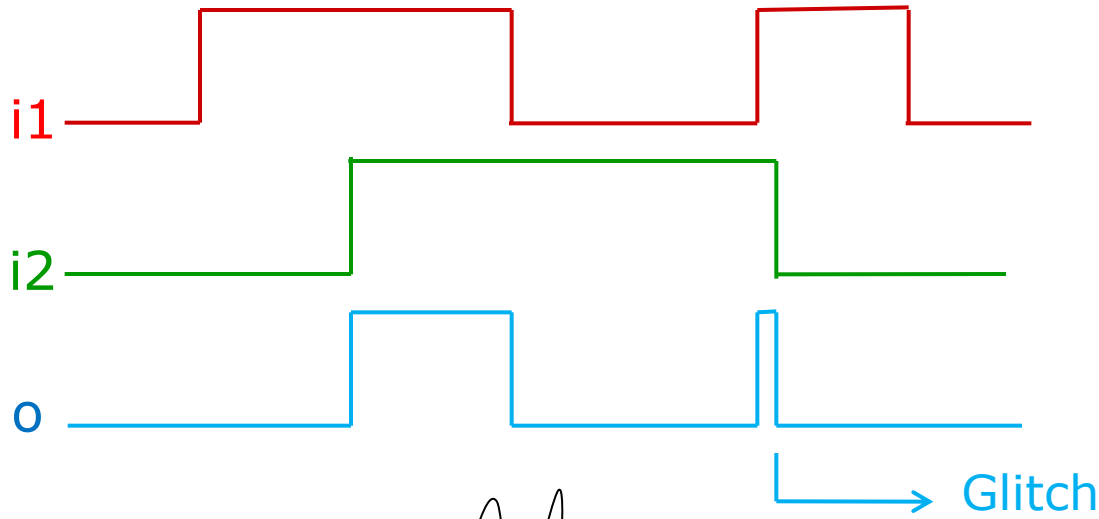


FPGA - Lego

`o <= i1 and i2;`

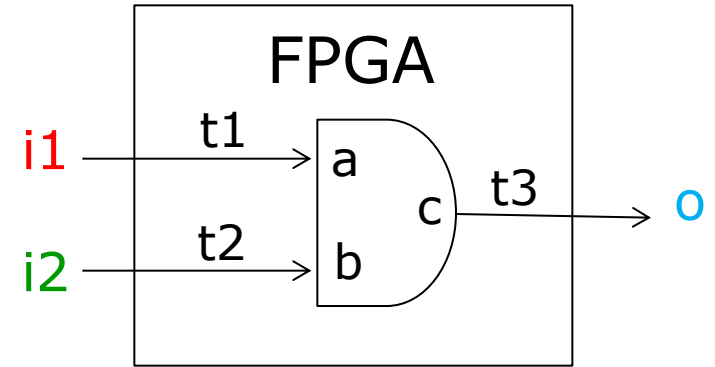
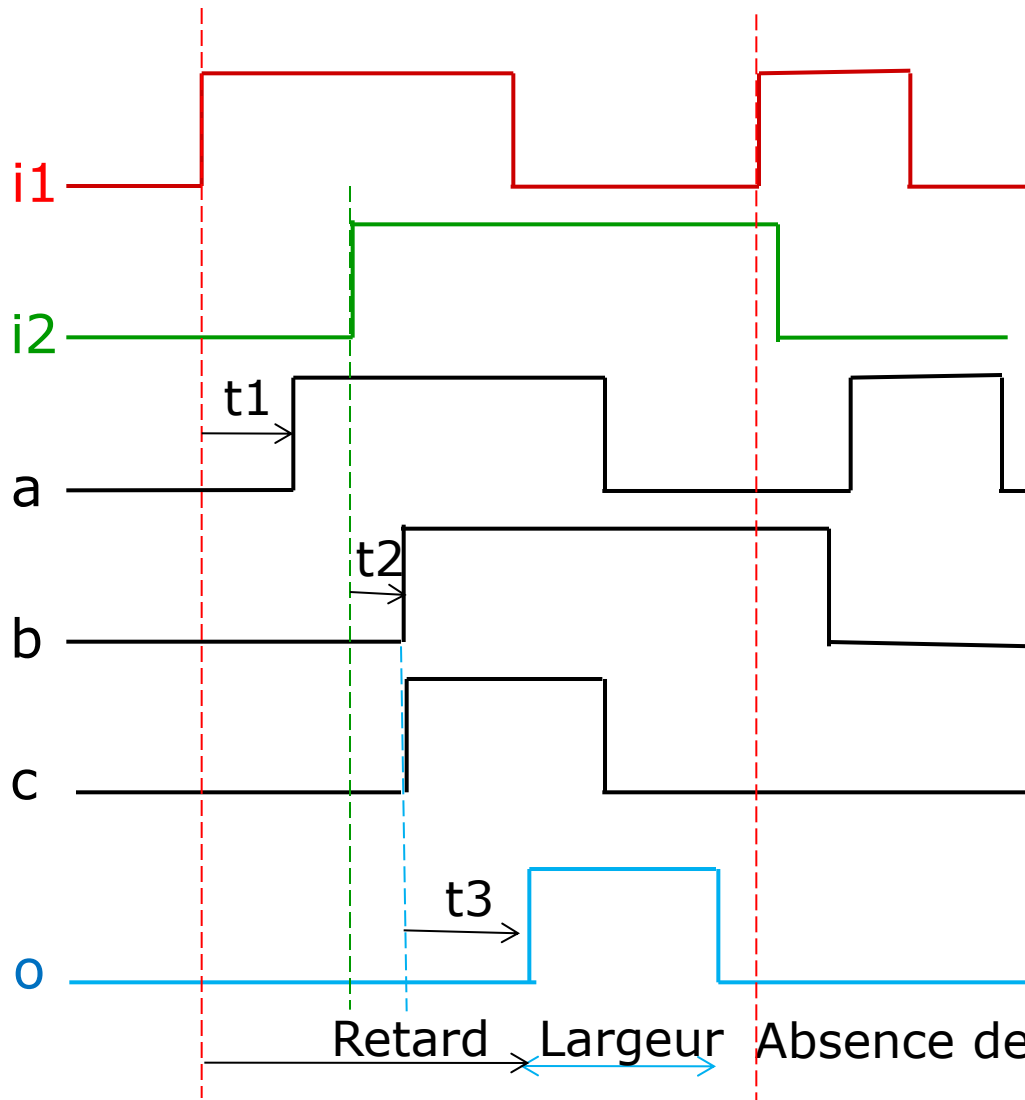


FPGA-Logique Asynchrone



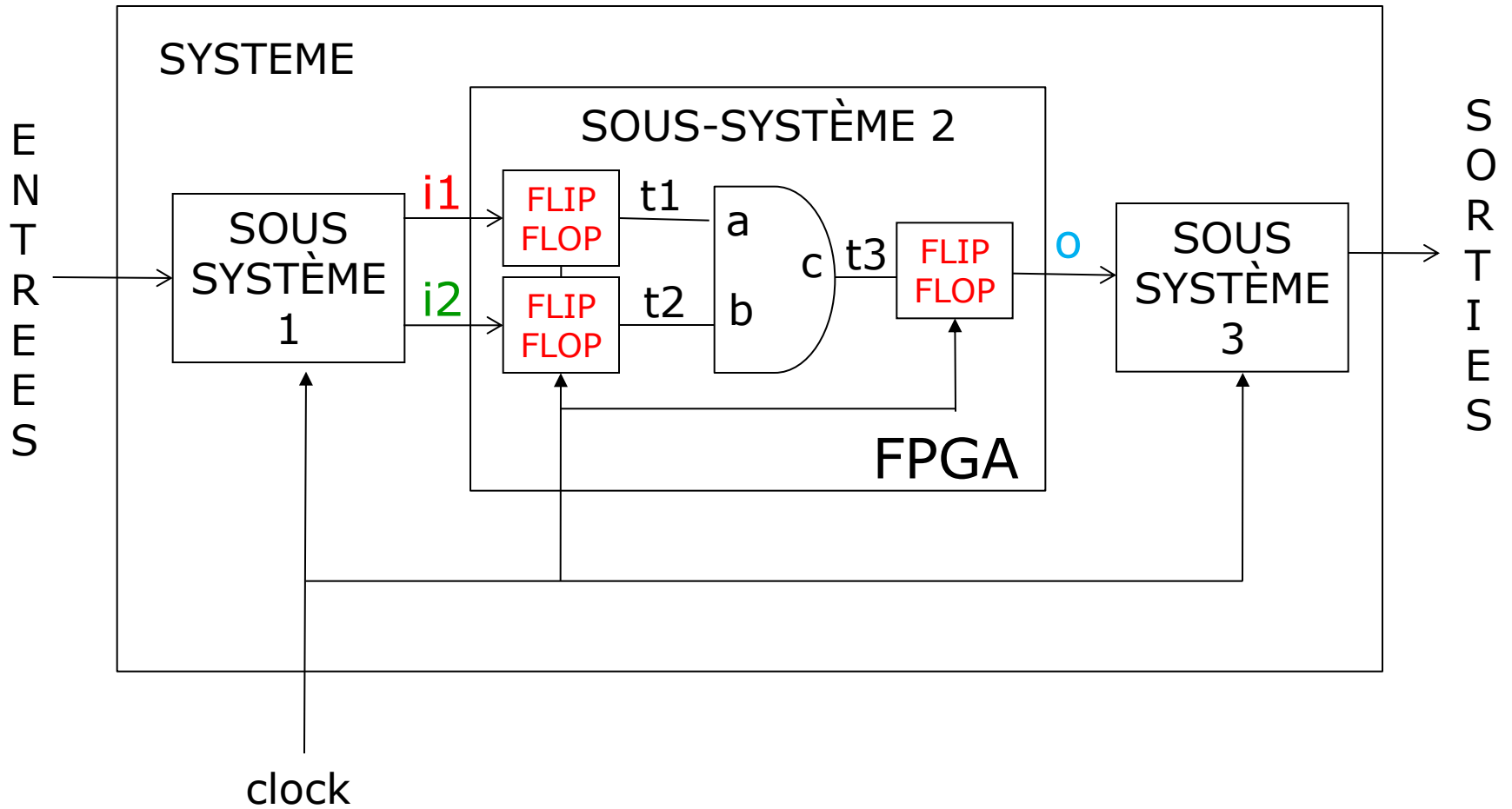
- Analyse au niveau système des conséquences d'un glitch :
- Ordre de conversion N/A erroné
 - Ecriture mémoire erronée

FPGA-Logique Asynchrone

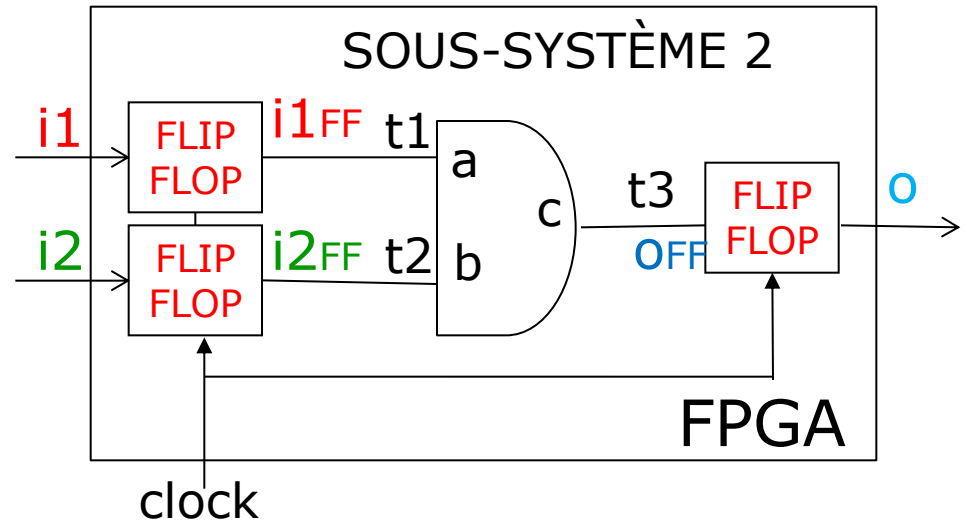
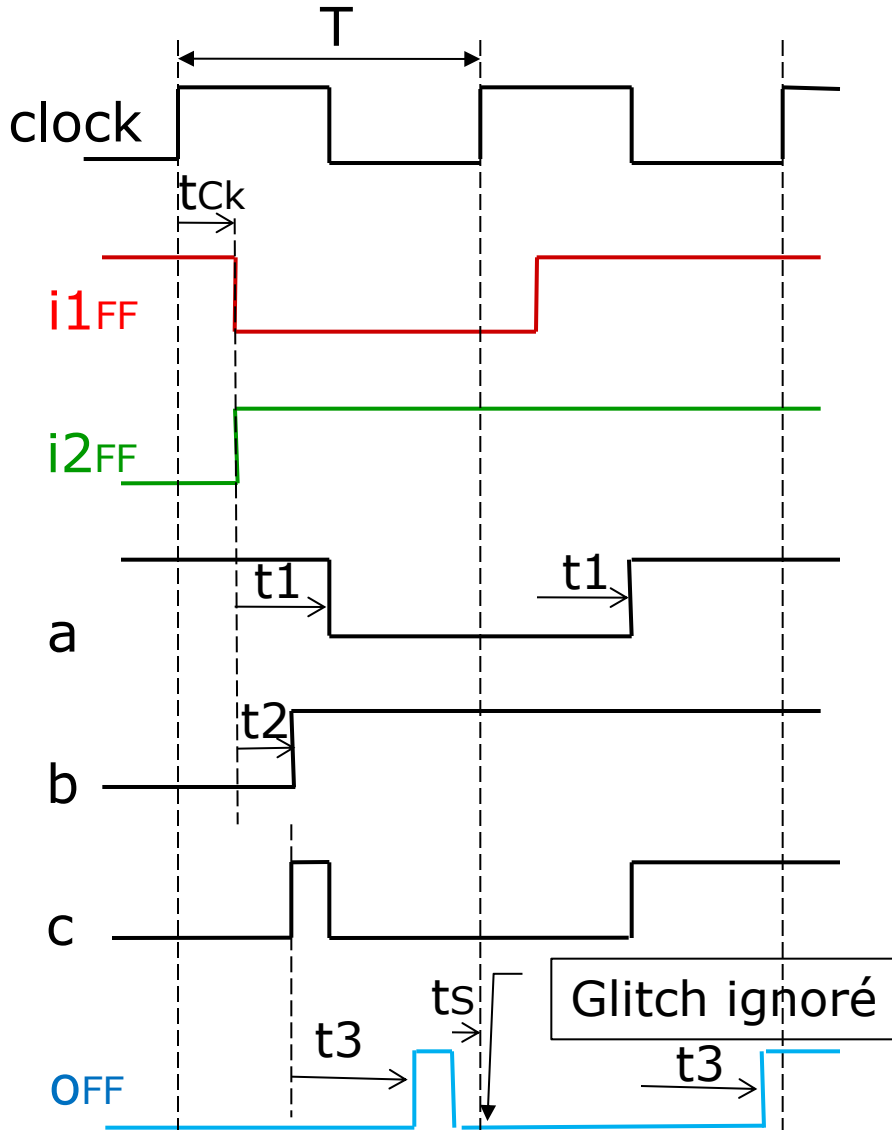


- Prise en compte des délais de routage
- modification fonctionnelle
 - Reproductivité des délais de routage

FPGA-Logique Synchrone



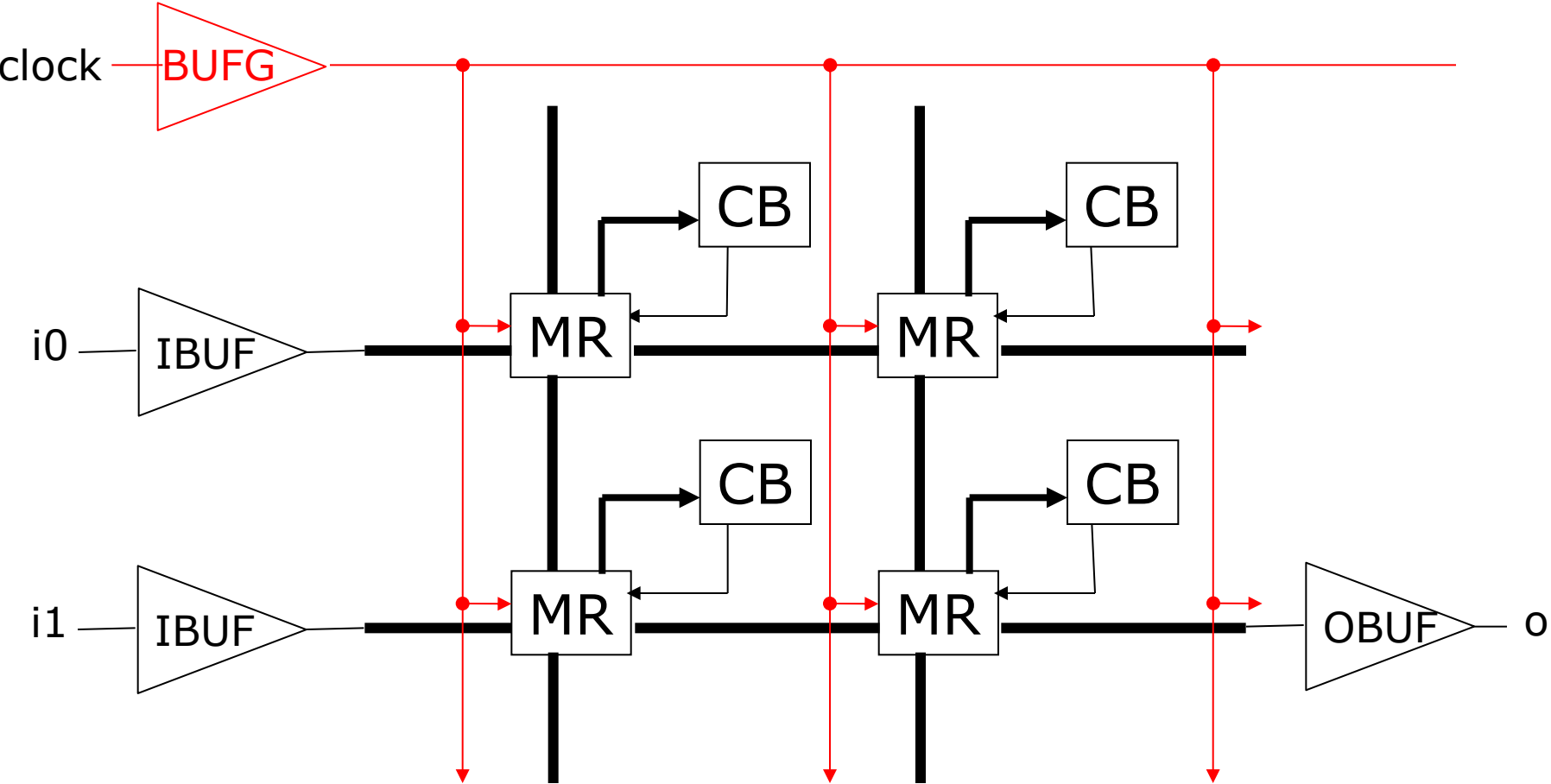
FPGA-Logique Synchrones



- Période T , Fréquence $F=1/T$
- temps de propagation
- t_{Ck} : horloge vers sortie (maximum)
- $t1, t2, t3$: routage (maximum)
- Temps de setup t_s (minimum)
- Fréquence maximale applicable
- $F_{MAX} = 1/(t_{Ck} + \max(t1, t2) + t3 + t_s)$
- Comportement déterministe du système pour $F \leq F_{MAX}$

FPGA-Buffers Globaux

Distribution de l'Horloge sur des lignes dédiées-
Equilibrage de l'arbre d'horloge



FPGA – Fréquence d'opérations

$t_{Cko}=1.016$ ns

$t_{Setup}=0.742$ ns

$t_1=0.379$ ns

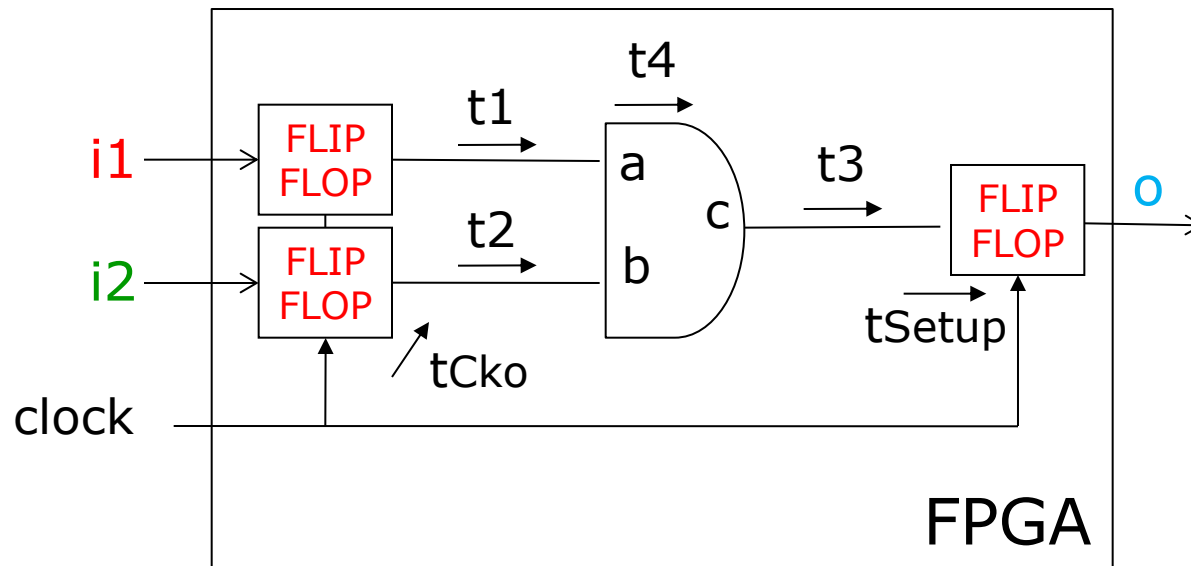
$t_3=2.491$ ns

$t_2=0.378$ ns

$t_4=0.643$ ns

Pour l'exemple :

- les 3 FLIP-FLOP sont associés à la broche (registre IOB)
- broche 'O' physiquement opposée aux broches 'i1' et 'i2'



Fréquence Maximale ?

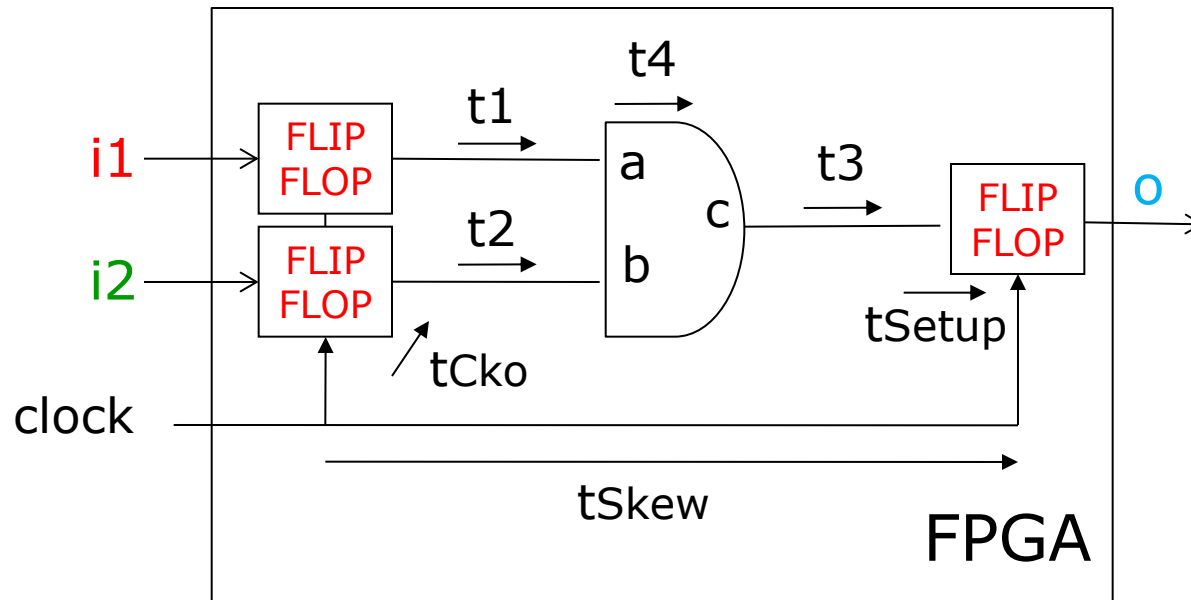
FPGA – Fréquence d'opérations

$$F_{MAX} = 1 / (t_{Ck0} + t_1 + t_4 + t_3 + t_{Setup}) = 189.7 \text{ MHz}$$

calcul de F_{MAX} exact ?

FPGA – Fréquence d'opérations

$t_{\text{Skew}} = -0.127 \text{ ns}$



$$F_{\text{MAX}} = 1 / (t_{\text{Cko}} + t1 + t4 + t3 + t_{\text{Setup}} + t_{\text{Skew}}) = 185.2 \text{ MHz}$$

FPGA – Fréquence d'opérations

Timing constraint: TS clk = PERIOD TIMEGRP "clk" 5 ns HIGH 50%:
4 paths analyzed, 2 endpoints analyzed, 1 failing endpoint
1 timing error detected. (1 setup error, 0 hold errors) ←
Minimum period is 5.398ns.

Slack: -0.398ns (requirement - (data path - clock path skew + uncertainty))

Source: i1p (FF)	clk: clk_BUF0P rising at 0.000ns
Destination: s1 (FF)	clk: clk_BUF0P rising at 5.000ns

Requirement	Data Path Delay	Clock Path Skew:	Clock Uncertainty
5.000ns	5.271ns (Levels of Logic = 1)	-0.127ns (0.549 - 0.676)	0.000ns

[Timing Improvement Wizard](#)

Maximum Data Path: [i1p](#) to [s1](#)

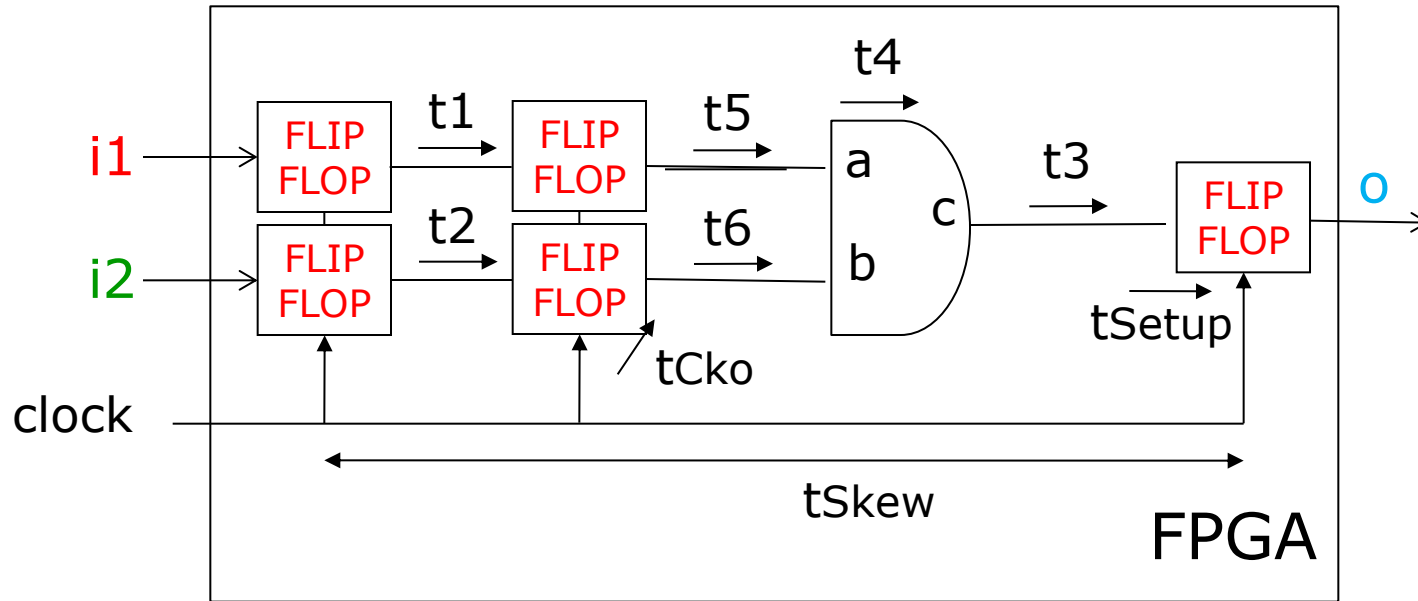
Delay type	Delay(ns)	Logical Resource
Tiocki	1.016	i1p
net (fanout=2)	0.379	i1p
Tilo	0.643	s1_or00001
net (fanout=1)	2.491	s1_or0000
Tioock	0.742	s1
Total	5.271ns	(2.401ns logic, 2.870ns route) (45.6% logic, 54.4% route)

Violation des contraintes temporelles (F=200 MHz)

Comment augmenter la fréquence ?

Délais de routage vs délais des opérations logiques

FPGA – Fréquence d'opérations



Diminution des délais de routage

FPGA – Fréquence d'opérations

Timing constraint: [TS clk = PERIOD TIMEGRP "clk" 5 ns HIGH 50%](#)

6 paths analyzed, 4 endpoints analyzed, 0 failing endpoints
0 timing errors detected. (0 setup errors, 0 hold errors)
Minimum period is 4.586ns.

Slack: [0.414ns \(requirement - \(data path - clock path skew + uncertainty\)\)](#)

Source: i2pp (FF)	clk: clk_BUFGRP rising at 0.000ns
Destination: s1 (FF)	clk: clk_BUFGRP rising at 5.000ns

Requirement	Data Path Delay	Clock Path Skew:	Clock Uncertainty
5.000ns	4.495ns (Levels of Logic = 1)	-0.091ns (0.549 - 0.640)	0.000ns

[Maximum Data Path: i2pp to s1](#)

Delay type	Delay(ns)	Logical Resource
Tcko	0.676	i2pp
net (fanout=2)	0.406	i2pp
Tilo	0.692	s1_or00001
net (fanout=1)	1.979	s1_or0000
Tioock	0.742	s1
Total	4.495ns	(2.110ns logic, 2.385ns route) (46.9% logic, 53.1% route)

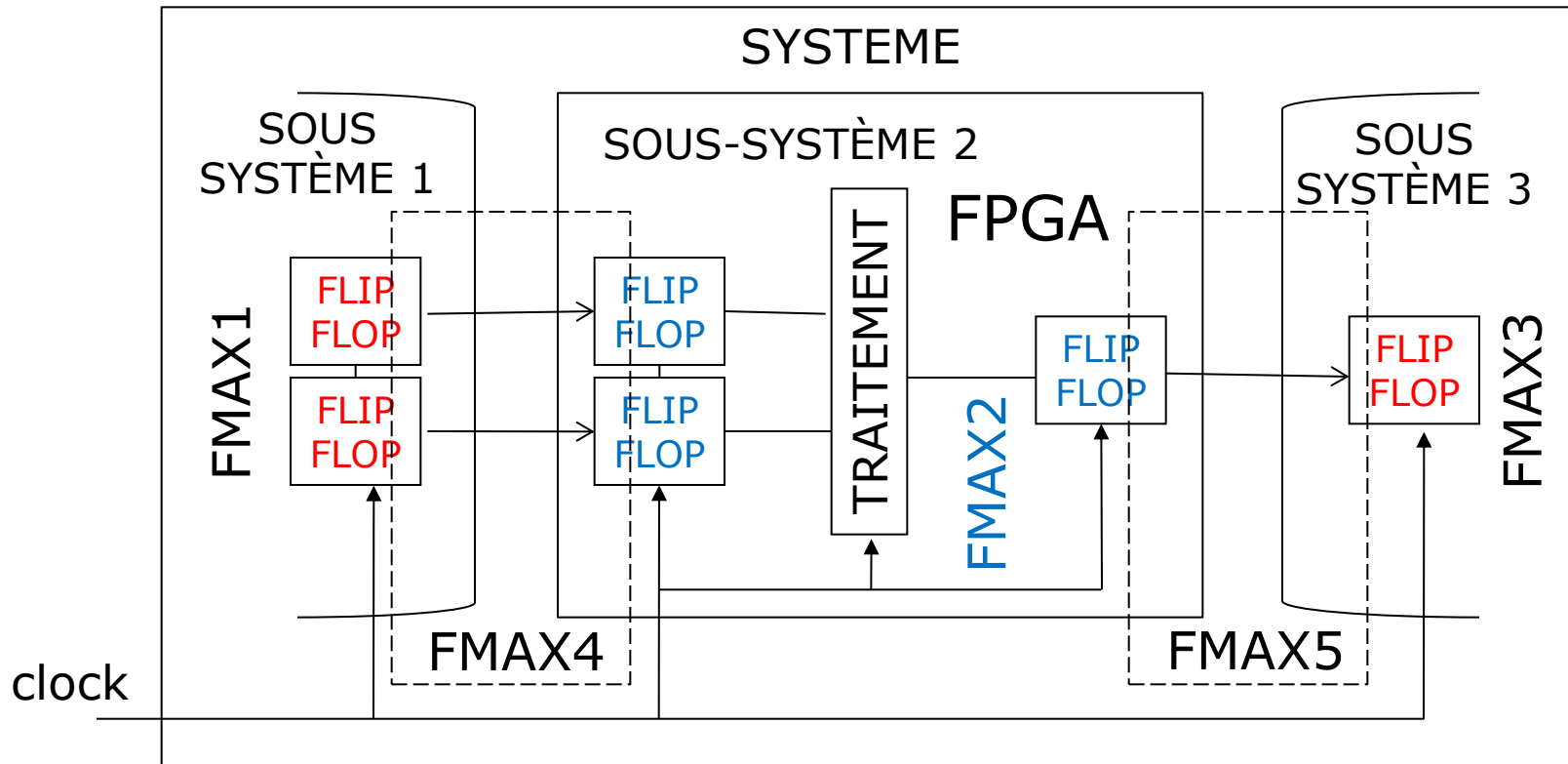
FMAX = 218 MHz

Réduction du délai de routage du fil le plus long

FPGA – Fréquence d'opérations

FLIP FLOP

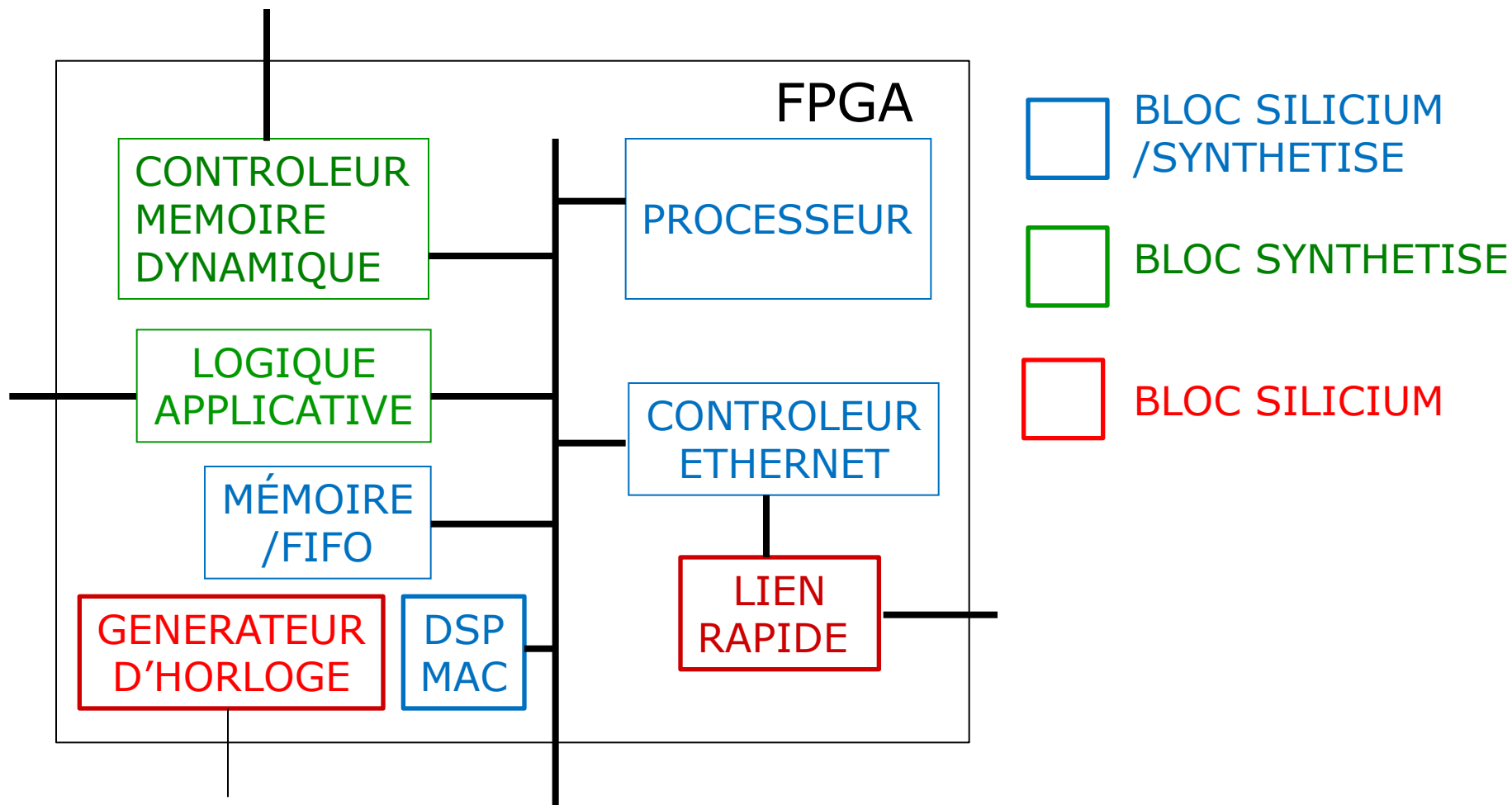
Placement dans un registre d'entrée/Sortie (RIOB)



Fréquence Maximale du système = $\min (FMAX1, FMAX2, FMAX3, FMAX4, FMAX5)$. RIOB : FMAX4 et FMAX5 indépendants des délais de routage interne non reproductibles du FPGA

FPGA – Les blocs de conception IP

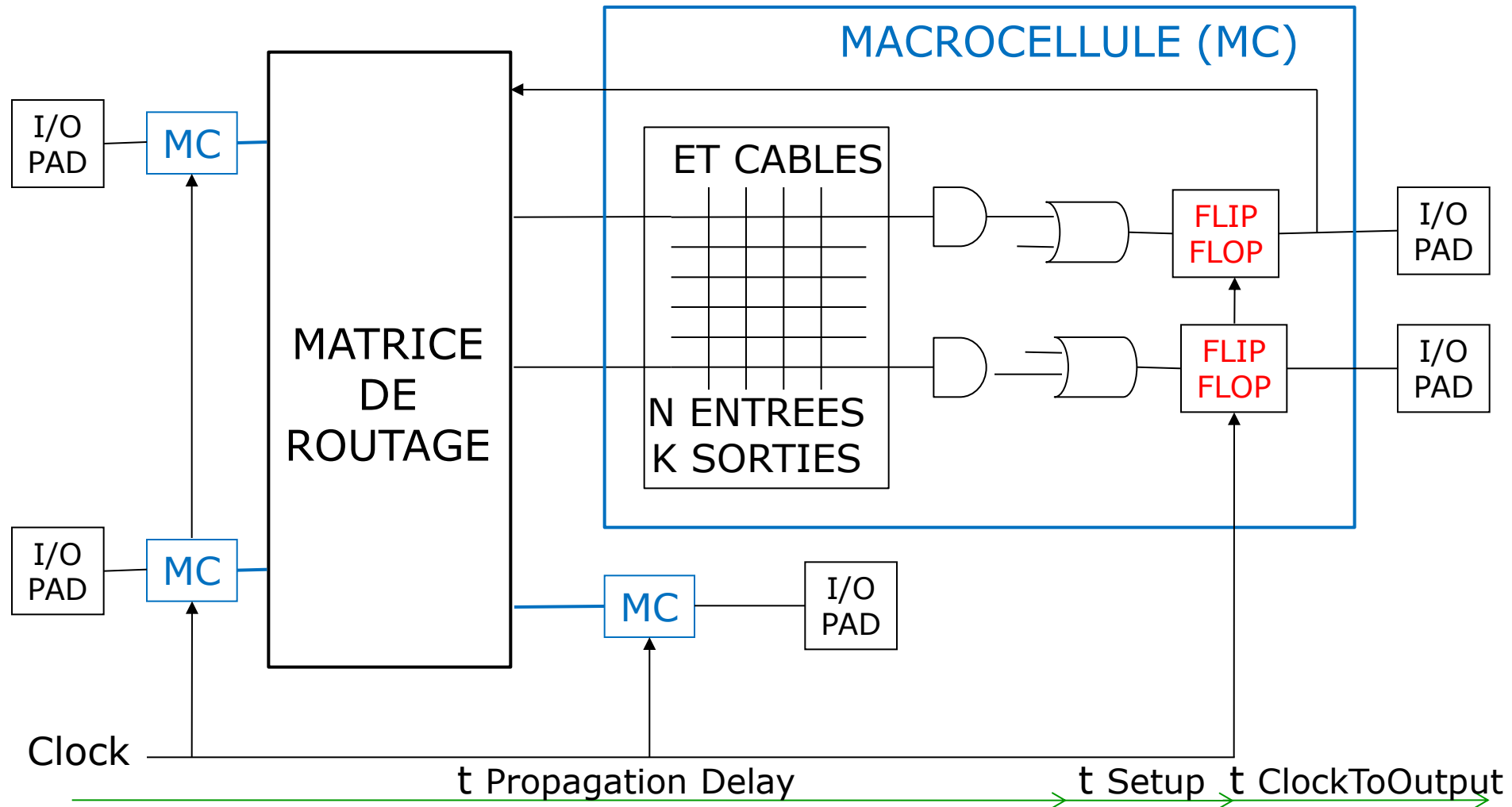
IP Intellectual Property



FPGA – Exemple Famille XILINX

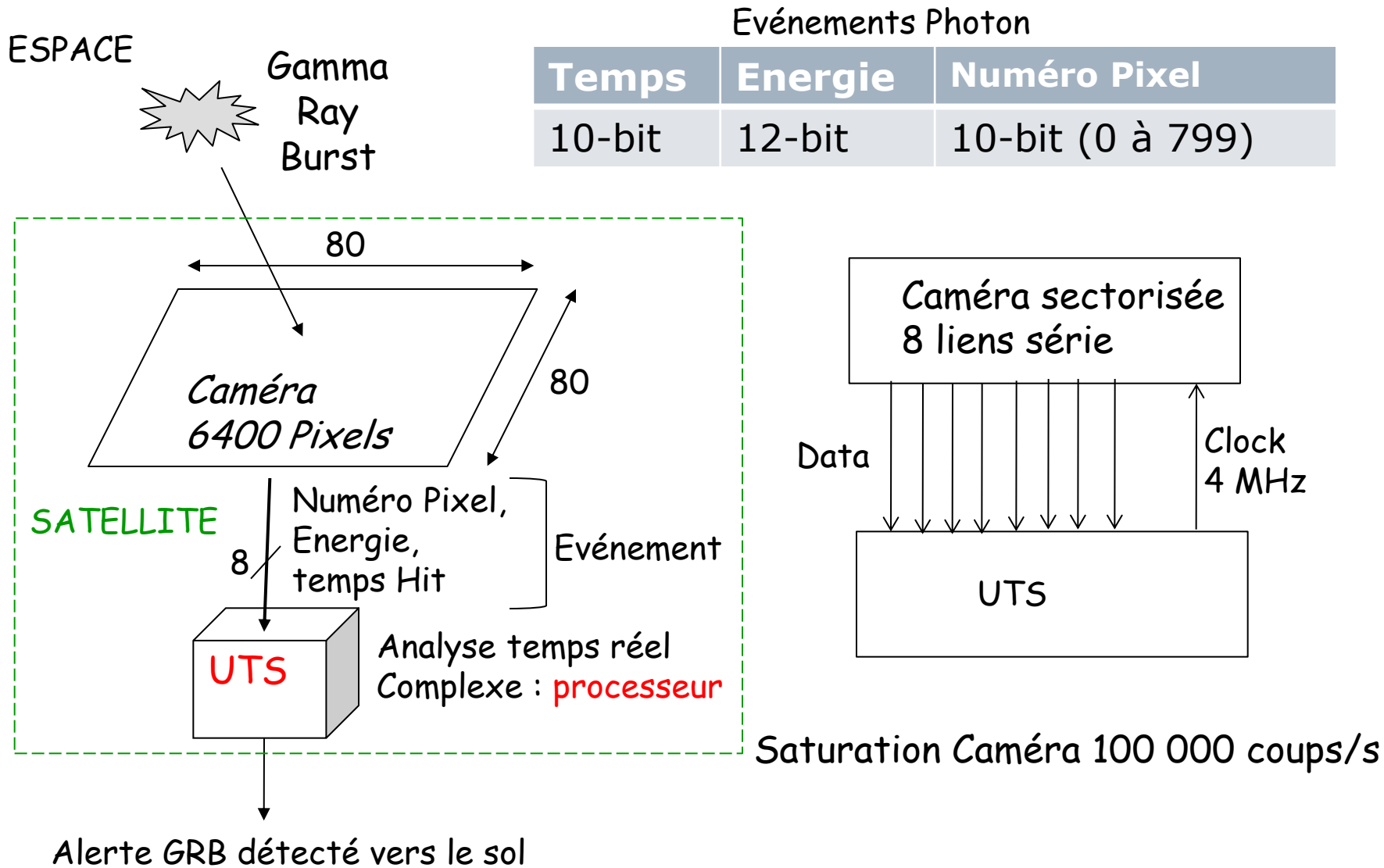
Ressources / Blocs en dur	XCE6VHX565T (VIRTEX-6)	XC5VFX200T (VIRTEX-5)	XC3SD3400A (SPARTAN-3A)
LUT	354240 LUT-6	122880 LUT-6	47744 LUT-4
FLIP-FLOP	708480	122880	47744
PROCESSEUR	0	2 PPC440@400MHz	0
RAM/FIFO	156 x 36Kbits	456 x 36Kbits	126 x 18Kbits
TRANSCEIVER	24 9,95 Gb/s -11,18 Gb/s	24 150 Mb/s -6,5 Gb/s	0
CONTROLEUR ETHERNET (MAC)	4	8	0
TAILLE MÉMOIRE DE CONFIGURATION	153,2 Mbits	70,9 Mbits	11,7 Mbits

FPGA- versus CPLD

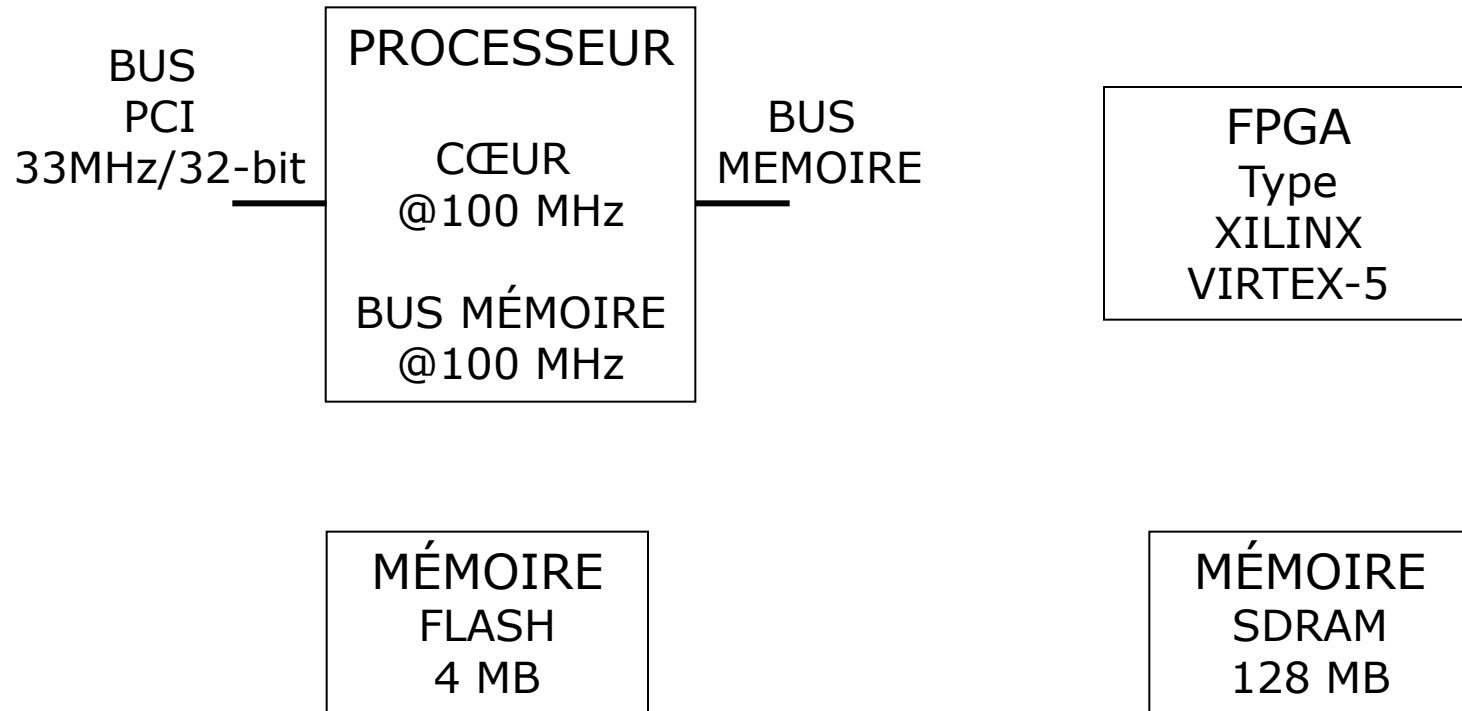


Valeurs Typiques : FMAX=250 MHz, Nombre de MC=256

FPGA- un design, les entrées

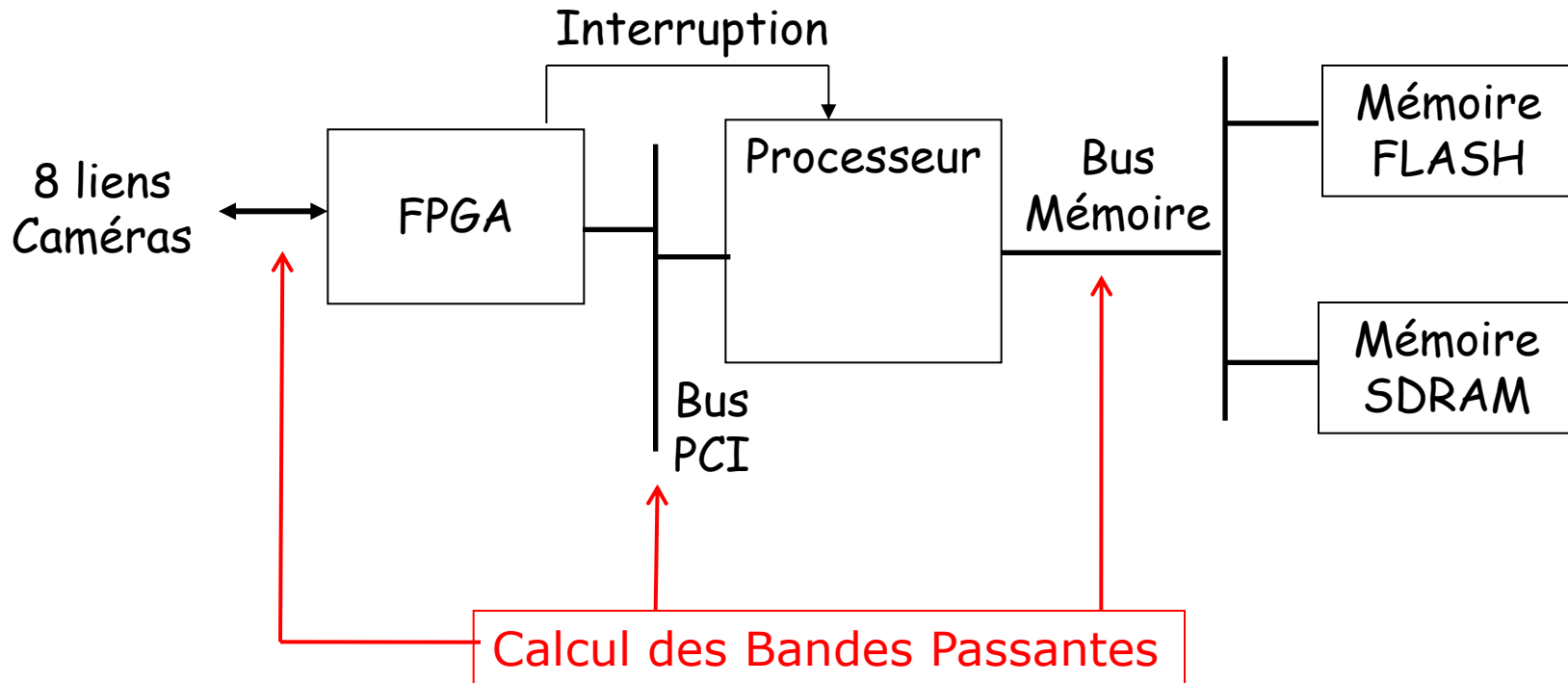


FPGA – Un design, les composants



Design ?

FPGA- Un design



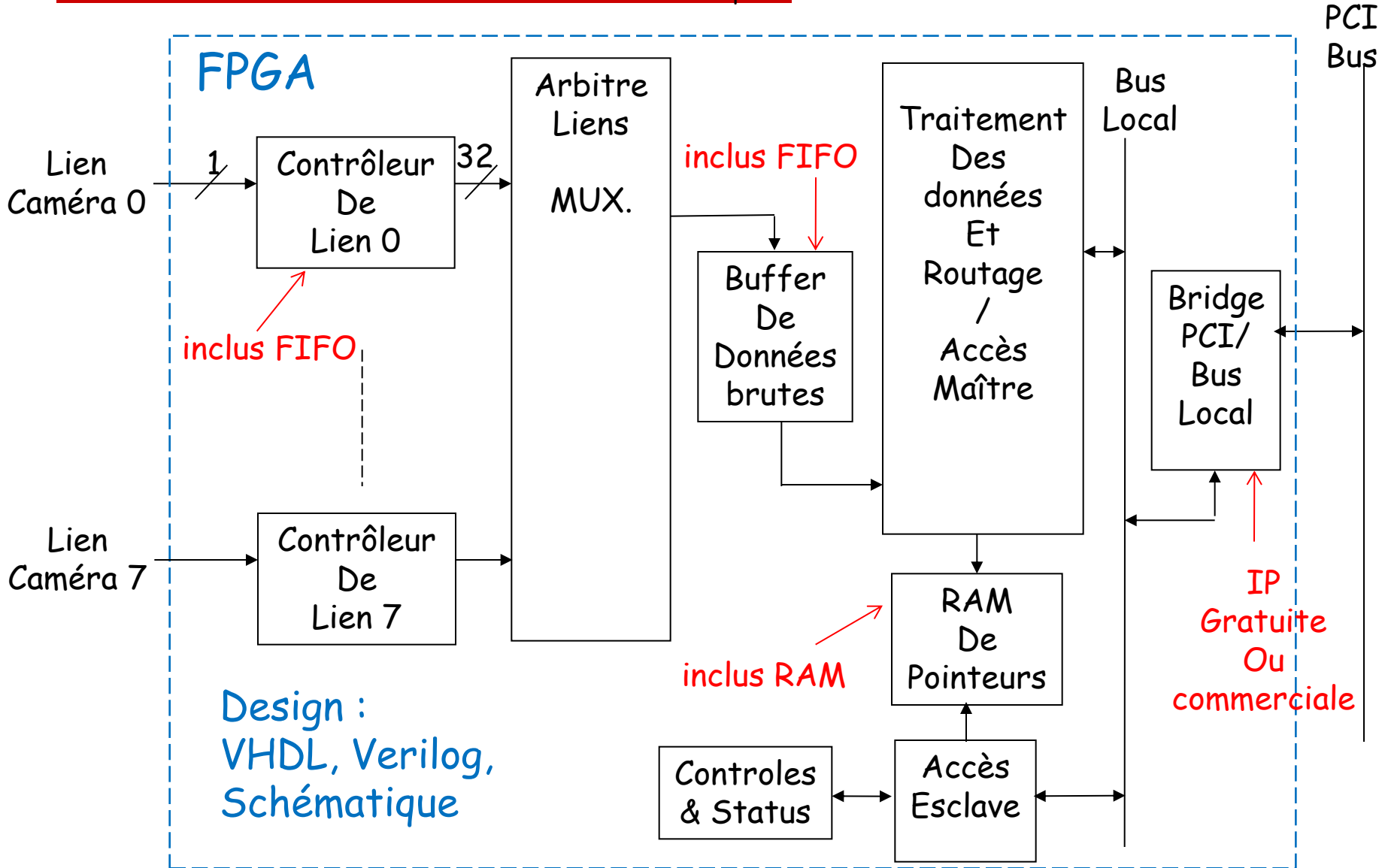
FPGA- Un design

	Caméra (Max)	Caméra (Saturation)	Bus PCI	Bus Mémoire
Largeur bus (bit)	1	32	32	32
Fréquence (MHz)	4	0,1	33	100
Nombre de bus	8	1	1	1
Bande Passante (M octet/s)	4	0,4	132	400

**Bande passante maximale,
efficacité des protocoles non prise en compte**

FPGA- Un design

CPU Interrupt 0-1



PCI Bus

FPGA-un design

interruption toutes les 10 ms
Programme d'interruption :
lecture du registre FPGA contenant
le nombre de photons écrits

