WP4 CHOPPER final report

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(Edited by A. Lombardi)

Abstract

This report summarises the achievements of the WP4 “Chopper” in the HIPPI Joint Research Activities within CARE for the years 2004-2008.

Introduction

Proton driver specifications for the next generation of spallation neutron sources, neutrino factories, and waste transmutation plants, call for more than an order of magnitude increase in beam power, typically from ~ 0.16 to ~ 5 MW. For the linac-accumulator or linac synchrotron schemes, beam loss at ring injection and extraction, and the consequent activation of components, can be minimised by a programmed population of ring longitudinal phase space, produced by 'chopping' the linac beam at low energy. The 'chopper' is required to produce precisely defined gaps in the bunched linac beam, and the chopping field must therefore rise and fall within, and be synchronous with, bunch intervals that are typically just a few nanoseconds in duration .

WP4 within HIPPI addressed two different approaches to chopping which have been proposed for two upcoming facilities: CERN Linac4 and RAL FETS [1,2] as well as for CERN SPL and the ISIS upgrade[3,4].

Two approaches (chopper A and chopper B)

Details of chopper A

In LINAC4 the bunches are spaced by 2.84 ns and come in 0.4 ms pulses repeated at 2 Hz, and for injection into the booster it is necessary to remove 133 over 352 pulses to match the 352 MHz structure to the 1 MHz frequency of the booster. The chopper is placed after the RFQ where the beam energy is 3 MeV. To avoid partially filled bunches the rise time of the chopper has to be less than 2 nsec. The effective voltage has to be at least ±400 Volts which corresponds to an effective kick on the 3MeV beam of 5.7 mrad for an effective chopper length of 800mm and a distance between the plates of 20 mm. The above choice are the result of a compromise between beam dynamics needs (compact elements, big apertures, high voltage, sufficient separation between chopped and un-chopped beams) and the driver constraints of short rise time and high voltage. Besides the above function, the chopper is also removing 1 microsecond of beam (357 bunches) every 100 microsecond to make a hole for the rise-time of the distributor to the 4 booster ring

The chopper is embedded in a transfer line between the RFQ and the DTL which comprises: a matching section (4 quadrupoles and a buncher cavity), the beam chopper housed in 2 quadrupoles, buncher cavity a quadrupole and a dump (for the chopped beam), and a re-matching section (4 quadrupoles plus buncher cavity). The 11 quadrupoles are independently powered. The buncher cavities, resonating at 352 MHz and delivering a maximum voltage of 150 kV to the beam, have been manufactured (2/3) and have been tested at CERN. The chopper line has been fully assembled in 2008 [5]. Currently the chopper is housed in a pulsed quadrupole, nevertheless the influence of the transient on the chopper efficiency has not been evaluated yet. The exchange with a DC quadrupole or a PMQ might be necessary. The beam dynamics of the entire CERN chopper line is designed to minimize the plate voltage by increasing the deflection via beam optics. On the other hand there is an effort to keep the actual chopper structure as short as possible in order to minimize emittance blow-up during long drifts.[6]

Details of chopper B

The FETS project, a UK based collaboration involving RAL, Imperial College London, and the University of Warwick, will test a fast beam chopper in a high duty factor MEBT line [4]. The key components are: an upgraded ISIS 'Penning' ion source, a three solenoid Low Energy Transport (LEBT) line, a high duty factor 324 MHz Radio Frequency Quadrupole (RFQ), a novel two stage beam chopper, and a suite of beam diagnostic instruments. The specification, as shown in Table 1, calls for significant technical development in attempting to address the generic, and specific requirements for a next generation proton driver and a 0.16 to 0.5 MW upgrade for ISIS [5], respectively. The peculiarity of the chopper B is the two stage chopping scheme as developed for the European Spallation Source (ESS) [6, 7]. This novel configuration addresses the conflicting chopping field requirements of fast transition time (~ 2 ns) and long duration (~ 0.1 ms), with the tandem combination of 'fast' transition time short duration, and slow transition time long duration, fields. The upstream chopping field is generated by a pair of AC coupled 'fast' transition time pulse generators (FPG) that output high voltage, dual polarity pulses into a transmission line electrode structure [8], where partial chopping of beam bunches is avoided by ensuring that the deflecting E-field propagates at the beam velocity. The 'fast' chopper deflects just five bunches at the beginning and end of each chopped beam interval, creating two ~ 18 ns gaps in the bunch train. These gaps ensure that partial chopping of beam bunches is avoided in the downstream 'slow' chopper, whose field is generated by eight pairs of DC coupled, 'slow' transition time pulse generators (SPG) that output high voltage dual polarity pulses to a set of discrete, close coupled, electrodes. The 'slow' chopper generates a long duration E-field that deflects the remaining bunches in each chopping interval. Deflected beam is directed to dedicated beam 'dumps' situated immediately downstream of the fast and slow electrode structures. A sketch of the RAL FETS chopper line is shown in Figure1 and the corresponding beam envelopes in Figure 2.

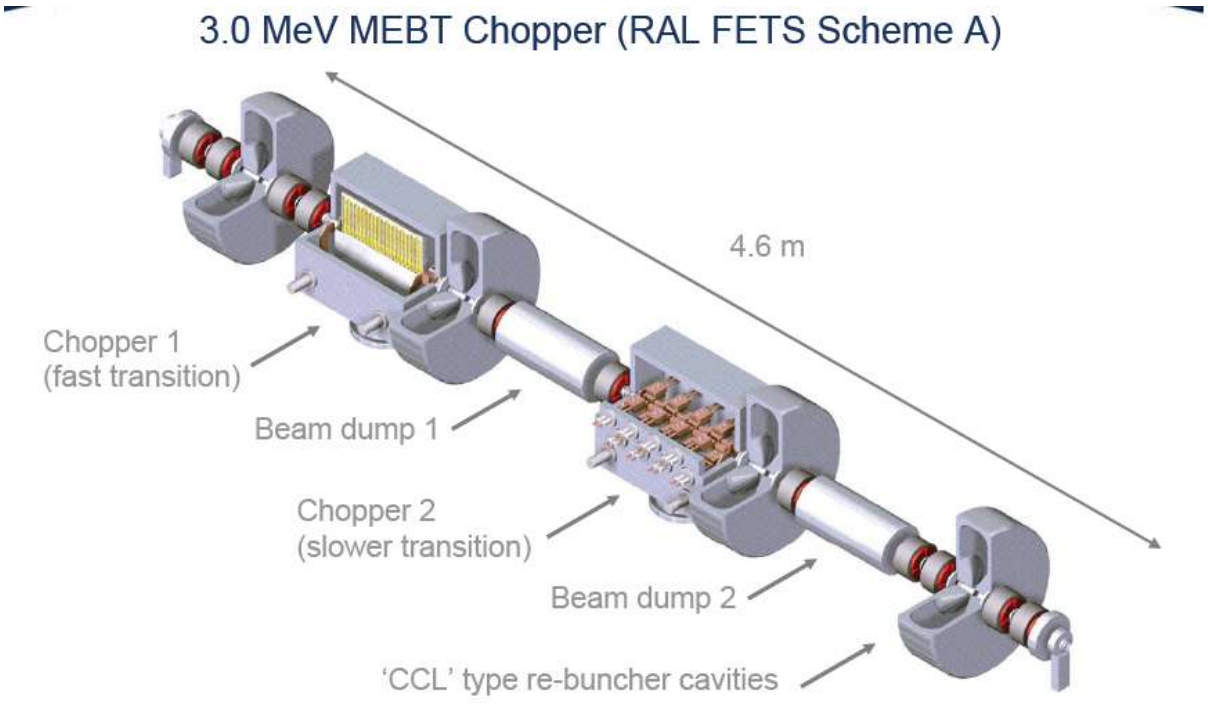

Figure 1 : The RAL FETS chopper line

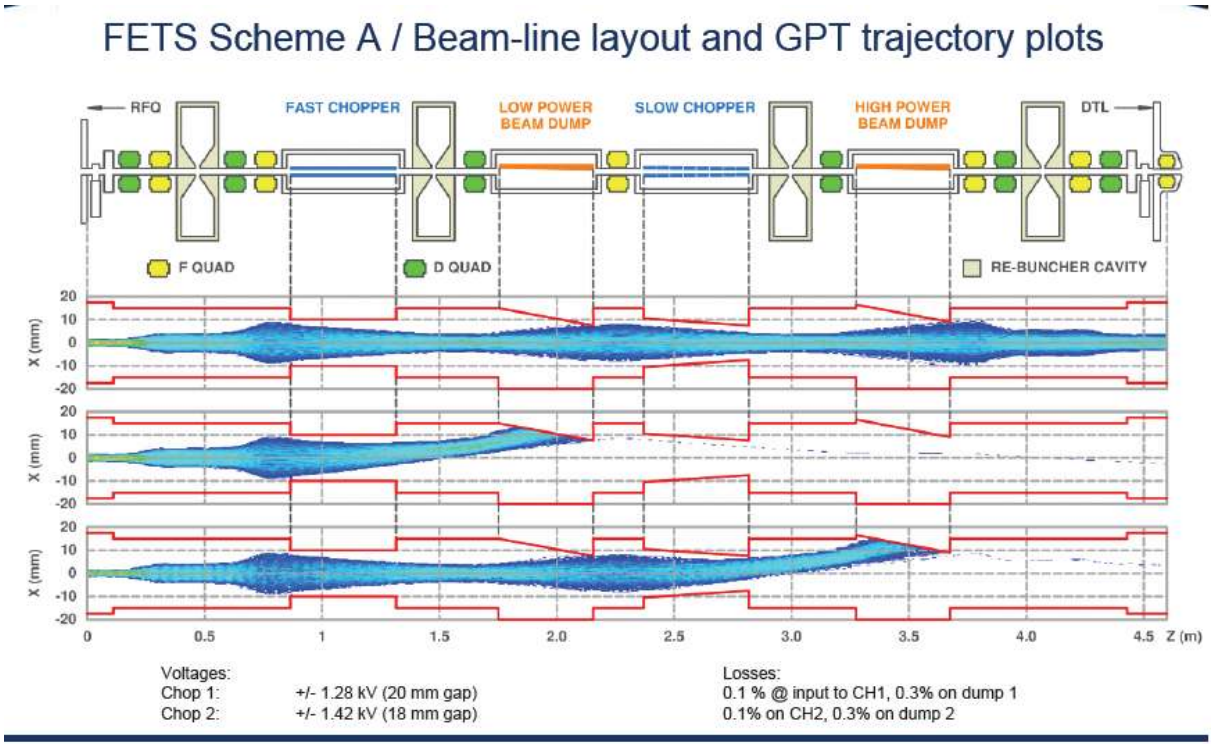

Figure 2 : Beam dynamics in the RAL FETS chopper line

Table 1 contains the main parameters of the two chopper systems.

Table 1 : Chopper parameters

	Chopper A (CERN)	Chopper B (RAL)	
	Fast	Fast	Slow†
Rise/fall time	< 2 nsec	≤ 2 nsec	≤ 15 ns
Max. rep rate	50 MHz	2.6 MHz	1.3 MHz
Max. voltage/target	250 V/500V	1400V / 2200V	≤ 6kV
Reliability	TBD	TBD	TBD
Flexibility	Min 8 nsec (3 bunches)	7 – 15 ns	200 ns – 100 us
Chopping effectiveness (calculated)	99.7%	99.0 %	
Emittance growth of the un-chopped beam	8%	8% (New 3 MeV MEBT design)‡	

Hardware- chopper A

Structure

The chopper has to fulfill tough electrical specifications, in particular the short rise time, low attenuation and the highest possible coverage factor. Errors in the line's electrical length cause the pulse to propagate at a different speed from the beam, thus possibly affecting adjacent un-chopped bunches. In addition it has to stand a significant amount of radiation and therefore a considerable heat load. It must operate in ultra-high vacuum and have sufficient high-voltage capabilities. Due to the given space constraints, a meander line structure appeared to be the most promising candidate for the design. When printed on a high permittivity substrate it is possible to reduce the transverse meander dimension and fit the chopper plates into the existing quadrupoles. Alumina (Al_2O_3, $\varepsilon_r \approx 9.8$) was chosen for the support because of its good radiation resistance (in particular compared to organic materials), good vacuum properties, good heat resistance and conduction and finally because a high ε implies small transverse meander size. For sufficient mechanical robustness, the substrate thickness of 3 mm was chosen. At first the parameters of a 50 Ω meander line were determined. However it turned out that the line width needs to be very close to the substrate height. In this case the spacing between parallel lines would be small, leading to high dispersion. These problems could be avoided by combining two 100 Ω lines to form one 50 Ω double meander (Fig. 3).

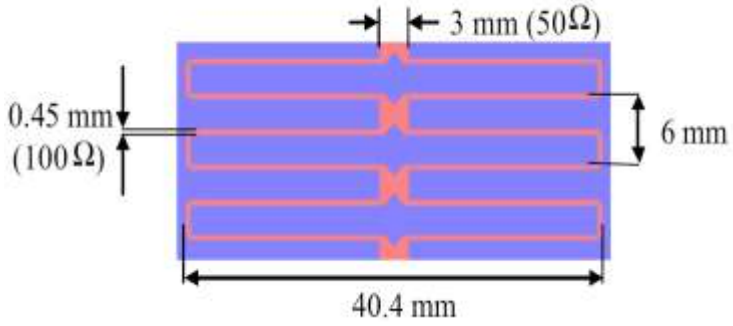

Figure 3: Geometry of the double meander line (version 2002).

First prototypes were manufactured at CERN but the final ceramic plates were produced in the industry by Kyocera. The manufacturing process went through many revisions and was adapted to the available technology. Fig. 4 shows the three layer final structure. First a 10 to 15 µm silver thick-film layer is applied on the ceramic plates. Then a 30 µm copper main conduction layer can be deposited electrochemically and finally a thin finishing of gold is applied for low contact resistance and as a protection against oxidation.

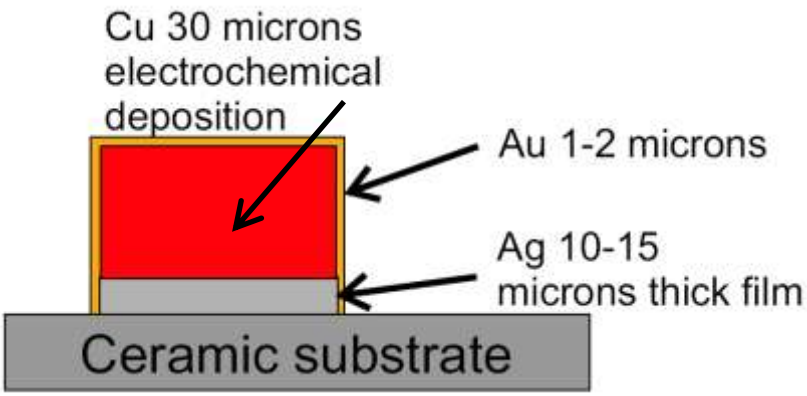

Figure 4: Kyocera plates layer structure.

In order to provide good mechanical stability for the ceramic plate a 10 mm thick, 70 mm wide and 46 cm long stainless steel plate is used as ground plane. The RF connections to the meander line are done with feed-throughs. Fine adjustment of the electrical length is foreseen by cutting longitudinal grooves under the ceramic plates. On the back of the ground plane the water cooling is installed. A small copper "scraper" is placed on the front side. It protrudes by ≈ 0.3 mm farther than the ceramic plate into the beam aperture to limit beam losses there. This should be effective in particular for the second chopper tank where the beam envelope has its maximum size (Fig. 4). For the first tank and for chopped beam, however, the scraper is not expected to reduce much the losses on the ceramic plates. Fig. 5 shows the chopper plates with the accessories. The ground plates are held in place by two support rings at the ends of the tank. Each of these rings can be aligned with three screws. This way the position of the plates can be easily adjusted. It is also possible to tilt them to change the kick strength or to reduce beam losses on the ceramic plates. The tank after installation of the first plate is shown in Fig. 6.

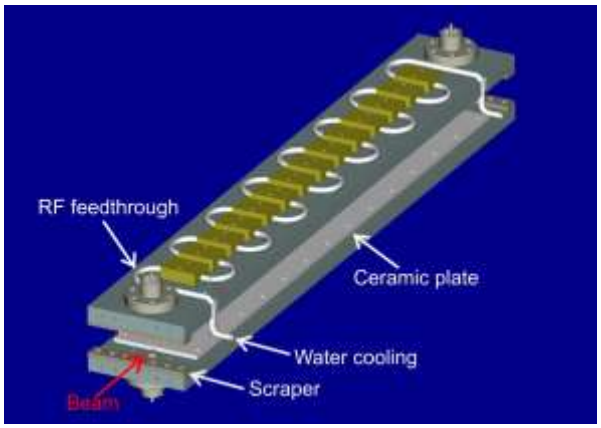

Figure 5: Two ceramic plates fixed on their support plates with the water cooling lines mounted on the back.

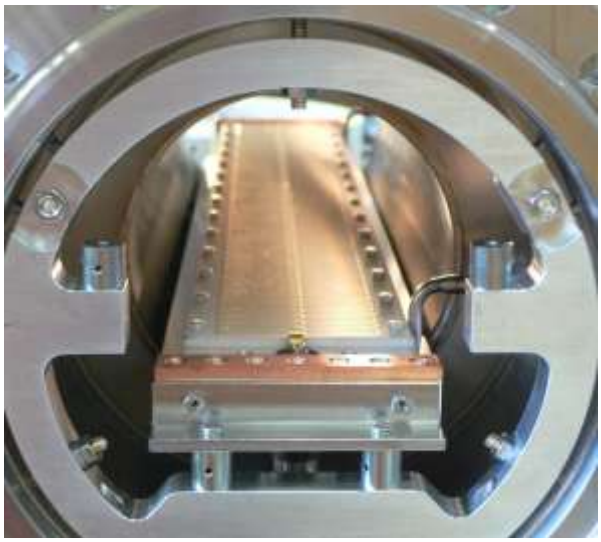

Figure 6: The first plate installed in the chopper tank.

A series of RF measurements were performed on the chopper plate. The transmission magnitude S_{21} of the single chopper plate is shown in Fig. 7. This attenuation was measured at the end of the plate. When averaged over the operational frequency range (≈200 MHz) and the plate length, it corresponds to 0.3 dB effective attenuation and to a kick field decrease of 3.4 %. At DC a resistance of 1.1 Ω was measured.

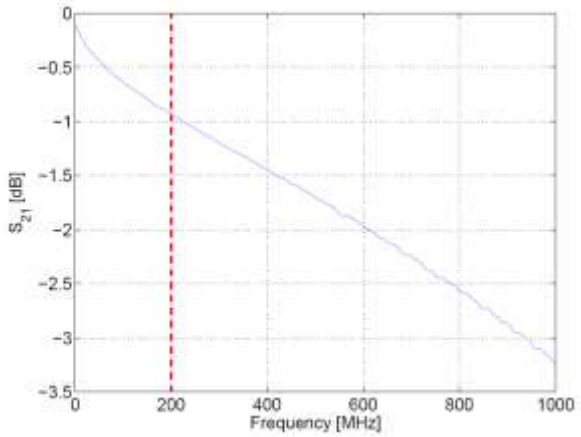

Figure 7: Magnitude of S_{21} over one plate.

The phase response is plotted in Fig. 8 after correction for the meander line electrical length (≈16.7 ns).

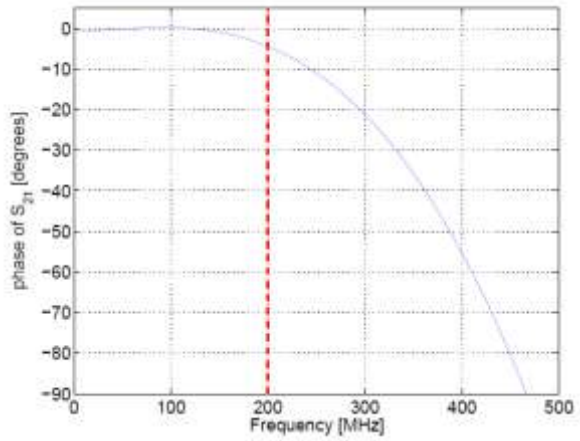

Figure 8: Phase of S_{21} over one plate.

Figure 9 shows a 2 ns rise time input pulse and the corresponding 2.2 ns output pulse. This can be calculated as corresponding to a structure rise time of 1 ns.

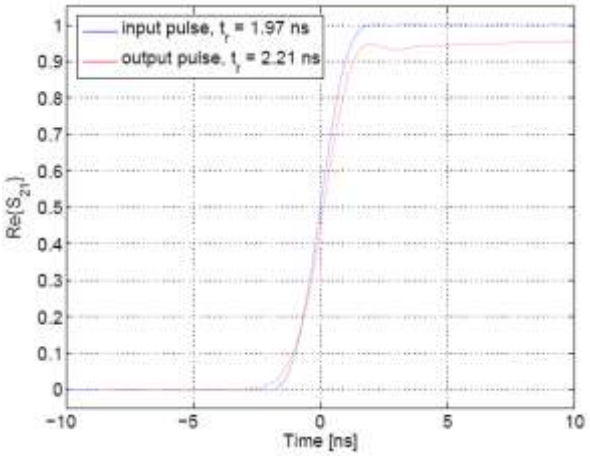

Figure 9: Input and output pulse on the chopper plate.

Input matching has been measured at -26 dB and the structure proved fairly insensitive to the presence of the image plane meaning that the interaction with the other plate will be negligible. Simulations to determine the coverage factor (CF) of the meander line structure were carried out using different tools. A value of CF = 0.78 can be assumed on the beam axis. As an experimental check for the coverage factor simulation, a measurement was performed using a single ceramic plate with a metallic image plane at the beam position (Fig. 10). In the centre of the image plane a 10 mm wide button-type probe measures the electric field at and around the beam position. In order to calibrate the measurement, a reference line consisting of a fully metal-coated plate was used. The measurement confirmed the simulation results.

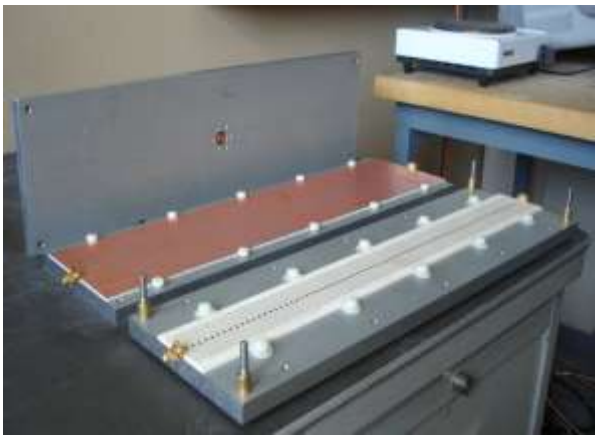

Figure 10: Coverage factor measurement set-up.

As far as the chopper driver is concerned, the chopper deflecting structures are essentially two matched 50 Ω transmission lines. They face each other and must be driven with opposite polarity signals with minimum amplitude of 500 V. To avoid perturbations of the accelerated beam, the extraction field must be established or removed within the time separating two bunches (2 ns). For maximum flexibility, the system must be able to remove any number of consecutive bunches (minimum 3) with repetition rates spanning from below 1 MHz to 44 MHz. The required generator is then a high power (5 kW, 5 % duty-cycle), 200 MHz (10 % to 90 %, 2 ns fronts), DC coupled amplifier. Further information on the CERN chopper electrodes approach can be found in [7,8,9,10].

Driver- CERN option:

Many active devices and amplification configurations have been considered to achieve the specified requirements that cannot be achieved with a conventional design. A possible solution of the problem was first identified in the idea of generating the low and high frequency parts of the required spectrum with two separate amplifiers. The two signal are then added at the beam using a tri-axial deflector in which the meander line reference plane is used as a quasi static electrode for the low frequencies. In-depth studies and prototyping have proven the principle but also shown its drawbacks. In fact to sum the two signals correctly they must be perfectly matched in terms of amplitude, phase and timing response. Distortions, saturation effects in the ferrite or in the driving circuits, etc. are then difficult to be kept within the limits required for proper and long term operation. To relax the stringent requirements involved in the unipolar deflecting fields, a second proposal has then been made. The original single direction beam deflection scheme requires driving one deflector plate positive and the other one negative. The same beam chopping effect can also be obtained by alternating the field polarity as shown in Fig. 11 with the advantage that the DC component self compensates every second cycle. For this reason, this scheme does not need DC coupling and allows the use of wideband transformers for combining large numbers of amplification modules built around RF MOSFETs. Moreover, as the positive and negative pulses are actually generated by separate amplification modules, each path only operates at half the required frequency (i.e. 22 MHz). The extraction of a long sequence of bunches is also possible by simply switching from one polarity to the other as shown in Fig. 12 and adjusting the first and last pulse length.

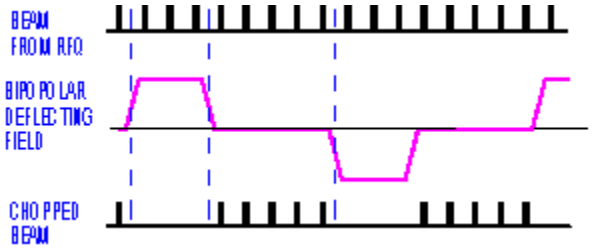

Figure 11: Alternate polarity extraction scheme.

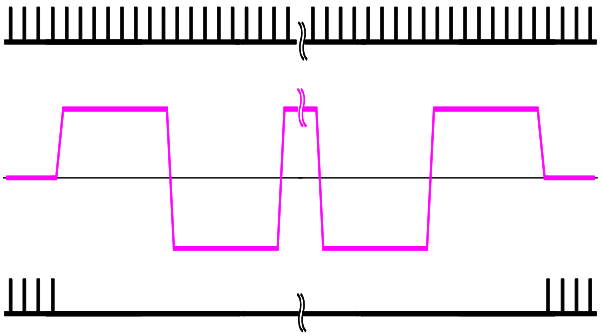

Figure 12: Long extraction sequence.

Based on these considerations a modular system allowing the achievement of the required specifications has been defined and the required components designed, built and tested. Construction has been limited to a half scale prototype (±250 V), and coupling of four such modules would give the required ±500 V. 128 MOSFETs are used to achieve the nominal voltage and individual adjustment of the delay is required in order to minimize the transition fronts.

Figure 13: CERN driver ±250 V prototype.

The main characteristics of the prototype are listed in Table 2, Figs. 14 to 16 plot relevant data.

Table 2: 250 V module main characteristics.

Output voltage	± 270 V
Input / Output impedance	50 Ω
Rise / Fall time	≤ 2.1 ns
Repetition frequency	≤ 45 MHz
Burst length	≤ 2 ms
Burst repletion rate	≤ 50 Hz
DC supply	100 V
Cooling	water

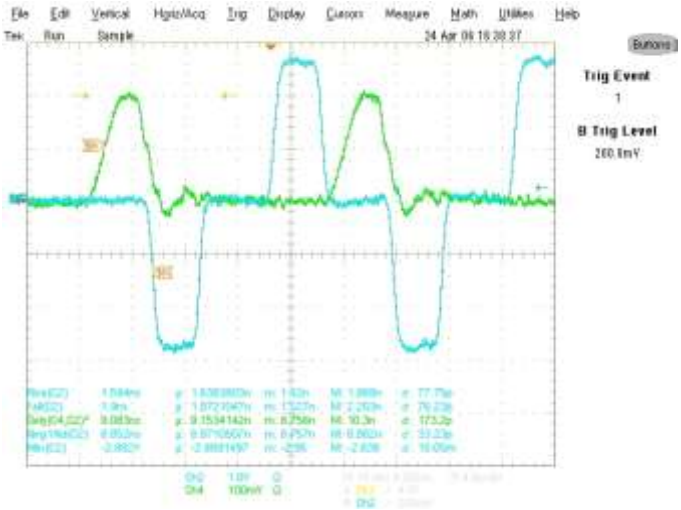

Figure 14: 8.5 ns pulses, 44 MHz chopping
green: input pulse [2 V/div], blue: output pulse [100V/div], abscissa: 10 ns/div

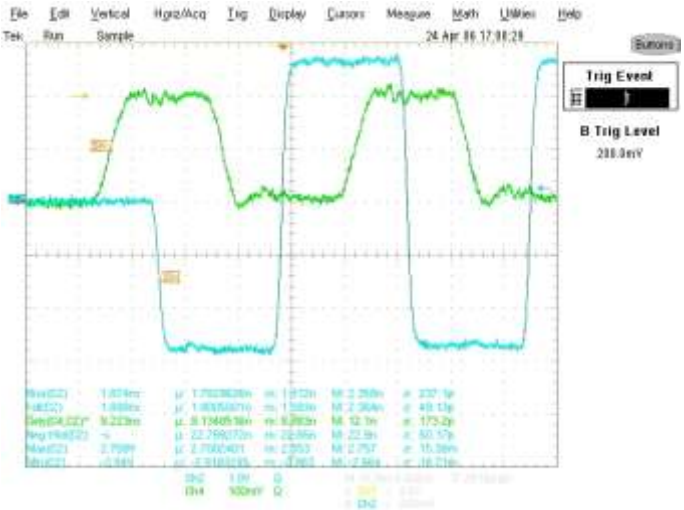

Figure 15: Long bunch sequence chopping.
green: input pulse [2V/div]: blue: output pulse [100V/div], abscissa: 10 ns/div

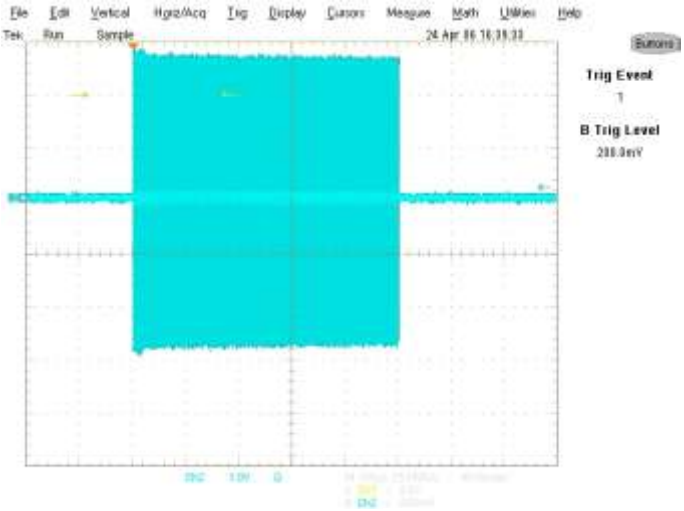

Figure 16: 500 µs burst.
blue: output pulse [100V/div], abscissa: 100 µs/div

The driver delay and pulse length distortion are very important parameters to synchronize the driving signals to the beam. Data plotted in Fig. 17 shows that after the third pulse, the pulse length distortion becomes sufficiently stable and variations are limited to ±100 ps.

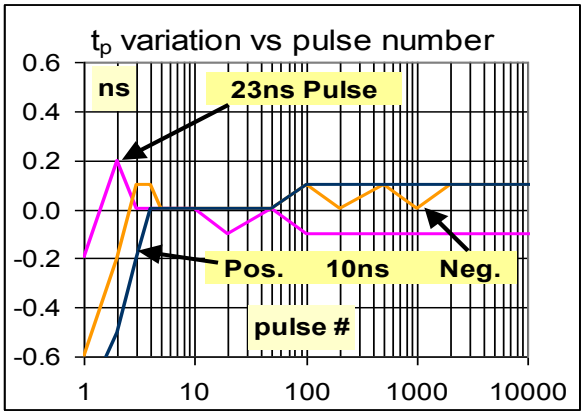

Figure 17: Pulse length distortion within the burst.

The pulse delay plotted in Fig. 18 exhibits variation in the order of ±500 ps (after the 3rd pulse). Moreover, the absolute delay is temperature dependent so that a compensation scheme had to be devised. It is composed of a fast a synchronism detector, an adjustable delay and a digital pulse-to-pulse loop that locks the rising front of the amplifier output pulse to a reference pulse. This compensates slow delay variations (max 30 ps/pulse) over a 10 ns range at working frequency up to 25 MHz. Fig. 19 shows the compensation effect on a test circuit.

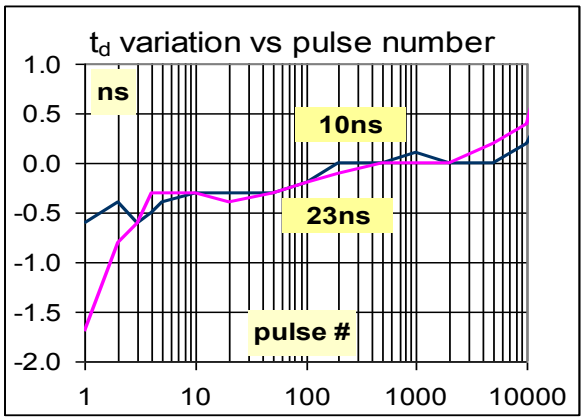

Figure 18: Pulse delay within the burst.

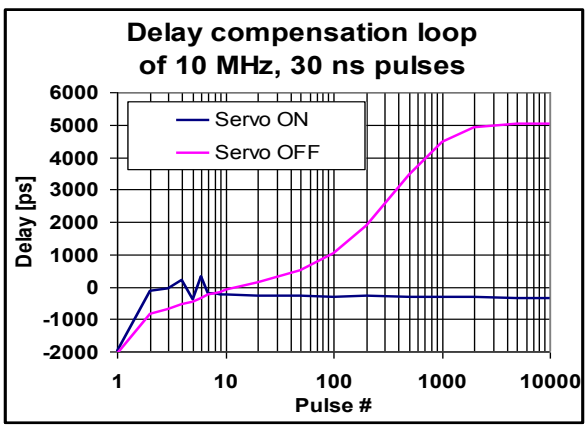

Figure 19: Delay compensation loop.

Driver-industrial option

The CERN driver described above represents a sound solution to the problem of generating the signals for the chopper deflectors. Nevertheless its operation is more complicated when compared to that of a DC coupled amplifier. For this reason, before starting the production of the full set of modules, an additional market survey was carried out with the specification listed in Table 3. The only positive answer to the survey came from FID GmbH, the German branch of FID Technology located in St. Petersburg. A visit disclosed a company highly specialized in very fast, high voltage pulse generators based on a proprietary high voltage, high current device (Fast Ionization Dynistor). The main characteristics are superfast switching (<1 ns current rise time), very low resistance and excellent reliability due to uniform current distribution across the device junction. The company's activities include the design and the production of the semiconductor devices as well as their integration into operational pulse generators. The order was placed beginning 2006 for delivery within 12 months but design difficulties and reliability problems delayed the contract completion and presently only one positive output polarity and one negative output polarity prototypes are in house. The present version generators only partially fulfill the specifications as listed in Table 3.

Table 3: Specifications and present status of FID commercial driver.

PARAMETER	REF.	SPEC.	ACHIEVED
Output signal			
Output voltage	V_{out}	700 V	670 V
Load impedance	Z_{out}	50 Ω	OK
Pulse length	T_{Wout}	8 ns to 1 μs	OK
Minimum off pulse time	T_{off}	14 ns	40 ns
T_{off} dep. on T_{Wout}		No	OK
T_{off} dep. on rep. freq.		No	OK
Propagation delay time	T_D	<500 ns	<100 ns
T_D dependent on T_{Wout}		No	No
T_D dep. on rep. freq.		No	Yes
Pulse dist. | T_{Wout} - T_{Win}|	Pd	<5 ns	<3 ns
T_{Pd} dep. on T_{Wout}		No	Yes
T_{Pd} freq.		No	Yes
Maximum rep. freq.	f_{max}	45 MHz	10 MHz
Minimum rep. freq.	f_{min}	Single pulse	OK
Maximum burst length	T_B	1 ms	1 ms
Maximum burst rep. freq.	f_{Bmax}	50 Hz	50 Hz
Rise time (10 % - 90)	T_R	<2 ns	<2.5 ns
Rise time (3 % - 90)	T_{RR}	<2.5 ns	<3 ns
Fall time (90 % - 10)	T_F	<2 ns	<2.5 ns
Fall time (90 % - 3)	T_{FF}	<2.5 ns	<3 ns
Max. voltage between two pulses	$\|V_n\|$	<2 % of V_{out}	<2 %

Tests to prove the reliability of the semiconductor devices were made on a preliminary unit that was continuously operated during two weeks producing 1 MHz, 300 ns pulses in 1 ms

bursts repeated at 50 Hz. The configuration of the unit was based on a single serial switch that got close to the required transition times but unfortunately could not quite reach the specification. The present version pulse generator is built with a different configuration based on a series and a parallel device 1used to start and stop the pulse. These units exhibit a much better rise time, pulse distortion stability and pulse delay stability but with poor reliability. Problems are thought to come from the triggering electronics, which in some situations (i.e. at power turn off) fire simultaneously the two devices that destroy each other. Improved triggering modules are being installed in the positive output unit. Should they prove effective they will be adopted for the whole production.

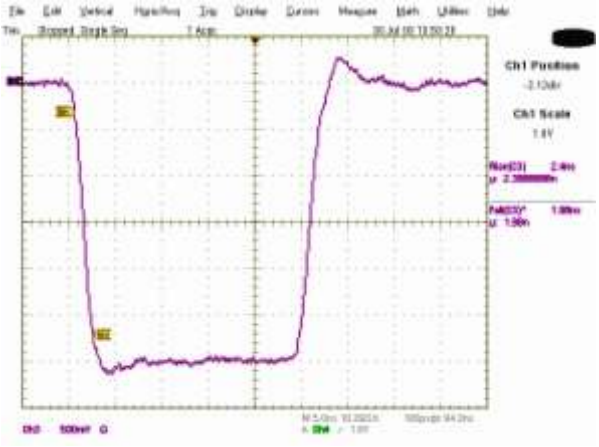

Figure 20: Negative pulse on 50 Ω load
100V/div, 5 ns/div

The design and production of a new version is being carried out and delivery is expected for the end 2008. Fig.20 shows the output pulse of the negative polarity generator when loaded on a 50 Ω load. Fig. 21 shows the waveforms at the chopper input and output ports. The amplitude attenuation and the effects on the fronts are quite evident as well as the effect of the meander line mismatch that produces reflections. Although significant in the plot, this effect can be easily compensated by a fine adjustment of the load impedance.

Figure 21: Chopper input and output waveforms
Yellow: chopper input, red: chopper output, 100 V/div, 10 ns/div

Further information on the CERN chopper driver can be found in [11,12,13]

Hardware – Chopper B

Fast Pulse Generator

A block schematic of the high voltage pulse generator system for the FETS beam chopper is shown in Figure 22.

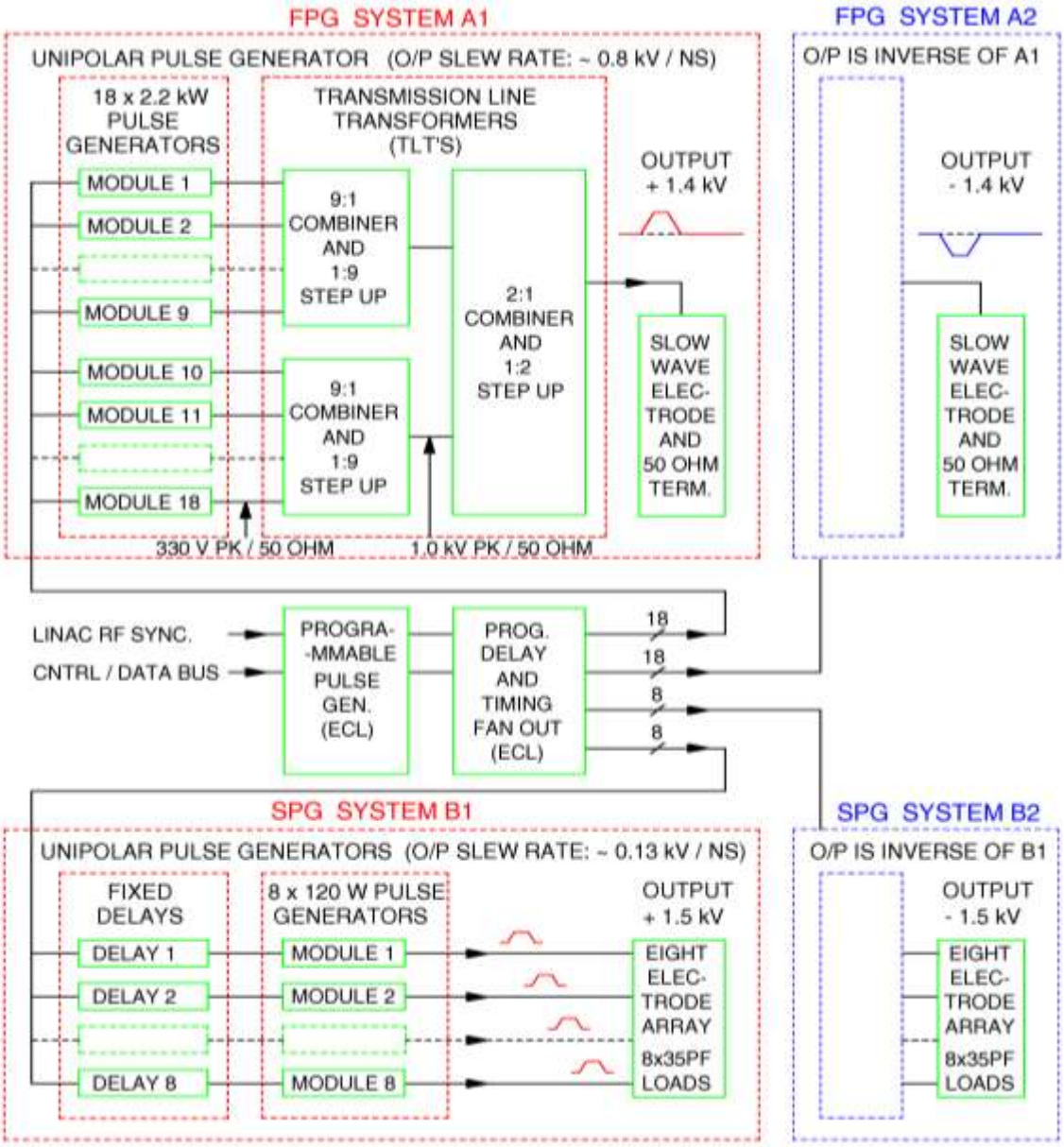

Figure 22: Fast and slow pulse generator block diagram

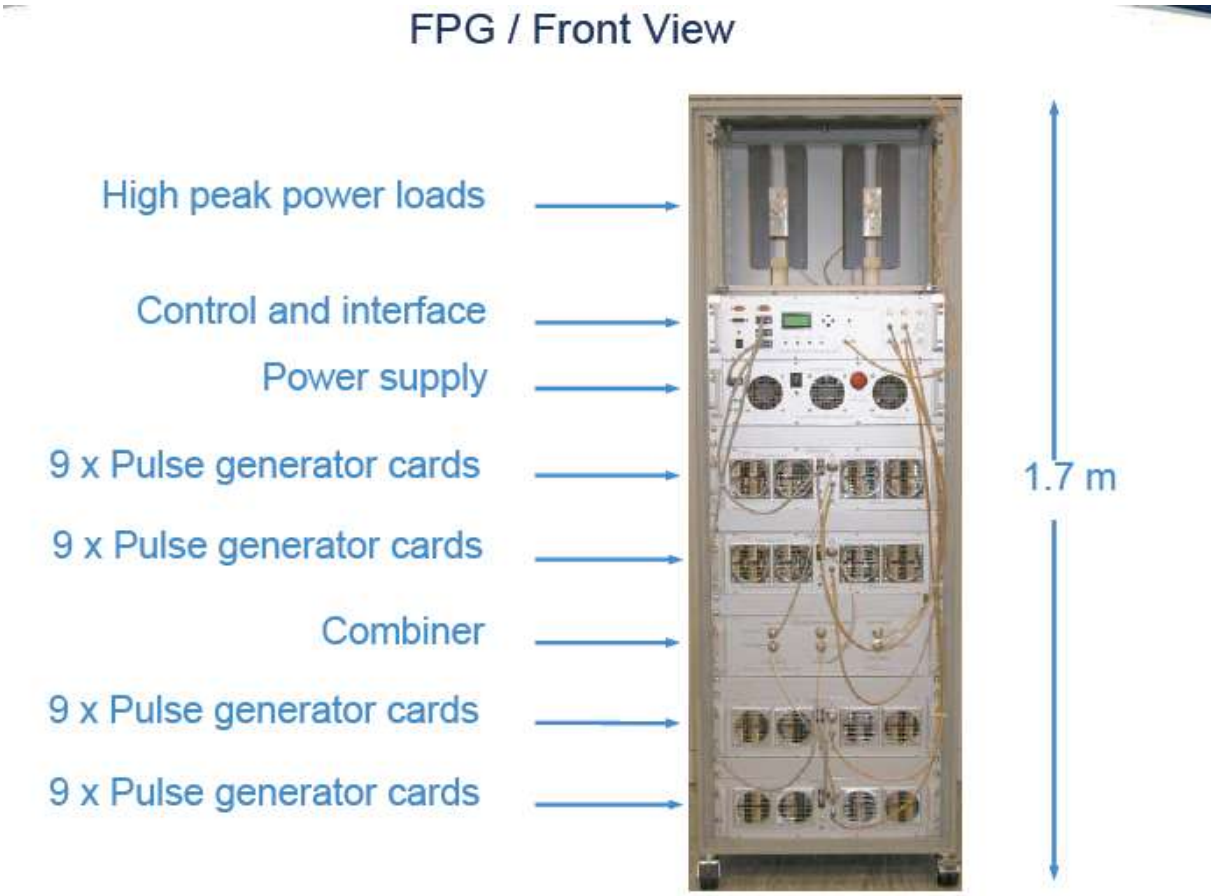

Figure 23 The FPG

The FPG is a high voltage pulse generator (Fig 23) , designed and manufactured in the UK [14], to meet the specification for the previous ESS fast chopper [15]. Measured performance parameters as shown in Table 4, and Figures 24 shows the results of the measurements done at RAL. The results indicate that the design is generally compliant with the RAL FETS requirements. However, the AC coupled unipolar nature of the FPG, places an upper limit on output pulse duration, and introduces a low frequency (LF) cut-off and duty cycle dependent shift in baseline potential, as shown in Figure 25. A scheme to compensate for the duty cycle induced baseline shift, for the case of a fixed or slowly varying duty cycle, has been described [10], and indicates that the resulting residual baseline shift due to LF cut-off can be balanced around the zero volt level, giving values of ± 1.5 % for five bunch chopping in the FETS MEBT. For the case of a rapidly varying duty cycle, duty cycle induced baseline shift can be eliminated, by utilising an FPG with a bipolar output pulse, resulting in alternate beam bunches, or sets of beam bunches, being deflected, in opposite directions [16].

Table 4: FPG / Measured performance parameters

Parameters		Parameters	
Pulse amplitude	± 1.5 kV	Pulse repetition freq.	2.6 MHz
Load	2 x 50 Ω	Burst duration	1.5 ms
Duty cycle	0.27 %	Burst repetition freq.	50 Hz
Transition time	≤ 2.0 ns	Timing stability (1 hour)	± 50 ps
Pulse duration	10-15 ns	Burst amplitude stability	+10, -5 %
Pulse droop	2% in 10 ns	Post pulse aberration	± 5 %

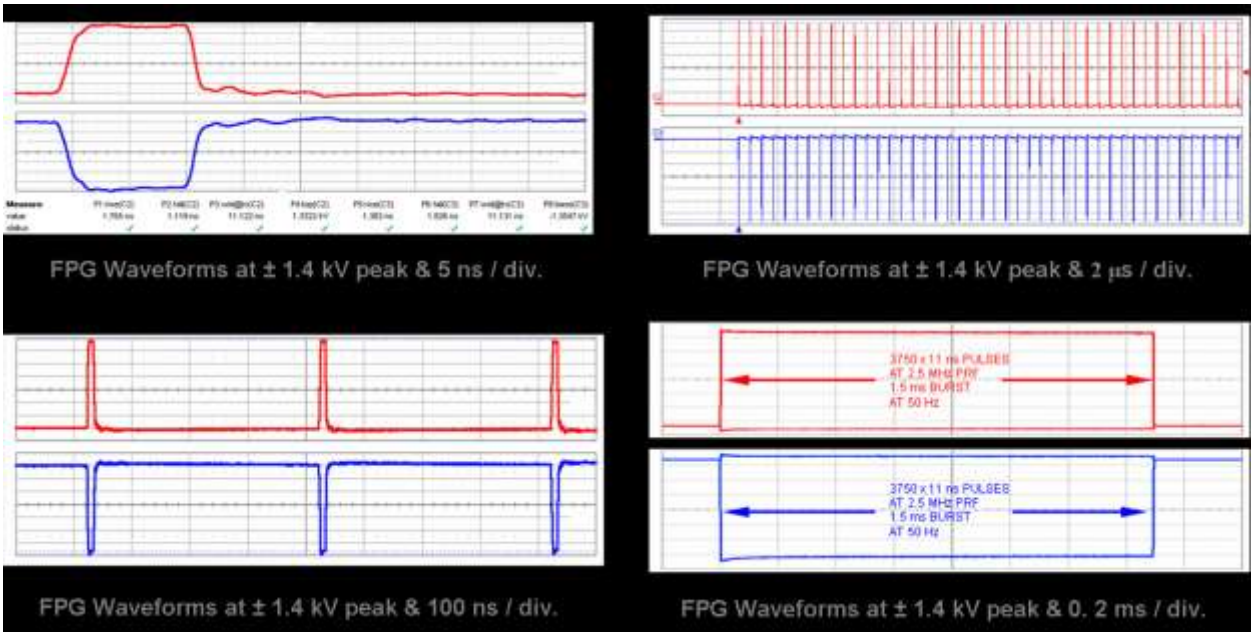

Figure 24: FPG waveforms at ± 1.4 kV peak

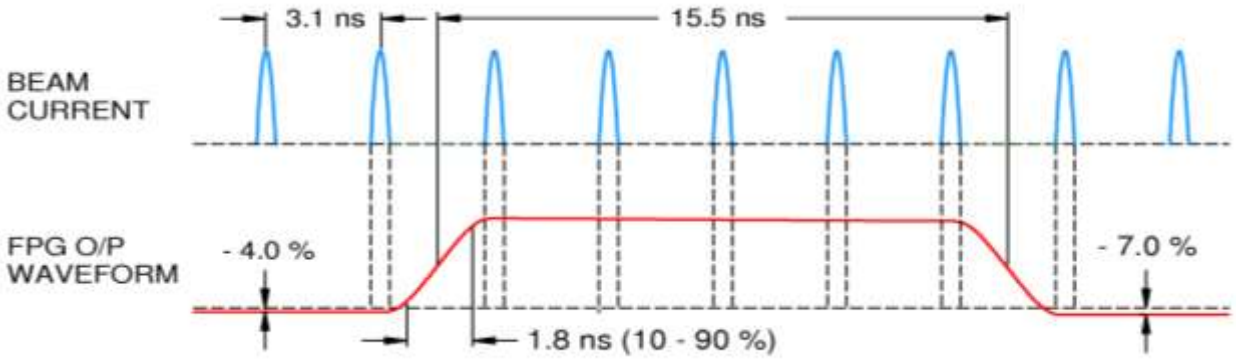

Figure 25: FPG baseline shift for five bunch chopping

Slow Pulse Generator

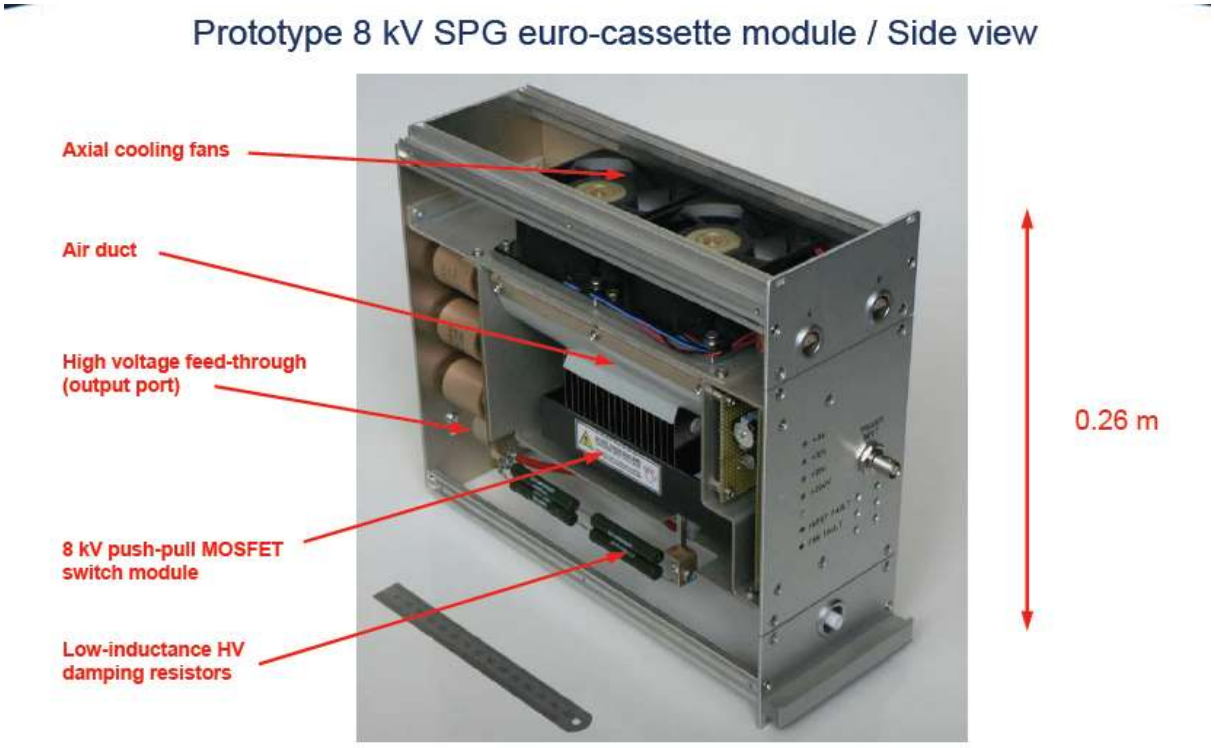

Figure 26 The Slow Pulse Generator

The FETS SPG is a DC coupled high voltage pulse generator, based on an 'off the shelf', 'push-pull' high voltage MOSFET switch module Fig. 26 and [17]. Previous measurements of the performance of an 8 kV rated switch had shown that when operated at 6 kV, pulse transition times increased, and durations decreased, during the first 20 us of the burst, characteristics that were significantly non-compliant with the ESS SPG specification [18]. However, the new 'Scheme A' optical design for the FETS MEBT significantly lowers the SPG voltage requirement from ± 6.0 to ± 1.5 kV, and consequently, the most recent measurements have been made on a lower voltage, 4 kV rated MOSFET switch [17]. Measured parameters as listed in Table 5, and output waveforms as shown in Figures 27, , show that the switch performance is generally compliant with the FETS specification at a burst repetition frequency (BRF) of 25 Hz. A power supply and cooling upgrade should enable testing at the full BRF of 50 Hz. Measurement of pulse duration during the burst, as shown in Figure 29, indicates that there is a step change in the pulse duration between the first pulse in the burst and subsequent pulses, and that the change in duration between the second pulse in the burst and subsequent 500 pulses is then, less than ~ 1 ns. Although these shifts in pulse duration are not compliant with the required specification, they can be corrected by a programmable compensation technique.

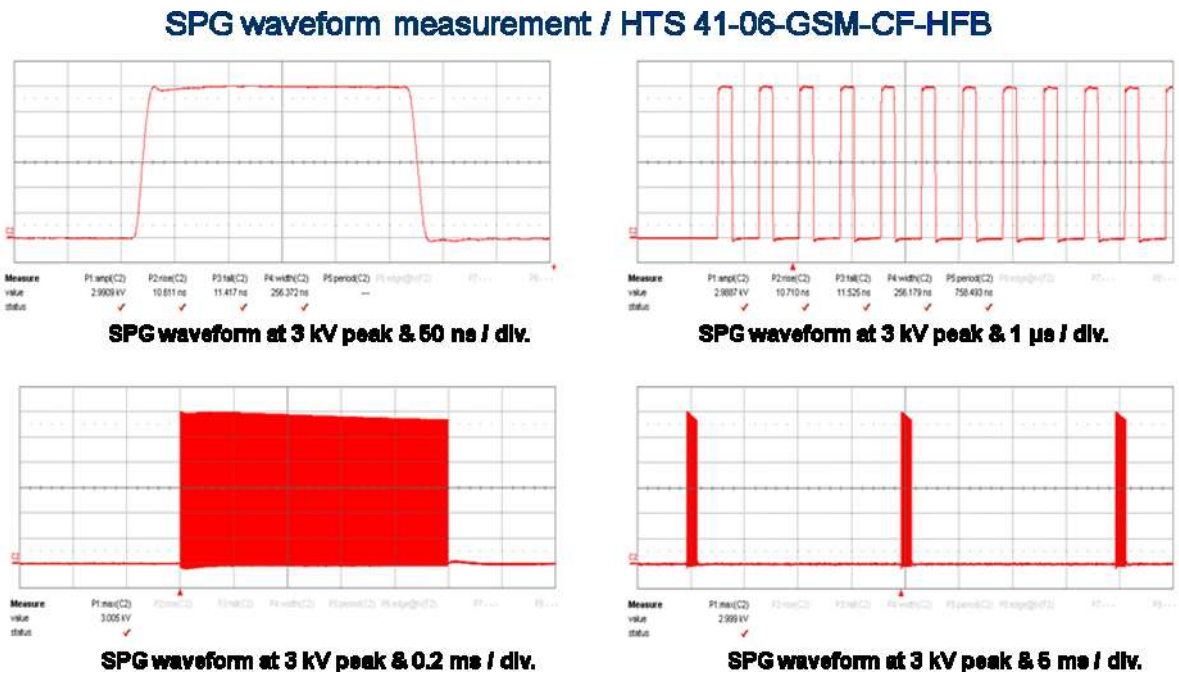

Figure 27 : SPG waveform measurements

Table 5: SPG / Measured performance parameters

Parameters		Parameters	
Pulse amplitude	4.0 kV	Pulse repetition freq.	1.3 MHz
Load	20 pF & 50 nH	Burst duration	1.0 ms
Duty cycle	1.7 %	Burst repetition freq.	25 Hz
Transition time	≤ 12.0 ns	Timing stability (1 hour)	± 0.3 ns
Pulse duration	0.17-100 µs	Burst amplitude stability	< +10, -5 %
Pulse droop	DC coupled	Post pulse aberration	< ± 5 %

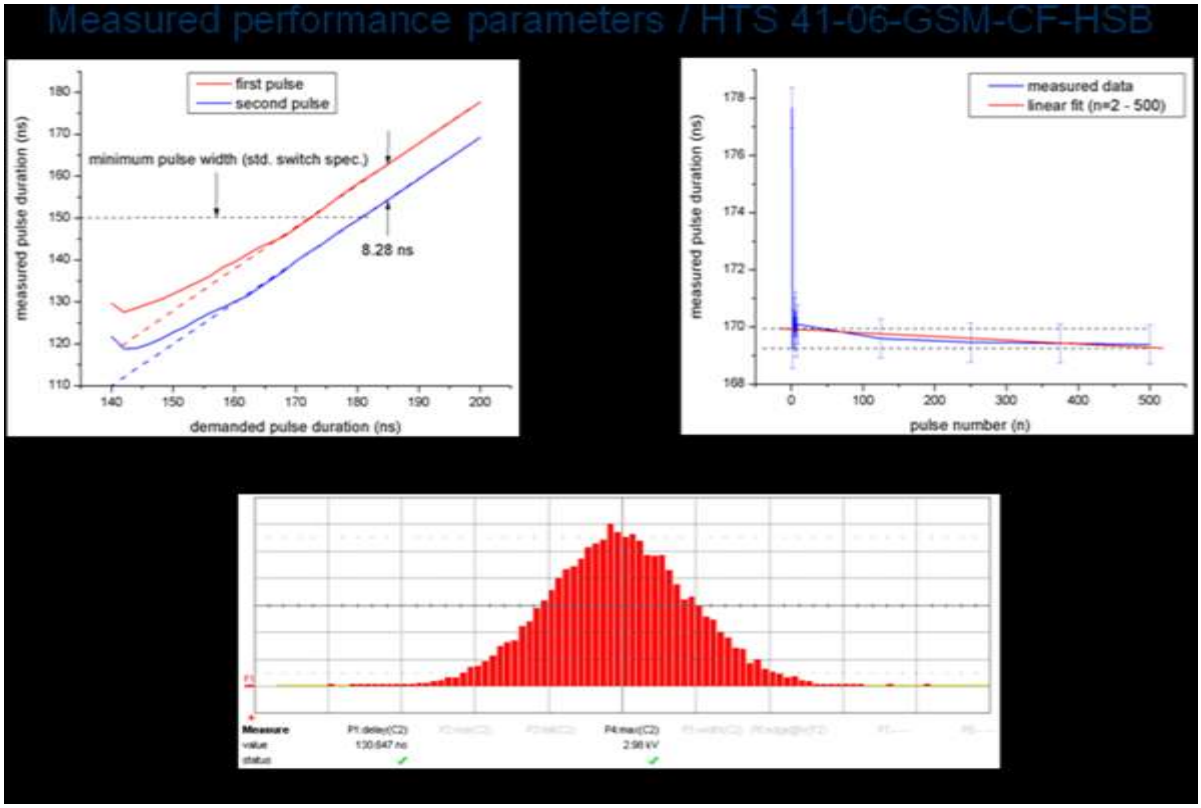

Figure 28 :

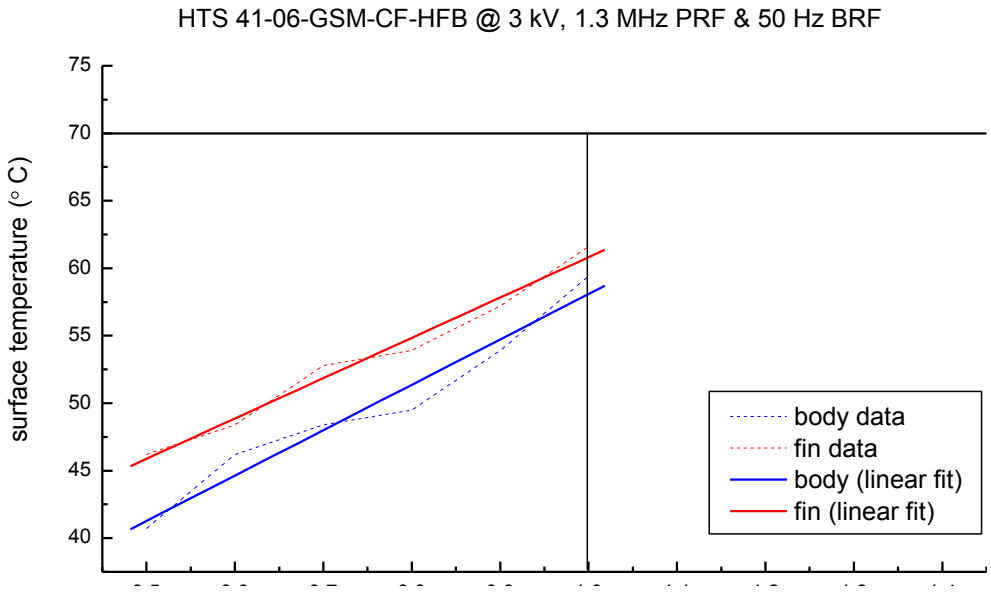

Figure 29

Measured performance parameters compared to FETS specification, as listed in Figure30, indicate that the design is generally compliant with the FETS specification. Passive techniques to reduce post-pulse aberration can be implemented when the precise configuration of the load circuit is determined. A compensation scheme to reduce the duty cycle induced baseline shift in potential to 1.5 % of peak pulse amplitude has been identified.

Measured performance parameters compared to FETS specification, for the SPG as listed in Figure 30, indicate that the 4 kV rated switch is generally compliant with the RAL FETS specification. The new 'Scheme A' optical design for the FETS MEBT significantly lowers the SPG voltage requirement to ± 1.5 kV for a bipolar, or 3.0 kV for a unipolar SPG implementation. The results of the 4 kV SPG tests indicate that a unipolar implementation of the 'slow' chopper, may now be viewed as a practical possibility.

More details on the RAL FPG and SPG can be found in [19,20,21,22,23]

Pulse Parameter	FETS Requirement	Measured	Compliancy	Comment
Amplitude (kV into 50 Ohms)	± 1.4	± 1.5	Yes	Scalable
Transition time (ns)	≤ 2.0	T_{rise} = 1.8, T_{fall} = 1.2	Yes	10 – 90 %
Duration (ns)	10 - 15	10 - 15	Yes	FWHM
Droop (%)	2.0 in 10 ns	1.9 in 10 ns	Yes	F_{3dB} ~ 300 kHz
Repetition frequency (MHz)	2.4	2.4	Yes	
Burst duration (ms)	0.3-1.5	1.5	Yes	
Burst repetition frequency (Hz)	50	50	Yes	Duty cycle ~ 0.27 %
Post pulse aberration (%)	± 2	± 5	No	Reducible
Timing stability (ps over 1 hour)	± 100	± 50	Yes	Peak to Peak
Burst amplitude stability (%)	+ 10, - 5	+ 5, - 3	Yes	

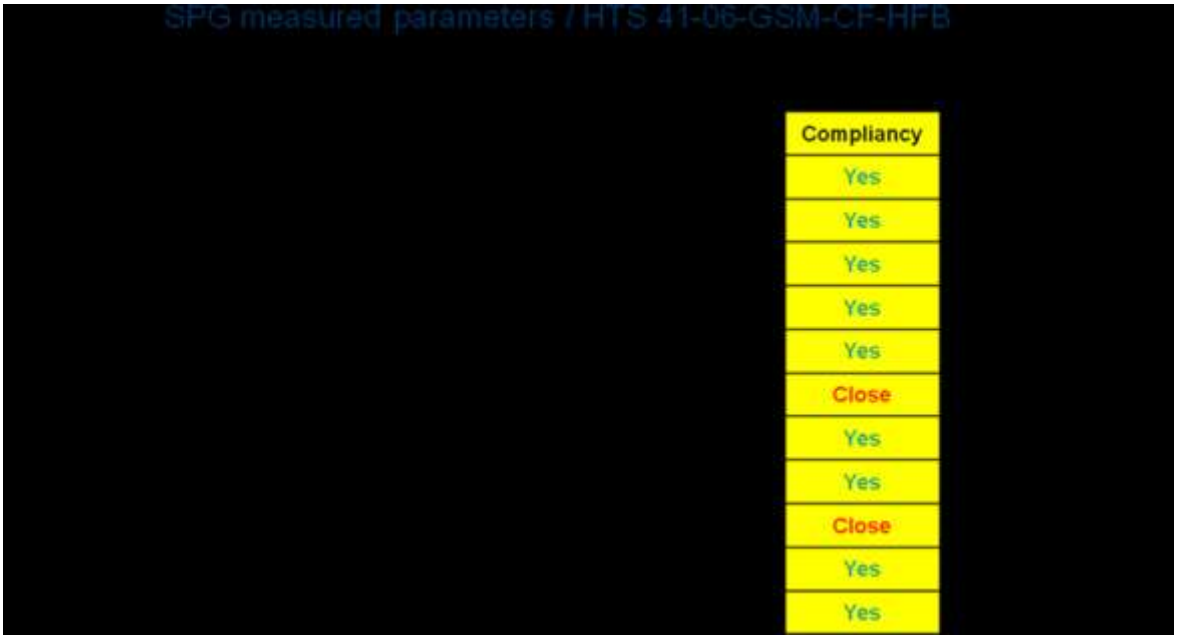

Figure 30 : comparison between FPG and SPG meausred parameters and FETS requirement

Electrode structure design

RAL has developed 3 different electrodes structures : coaxial, planar and helical [ref]. For test assemblies. The manufacture and test of these preliminary assemblies will provide important information on the following:

Accuracy of the 3D high frequency design code.
Construction techniques.
NC machining and tolerances.
Selection of machine-able ceramics and of copper and aluminium alloys.
Electroplating and electro-polishing.

The motivation to develop an alternative to the CERN electrode design is to to improve on the transverse field uniformity, the overall coverage factor and also to investigate the upper frequency limit for a s-w structure and to address a possible differential thermal expansion issue. A sketch of the helical electrodes is shown in Figure 31. A comparison of the effective field is shown in Figure 32 : the RAL helical structures offers a higher field homegeneity as well as a higher coverage factor.

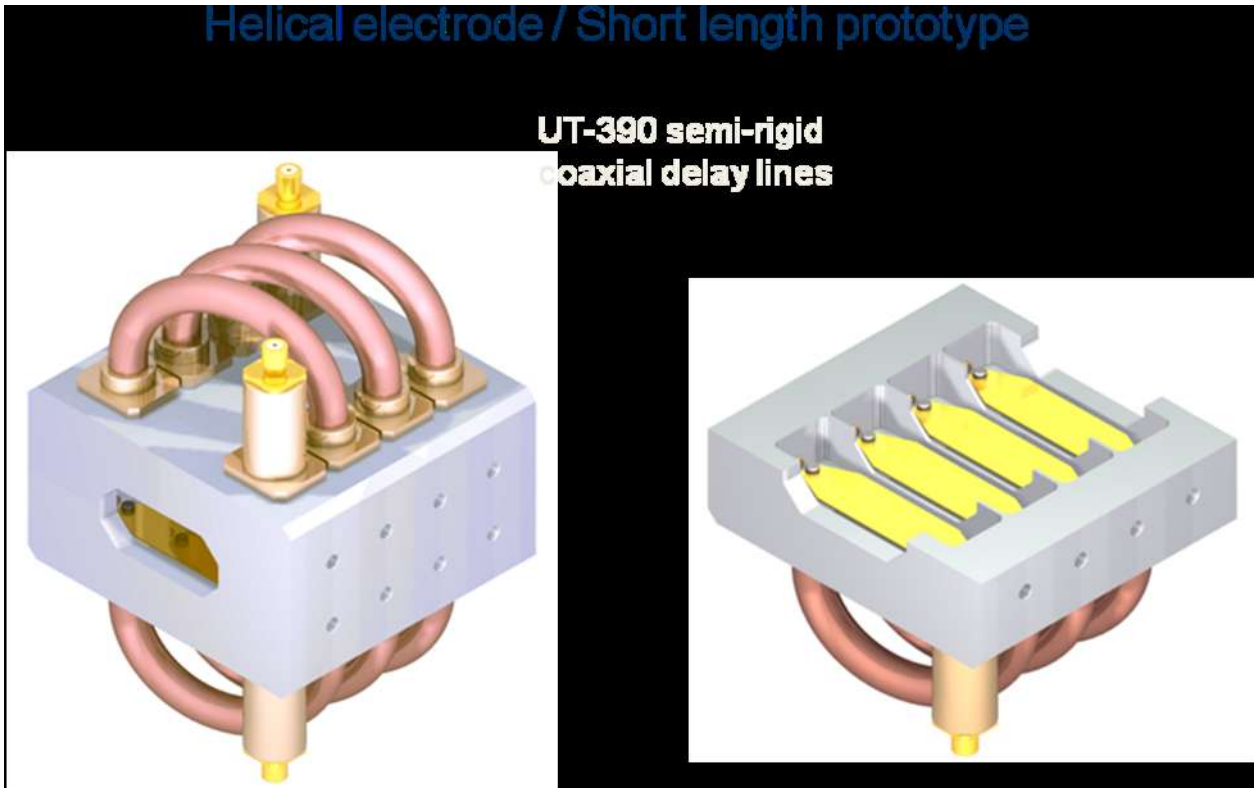

Figure 31 Helical electrode, short lenght prototype

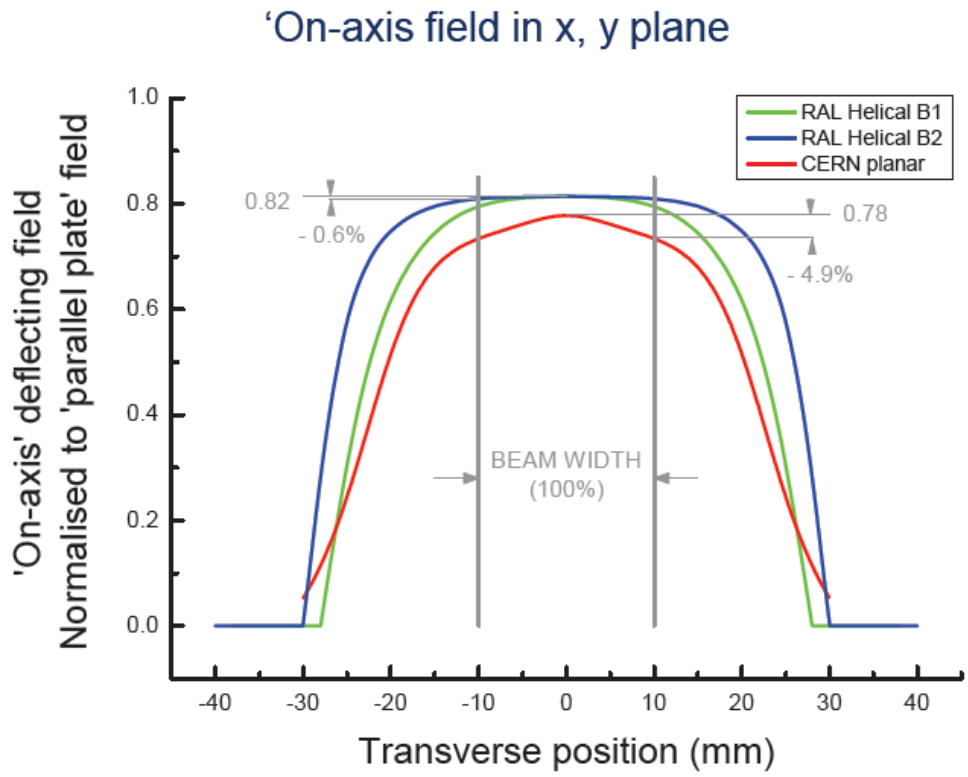

Figure 32 Comparison of on-axis field for different electrodes design.

Conclusions

The work performed in WP4 has produced important experimental data on the characterisation of two different chopping systems. The technological choices taken during the development of the work are appropriate for the respective field of application of the two choppers. The work towards ultimate performance will continue as the parameters to be improved have been identified. Finally a test with beam, not possible during the HIPPI period due to external conditions, will be performed in the CERN 3 MeV test stand and at the RAL FETS.

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Acknowledgements

We acknowledge the support of the European Community-Research Infrastructure Activity under the FP6 "Structuring the European Research Area" programme (CARE, contract number RII3-CT-2003-506395)