16 July 2002

Production Readiness Review

ATLAS E.M. CALORIMETER

BIMUX ASIC

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1 Chip description.

1.1 Layout.

This circuit is a programmable 8 channels analog bi-multiplexer :

- The dynamic linear range extends from +2 V to –3 V.
- The programmable memory is a read-write 3 bits data register.

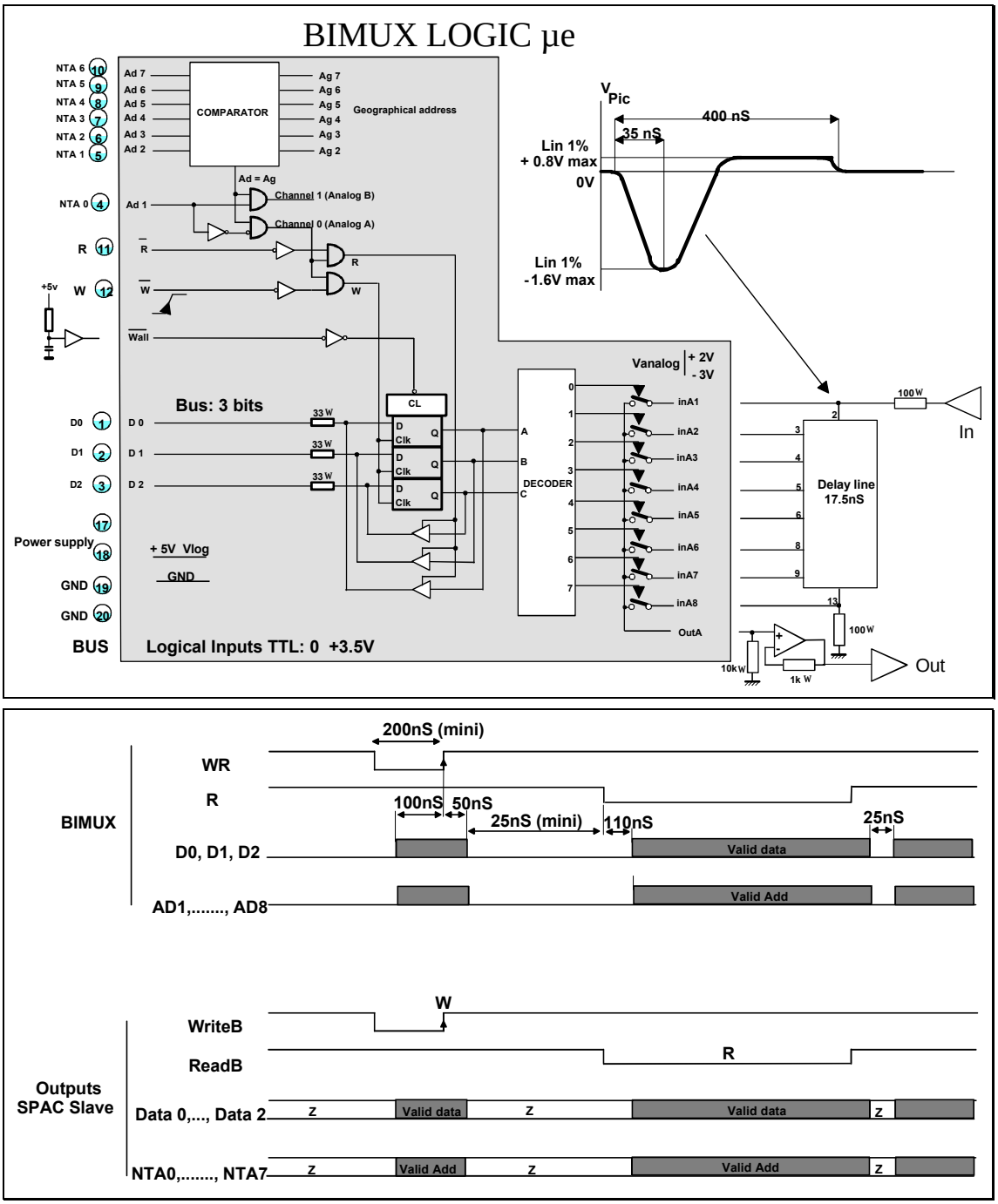


Figure 1 : Schematic diagram of one half of the *BiMux* chip, and timing for reading and writing in *BiMux* registers.

- The logic includes a geographic address decoder.
- The inputs are all protected against electrostatic discharges.
- The package is connected to the ground.
- The design is carried out on DMILL, a rad-hard technology.
- Two circuits are implemented on a single chip.
- The package used is a PQFP 44.

The general scheme of the Bimux is given in figure 1, and a selection of electrical schemes in annexe (figures 13 to 16).

The register, the demultiplexer and the analog switches are duplicated in the chip and are selected by the external bus address Ad1. They are called A and B.

1.1.1 The logic part

All the logic parts described below are powered by +5 V power supply.

The comparator.

It compares the 6 bits of the geographic board address (Ag2 to Ag7) with the 6 input bus adresses (Ad2 to Ad7), provided from an external controller. It allows to select one among the 64 Bimux chips of the Tower Builder Board (TBB). If the comparison is valid, the chip is selected and one can write or read in one of the two data registers. The Ad1 bus address selects which of the two data registers (A or B) is selected.

The data register.

It is composed of 3 D flip-flops in which 3 bi-directional buses are connected (D0 to D2).

The decoder.

It is an 8 bits binary decimal decoder. At the output of the decoder there is 8 DC level transfer in order to go to the analog part of the circuit which is powered between +2 V and –3 V.

1.1.2 The analog part.

It is composed of two analog multiplexers with 8 inputs (InA1 to InA8 and InB1 to InB8) and 1 output (OutA and OutB). Each input is connected to one CMOS analog swich. The output is the OR of all analog switches.

1.2 Pin-out.

The pin-out is given in the table below and is shown in the figure 2 :

Pin number	Name	Description	Voltage range
1	InB4	Analog input 4 of B multiplexer	+2 V / –3 V
2	InB3	Analog input 3 of B multiplexer	+2 V / –3 V
3	InB2	Analog input 2 of B multiplexer	+2 V / –3 V
4	InB1	Analog input 1 of B multiplexer	+2 V / –3 V
5	InB0	Analog input 0 of B multiplexer	+2 V / –3 V
6	+5V	Logical power supply	+5 V (+5.5 V max)
7	InB7	Analog input 7 of B multiplexer	+2 V / –3 V
8	D2	Bit 2 of bi-directional data register (for analog input selection)	0 V / +5 V
9	D0	Bit 0 of bi-directional data register (for analog input selection)	0 V / +5 V
10	/W	Write command signal (complement)	+5 V / 0 V

11	Ad1	Bit that selects the A or B multiplexer (input)	0 V / +5 V
12	Ad2	Bit 2 of chip select address (input)	0 V / +5 V
13	Ag2	Bit 2 of chip geographical address (input)	0 V / +5 V
14	Ad3	Bit 3 of chip select address (input)	0 V / +5 V
15	Ag3	Bit 3 of chip geographical address (input)	0 V / +5 V
16	Ad4	Bit 4 of chip select address (input)	0 V / +5 V
17	Ag4	Bit 4 of chip geographical address (input)	0 V / +5 V
18	Ad5	Bit 5 of chip select address (input)	0 V / +5 V
19	Ag5	Bit 5 of chip geographical address (input)	0 V / +5 V
20	Ad6	Bit 6 of chip select address (input)	0 V / +5 V
21	Ag6	Bit 6 of chip geographical address (input)	0 V / +5 V
22	Ad7	Bit 7 of chip select address (input)	0 V / +5 V
23	Ag7	Bit 7 of chip geographical address (input)	0 V / +5 V
24	/R	Read command signal (complement)	+5 V / 0 V
25	D1	Bit 1 of bi-directional data register (for analog input selection)	0 V / +5 V
26	/Wall	Write command signal in A and B regeisters (complement)	+5 V / 0 V
27	InA7	Analog input 7 of A multiplexer	+2 V / –3 V
28	GND	Logical ground	0 V
29	InA0	Analog input 0 of A multiplexer	+2 V / –3 V
30	InA1	Analog input 1 of A multiplexer	+2 V / –3 V
31	InA2	Analog input 2 of A multiplexer	+2 V / –3 V
32	InA3	Analog input 3 of A multiplexer	+2 V / –3 V
33	InA4	Analog input 4 of A multiplexer	+2 V / –3 V
34	InA5	Analog input 5 of A multiplexer	+2 V / –3 V
35	InA6	Analog input 6 of A multiplexer	+2 V / –3 V
36	–3VA	Analog negative power voltage for A multiplexer	–3 V
37	OutA	Analog output of A multiplexer	+2 V / –3 V
38	+2VA	Analog positive power voltage for A multiplexer	+2 V
39	LF	Package ground	0 V
40	+2VB	Analog positive power voltage for B multiplexer	+2 V
41	OutB	Analog output of B multiplexer	+2 V / –3 V
42	–3VB	Analog negative power voltage for B multiplexer	–3 V
43	InB6	Analog input 6 of B multiplexer	+2 V / –3 V
44	InB5	Analog input 5 of B multiplexer	+2 V / –3 V

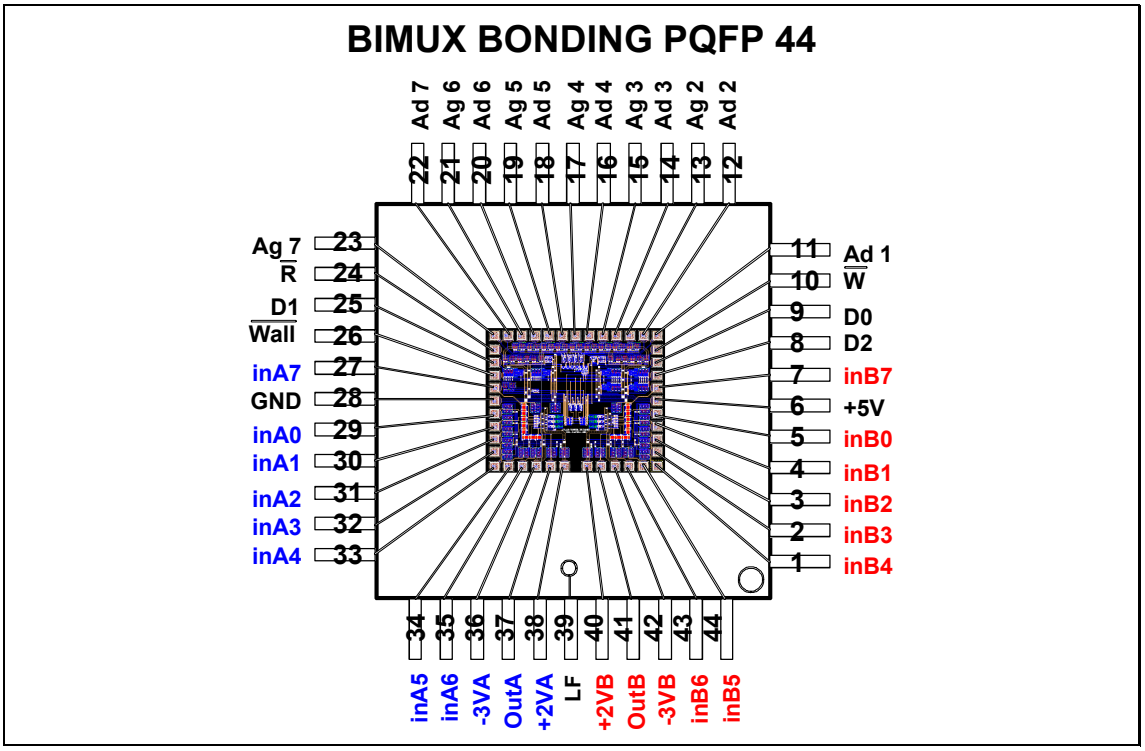


Figure 2 : *BiMux* bonding (top).

2 Pre-production test bench.

For the test of the chip one proceeds in two steps.

2.1.1 Control of the power supply input impedance.

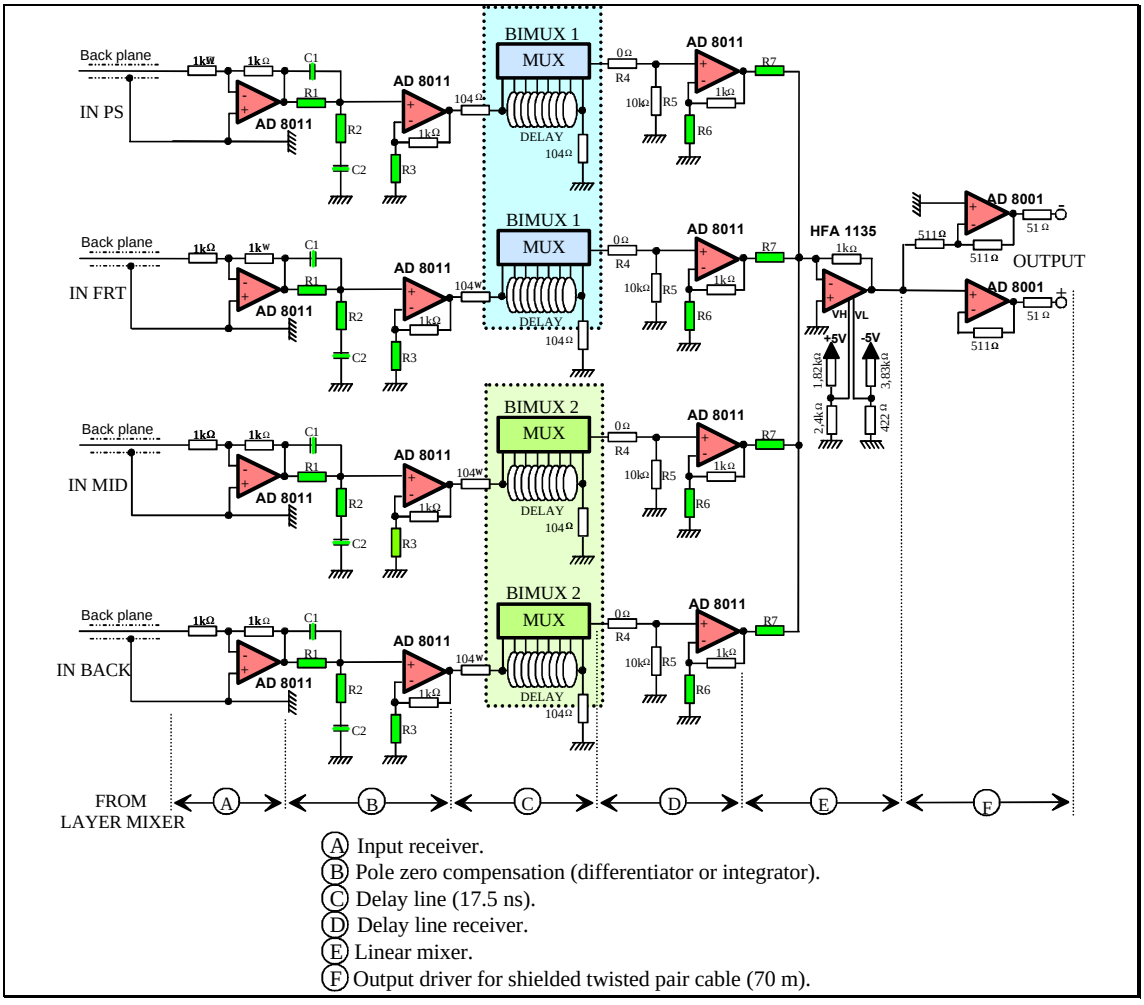
This control is simply done by measuring with an ohmmeter the input impedance of the +5 V used for the digital part of the chip. If the measured value is ≈40 Ω, then the Bimux is out of order. If the measured value is between 2.5 kΩ and 3 kΩ, then the Bimux has no power supply problem.

2.1.2 Control of the digital and the analog parts of the chip.

The test bench is composed of a small board with four channels identical to the final Tower Builder channels. It uses two Bimux. A software written in Labview sends an address and a data with a write command followed by a read command. The data are randomly generated. The read data are compared with the write data and the program sets a flag if there is a mismatch.

The analog channel is tested by applying a standard pulse at each input and reading out the output. During this test the seven delays are successively addressed. One checks that each pulse is delayed in accordance with the corresponding data.

The chips are inserted manually in a socket, so no soldering is required but it remains a relatively lengthy procedure. The test rate is around 30 chips/h. The figure 3 shows the schematic diagram of the test board and the figure 4 a photography.



(A) Input receiver.
(B) Pole zero compensation (differentiator or integrator).
(C) Delay line (17.5 ns).
(D) Delay line receiver.
(E) Linear mixer.
(F) Output driver for shielded twisted pair cable (70 m).

Figure 3 : Schematic diagram of one of the 32 analog summation cells of the TBB.

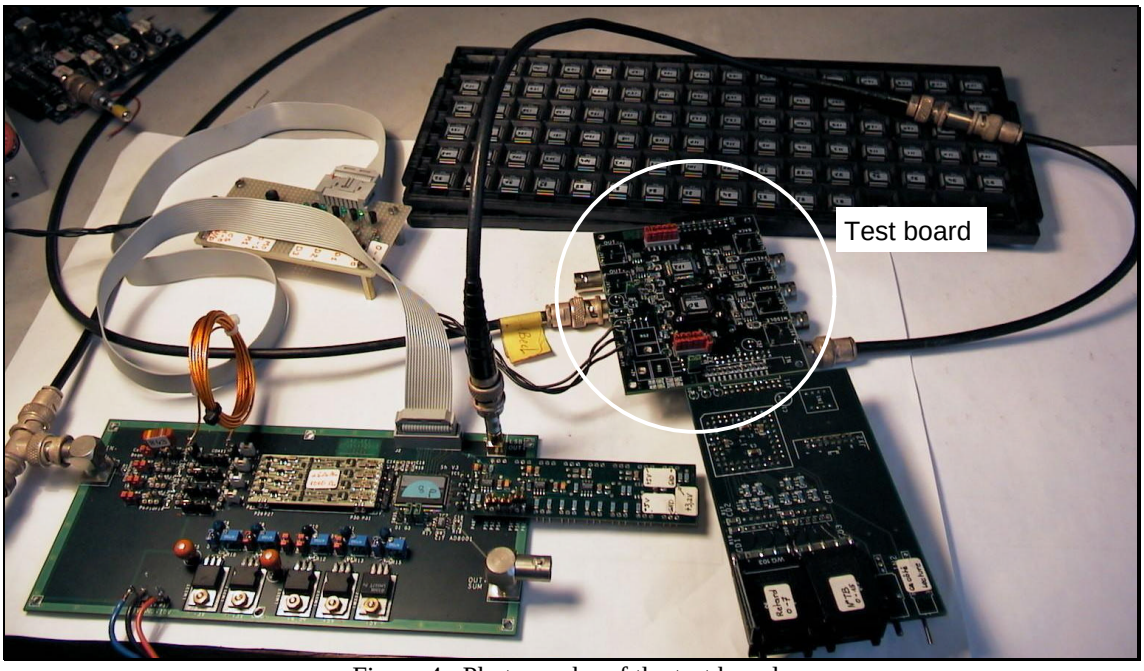


Figure 4 : Photography of the test board.

3 Pre-production test results.

The pre-production was achieved through two runs :

- One took place in December 1998 (MPW 270) and produced a total of 80 PLCC chips with a yield of 85 %. Part of the 15 % failures was due to a short between the +5 V logic power supply pins (12 %), and the rest (3 %) was due to read or write errors in the registers. No failures were found on the analog part of the switches.
- The second run took place in October 2001 (MPW 646) and the packaged PQFP chips where delivered in May 2002. Out of the 268 chips received only one (0.4 %) had a power supply impedence problem. We have then controled the digital and the analog parts of 200 Bimux. 4 Bimux failed (2 %) : 3 in the digital part, and 1 in the analog part. So the total measured yield is 97.5 %.

It has to be emphasized that we introduced absolutely no modification in the layout between the two submissions. At the request of the collaboration we switched from PLCC44 to a PQFP44 package.

4 Irradiation tests.

4.1 Measurement conditions.

4.1.1 Hardware.

Six one-tower TBB boards, of 4 channels each, have been used (see figure 3) :

- one reference board,
- one gamma irradiated board,
- two neutron irradiated boards,
- two proton irradiated boards.

4.1.2 Irradiation conditions.

Three irradiation sources have been used :

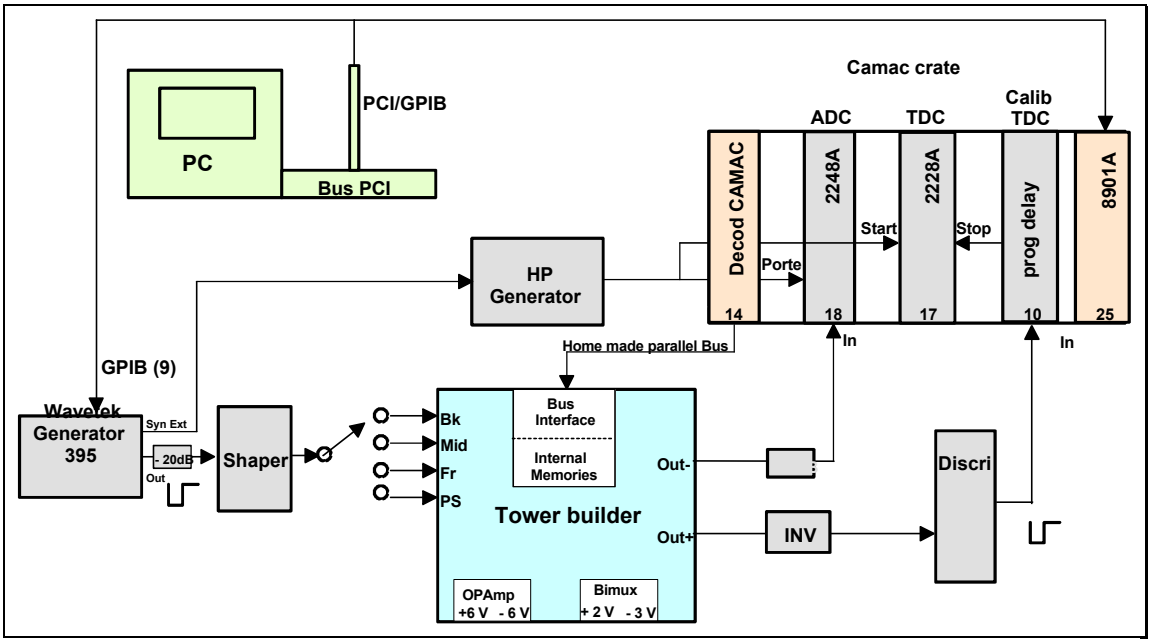


Figure 5 : Schematic diagram of the pre-production test bench.

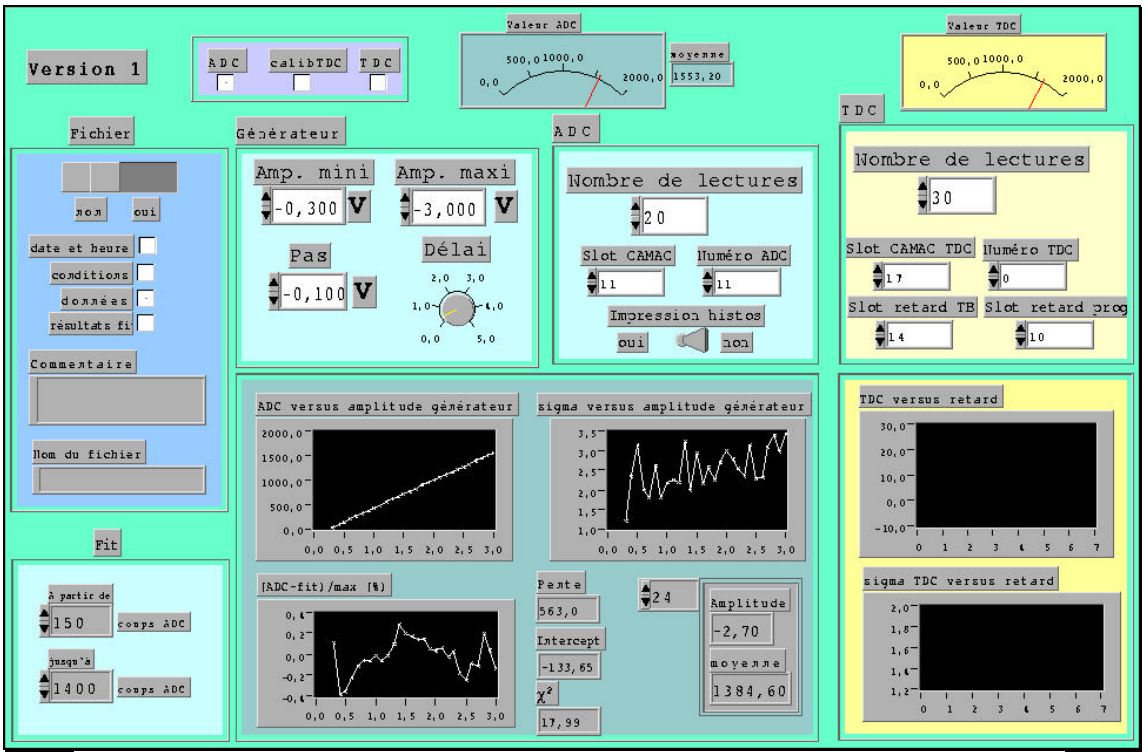


Figure 6 : Display of the PC screen for radiation tests.

- Gamma source at PAGURE (Cobalt 60) :

  0 → 203 krad ; 16 krad / h.

- Neutron source at ULYSSE Saclay (sub-critical reactor).

  Total dose measurements for 1 MeV neutrons :

  a) 1.1×10^{13} n/cm^2 (20/08/99 → 23/08/99).
  b) 3.2×10^{13} n/cm^2 (04/11/99 → 17/11/99).

- Proton source at Louvain-la-Neuve (measurements of SEU and latch-ups) :

  Total fluence for 60 MeV protons : 3×10^{13} protons/cm^2 on each boards.

4.1.3 Expected radiations levels at front end crate location.

- Total gamma dose (10 years) : 5 krad (safety dose 53 krad).
- Gamma dose rate : 0.15 rad/h.
- Neutron total dose (10 years) : 1.6×10^{12} n/cm² (safety dose 5.6×10^{12} n/cm²).
- Proton total dose (10 years) : 7.7×10^{11} p/cm^2 (safety dose 2.7×10^{12} p/cm^2).

4.2 Measurement methods.

For the measurements we use the test bench described in the schematic diagram of figure 5. The test bench is composed of :

- A Wavetek generator which provides an adjustable voltage step.
- An ORSAY built shaper with CR RC² filter. It can deliver pulses with a peaking time of 30 ns (close to the real peaking times of the calorimeters). At the output of the shaper the pulse amplitude was adjusted from 0 to 3 V and was fed successively in each tower builder channel.
- A Lecroy 2248 ADC coded the amplitude of the TBB output.
- A lecroy 2228A TDC coded for the delay between the generator and the TB output.
- A CAMAC system was used to address the delays.

The display of the PC screen is shown in figure 6.

4.2.1 Measurements performed as a function of irradiation.

The measurements were performed for the full circuit in which the Bimux was imbedded. The properties we measured as a function of irradiation were :

- gain,
- output noise,
- power supply currents,
- latch-up,
- SEU.

The measurements were performed on the irradiated boards and on an identical reference board. The comparison between the measured board and the reference board allows to correct for :

- temperature variations,
- power supply shifts,
- ADC shifts,

in the test bench.

4.2.2 Measurements methods.

4.2.2.1 Gain.

To measure the gain for a given channel *n* and for the reference channel we perform a fit on the ADC counts versus increasing input amplitude (0.3 V → 3 V, steps 0.1 V). The gain is the slope of the fit. We plot :

(Tower gain – Reference gain) / Reference gain = f(Irradiation).

4.2.2.2 Output noise.

We use a 10 KHz → 1.2 GHz bandwidth HP RMS voltmeter on both boards. We measure separately the noise of + and – TBB differential outputs. We plot :

(Tower noise – Reference noise)$_+$ / Reference noise$_+$ = f(Irradiation),

(Tower noise – Reference noise)$_-$ / Reference noise$_-$ = f(Irradiation).

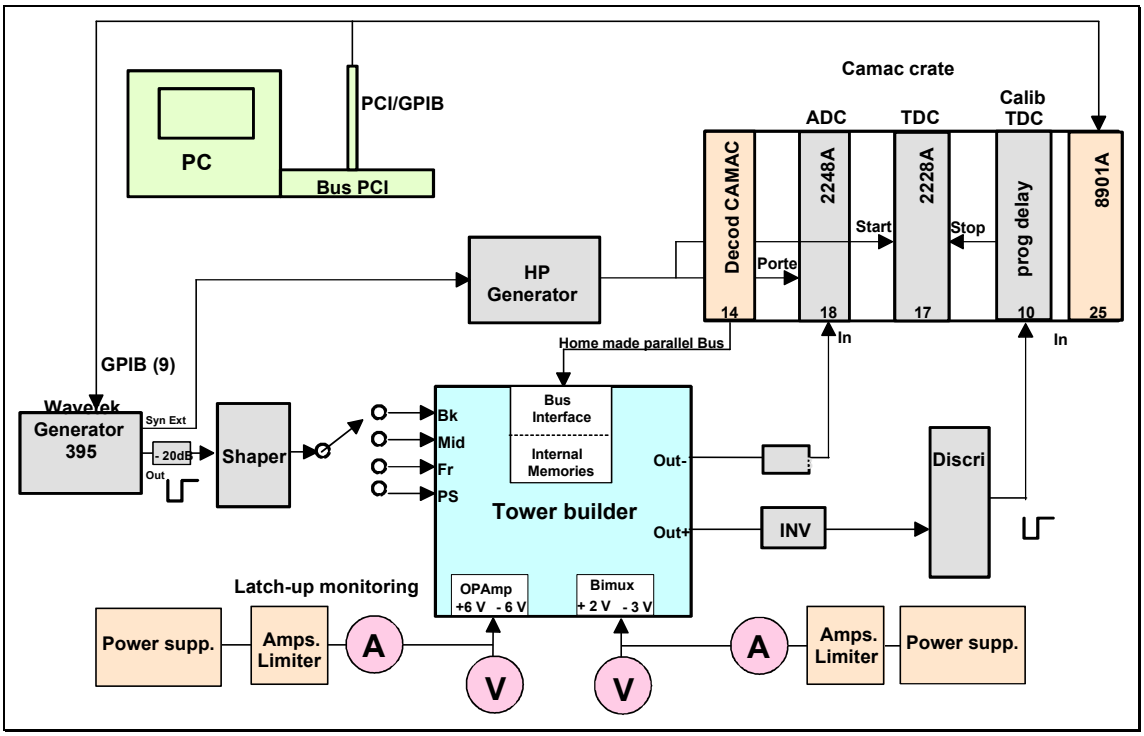


Figure 7 : Irradiation test bench (S.E.U. and latch-up).

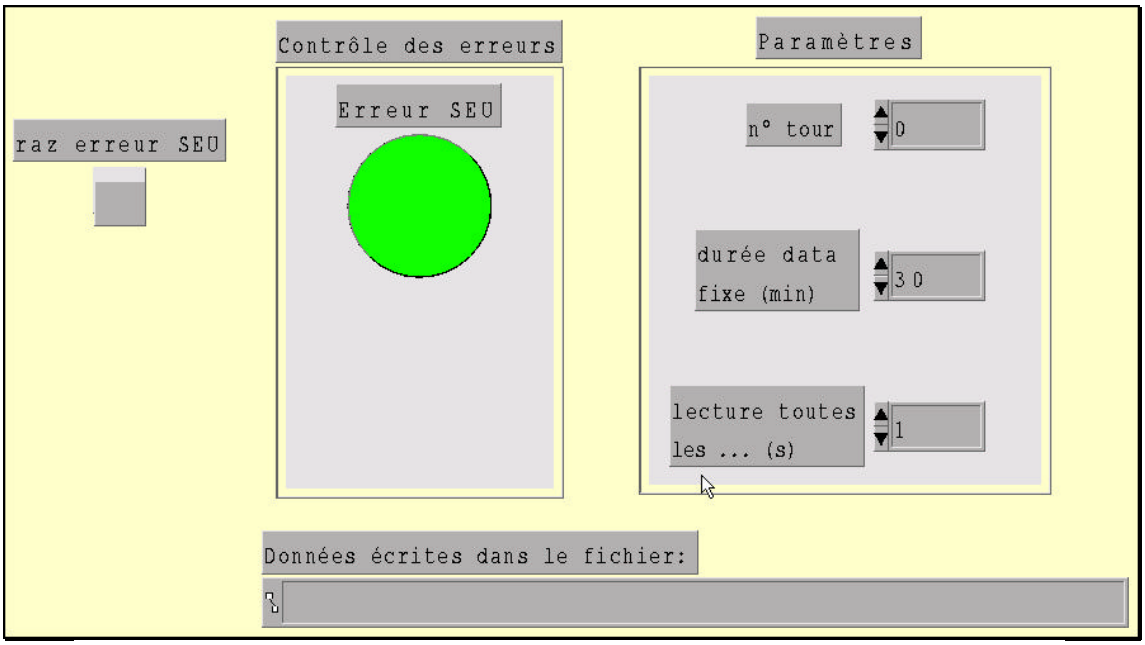


Figure 8 : Labview screen of the irradiation test bench (S.E.U. and latch-up).

4.2.2.3 Power supply currents.

Power supplies are partially separate for the bipolar op. amps and the Bimux DMILL chip :

Op. amps : +6 V, –6 V.
Bimux : +2 V, –3 V, +6 V (logic).

We plot for every voltage :

(Tower power supply – Reference power supply) / Reference power supply = f(Irradiation).

4.2.2.4 Latch-up.

To perform this measurement we used one of our test board (it has two Bimux chips). The Bimux chips were powered with a dedicated power supply which was equipped with a current limiter and a sensitive voltmeter. The current limiter was set slightly (5 %) above the typical current consumption. In case of latch-up on should observe a drop in the voltage.

The voltmeter was monitored versus time.

4.2.2.5 SEU.

Each tower builder has four 3 bits memories for the delay addressing. The test bench was set according to figures 7, and figure 8 shows the PC screen. In case of SEU the green light turned to red. The Labview software performed the following tasks :

- write 0 or 7 every 5 mn,
- read back every 1 seconde,
- compare,
- set alarm if discrepancy.

SEU rate = Number of discrepancies / hour.

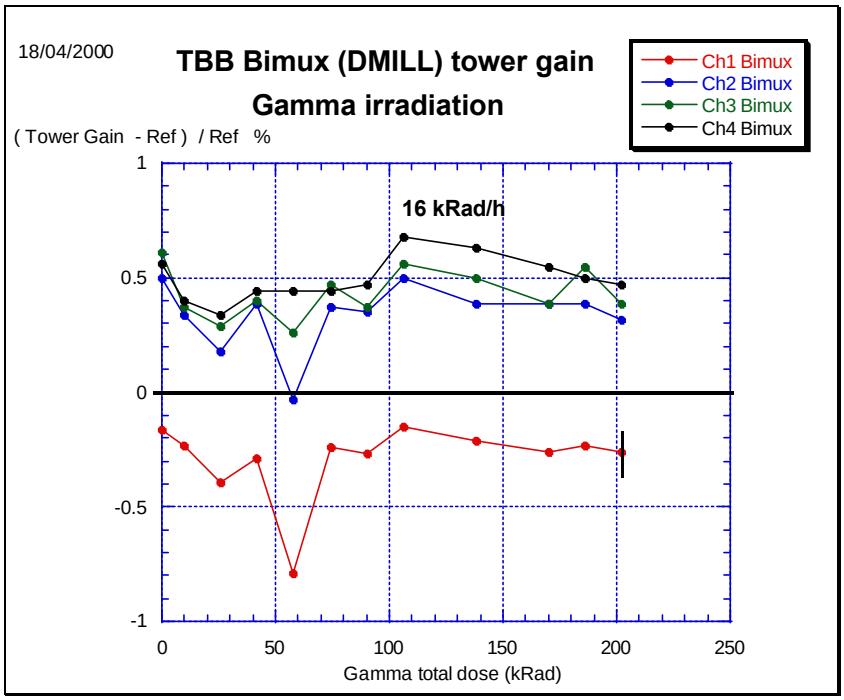
4.3 Gamma results.

The chips were irradiated with their power supply on.

The total dose was 218 krad.

4.3.1 Gain shift.

The gain shift is given in the following figure :

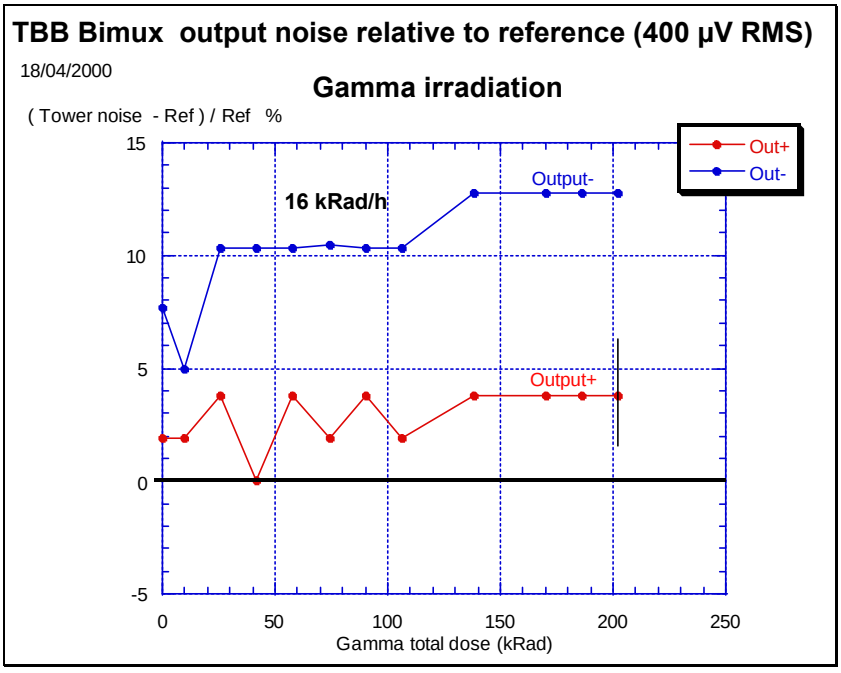


We find : (±0.2 ± 0.1) %.

This implies that the analog amplifiers as well as the analog part of the Bimux are both imune to gamma irradiation. In particular the Bimux, as expected, withstands a dose (200 krad) much higher than the required one (53 krad).

4.3.2 Output noise shift.

The output noise is given in the following figure :

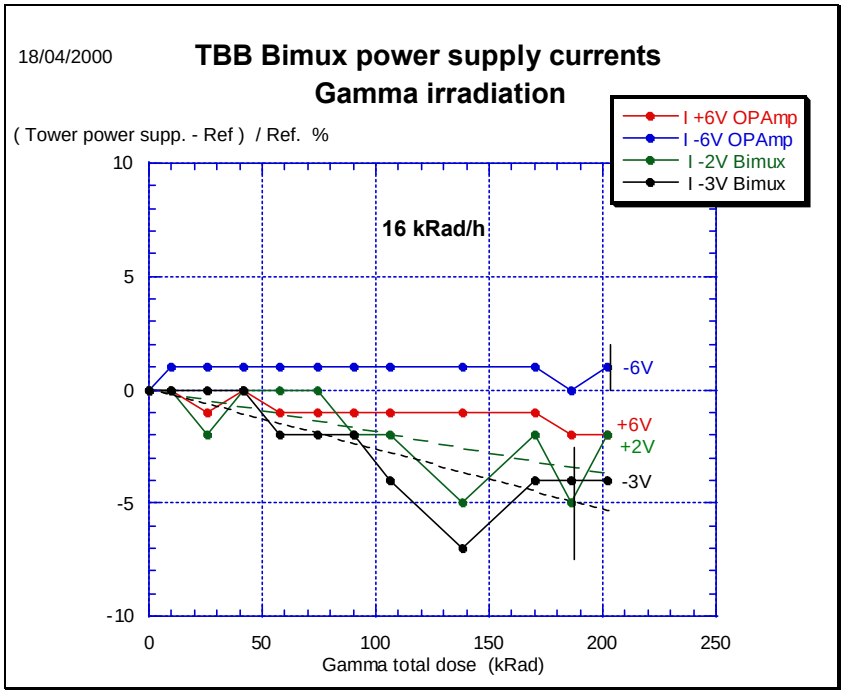


We find : ±3 % output +, ± 4 % output –.

This again implies that the op. amps as well as the analog part of the Bimux are immune to gamma irradiation.

4.3.3 Bimux current shift.

The current shift is given in the following figure :



We find :

- +2 V (–3.5 ± 2.5) % (Bimux analog part, fit, dashed line),
- –3 V (–5 ± 2.5) % (Bimux analog part, fit, dotted line),
- +6 V (–1 ± 1) %. (power supply for the op. amps and the Bimux logic part).

This implies that the op. amps as well as the Bimux are immune to gamma irradiation.

4.3.4 Conclusion.

In the batches used the Bimux analog part is immune to gamma irradiation, as demonstrated by the above measurements. Using the TDC of the test bench we checked this was true by addressing each delay after irradiation. This checked also the digital part of the chip.

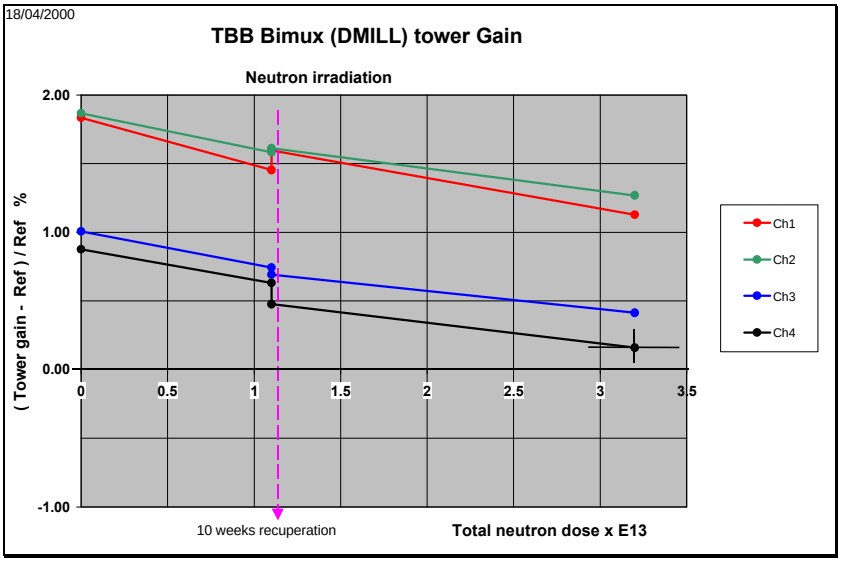
4.4 Neutron dose results.

The chips were not powered during irradiation at Ulysse sub-critical reactor 1 MeV neutrons.

The total dose is 3.2×10^{13} n/cm².

4.4.1 Gain shift.

The gain shift is given in the following figure :

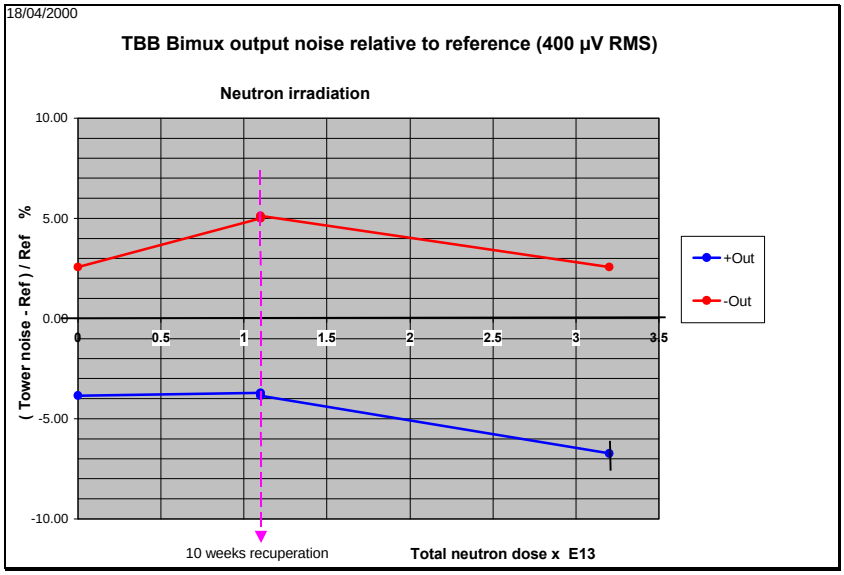


We find : (±0.3 ± 0.1) %.

This implies that the analog amplifiers as well as the analog part of the Bimux are both immune to neutron irradiation. In particular, for the Bimux, this means that the R_{on} resistor of the analog switch has not changed.

4.4.2 Output noise shift.

The output noise is given in the following figure :



We interpret this result as showing that the neutron irradiation has no effect on the noise.

4.4.3 Bimux current shift.

We find the following shifts for the total fluence ($3.2\ 10^{13}$ n/cm^2) :

- +2 V (+12 ± 5) %,
- –3 V (–12 ± 5) %.

This again implies that the op. amps as well as the analog part of the Bimux are immune to neutron irradiation.

4.4.4 Conclusion.

As said for the gamma irradiation we checked after each fluence that we could still address every delay. The Bimux chips are immune to neutrons.

4.5 SEU results.

Using the set-up described under section 4.2.2.5 we perfomed an irradiation with 60 MeV proton beam at Louvain-la-Neuve. Four Bimux were placed in the beam which amounts to eight registers. Each received a total of $3\ 10^{13}$ p/cm^2 during three hours without any SEU occurring. Given the fact that in ten years of Atlas running we expect in the Barrel Front End Crate $2.7\ 10^{12}$ p/cm^2, we foresee **at most 1 SEU in the full calorimeter every 8 days**[1].

4.6 Latch-up results.

The same negative results were found as a by-product of the SEU tests. There was no latch-up and there will be none during the Atlas experiment as DMILL technology is fully latch-up free.

4.7 Conclusion.

The Bimux chip is working well and is radhard.

[1] We use 6744 Bimux in the full calorimeter. This amounts to 13488 registers. From our test we know we get ($3\ 10^{13}$ / 3 hours) / ($2.7\ 10^{12}$ / 10 years) = 13519 days without any SEU for eight registers. For one register this corresponds to $13519 \times 8 = 108148$ days. For the full calorimeter we get 108148 / 13488 = 8 days at least.

5 Production plan.

5.1 Number of needed chips.

Total needed of Bimux circuits for the experiment itself (not each tower builder board has the full set of Bimux circuits) :

Barrel TBB	64 boards × 59 chips	3776
End Cap Standard TBB	32 boards × 65 chips	2080
End Cap Special 0 TBB	8 boards × 49 chips	392
End Cap Special 1 TBB	8 boards × 41 chips	328
End Cap Special 2 TBB	8 boards × 21 chips	168
	Total 1 :	**6744**

Spares needed for spares boards :

Barrel TBB	6 boards × 59 chips	354
End Cap Standard TBB	3 boards × 65 chips	195
End Cap Special 0 TBB	2 boards × 49 chips	98
End Cap Special 1 TBB	2 boards × 41 chips	82
End Cap Special 2 TBB	2 boards × 21 chips	42
	Total 2 :	**771**

Individual spares :

	10% of Total 1	**674**
	GRAND TOTAL	**8189**

Production needs :

Measured yield : $y = 97.5\ \%$

Number of measured chips : $N = 200$

Errors on the yield (Δy) as a function of the number (N) of the measured chips :

$$\Delta y \approx \sqrt{(y\ (1-y)/N)} = 1.1\ \%$$

Total expected yield (it includes packaging) : $(97.5 - 2\times1.1)\ \% =$ **95.3 %**

Total of needed for a given batch : 8189 / 95.3 % = 8593 chips

Supposed maximal batch to batch yield difference : ±10 %

Total production needed for ATLAS : 8189 / (95.3–10 %) = 9600 chips

Total production asked by CMS : 150 chips

Grand total production : 9750 chips

5.2 Proposals for de combined production of the OpAmp and Bimux chips.

We intend to produce in one run the totality of the needed chips. As said, these chips will be submitted in a mask which will be shared with the OpAmp design of Orsay. If this PRR is accepted, the production will be launched end of July. We should receive the chips by the end of October. We give there after three possible reticules for a combined production of the Orsay OpAmp and the Bimux.

- The two methods of calculation of corresponding chip quantity is shown in figure 9 (the right method of calculation is the second one).
- We know that Orsay needs at least 28571 and that we need 9750.
- The cost ratio is given by the ratio of the total surface needed by Saclay and by Orsay :
  - Saclay : $(2.12 \times 2.42)\ mm^2 \times 9750 = 50021\ mm^2 \quad \Rightarrow 35\ \%$
  - Orsay : $(2.10 \times 1.58)\ mm^2 \times 28571 = 94799\ mm^2 \quad \Rightarrow 65\ \%$

5.2.1 Solution 1.

The first reticule proposed (figure 10) requires a production of :	14 wafers	
and delivers :	12570 Bimux	
	29680 OpAmps	
The total cost for 14 wafers is : 14 x 6280 =	87920 €	
Mask cost :	54778 €	
TOTAL :	142698 €	
Cost of the Bimux chip : 142698 x 35% =	49944 €	Unit cost => 3.97 €
Cost of the OpAmp chip : 142698 x 65% =	92754 €	Unit cost => 3.13 €

5.2.2 Solution 2.

The second reticule proposed (figure 11) requires a production of :	13 wafers	
and delivers :	9828 Bimux	
	29980 OpAmps	
The total cost for 13 wafers is : 13 x 6280 =	81640 €	
Mask cost :	54778 €	
TOTAL	136418 €	
Cost of the Bimux chip : 136418 x 35% =	47746 €	Unit cost => 4.86 €
Cost of the OpAmp chip : 136418 x 65% =	88672 €	Unit cost => 2.96 €

5.2.3 Solution 3.

The second reticule proposed (figure 12) requires a production of :	12 wafers	
and delivers :	11064 Bimux	
	29976 OpAmps	
The total cost for 13 wafers is : 12 x 6280 =	75360 €	
Mask cost :	54778 €	
TOTAL	130138 €	
Cost of the Bimux chip : 130138 x 35% =	45548 €	Unit cost => 4.12 €
Cost of the OpAmp chip : 130138 x 65% =	84590 €	Unit cost => 2.82 €

5.2.4 Conclusion.

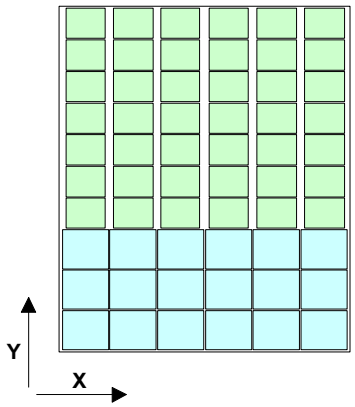
The **third solution** is better as it is the cheapest. **In this case the minimum yield will have to be 75 % with packaging** (without packaging : 76.5 % if the packaging yield is 98 %). How ever we leave a decision to the discussion during the PRR. Other reticule arrangements are also possible.

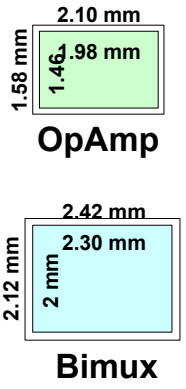
Pascual
la Broise
10/07/02

RETICULE B

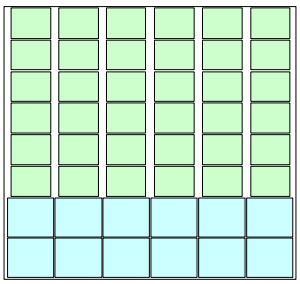
Stepper CANNON

42 OpAmp
18 Bimux





36 OpAmp
12 Bimux



Total per reticule
X: (6x2.42)+(5x0.1)+0.12 = 15.14 mm
Y : (3x2.12)+(7x1.58)+(9x0.1)+0.12= 18,44 mm

1) Calculation from surface :

Wafer surface: 139x139 x 3.14 / 4 = 15 167 mm²
Reticule surface: 15.14 X 18.44 = 279.2 mm²
Reticule number: 15 167 / 279.2 = 54.3

OP Amp: 54.3 x 42 = 2280
Bimux: 54.3 x 18 = 977

2) Calculation from exact counting :

OP Amp = 2120 (2120-2280)/2280 **= - 7%**
Bimux = 898 (898-977)/977 **= - 8%**

Total per reticule
X: (6x2.42)+(5x0.1)+0.12 = 15.14 mm
Y : (2x2.12)+(6x1.58)+(7x0.1)+0.12= 14.54 mm

1) Calculation from surface :

Wafer surface: 139x139 x 3.14 / 4 = 15 167 mm²
Reticule surface: 15.14 X 14.54 = 220.2 mm²
Reticule number: 15 167 / 220.2 = 68.8

OP Amp: 68.8 x 36 = 2476
Bimux: 68.8 x 12 = 825

2) Calculation from exact counting :

OP Amp = 2306 (2306-2476)/2476 **= - 6.8%**
Bimux = 756 (756-825)/825 **= - 8.3%**

Total per reticule
X: (7x2.42)+(6x0.1)+0.12 = 17.66 mm
Y : (3x2.12)+(7x1.58)+(9x0.1)+0.12= 18,44 mm

1) Calculation from surface :

Wafer surface: 139x139 x 3.14 / 4 = 15 167 mm²
Reticule surface: 17.66 X 18.44 = 325.6 mm²
Reticule number: 15 167 / 325.6 = 46.58

OP Amp: 46.68 x 56 = 2614
Bimux: 46.68 x 21 = 980

2) Calculation from exact counting :

OP Amp = 2498 (2498-2614)/2614 **= - 4.5%**
Bimux = 922 (922-980)/980 **= - 5.9%**

56 OpAmp
21 Bimux

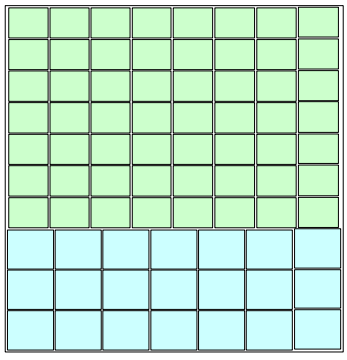


Figure 9 : Reticule and chip quantity calculation.

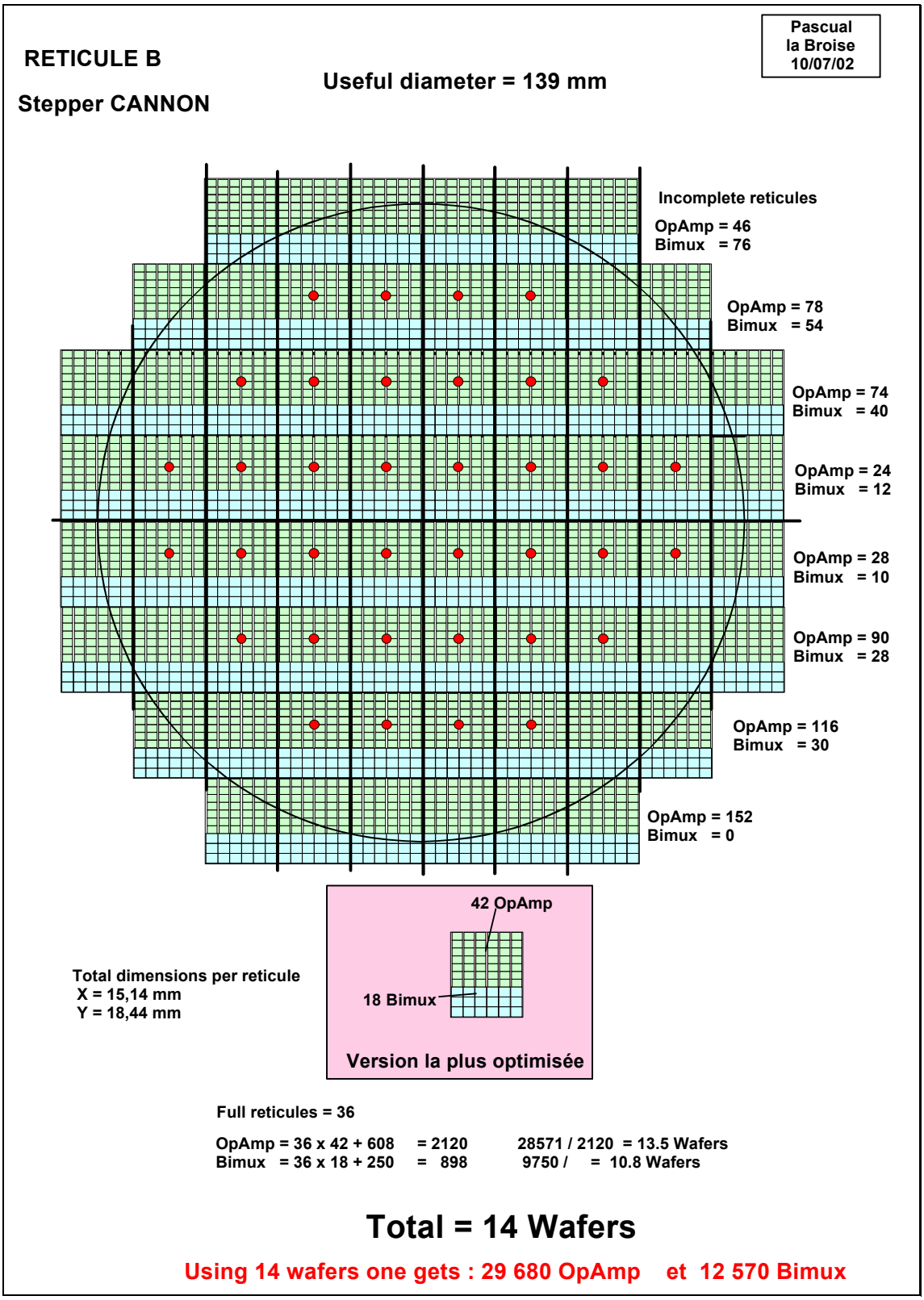


Figure 10 : Solution 1 for combined production.

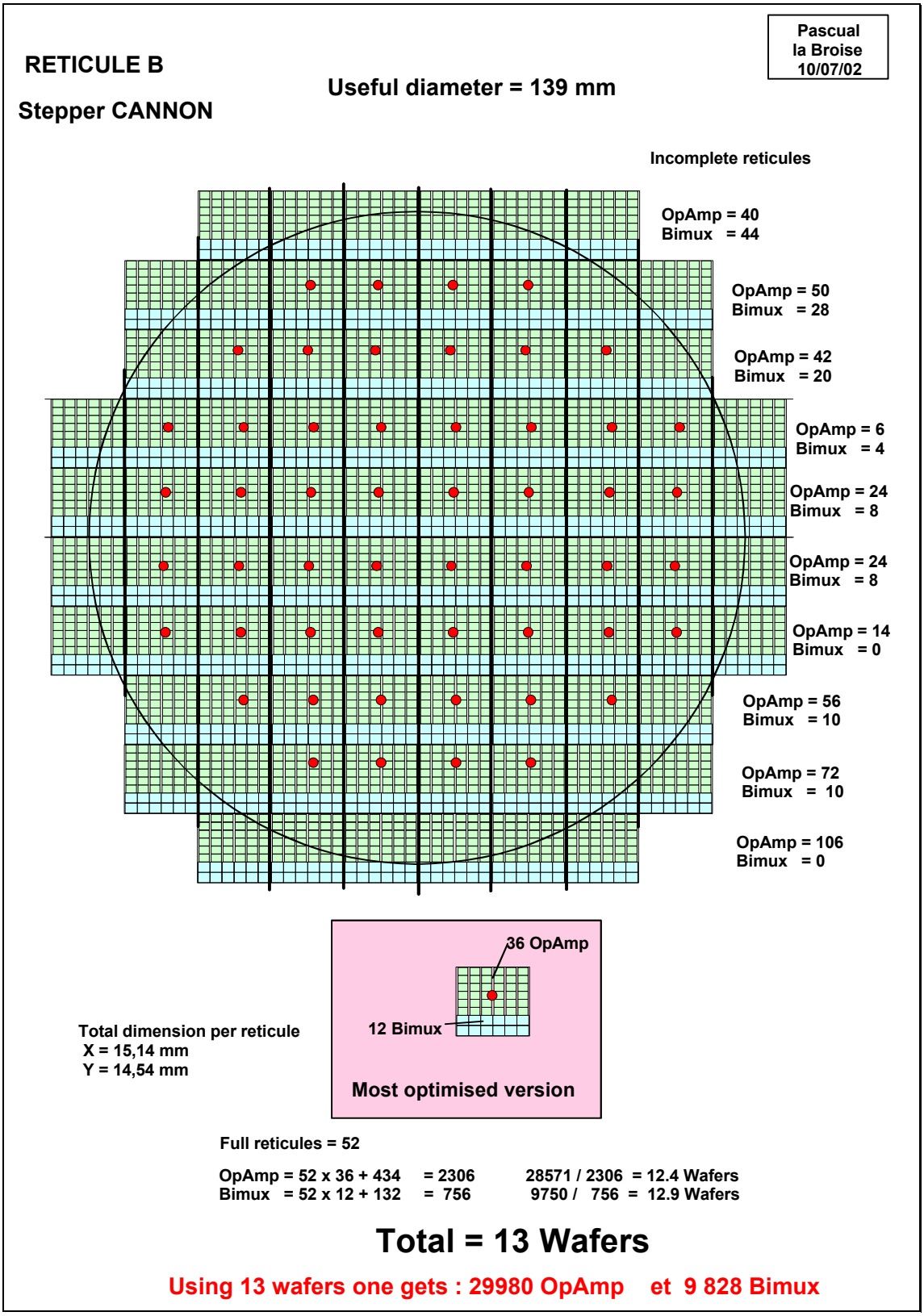


Figure 11 : Solution 2 for combined production.

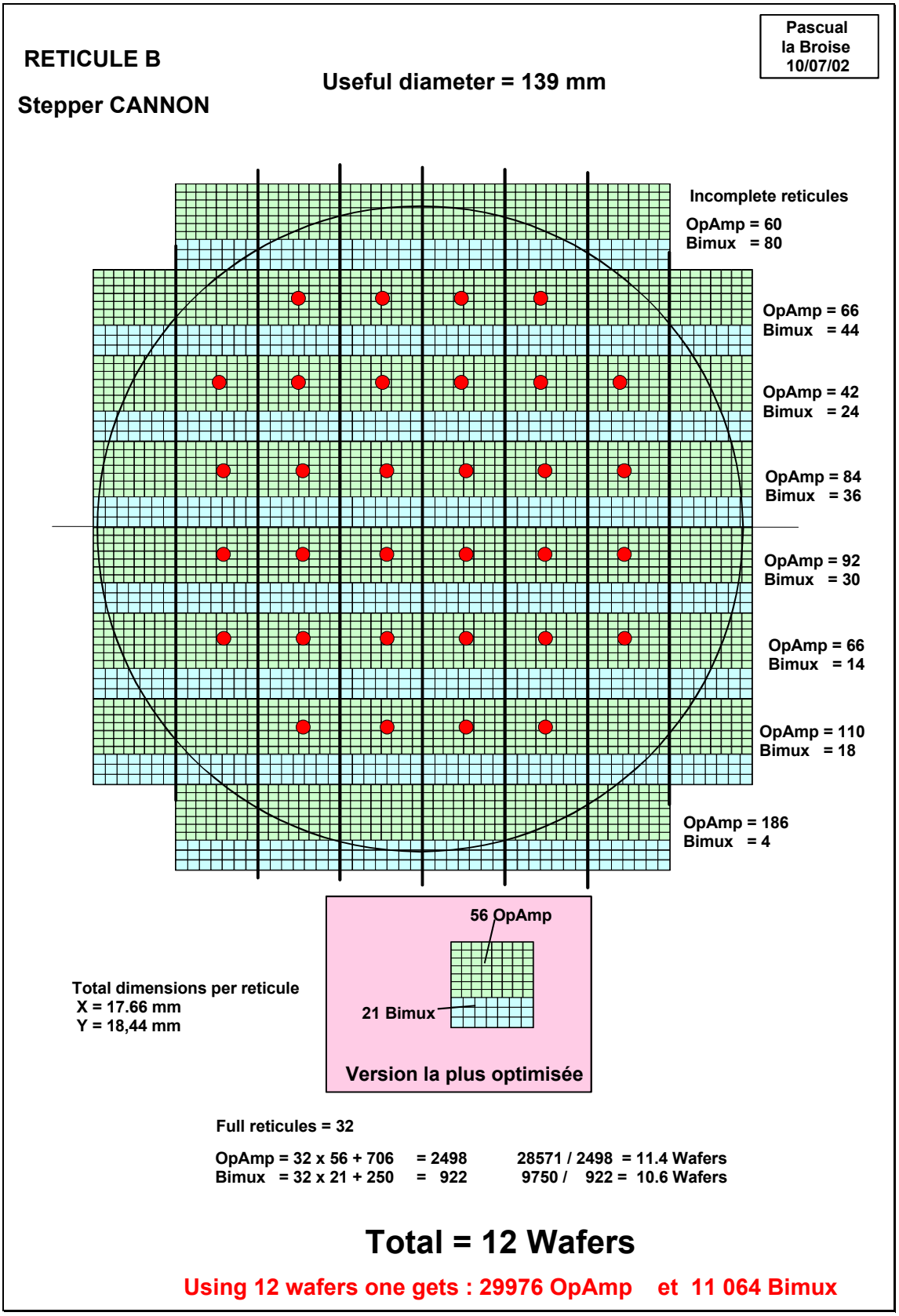


Figure 12 : Solution 3 for combined production.

6 Quality assurance.

6.1 Scope of this chapter.

This chapter describes the QA procedures to be applied to Bimux ASICs during production. The QA procedures are described in this chapter, and if necessary additional ones will be released later. In this chapter we refer to the other relevant chapters and describe the procedures for QA with respect to radiation resistance of the Bimux ASICs.

The following aspects will be covered :

- Subcontractors' certification.
- Data and material tracking.
- Testing.
- Infant mortality tests.
- Radiation hardness.

6.2 Subcontractors.

All the subcontractors selected for packaging will be ISO 9001-2000 certified.

6.3 Data and material tracking.

During all the packaging and test operations a tracking form which is still to be defined will follow each wafer. It will be filled up at each step.

All the chips will be marked at the packaging level, with the number of their origin wafer.

As the test is a go-no go test, only the bad chips will be marked "H.S n" with an appropriate ink on the package white square provided by the packager. We intend to give a number "n" increasing from 1 on only to the bad chips.

A file containing the bad chips wafer number and "n" will be implemented. It will describe the type of failure.

6.4 Testing.

100 % of the packaged ASICs will be fully tested and only ASICs passing all test criteria will be used for being mounted on the TBB. The test procedure and qualification criteria are described in detail in the chapter 7.

6.5 Electromigration, reliability.

The chip has been designed to follow the rules described in the DMILL electrical rules document [1], this concerning electromigration and hot carrier effects.

For the defects activation, no test have been performed on this present circuit, but tests on the DSMD circuit which is quite similar to the HAMAC chip have shown no bad effects.

6.6 Infant mortality test.

A burn-in test of the chip is necessary to increase the TBB reliability. It is not foreseen to perform this test at the chip level, but only at the overall TBB level. The aim of this test is to get rid of infant mortality problems. This test is performed at the production plant and is specified in the contract with the manufacturer.

6.7 Monitoring of radiation resistance.

6.7.1 Radiation levels expected.

The Table 1 summarizes data extracted from the ATLAS Policy on radiation tolerant electronics document [2].

	Total ionising dose		Neutron fluence (1MeV)		SEU effects (proton = 60 MeV)	
Raw simulated radiation level (10y)	5	krad	$1.6\ 10^{12}$	n/cm^2	$7.7\ 10^{11}$	p/cm^2
Safety factor on simulations	3,5		3.5		3.5	
Safety factor for low dose rate	1,5		1		1	
Safety factor for lot to lot variations	2		1		1	
Radiation tolerance criteria	53	krad	$5.6\ 10^{12}$	n/cm^2	$2.7\ 10^{12}$	p/cm^2
Failure at (for pre-production)	> 218	krad	$> 3.2\ 10^{13}$	n/cm^2	$> 3\ 10^{13}$	p/cm^2

Table 1

The line "Radiation tolerance criteria" corresponds to the dose the chips have to be qualified for, according to [2]. The line "Failure at" corresponds to the level of irradiation we used for the qualification tests.

6.7.2 Foundry radiation hardness assurance.

Radiation hardness verification is a part of the acceptance criteria in the foundry. A 10 Mrad (SiO_2) radiation test is performed to control radiation hardness stability and to statistically measure the process capability to satisfy radiation sensitive parameter drift tables as specified in the DMILL electrical specification document (RDER24O1). Every production lot is controlled according to the sampling plan defined in the in-house procedure EDR97043 . Test conditions and radiation conditions are described in this document. After irradiation, in case one parameter would exhibit larger drift or greater absolute value than expected, a deeper analysis would be performed and, when failure is confirmed, wafers would be rejected.

6.7.3 Neutron irradiation.

As the DMILL technology is guaranteed for a 1×10^{14} n/cm^2 operation, we do not plan to perform NIEL tests during production.

6.7.4 Gamma irradiation.

The DMILL technology is guaranteed for a 10 Mrad operation. This is 200 times greater than the requirements, these moreover including already a large safety margin.

So we do not plan to perform systematic TID tests of the chip.

6.7.5 SEE.

The Bimux chip includes only two digital memory cells (3 bits each), which are of D type.

As was shown in the pre-production SEU tests no effect was seen (see chapter 4), we do not plan to do any SEU test on our production batch.

6.8 Summary.

The QA procedures for the Bimux ASICs are defined to ensure the quality and performance requirements for every Bimux ASIC delivered for TBB mounting. Every chip will undergo a thorough

test procedure, and the bad chips will be documented in a database. The infant mortality procedure will be performed on the TBB. The radiation hardness will be monitored all along the production process.

6.9 References.

[1] *DMILL electrical rules*, REDR2401 rev C, *ATMEL*

[2] *ATLAS policy on radiation tolerant electronics*, ATC-TE-QA-0001, *M. Dentan* : http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/ATLASPolicy/APRTE_rev2_250800.pdf

7 Production test bench.

The production test bench will be quite similar to the one described for the pre-production one, except for the PQFP socket which is a special one (BFI OPTILAS, “WELLS-CTI”, reference : 7310-044-4-08) which allows to plug and make contacts with a spring mechanism which allows much faster chip interchange. We intend to test manually the 10000 chips, which should take about 1.5 months. To shorten this delay we are planing to build a board identical to the one described above, but containing ten channels instead of two.

8 Annexe.

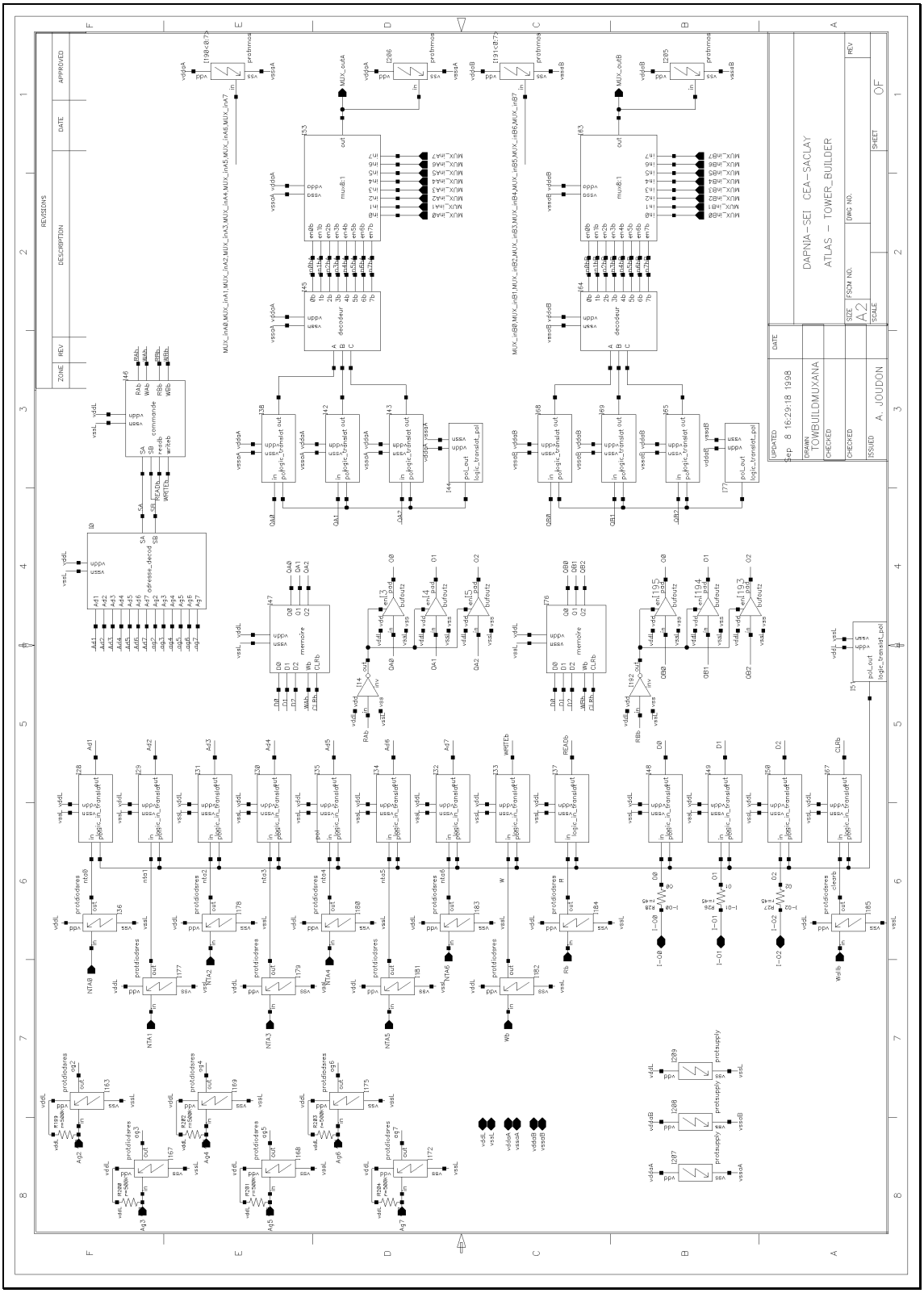


Figure 13 : General electrical layout of the Bimux circuit.

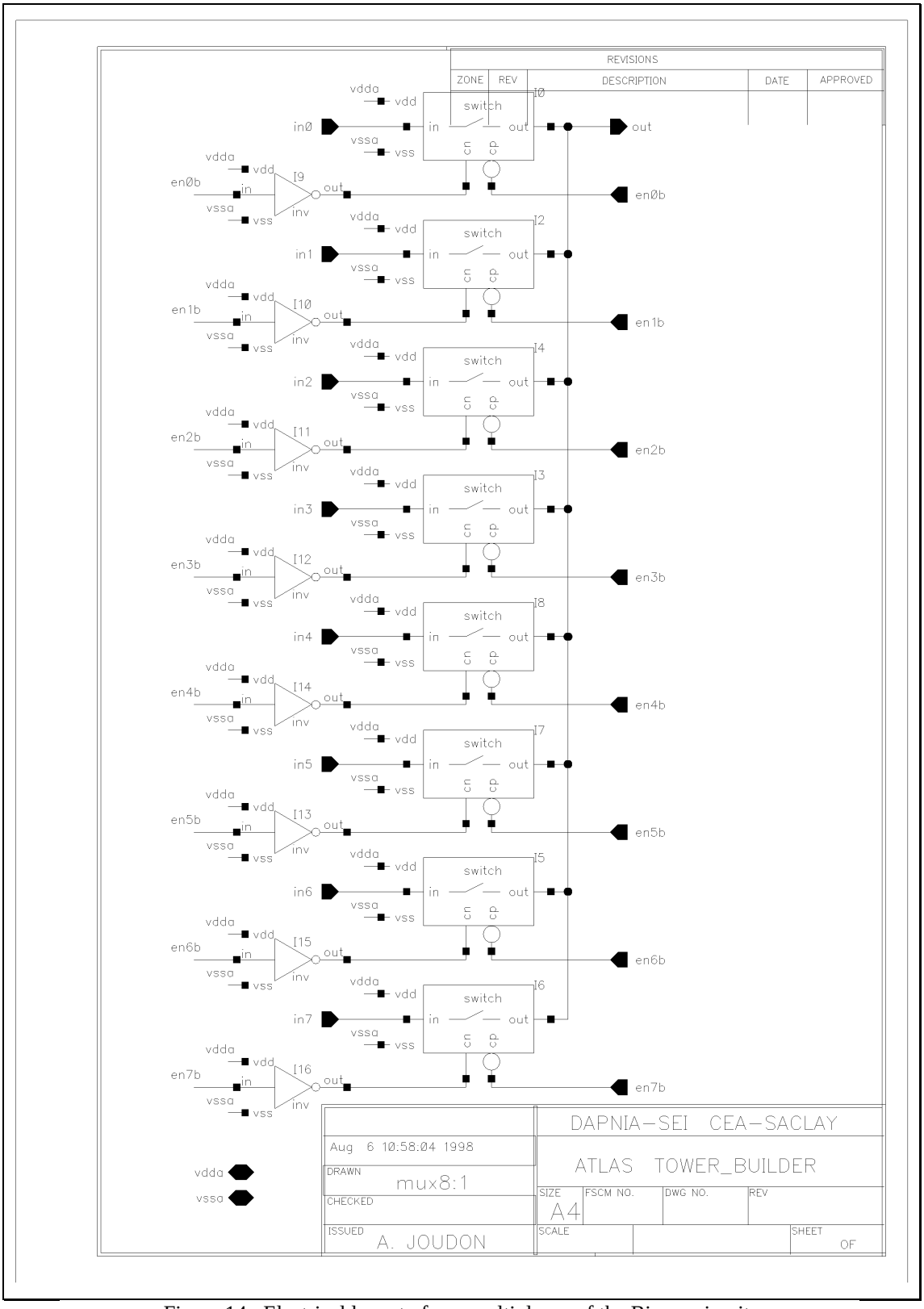


Figure 14 : Electrical layout of one multiplexor of the Bimux circuit.

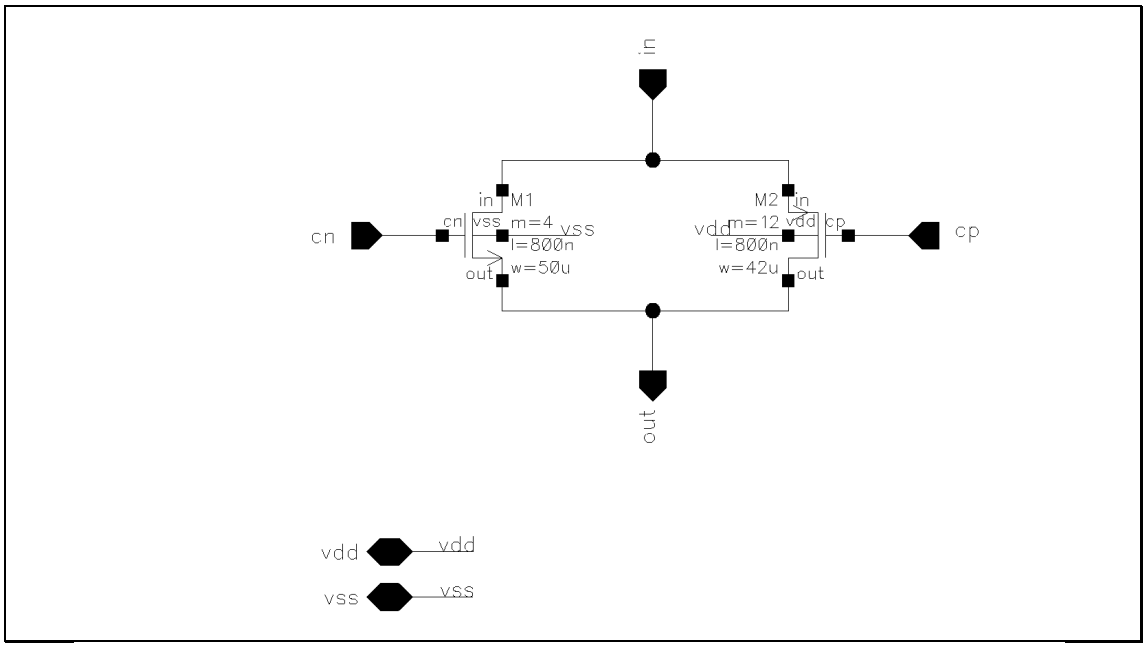


Figure 15 : Electrical layout of one multiplexer switch cell of the Bimux circuit.

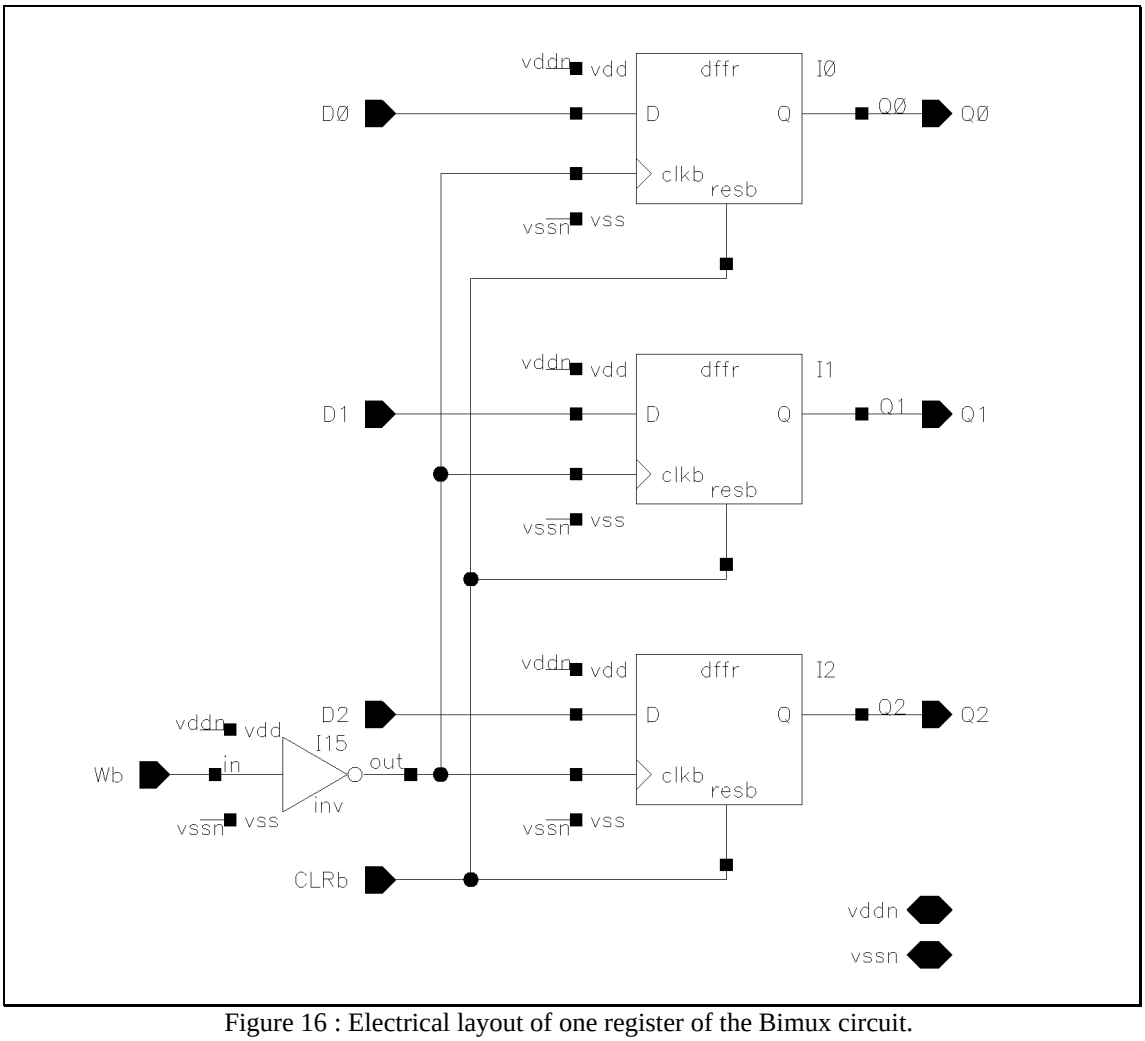


Figure 16 : Electrical layout of one register of the Bimux circuit.