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Low-Power Autozeroed High-Speed Comparator for the Readout Chain of a CMOS Monolithic Active Pixel Sensor Based Vertex Detector

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Abstract - Future high energy physics experiments will require the development of a linear collider in the TeV region such as TESLA. Because of physics requirements it will be necessary to make precision vertex measurements. This makes a high-resolution vertex detector an essential part of the detecting system. One of the possibilities is to develop a CMOS Monolithic Active Pixel Sensors (MAPS) based detector. A planned prototype chip for the TESLA developments would include an array of identical pixels with their addressing circuits, signal processing within the chip, data sparsification and analogue to digital conversion. For this purpose we have developed a column-based, low power, fully offset compensated multistage comparator (discriminator), to read out the active pixels. For one of the versions implemented a resolution better than 1mV was obtained at operating speeds higher than 10MHz. The power dissipation is of the order of 200µW. A test chip was designed on a 0.35 µm CMOS process from AMI Semiconductor. As the pixel pitch is only 28µm, the dimensions of the comparator are 300µm x 28µm. This design is compatible with the clocking scheme of the pixel array.

I. Introduction

Many projects have been proposed such as the Next Linear Collider (NLC) and the Japanese Linear Collider (JLC) for future high energy physics experiments. Another project is the TeV Energy Superconducting Linear Accelerator (TESLA) that is an e-e+ collider and could be commissioned near Hamburg (Germany) within the next ten - fifteen years [1]. Because of the physics requirements, it will be necessary to make precision vertex measurements. One of the aims of the vertex detector is to study the Higgs mechanism. In some cases, it will be necessary to measure the secondary vertex, making a high-resolution vertex detector an essential part of the detecting system. To build this high performance detector three options are possible: Charge Coupled Devices (CCDs), Hybrid Pixel Detectors (HPDs), and CMOS Monolithic Active Pixel Sensors (MAPS). The CCDs have already been used successfully at the Stanford Large Detector of the SLAC [2], despite being highly sensitive to point and extended defects and subsequently irradiation [3] and limited in terms of readout speed. HPDs offer good speed performance but have a limited spatial resolution due to their large pixel and readout chip area; in addition their thickness (~ hundredths of μm) degrades the spatial resolution. These HPDs were developed for the forthcoming LHC experiments, where less precision is required [1]. For nearly a decade there has been huge progress in optical imaging with the so called CMOS active pixel sensors, which integrate monolithically in a silicon chip an array of active photosensors with a readout circuitry [4]. Recently there has been a technological breakthrough by the Strasbourg group [5]: evidence that CMOS active pixel sensors can be used for the detection of Minimum Ionizing Particles was clearly established. Moreover these pixel sensors have some advantages over CCDs such as their lower power dissipation and higher readout speed. They require only standard CMOS technology and make the monolithic integration of complex readout circuitry on the same chip possible. Thinning the silicon substrate is possible as for the CCDs. The size of the pixel can be reduced to match the precision requirements at, of course, the expense of on pixel signal processing. Radiation hardness is an

important issue but it seems clear that CMOS active pixel sensors have a greater radiation tolerance than CCDs, especially to ionizing irradiation [6].

Figure 1 shows the global architecture of the planned MAPS chip for a TESLA development [7]. The circuitry can be divided in four different parts.

- The array of identical pixels.
- The digital addressing of the pixel row, in the left of the figure.
- At the bottom of a pixel column, the column readout, which comprises an interface and a comparator (discriminator) for zero suppression. In a further step an (analogue-to-digital converter) ADC should convert the analogue useful data in to digital data.
- The data processing part that could be at the right of the circuit. This could process the digital raw data to extract pixel clusters etc…

The basic operation mode is described in the following. The pixels have an internal double sampling operation with capacitor storage of the signal. This should strongly reduce fixed pattern noise. The pixels are read in parallel row by row in order to increase the speed of the readout compared to pixel-by-pixel readout. To reduce power dissipation the pixels are only switched on during readout. Moreover the whole circuitry can be switched off during the machine dead time. As the active time of TESLA is about only 1 ms for 200 ms total time, this procedure reduces greatly the power dissipation. This is a strong requirement if 800 Mpixels are to be operated in the vertex detector, the dissipation problem clearly being an issue.

It is challenging to reach a few hundreds μV sensitivity for the comparator at readout speeds foreseen for the vertex detector (up to 50MHz). The signal of the pixel must be amplified before the comparator. This can be accomplished at the column level or in the pixel. The first has to advantage to offers more relaxed constraints in terms of power dissipation and available silicon surface. Closed-loop amplification with auto-zeroing is also possible at column level reducing gain mismatches. However, with the photodiode-based pixels operating in integration mode, the correlated double sampling (CDS)

process is difficult to accomplish at the column level [8][9] and an in-pixel memory is necessary. This adds some mismatches which are difficult to correct. An in-pixel preamplification may also be necessary.

In the pixel used for this chip, shown in Figure 2a, the double sampling and amplification is carried out on the pixel[1]. The surface and available power budget limitations in the pixel forces to use an open-loop amplifier with small sized transistors. The detector used in the pixel is a photodiode operating in current mode. It is continuously biased, so it gives a voltage proportional to the charge deposited by the incident particle. The readout time is short compared with the discharge time of the photodiode. The sensing node is followed by a source follower and a sample and hold stage. At this stage the signal is also amplified. Two storing capacitors are used enabling an "on pixel" double sampling. The signals from the capacitors are output to a differential stage. The readout sequence of the pixel is as follows (Figure 2b):

- The inputs of the output differential stage of the pixel is shorted by CALIB,
- The present value of the detector element is amplified, sampled and stored in the pixel (SMP1),
- The difference between the present and the previous values of the detector element is the useful signal. It is sent on the column bus (RD),
- The detector element is sampled and this value is stored in the pixel by SMP2 (this information is stored for the next readout cycle).

The double sampling enables the correction of the detector offset together with the offset of the source follower, and the sample and hold stage. The offset of the output stage, available during the CALIB phase, needs to be corrected by the column readout circuitry.

The first and most important part of the column circuitry is the comparator shared by all the pixels of one column. Each pixel has its output switched sequentially to the front end of the

[1] This pixel and the interface were designed mainly by IReS/LEPSI group and details can be found in [10].

comparator. The width of the comparator should be the same as the pitch (28 μm in this case) for these pixels. As the area occupied by the readout circuitry acts as a dead zone, the length of the comparator should be limited by a careful layout design. The comparator must accomplish the following tasks.

During the CALIB phase:

- Sample the pixel output stage offset voltage,
- Sample its offset voltage,
- Sample the threshold (reference) level.

During the RD phase:

- Correct the pixel output stage offset and its offset,
- Amplify the signal and compare it to the reference level, then give a logic level.

In this paper we will focus on the development of a MAPS architecture running in a binary information output mode. For this purpose we have studied a low-power column comparator, fully offset compensated, to readout the active pixels of the array [11]. A resolution better than 1mV is targeted, which corresponds to $100e^-$ for a pixel charge-to-pixel conversion factor of $10\mu V/e^-$, and to $10e^-$ for $100\mu V/e^-$. We note that, for future applications, if necessary, an ADC can be constructed based on this comparator[2].

II. Offset compensated comparator architecture

The offset compensated comparator architecture used in this work is shown in Figure 3, with related simplified timing in Figure 4. The complete active pixel sensor chip will include digital circuits. So, to overcome the issues related to substrate coupling in the mixed-signal environment, to improve the PSRR, and to reduce the effects of the charges injected by the switches used in the comparator, a

[2] The projected ADC would be a 2 or 3-bit over a dynamic range of a few tens of milivolts [12], the signal generated by an impinging charged particle being very small.

fully differential architecture is chosen. The comparator uses both input offset storage and output offset storage [13]-[16]. This allows eliminating the offset voltages of both the stages using only one-capacitor pairs and offset sampling phase. Note that, capacitors are very space consuming on the chip. Another advantage of this architecture is that the input capacitance of this structure is very small. During τ_1, the offset voltage of the first stage and the threshold voltage level are amplified and stored on the capacitors. At same time, the offset of the second stage, which is in a unity gain closed-loop configuration, is sampled on the capacitors. During τ_3, the input signal is amplified and fed to the latch, the offsets of both stages being corrected. Then, during τ_4, the latch amplifies rapidly this level and gives logic signals depending on the difference between the threshold level and the analog input signal. The input referred residual offset of this architecture is given by:

$$V_{OSR} = \frac{V_{OS2}}{A_{01}(1+A_{02})} + \frac{\Delta Q}{A_{01}C} + \frac{V_{OSL}}{A_{01}A_{02}} \qquad (1)$$

where A_{01} is the static gain of the first stage, A_{02} the static gain of the second stage; V_{OS1} the input referred offset of the first stage, V_{OS2} the input referred offset of the second stage, V_{OSL} the input referred offset of the latch, and ΔQ the charge injection mismatch from S_5-S_6. Note that the input referred charge injection mismatch is also attenuated by A_{01}.

III. Detailed schematic of the comparator

A more detailed schematic of the comparator is shown in Figure 5. To speed up the comparator, each gain bloc illustrated in Figure 3 is realized using two cascaded low gain amplifiers. Further cascaded gain stage may saturate the final stage due to the offset of the first one. Also, it can causes stability problems for the gain stages in the closed-loop bloc. The two source follower buffers are used to reduce the kickback effects of the latches on the outputs of the amplifying stages. The processed signal levels and the output common levels of the amplifiers being closer to V_{DD}, all the switches are

realized using PMOS transistors. Dummy PMOS transistors are added for S_5 and S_6 to reduce the charge injection. All the current sources, expect i_{ref1} and i_{ref2} (explained later), are implemented with simple MOS transistors.

As already mentioned, the comparator must also cancel the offset of the output stage of the pixel. During τ_1, this offset must also be sampled on the capacitors. So, the input switch configuration shown Figure 3 is not suitable for this application. In fact, voltages cannot be summed on a node unlike the currents. This issue will be addressed in the following sub-sections.

A) Amplifier Stage

The amplifier used is a simple differential gain stage with "resistive" loads (Figure 5). The output common mode voltage of this circuit is well defined and given by:

$$V_{CM(O)} = \frac{V_o^+ + V_o^-}{2} = V_{DD} - \frac{i_{b1} R}{2} \qquad (2)$$

where R is the equivalent resistance of the load. The need of common mode feedback circuits is avoided in this way. This circuit gives a moderate gain. The resistive loads are realized using diode-connected PMOS transistors. The components of the gain stage are sized to obtain a static gain of 4 with a bias current of 10µA. The output voltage swing is 500mV. A minimum gate length of 1µm is used for the input transistors to reduce the offset voltages at the cost of reduced speed. Note that the gain of this stage is nonlinear and falls at high input signal levels. The transconductance of the input devices is maximum at the origin.

A particular problem arises for A_3 of the Figure 5 due to the input capacitive attenuation. In fact, the sampling capacitors and the Miller capacitance C_{gd} of the input transistors of this stage form a capacitive divider, attenuating the effective signal seen at its inputs. One way to boost the gain of this stage is to inject some additional current to increase the transconductance of the input transistors [14][16], or to use controlled capacitive positive feedback with small cross-coupled capacitors [17].

While the two options were simulated, only the first option was used in the final design with i_{b2}=2.5μA. The absolute values of the small feedback capacitors being critical, oscillations may occur due to the additional parasitic capacitors.

B) Threshold voltage generation

As already mentioned, during the offset and threshold voltage-sampling phase τ_1 of the comparator (Figure 4), the offset voltage of the output stage of the pixel must also be sampled. This poses an additional constraint for the input stage. It is well known that the summing of currents is easier than that of voltages. So, we chose to inject the reference level in form of current instead of voltage. The Figure 6a shows the proposed solution and Figure 6b the transistor level implementation. Unfortunately, the transistors added, especially the two current source transistors are a new source of mismatch and must be corrected. During τ_1, the threshold level, which is proportional to V_{ref1}-V_{ref2}, is amplified and stored on the capacitors. Then, during τ_3, a fixed voltage V_{ref2} is applied to the gates of the current source transistors. In this way, the mismatch is measured at the output and subtracted from the previous threshold level. Note that the current levels are in the order of a few hundreds nA. If these transistors are biased in weak inversion, the gate voltage / drain current relationship is nonlinear and the mismatch suppression process is not very effective. To force these transistors to operate in strong inversion with the same current levels, and to improve the matching of currents [18][19], they are sized with small aspect ratios and long channel lengths. Note also that, the additional current sources increase slightly the gain of this stage. Figure 6c shows the simulated input referred threshold voltage Vth as a function of the applied external voltage difference V_{ref1}-V_{ref2}.

It is important to note that, due to the input configuration chosen for the comparator, the sum of the input referred offset voltage of the first two gain stages of the comparator, the output offset voltage

of the output stage of the pixel, and the reference voltage do not saturate the output of the second gain stage during autozeroing phase (CALIB).

C) Latch

Several latches are studied and 2 of them are implemented in the final design. The first one is a dynamic latch shown in Figure 7a [20]. It offers good speed and no-static power dissipation. When the LATCH signal is low (resetting period), the lower NMOS transistor prevents the static current flow and the outputs are held at V_{DD}. Once the LATCH signal goes high, the transistors forming the two cross-coupled inverters immediately go into the active region. Because these transistors turn off, there is no static power dissipation from the latch once the latch outputs are fully developed. Two additional small inverters are used to symmetries the charges seen by the outputs of the latch. The switching time is in the order of 2ns loaded by a FF (Flip-Flop).

The second one is a static latch (Figure 7b) [21], [22]. This latch operates in two phases. During tracking (LATCH=0) the differential pair is connected to the current source and the latch operates as a differential amplifier. When a signal is applied to the input, the output slightly changes and then latching is put into operation (LATCH=1). The differential pair is progressively cut off, the latch pair is connected and the positive feedback makes the latch flip. The current from the latch pair is limited by the current source. This architecture necessitates at its output a level shifter to generate the CMOS levels. We used a simple CMOS level shifter. In our case, when a static bias current of 40 µA, the power dissipation is of the order of 200µW at a 40 MHz main clocking frequency, but this may be reduced by improving the level shifter.

IV. Implementation and results

A test chip is designed together with the Strasbourg group on a 0.35µm CMOS process from AMI Semiconductor. The chip includes a pixel array (30x128), column-level comparators, programmable shift registers and output multiplexers. The pixel pitch is 28µm. The pixel charge-to-pixel conversion factor (CVF) is adjustable from 10µV/e^- to 100µV/e^-. Three different comparator architectures are implemented on the chip with:

- 4 differential gain stages with a dynamic latch (T0 and T1)[3],
- 3 differential gain stages with a dynamic latch (T2),
- 3 differential gain stages with a static latch (T3).

Figure 8 shows the layout of the comparator T0 (or T1). The dimensions are 28µmx300µm for this comparator. A positive-edge triggered D-FF from the standard cells is added at the output of the comparator to memorize the output of the latch (not shown here). The signal $\overline{\phi 2}$ ($\overline{RD}$) is used as the clock signal for this FF. This means that, the output of the latch is memorized half a period after the activation of the LATCH signal. The complementary output of the latch ($\overline{Y}$) is not used.

Figure 9 shows the transient simulation results for the first comparator structure. The comparator is synchronized with the pixel. The main clock frequency is 33MHz. ΔVi is the differential voltage signal applied to the input of the comparator. Note that, all the switches used in the comparator being PMOS transistors, the control signals are inverted. ΔVo is the analog voltage waveform at the inputs of the latch. $\overline{X}$ and $\overline{Y}$ are the latch outputs, *XD* the output of the FF. During the first period, an input signal level superior to the threshold level is injected (ΔVth=1.5mV), so the FF gives a logic one level. Then, during the second period, the input level is zero, and the output of the FF remains at 0 level. Note that, the speed of the comparator could be increased externally by increasing the bias

[3] T0 and T1 are identical comparators implemented on the chip to observe the mismatch between them.

currents of the gain stages, at the expense of reduced resolution and increased power dissipation. Note that the autozeroing reduces the low-frequency noise contribution [23] [24]. However, due to its large bandwidth, the temporal noise of the comparator is mostly white. So, the autozeroing process increases the noise power. For a pixel CVF of 10μV/e^-, the comparator threshold can be adjusted up to 500 e^-, depending on the offset voltage values of the comparator gain stages and the pixel output stage.

The static power dissipation is 150μW, and at 33MHz or 40MHz main clock frequency with 8 sub-cycles, the dynamic power dissipation of the dynamic latch is in the order of 15μW. So, the total power dissipation is approximately 165μW. A resolution better than 1mV is expected for this comparator.

For the second comparator (T2), designed for higher pixel CVFs, the threshold level must also be increased. This may saturate the differential gain stages during the autozeroing phase. So, the second gain stage (A_2 in Figure 5) is removed and only 3 gain stages are used. For a pixel CVF of 100μV/e^-, the comparator threshold dynamic range decreases due to the increase of the pixel output offset, and can be adjusted up to 300 e^-.

The test bench used to test the functionality of comparators, to measure the residual offset, the temporal noise, and the threshold voltage dynamic is shown in Figure 10. An FPGA generates the digital control signals. A pulse generator, triggered by the FPGA, generates a signal synchronous with the control signals. The signal is attenuated and mixed with a common mode voltage reference. This gives an analog stimulus with variable amplitude similar to the signal of the pixel. A digitizing scope is used to visualize the control signals and the output of the comparators, and also to compute the average number of "1" over a significant number of cycles. All the comparators studied here are functional up to 80MHz main clock frequency, at the expense of a reduced sensitivity at high frequencies.

Figure 11 shows the main clock signal (f_{CK}=40MHz) and output signal for T0 observed on the scope with the inputs shorted to a common mode voltage with two different threshold voltages. When the threshold voltage is close to the offset, the comparator triggers on its own temporal noise giving

random "1"s. Figure 12a shows the normalized noise response of the comparators versus threshold voltage with f_{CK}=33MHz, V_{ref2}=2V, τ_1=90ns, τ_2=15ns, τ_3=45ns, τ_4=30ns. The four comparators were tested. For the two four stages devices (T0 and T1), the residual offset voltage is very low; for the three stage device T2 the offset is higher. From the derivative of these plots, which gives a gaussian law, we obtain the residual offset and the temporal noise. In these conditions, for T0 and T1, the residual offset is negligible, and temporal noise variance σ in the order 85μVrms. For T2, the residual offset is below than 300μV. Theses results show the effectiveness of the offset compensation. As shown, the type of latch has no noticeable effect on the residual offset and the temporal noise (Figure 12b). Only the number of gain stages has a significant effect.

As shown on the following graphs (Figures 12b and 12c), the effect of reducing the calibration time τ_1 is to increase the residual offset. The residual offset remains below 1mV for calibration times higher than 60ns. In addition the temporal noise increases certainly because the read time is slightly reduced. For example, from Figure 12c, we see that the reduction of the calibration time compared with Figure 12a affects the residual offset which is of the order of 700μV for T0 and T1, and higher for T2. This stems from the time constant necessary to make an efficient offset correction. The product of the compensation capacitances with the transconductance of the intermediate amplifiers determines this time constant.

Note that the measurements on the comparators are made while the digital part of the chip is running, and we observed no effect on the comparators, thanks to the differential architecture.

The number of amplifying stages is chosen as a function of the resolution requested. Considering a typical offset of ~100mV for the latch [25], to obtain a resolution better than 1mV, three amplifying stages giving a gain of ~64 are not sufficient and at least four are necessary. Comparison of the three amplifying stages comparators with the ones with four amplifying stages, shows, as expected,

that the latches have a significant offset. Measurements made on a second chip (not shown here) confirm the validity of our conclusions.

V. Conclusions

This chip is the first step towards the development of a smart particle MAPS based vertex detector. We have demonstrated the functionality of all the column based comparators studied here up to 80 MHz. The measurement results show that a residual offset below 1mV can be achieved at a clock frequency of 40MHz (5MHz operating frequency). The temporal noise remains below a few hundreds of microvolts as expected. Power consumption is in the order of 200μW at these operating speeds. In order to improve the operation speed for a given power dissipation and residual offset, in future designs, the value of compensation capacitances could be reduced.

We remember that only the positive outputs of the latches are used in this application (the outputs X in Figure 7). When there are no hits, even if the positive outputs are 0 during latching, the complementary outputs flip to V_{DD}, absorbing currents during the transitions. This causes useless glitches on power supplies and increases power consumption. So a further step should be to prevent the outputs Y to flip to V_{DD}.

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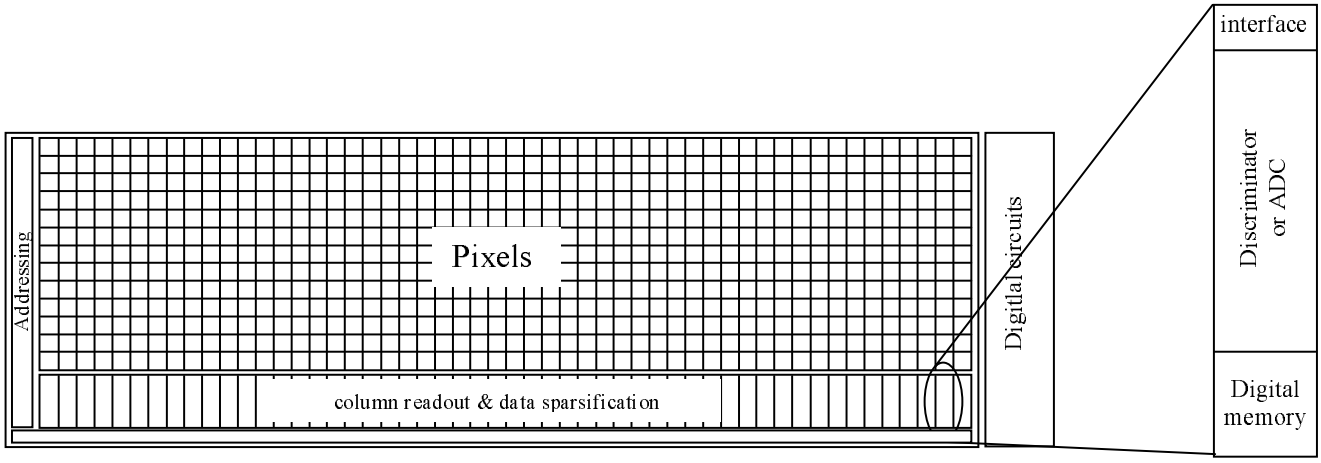
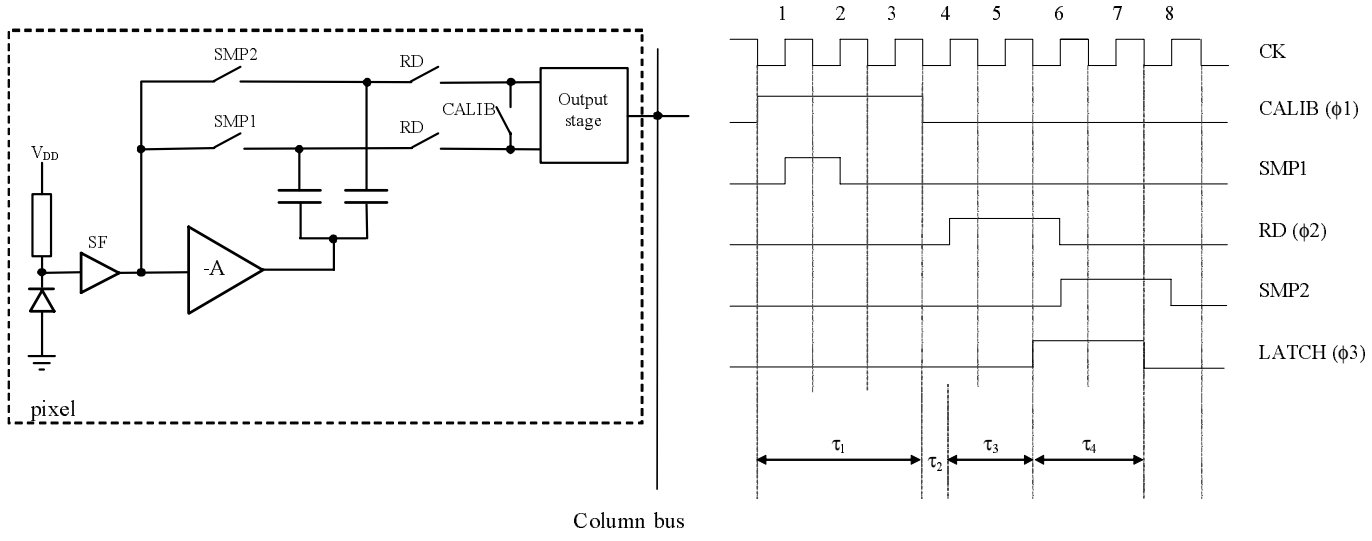


Figure 1 : CMOS pixel array with the readout at the bottom of each column.



(a) (b)

Figure 2 : (a) Simplified schematic of the pixel and, (b) related timing (clocking stimuli). ϕ1, ϕ2, and ϕ3 are the control signals also used by the comparator.

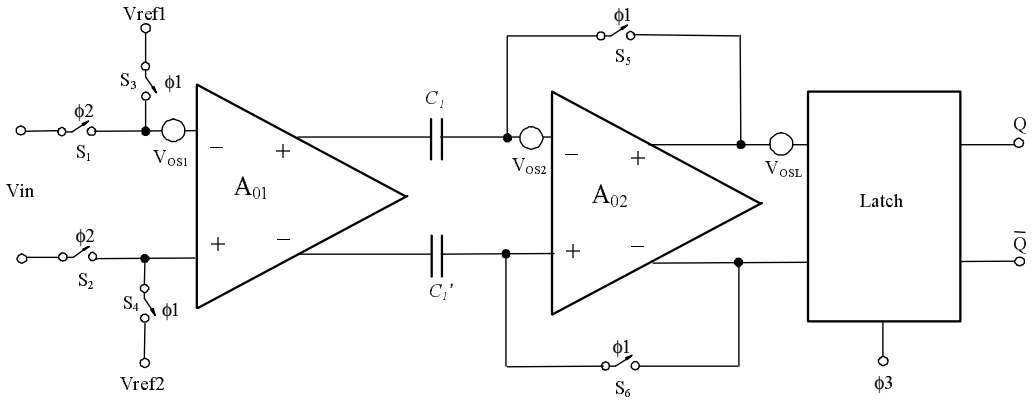


Figure 3 : Offset compensated comparator architecture studied.

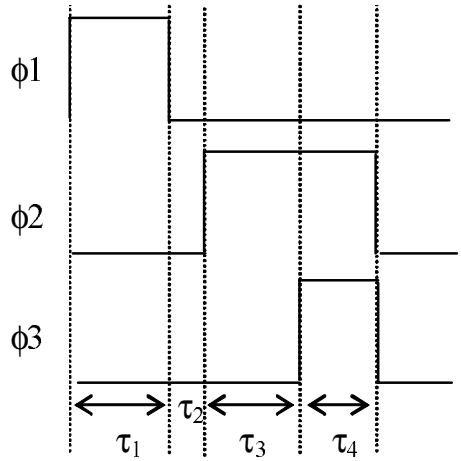


Figure 4 : Timing for the comparator. τ_1 is the offset and voltage reference sampling phase, τ_3 the offset correction (autozero) and comparison phase, and τ_4 the latch phase.

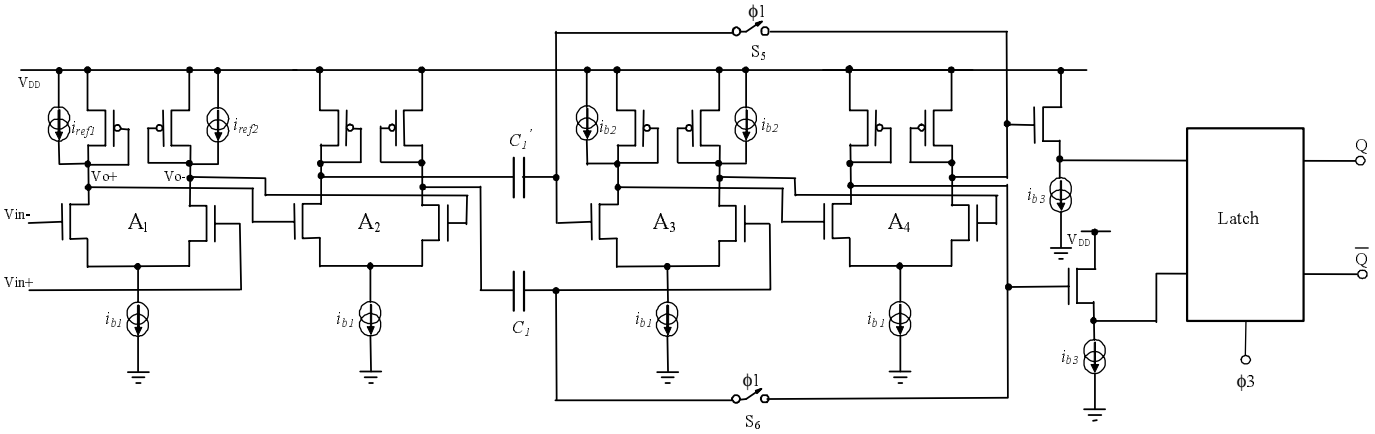
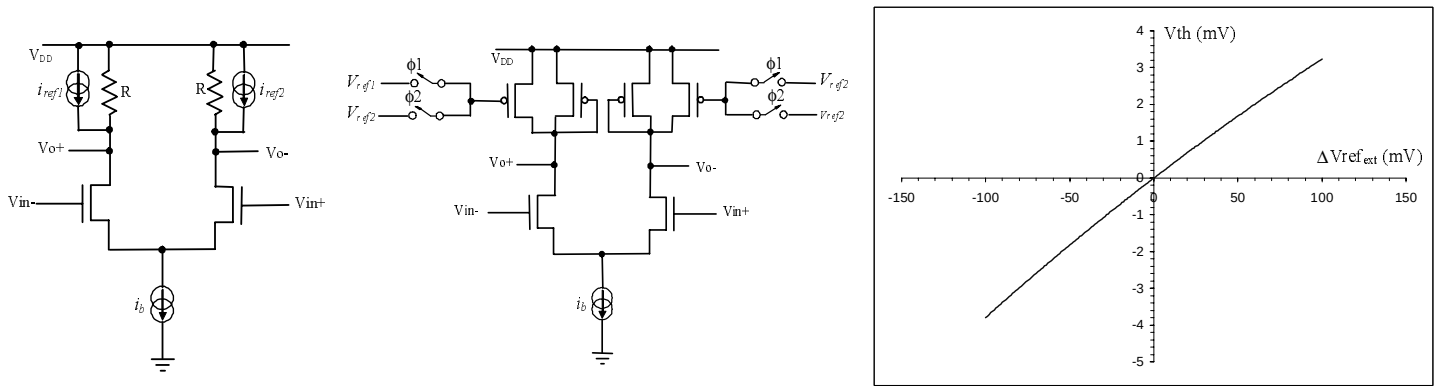
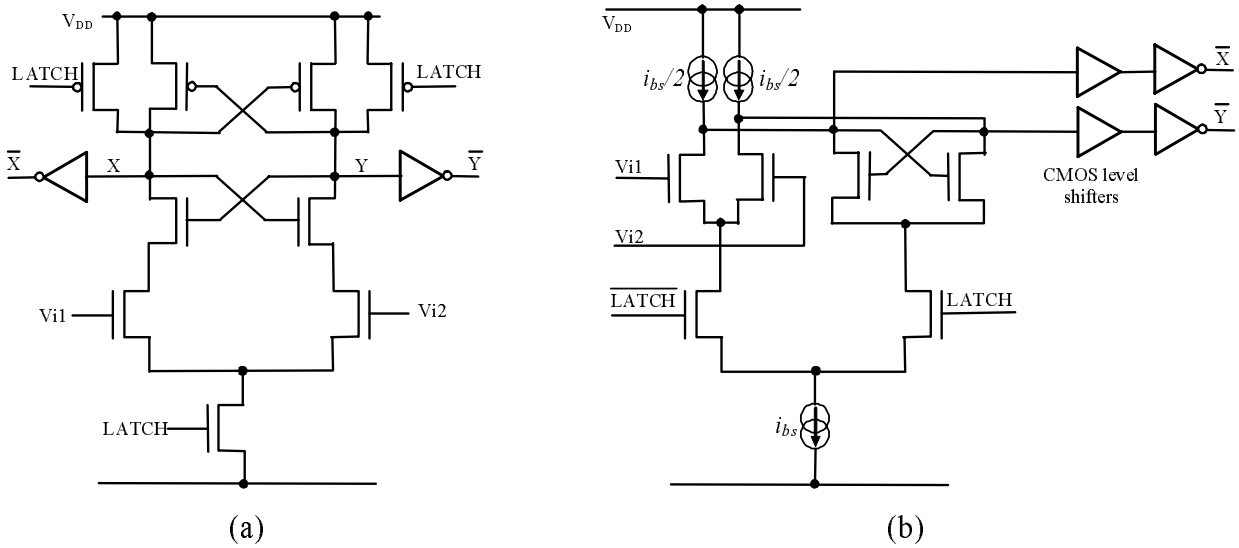


Figure 5 : Detailed schematic of the comparator (see Figure 6 for details concerning the first stage A_1).



(a) (b) (c)

Figure 6 : (a) Threshold voltage generation, (b) practical implementation (c) Input referred threshold voltage as a function of applied external voltage with V_{ref2}=2V ($\Delta Vref_{ext}=V_{refl}-V_{ref2}$).



(a) (b)

Figure 7 : Schematic (a) of the dynamic latch and (b) of the static latch.

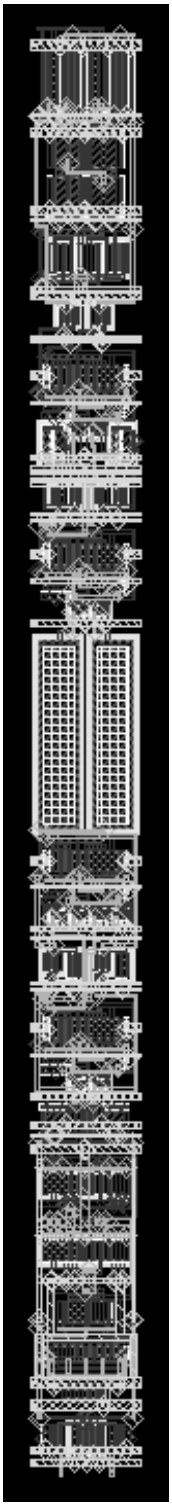


Figure 8 : Layout of the comparator T0 or T1 (28µmx300µm).

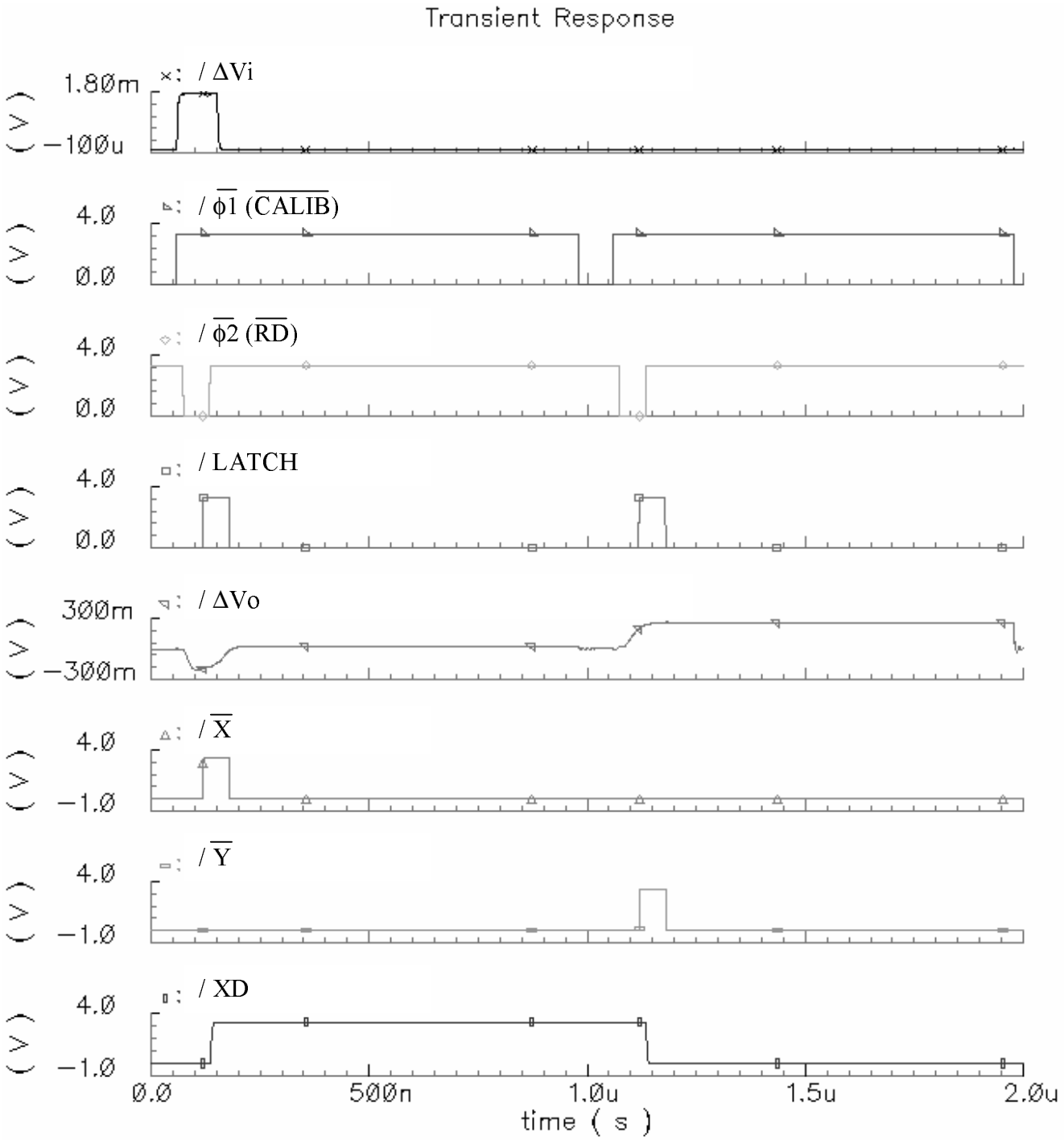


Figure 9 : Transient simulation results for the comparator with 4 gain stages and dynamic latch.

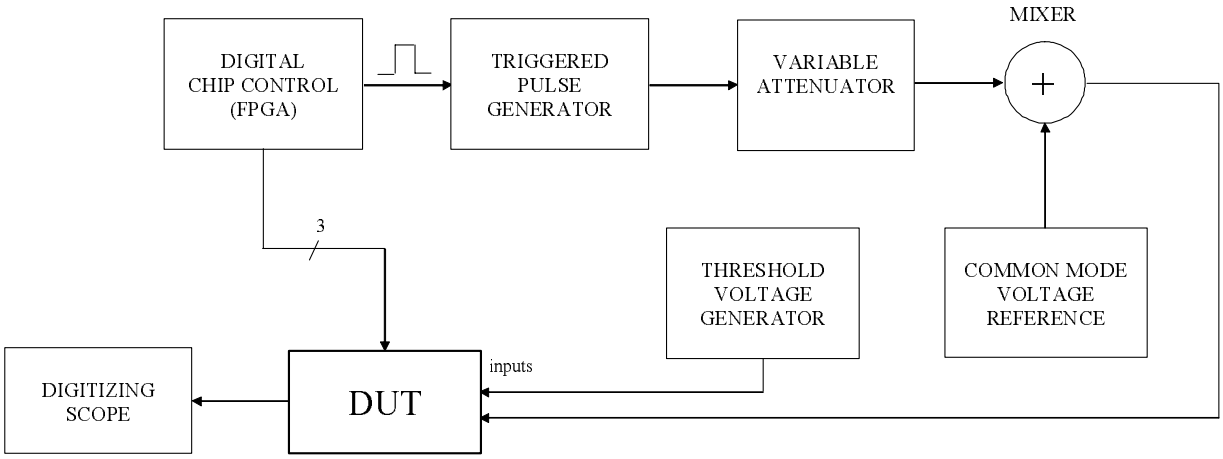
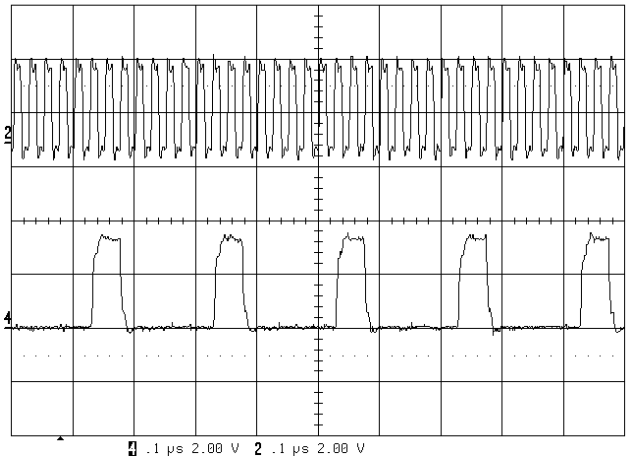
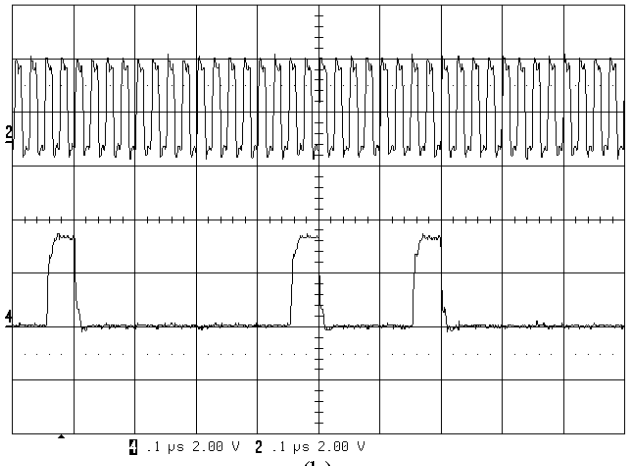


Figure 10 : Testbench comprising a FPGA to generate the control signals, a pulse generator, a variable attenuator, a mixer based on discrete operational amplifiers in order to generate the analog stimuli with a common mode level, a precision voltage calibrator to generate the threshold voltage, and a digitizing scope.

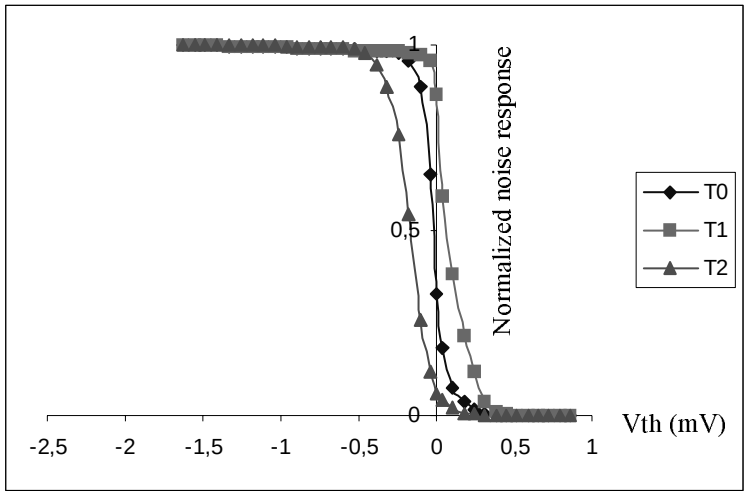


(a)

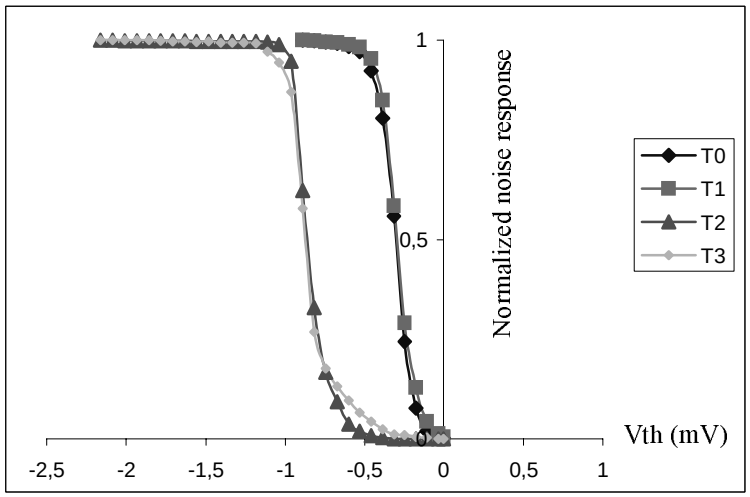


(b)

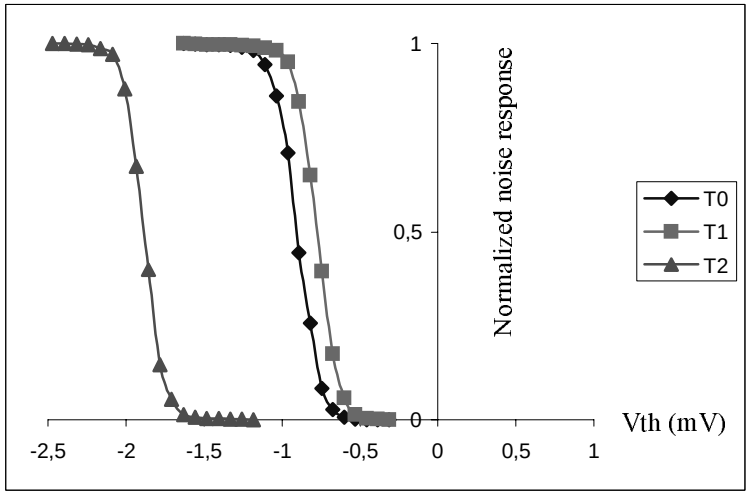
Figure 11 : Main clock signal (40MHz) and output signal for T0 observed on a scope with the inputs shorted to a common mode voltage: (a) The threshold voltage is below the offset voltage of the comparator, (b) the threshold voltage is close the offset voltage and the comparator triggers on its noise giving random "1"s.



(a) f_{CK} =33MHz, τ_1=90ns, τ_2=15ns, τ_3=45ns, τ_4=30ns



(b) f_{CK} =40MHz, Vref2=2V, τ_1=75ns, τ_2=12.5ns, τ_3=62.5ns, τ_4=25ns



(c) f_{CK} =33MHz, Vref2=2V, τ_1=60ns, τ_2=15ns, τ_3=45ns, τ_4=30ns

Figure 12 :. The normalized noise response of the comparators versus threshold voltage with the inputs at the same reference voltage (Vref2=2V).