Very High Dynamic Range and High Sampling Rate VME Digitizing Boards for Physics Experiments

Dominique Breton , Eric Delagnes and Michael Houry

***Abstract*--The trend in data acquisition systems for modern physics experiments is to digitize analog signals closer and closer to the detector. The digitization systems have followed the progress of commercial analog to digital converters. The state of the art for these devices is currently 225 MSample/s for a 10 to 12 bit range. The new boards, described in this paper, have been designed to improve these performances by an order of magnitude. In its simplest version, this board mainly includes 4 channels sampling analog data up to 2 GSample/s with an analog bandwidth of 300 MHz, and digitizing it with a 12-bit dynamic range. It is based on the custom-designed MATACQ chip. The latter's innovative design permits reaching these performances with power consumption smaller than 1W. The boards are triggerable either by internal or external signals and several boards are easily synchronizable. The board integrates both GPIB and VME interfaces that permit a maximum readout speed of 500 events/s with the whole memory depth of the 4 channels read.**

***Index Terms*— Application-specific integrated circuits, analog memories, analog-to-digital conversion, very-high-speed integrated circuits**

I. Introduction

THE trend in data acquisition systems for modern physics experiments is to digitize signals closer and closer to the detector. It offers more flexibility for online or offline treatments and is particularly useful in the prototyping or early phases of the experiments. Commercial digitization boards have followed the evolution of ADC technologies and are today available with sampling frequencies of a few hundred MSample/s for a 10-bit to 12-bit resolution. ADC chips with higher performances (8 bits to 10 bits at 1.6 GSample/s) have been developed, mainly for military applications. But they are expensive, difficult to purchase and to implement and exhibit huge power consumption (5 W to 10 W for the sole ADC chip). Moreover, as the data rate at the ADC output is as high as 10 Gbit/s, it is mandatory to use very fast memories or very fast in-flight treatment digital electronics that are also expensive and power consuming. Other commercially available solutions, less compact, based on interleaved lower speed ADCs suffer from the same cost and power consumption limitations. For these reasons, the available commercial boards offering sampling frequencies higher than 1 GSample/s are all limited to dynamic ranges below 10 bits, and to a modularity of only 1 or 2 channels per board. These boards are expensive and several boards are not easily synchronizable, so that their use in multichannel systems is difficult. Yet, there are important needs, particularly in physics experiments, for digitization systems covering a high dynamic range with sampling frequency higher than one GHz. In association with fast detectors, they can be used for timing, pulse shape discrimination and charge measurement even in a high rate or high background environment. The MATACQVME board described here has been developed especially for this purpose. It is built around the MATACQ chip, an analog memory described below.

Manuscript received November 14, 2004; revised April 7, 2005.

Dominique Breton is with CNRS/LAL, BP34, 91898 Orsay, France.

Eric Delagnes is with CEA/DSM/DAPNIA/SEDI, 91191 Gif-sur-Yvette Cedex, France (Corresponding author) email: eric.delagnes@cea.fr.

Michael Houry is with CEA/DIF/DCRE/SDE, BP12, 91680 Bruyères-le-Châtel, France.

II. Description of the MATACQ Chip

The MATACQ chip is a circular buffer based on a new and innovative matrix structure. It was originally designed in the inexpensive AMS CMOS 0.8 µm technology. It makes use, as some former fast analog sampler chips [1], [2], [3] of an array of switched capacitors associated with Delay Locked Loops (DLL). But, thanks to its new matrix structure, its memory depth has been extended to more than 2500 samples.

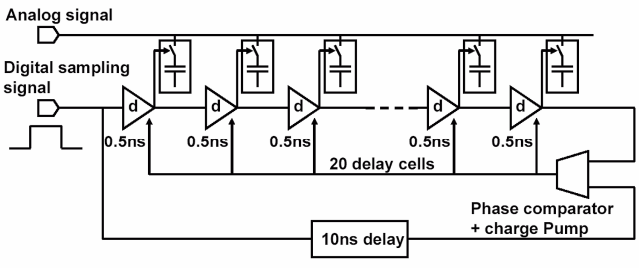

Fig. 1: Principle of the DLL

As in the previous chips, the 2 GHz sampling frequency is achieved with an input clock frequency of only 100 MHz thanks to the virtual frequency multiplication by DLLs. An

example of the corresponding principle is described on Fig. 1. A digital pulse propagates along a chain of 20 individual 0.5 ns delays. All of them can be finely tuned through an analog voltage command. Their respective outputs are connected to the sampling command input of analog memory cells. At the output of the last delay, the phase of the sampling edge is compared to the phase of the input pulse delayed by 10 ns. The phase comparator then produces an analog voltage which is used to servo-control the chain of delays.

As shown on Fig. 2 and Fig. 3, the MATACQ chip is mainly a matrix constituted of 128 sampling DLL like the one of Fig. 1, but arranged in columns. The DLL digital input pulses actually correspond to the successive outputs of a main shift register clocked by the 100 MHz clock reshaped in dedicated blocks. The 10 ns precise delay of each D.L.L is provided by a second shift register (called "reference") where the pulse is delayed by one clock period compared to the first register. During every clock period, the pointer propagates inside a new column, thus covering the full matrix after a while. After having reached the end of the last column, it comes back to the top of the first one.

To eliminate crosstalk between the lines, an input buffer is located between the common analog input and each line. Thus no effect of a switch sampling the signal on a given line can be seen on the next line which will get sampled right after. Moreover, for the same bandwidth, the total power dissipation is lower than with a single global input buffer.

In order to ensure the stability of the servo-control, the DLL has a limited frequency range of operation, typically ranging between 700 MSample/s and 2.5 GSample/s, making it impossible to sample at lower frequencies.

To overcome this limitation, the so-called validation registers can possibly be used to mask some chosen lines during the sampling operation, this thanks to an AND-gate located in each analog-memory-cell command circuit. After the write pointer has reached the end of the matrix, these registers are shifted. Depending on the initial value of the validation registers, this permits reducing the acquisition frequency by a factor 2 to 20 without reducing the memory depth.

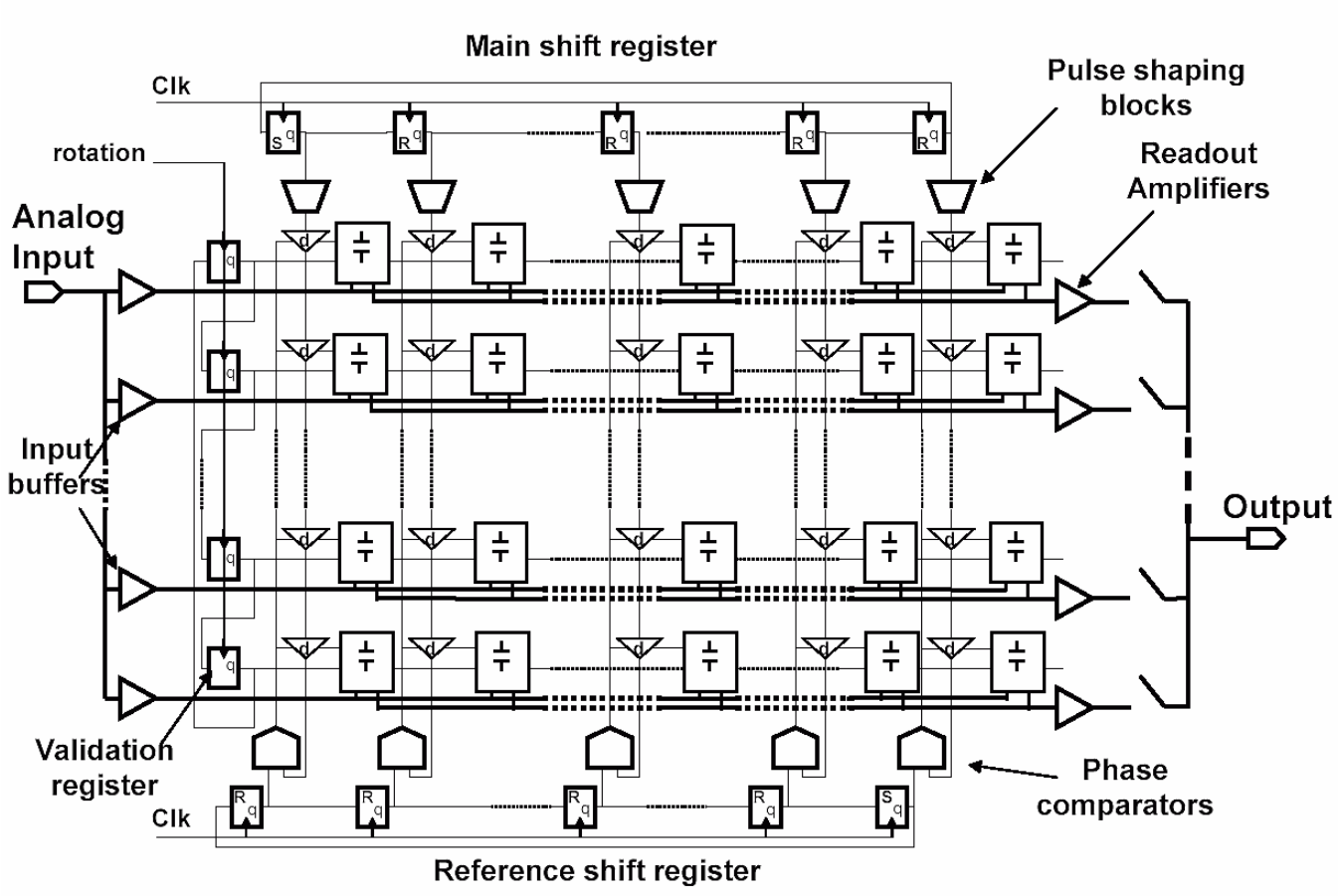

Fig. 2: Principle of the MATACQ chip.

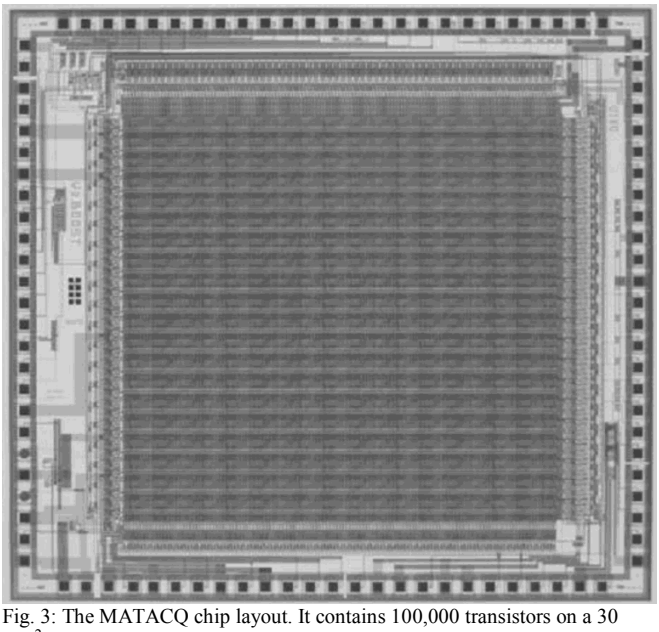

Fig. 3: The MATACQ chip layout. It contains 100,000 transistors on a 30 mm^2 silicon die. The 2560-cell switched capacitor array covers 80% of the chip area.

The input buffers are the most difficult elements to design on the chip. Their own bandwidth, more than that of the memory cells, is the main limitation to the overall bandwidth. They are the main power consumers in the chip. Their bandwidth, and thus the global chip power consumption, is actually programmable by slow control: 1 W for 300 MHz, ½ W for 250 MHz, ¼ W for 200 MHz, below 100 mW in stand-by mode. In order to save power, the amplifiers may also be turned off during the read-out operation of the matrix.

The acquisition is stopped upon reception of a stop signal. The latter derives from an asynchronous trigger signal which is also dated inside the chip by a Time to Digital Converter (TDC) based on a counter and an analog ramp interpolator, with a measurement step of 12 ps.

The analog data is then read in parallel column by column by the read-out amplifiers located on each line, and multiplexed towards an external 12-bit ADC. This can be done either from the first column to the last, or from the column where acquisition was stopped, thus allowing a partial and selective readout of the memory.

As the amplifiers of each line have individual offsets, the pedestal of each line has to be calibrated. This calibration remains valid for months.

This chip has been designed using techniques and structures originally developed for the ATLAS Liquid Argon Calorimeter (LARG) analog memory [4], thus allowing the new design to conserve a wide dynamic range of 12 bits.

III. Description of MATACQVME boards

A. MATACQVME boards overview

The MATACQVME board (see Fig. 4 and Fig. 5), based on several MATACQ chips, is suited for precise acquisition of fast analog signals. It performs the coding of 4 or 8 (depending on the version) analog channels with a bandwidth of up to 300 MHz and over a 12-bit dynamic range, at a sampling frequency (Fe) reaching up to 2 GHz and over a depth of 2520 usable points. This board, in the mechanical format VME 6U (9U for the 8-channel version), is compatible with several standards of acquisition (VME A32/D32, A24/D16 and GPIB). Almost all the board digital electronics is located inside a unique FPGA, of which the configuration EEPROM can be reprogrammed thanks to a JTAG connector. The FPGA provides the bus interfaces, the control of the MATACQ chips and of the RAM, the time-base and the trigger logics.

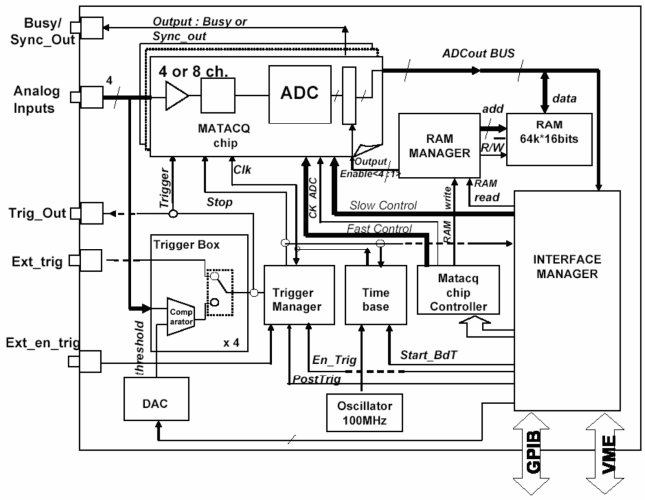

Fig. 4: Synopsis of the MATACQVME board.

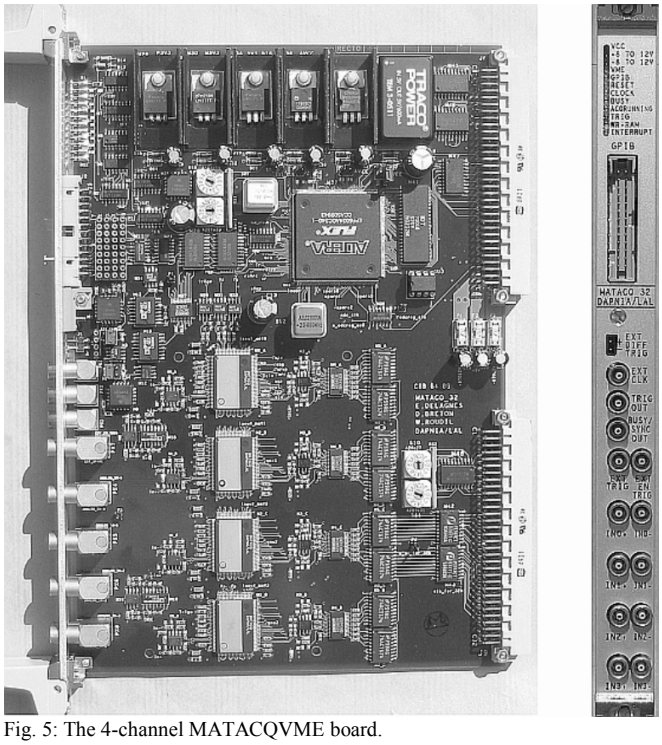

Fig. 5: The 4-channel MATACQVME board.

The board makes use of a 10-layer PCB, where power and ground planes have been carefully designed. All critical analog

and digital signals are sent to the MATACQ chips over differential low level and controlled impedance lines. Special care has been taken to avoid any type of crosstalk between the digital and analog parts.

The clock source is a 100 MHz oscillator. However, an external clock may be used for special purposes. A second oscillator provides a random clock for the trigger system.

The whole acquisition chain is DC coupled. The input analog signals cover the +-0.5 V range, but the latter can be shifted to cope with unipolar signals.

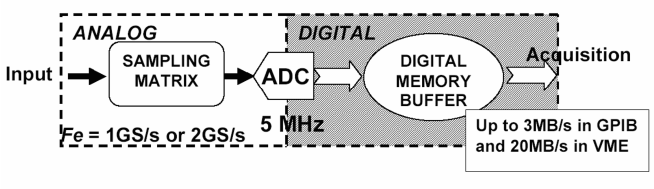

Fig. 6: Data flow in the MATACQVME board.

As shown on Fig. 6, the acquisition is realized in three phases:

-Acquisition: the analog signal is continuously sampled at the sampling frequency Fe in the MATACQ circular analog memory. The arrival of a trigger signal initiates the stopping phase of the sampling. At the end of this phase, the state of the memory is latched: it then contains the last 2560 points sampled (of which 2520 are valid).

-Digitization and storage: upon reception of the order to stop the acquisition, the samples stored under analog form in the MATACQ chips are read out rapidly (650 µs for 4 full channels) and coded into digital data over 12 bits, then stored in the event RAM. The acquisition is then informed of the end of the coding phase by an interruption (it may also scan a flag within an internal register).

- Reading: the RAM can then be read out by the acquisition system. For an acquisition system based on VME A24-D16 standard, this operation lasts a few ms for the full readout of a 4-channel board. This permits to reach an acquisition frequency of a few hundred Hz for the readout of 2500 points per channel. Using the 32-bit readout mode, a rate of 500 acquisitions of all the cells over the 4 channels is reachable. In standard GPIB, rates above 50 Hz are also possible. A special readout mode, allowing the user to transfer selectively only a subset of the memory permits increasing the acquisition rate if necessary.

The board power consumption ranges between 10 W and 20 W depending on its mode of operation. This could be improved by replacing some of the linear voltage regulators by DC-DC converters in a future version of the board.

B. MATACQVME board triggering

Several modes of triggering are available on this board (see Fig. 7). Each analog input is sent to a comparator receiving a common DAC-programmable threshold. Each output of these comparators or any logical-OR combination of them can be used to trigger the board. This can also be done through an external input, compatible with both ECL and NIM levels. Several MATACQVME boards can also be synchronized by using a common external trigger. This signal can be built externally from the "Trig_Out" output available on each board.

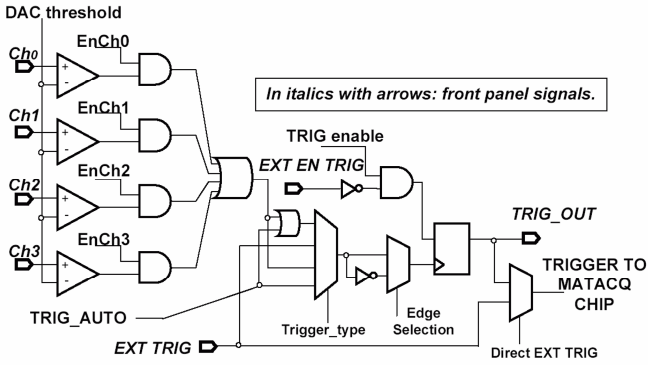

Fig. 7: The trigger selection tree.

The position of the 2500-point acquisition window relatively to the trigger is programmable over a 655 µs range. The on-chip interpolation system tags the trigger with steps of 12 ps, much smaller than the sampling period, thus allowing a good synchronization between channels or boards, and consequently the adequate use of this board in time measurement experiments. Moreover, it also permits performing acquisitions in equivalent time mode for repetitive signals like with an oscilloscope.

C. MATACQVME board performances

Fig. 8 shows the result of a one-shot baseline acquisition performed over 160 channels located in the same crate. The plots are superimposed. Fig. 9 displays an histogram of the rms value of the noise calculated for each channel and for the same data, thus showing a mean value of about 190 µV rms which, combined with the 1 V maximum range, confirms the dynamic range of 12 bits rms.

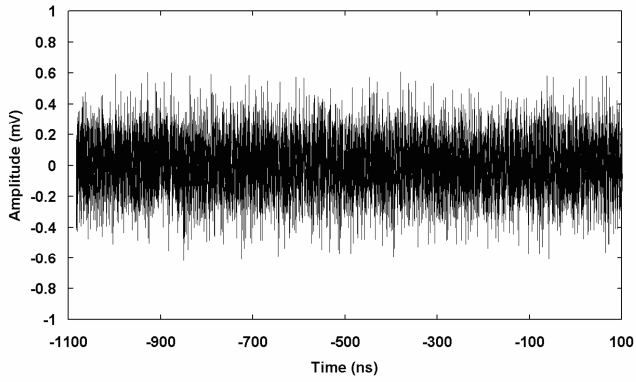

Fig. 8: One shot acquisition of the baseline of 160 different channels.

Fig. 10 shows a simple one shot acquisition of a 10 MHz sine wave signal. One can appreciate how smooth the signal appears thanks to the 12-bit signal to noise ratio when

compared to the same signal sampled with an expensive 8 bit oscilloscope as shown on Fig. 11.

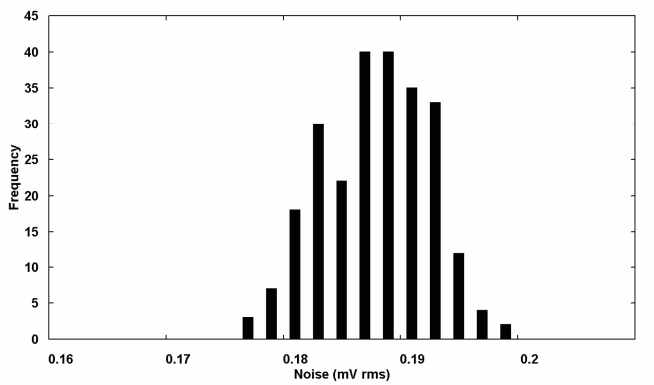

Fig. 9: Histogram of the Noise measured over 160 MATACQ channels.

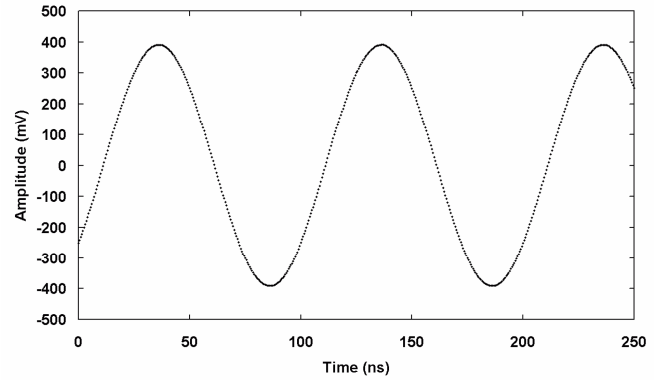

Fig. 10: Acquisition of a 10 MHz 0.8 V peak-peak sinewave with MATACQ.

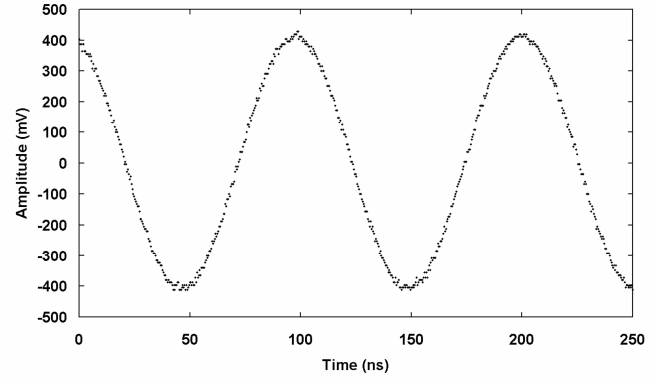

Fig. 11: Acquisition of the same 10 MHz 0.8 V peak-peak sinewave with a high-end (2002), commercial 10 GSample/s oscilloscope.

The integral non-linearity of the board was measured using the pulses (10 MHz of equivalent bandwidth), shown in Fig. 18, of the ATLAS Liquid Argon Calorimeter (LARG) calibration board. The latter is described below. Fig. 12 displays the residues to a linear fit for positive pulses ranging between 0 and 400 mV. The residue absolute values are smaller or equal to one LSB of the ADC, well within +/- 0.5 per mil of the full tested range. This includes the contributions of the MATACQVME board and of the calibration board plus the one of the ATLAS LARG shaper used.

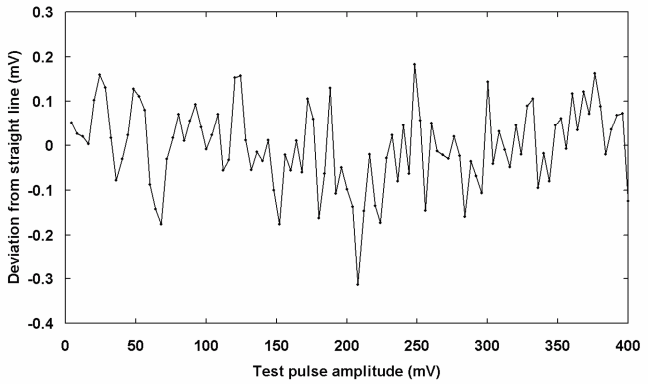

Fig. 12: MATACQ board non-linearity measured with the ATLAS Calorimeter calibration board.

Several different types of jitter can be distinguished inside the board: the clock jitter, the sampling jitter of the MATACQ chip, and the jitter of the trigger and datation chain. The convolution of all of them leads to an overall jitter of 60 ps rms. The latter is dominated by the clock and trigger chains in the range of 50 ps rms. The sampling jitter is much smaller. It can be evaluated from the distribution of the sampling time difference between two different channels of the same board simultaneously fed with the same signal, as displayed on Fig. 13. The extracted rms jitter per channel is indeed of only 20 ps. This permit performing accurate time measurements between channels, and even precise absolute datation if the trigger threshold crossing of the triggering channel is interpolated from the acquired data.

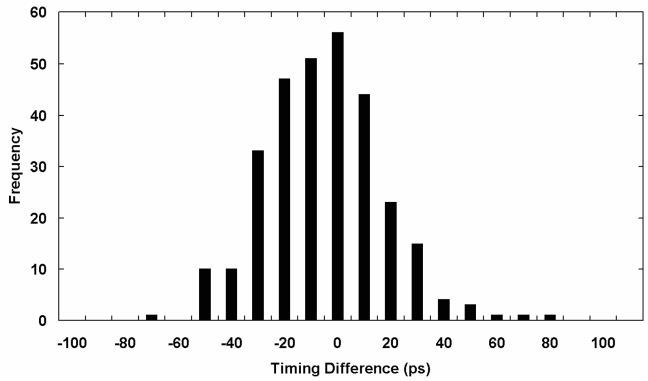

Fig. 13: Distribution of the sampling time difference between two channels.

Another important feature of the board is its ability to perform an FFT on a single acquisition thanks to its high SNR and very good linearity. Fig. 14 shows the result of an FFT measurement on a 10 MHz sine wave with no clock harmonic or spurious frequency above -65 dB.

The effective number of bits (ENOB) was measured on the same sine wave. The SNR was first extracted as the power

ratio between the fitted sine wave and the residues. Then the ENOB was calculated using the usual formula (1):

$$ENOB = (SNR-1.76)/6.02 = 8.7 \text{ bits.} \quad (1)$$

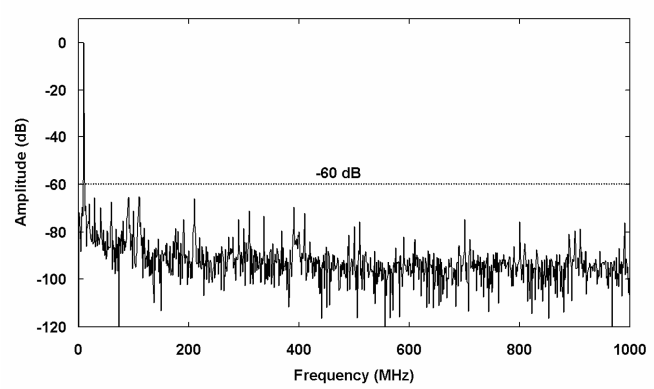

Fig. 14: FFT on a single 10-MHz 0.8-Vp-p sine wave acquisition.

This is dominated by the contribution of the 20 ps rms sampling jitter. The latter's theoretical contribution to the SNR calculated using (2) is indeed 58 dB, corresponding to an ENOB of 9 bits.

$$SNR = -20 \cdot \text{Log} (2 \cdot \pi \cdot f_{sin} \cdot \sigma_t) \quad (2)$$

Where f_{sin} is the sine wave frequency in Hz and σ_t is the sampling jitter in s rms.

For information, the ENOB calculated in the same conditions for the data of Fig. 11 acquired with an oscilloscope is 5.0 bits.

The board ENOB value may limit the application field of the board. However, the ENOB does not describe the board's ability to measure both big and tiny signals at the same time, or to finely discriminate and date piled-up signals, which are the main domains of application aimed at. The jitter value of 20 ps is mainly limited by the matrix structure of the sampler, and could hardly be greatly improved, for example by trying to improve the clock distribution.

TABLE I
MAIN PERFORMANCE AND CHARACTERISTICS OF THE MATACQVME BOARDS

NAME	QUANTITY	UNIT
INPUT IMPEDANCE	50	OHM
DYNAMIC RANGE	+/- 0.5	V
DIGITIZATION LSB	250	µV
NOISE	<200	µV RMS
ANALOG BANDWIDTH	300	MHZ
HARMONIC DISTORSION FOR A 10 MHZ INPUT	< -65	DB
INTEGRAL NON LINEARITY	<1	LSB
DIFFERENTIAL NON LINEARITY	<0.5	PER MIL
SAMPLING FREQUENCY	1 OR 2	GSAMPLE/S
SAMPLING JITTER	<20	PS RMS
CHANNEL TO CHANNEL JITTER	<30	PS RMS
TRIGGER CHAIN JITTER	<50	PS RMS
OVERALL JITTER	<60	PS RMS

The main characteristics and performances measured on the board are summarized in Table I. All the jitter measurements have been performed at 2 GSample/s.

IV. EXAMPLES OF APPLICATIONS

There are currently a lot of applications of the MATACQVME boards. Most of them are gathered within three main fields:

- Timing measurement in very high-rate or noisy environments.
- Test benches for fast detector or electronics chains characterization.
- Pulse shape identification and measurement.

Two examples of application are detailed here.

A. MATACQVME board reading the DEMIN detector

Even if it is now used in a lot of other experiments, as in the CERN Axion Solar Telescope (CAST) [5] since summer 2003, the MATACQVME board had first been developed to perform the readout of the DEMIN neutron detector. The goal of this detector is to perform neutron time-of-flight spectrometry on inertial confinement fusion experiments as NIF (National Ignition Facility) and LMJ (Laser Méga Joule) facilities. DEMIN is a thin Micromegas detector associated with a neutron-to-charged particle conversion foil [6]. It has been designed to offer a very good discrimination between neutrons and gammas. This intrinsic γ-ray insensitivity permits neutron measurements in large γ backgrounds.

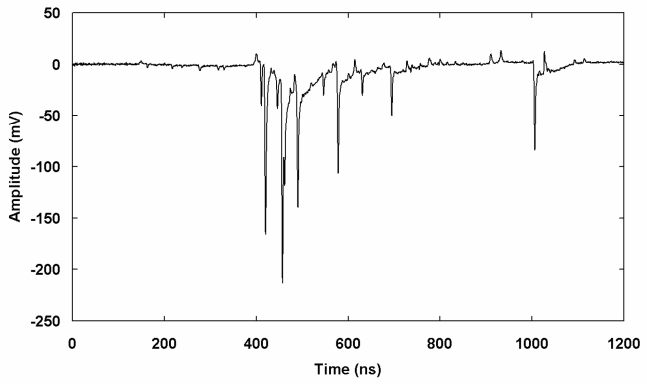

Fig. 15: DEMIN signal acquired with a MATACQVME board.

This detector delivers for each incoming neutron a 3 ns pulse followed by a few tens ns long tail. As the expected rate is very high, the anode of the detector is stripped. Each strip signal is digitized during a 1.2 µs window after the laser shot by a MATACQ channel, in order to extract the timing of the neutron impulsions referred to the laser pulse. This timing permits calculating the neutron energy.

In May 2003, a first 40-channel setup was tested with the Omega Laser (Laboratory for Laser Energetics, Rochester). The record of a complete laser shot is displayed in Fig. 15. It shows the complexity of the signal and the effects of pile-up.

Fig. 16 displays, for the same laser shot, the most occupied time window for two neighboring channels of the detector. It shows the ability for the board's user to measure neutron timing even in case of heavy pile-up (more than 100 MHz mean pulse rate per channel).

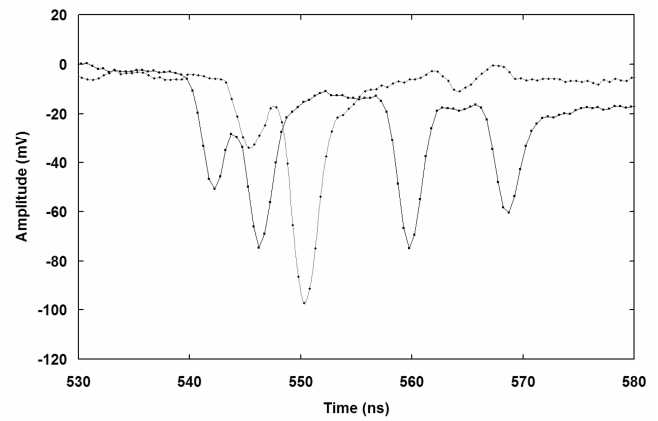

Fig. 16: Zoom on two DEMIN channels acquired with a MATACQVME board.

Due to these heavy pile-up and high pulse rate, a standard timing system built around constant-fraction discriminators and TDC would not have permitted a correct pulse timing measurement. Indeed, these systems introduce dead-time and are not able to distinguish superimposed pulses. Actually, the key point for extracting the neutron pulses is the knowledge of their shape. Their fine extraction would not have been possible with a slower sampling rate. Moreover, the wide dynamic range of the boards allowed the users to perform measurements yet with a good signal-over-noise ratio over a wide range of detector bias conditions without modifying the gain and offsets of the electronics chain.

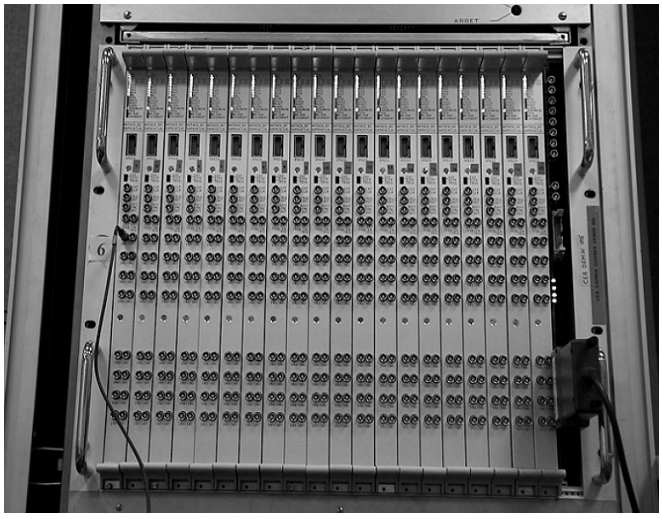

Fig. 17: The 160-channel crate used for DEMIN: a 160-channel 2 GSample/s digitizer.

The time resolution, dominated by the detector, is 300 ps rms, corresponding to a neutron energy resolution of 0.5%. These results, well within the experiment specifications, validated the setup and lead us to build the bigger system shown in Fig. 17. The latter actually consists of 20 8-channel boards located in a single 9U VME crate and powered by a dedicated backplane mounted in the P3 position. The same backplane is used to distribute the GPIB bus which is buffered in the board located on the right side, which is itself connected through its front panel to a laptop PC by a GPIB-USB or GPIB-Ethernet interface.

B. The production test bench of the ATLAS Liquid Argon Calorimeter 128-channel calibration board.

This board is in charge of delivering the very precise detector-like pulses which will be used to calibrate the calorimeter electronics of ATLAS inside the detector. It offers a signal with a steep negative edge followed by a 400 ns long rising decay. The dynamic range is as high as 16 bits, and the precision required is at the level of the per-mil. To validate the boards, the pulses are not measured directly, but at the output of a preamp-plus-shaper chain identical to the one of the calorimeter Front-End board. A plot of the shaped signal acquired by a MATACQVME board at 1 GSample/s is shown on Fig.18.

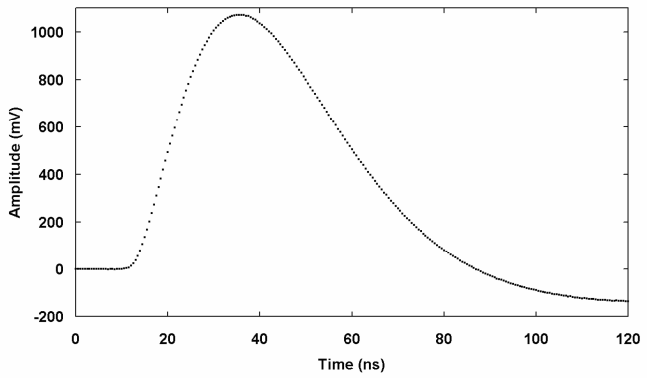

Fig. 18: The shaped ATLAS LARG calibration system signal measured with the MATACQVME board. Note that the shaper inverts the calibration signal.

About 300 of those calibration cards are in production. In order to perform the test of that series, it had first been envisaged to use a standard 40 MHz 12-bit ADC board. But a little dispersion in the peak time of the signal between channels forced people to also make use of an oscilloscope to record the shape and the timing of the signal in order to be able to inter-calibrate the channels. Thus the arrival of the MATACQVME board offered a unique and perfectly adequate solution to group all these measurements. Indeed, the shape can now be measured fast and precisely as shown on Fig. 18. This permits the precise extraction of the peak time and the skew between channels and even of their relative jitter, thanks to a precision better than the ATLAS required one of less than 100 ps rms. Due to the high SNR of the board, the number of acquisitions necessary to obtain the required amplitude precision of 0.1% was reduced by more than one order of

magnitude, particularly in the case of the non-linearity measurement. Thus the time needed for the whole production test could be decreased by a factor of 5.

V. CONCLUSIONS

Two digitizing VME boards based on the new MATACQ ASIC have been designed. These offer a sampling frequency up to 2 GS/s over 4 or 8 channels, a 12-bit dynamic range and a memory depth of more than 2500 samples/channel with a sampling jitter of 20 ps rms. These performances, not available together in any other commercial board, make it adequate for a wide range of applications in test benches or physics experiments where the needed acquisition rates do not exceed 500 Hz. This design was transferred to an industrial partner and is commercially available.

REFERENCES

[1] G. Haller and B. A. Wooley, " A 700 MHz Switched Capacitor Analog Waveform Sampling Circuit", IEEE journal of solid state circuits, vol. 29, no 4, pp. 500-508, April 1994.

[2] S. Kleinfelder, University of California, Berkeley, 1992 Thesis: "A Multi-Gigahertz Analog Transient Waveform Recorder Integrated Circuit", Thesis for M.S. in Electrical Engineering and Computer Science, 1992.

[3] D. Lachartre and F. Feinstein, "Application Specific Integrated Circuits For Antares Offshore Front-End Electronics", Nucl. Instrum. Meth. A442:99-104, 2000.

[4] D. Breton, J. Ardelean, E. Auge, R. Bernier, M. Bouchel, B. Lavigne, G. Martin-Chassard, E. Plaige, J.J. Veillet, E. Delagnes, and M. Huet "A 16 Bit-40 Mhz Readout System Based On Dual Port Analog Memories For LHC Experiments", Proceedings Of The 2nd Workshop On Electronics For LHC Experiments, Balatonfüred (Hungary), Sept 96.

[5] S. Andriamonje, S. Aune, T. Dafni, E. Delagnes, G.K. Fanourakis, E. Ferrer Ribas, T. Geralis, Y. Giomataris, K. Kousouris, T. Papaevangelou, K. Zachariadou, "A low Background Micromegas Detector for Axion Searches". Nucl. Instrum. Meth. A535, pp. 309-313, 2004.

[6] S. Andriamonje, D. Cano-Ott, A. Delbart, J. Derre, S. Diez, I. Giomataris, E.M. Gonzalez-Romero, F. Jeanneau, D. Karamanis, A. Lepretre, I. Papadopoulos, P. Pavlopoulos, D. Villamarin, "Experimental studies of a MICROMEGAS neutron detector", Nucl. Instrum. Methods A 481, pp. 36-45, 2002.