

# Fast neutron irradiation of Monolithic Active Pixel Sensors dedicated to particle detection

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## Abstract

Neutron induced effects have been studied in Monolithic Active Pixel Sensors (MAPS) designed at CEA/Saclay and IPHC/Strasbourg. <sup>55</sup>Fe X rays were used to assess the detection capabilities. The pedestals and the temporal noise were studied together with the charge collection efficiency. The results are compared to estimations of the deep trap introduction rates. For neutron integrated fluxes up to 10<sup>12</sup> cm<sup>-2</sup> these MAPS are weakly degraded by irradiation

*Keywords:* Monolithic Active Pixel Sensors; Neutrons; Charge Collection Efficiency; Noise ; Silicon; Carrier transport ; Irradiation; Defects;

## 1. Introduction

The aim of this work is an evaluation of neutron induced effects on Monolithic Active Pixel Sensors (MAPS). These MAPS [1][2] are currently being developed and characterized for the high spatial resolution Vertex detector devoted to future linear collider experiments. The MAPS studied were MIMOSA8/HIMAPS1 chips developed at CEA/Saclay in collaboration with IPHC/Strasbourg and manufactured by TSMC through MOSIS. They are based on the DC pixel architecture [3], which comprises in-situ double-sampling (Figure 1). Each pixel includes a detection diode with a limited sub-surface depletion region (less than a few  $\mu\text{m}$ ), a readout MOS amplifier followed by a capacitor and a switch which allows the storage of a reference level. Three 32 rows sub-arrays S2, S3, S4 were implemented on the chip, their only difference being the detection diodes of sizes 1.2  $\mu\text{m}$  x 1.2  $\mu\text{m}$ , 1.7  $\mu\text{m}$  x 1.7  $\mu\text{m}$ , and 2.4  $\mu\text{m}$  x 2.4  $\mu\text{m}$  respectively. The analog signals are read column wise by an output buffer and output extra board. The signal at the analog outputs (8 columns) is the difference between a reference signal (calibration) and the readout signal (read) and is

## 2. Effects of neutrons on MAPS: basic considerations

In epitaxial processes, such as the one used here (TSMC 0.25  $\mu\text{m}$ ) the degradation due to neutron irradiation is mainly due to atomic displacements in the thin epitaxial

computed offline. This enables the extraction of the signal and a reduction of the output pedestals (offsets). The pixel circuitry is synchronous and clocked externally, sequencing digital circuitry being integrated on the chip. The DAQ card was developed at IPHC/LEPSI (Strasbourg). A few un-irradiated reference chips were measured. For extensive design details, the clocking scheme description and preliminary measurements on these chips see reference [3][4].

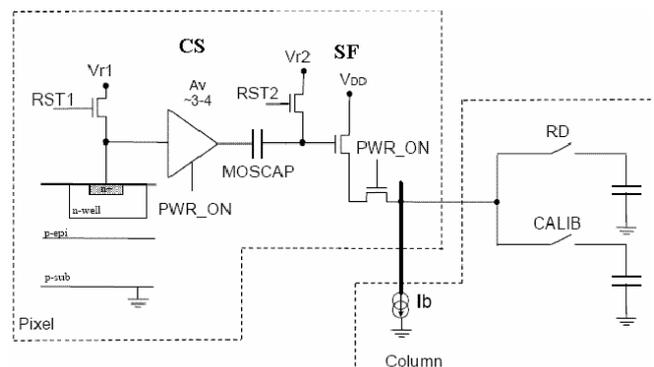


Figure 1: pixel architecture (after [3]) used for the present neutron irradiation study © IEEE 2005.

layer. Various defects are created. These defects induce deep levels that affect carrier transport in silicon and reduce the lifetime of the carriers. Electron transport is the dominant signal build-up mechanism in these MAPS. There are clearly two kinds of effects. The first one is the

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increase of the generation-recombination current in the depleted region of the sensing junction. This current is integrated on the sensing node and can be probed in this way. The second one is carrier capture that affects the free drift length of the electrons and their diffusion length, bearing in mind that in these sensors transport mainly occurs by diffusion. Let  $\sigma_n$  be the electron capture cross section, for one type of deep trap with concentration  $N_t$  the free drift length  $L$  is given by  $(N_t\sigma_n)^{-1}$ .  $L$  is reduced when the trap concentration increases along with neutron integrated flux. The electron lifetime  $\tau_n$  is reduced too and this induces a decrease of the electron diffusion length  $L_n = (D_n\tau_n)^{1/2}$  where  $D_n$  is the diffusion constant. For a single kind of trap  $\tau_n$  is related to the concentration through  $(v_{th}N_t\sigma_n)^{-1}$  where  $v_{th}$  is the carrier thermal velocity.

### 3. Measurement procedure

The devices characteristics (noise, pedestals, etc) were measured at room temperature with a 1 MHz clock frequency corresponding to 2.048 ms readout time. The neutron flux has a spectrum which extends to 20 MeV [5]. Its peak is located around 1 MeV. Flux measurements have a 25 % uncertainty. In this work seven chips were irradiated at room temperature up to  $\sim 10^{13}$  neutrons/cm<sup>2</sup>. The pedestals are defined as the offset voltages of each pixel measured at the columns output. The Fixed Pattern Noise (FPN) is defined as the standard deviation ( $\sigma$ ) of the pedestals distribution across the array. The distribution of each pixel output voltage during acquisition is determined. The mean value of its standard deviation to its average value represents then the temporal noise.

### 4. Effects on the pedestals

Figure 2 shows the distribution of pedestals on

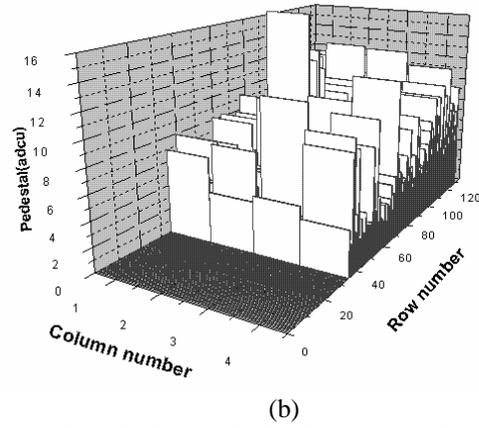
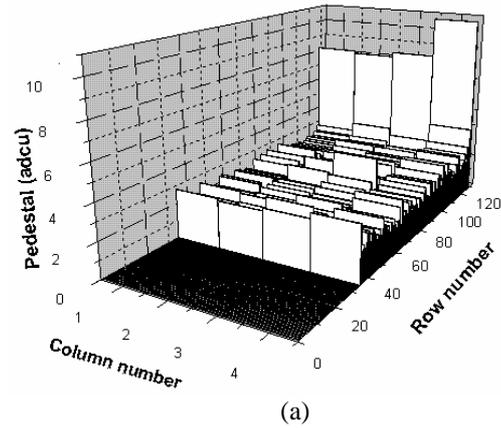


Figure 2 (a): distribution of pedestals on arrays of four column for a chip irradiated at  $1.44 \cdot 10^{11}$  n/cm<sup>2</sup>. The last rows, with large pedestals, are known to be noisy even before irradiation

(b): distribution of pedestals on the same arrays of four columns for a chip irradiated at  $1.13 \cdot 10^{13}$  n/cm<sup>2</sup>. The residual pedestals values are related to the characteristics of the

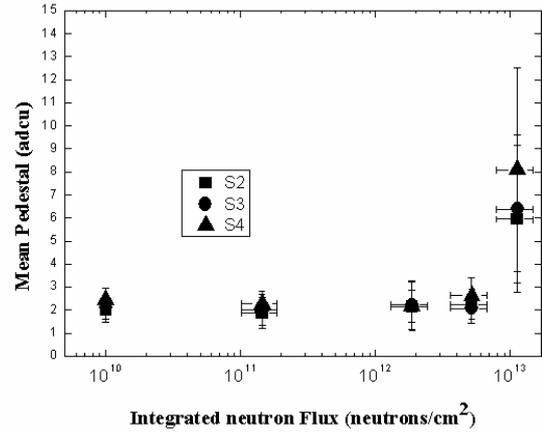


Figure 3: mean pedestals versus neutron-integrated flux for the central columns (3 sub-arrays). Four columns were taken in the computation; the first point corresponds to an irradiated sample. The error bars correspond to the sigma on the pedestals (vertical scale: 1 adcu=0.5 mV).

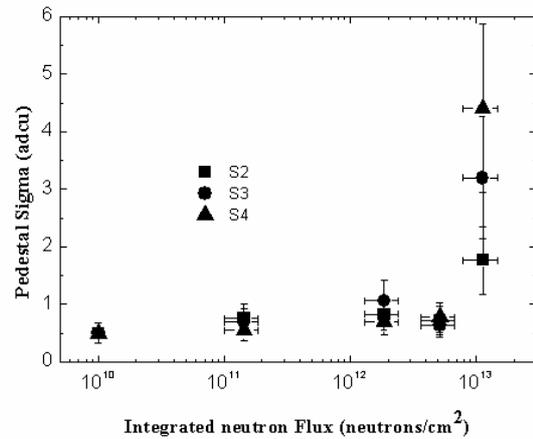


Figure 4: pedestal sigma (standard deviation of the offsets or fixed pattern noise) versus integrated neutron flux for the 3 sub-arrays studied. Four columns were taken in the computation (vertical scale : 1 adcu=0.5 mV). The far left point corresponds to a non-irradiated sample.

sensing elements and the material process. Figure 3 shows the variation of the pedestals with integrated flux and Figure 4 the dispersion of the pedestals (FPN) with integrated flux. Both plots show a remarkable stability of these pedestals characteristics up to  $5 \times 10^{12}$  neutrons/cm<sup>2</sup> and an important increase above  $10^{13}$  neutrons/cm<sup>2</sup>. The FPN varies by factors ranging from 3 to 8 while the corresponding pedestals vary by factors ranging from 3 to 4. The dispersion between neighbouring pixels (as seen in Figure 2) may find its origin in the non-homogeneous distribution of neutron-induced defects in the sensitive silicon epitaxial layer. Because of the size of the radiation induced cluster-defects it should be clear that the deep trap concentration can only be more homogeneous (see §6) at much higher integrated fluxes. Moreover, the FPN increase with the integrated neutron flux may be related to the spatial distribution of neutron-induced cluster-defects.

### 5. Effects on the temporal noise

The noise is weakly dependent on the total integrated flux (Figure 5) in this range.

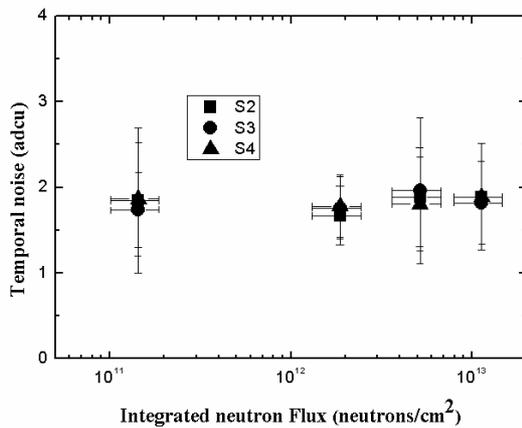


Figure 5: temporal noise versus integrated neutron flux in adc units for the three sub arrays (vertical scale : 1 adcu=0.5 mV).

Most of the noise is due to the readout noise, as previous measurements on un-irradiated chips have shown. The temporal noise is not due to the detector diode itself.

### 6. Origin of the pedestal and noise sensitivity to neutrons

Previous work shows that irradiation by massive particles in semiconductors produces defects that trend to form clusters. These macrodefects (different in size from point defects) have a linear spatial extension up to few  $\mu\text{m}$  [6][7][8]. The collision cross section for 1 MeV neutrons on silicon is approximately  $3 \times 10^{-24}$  cm<sup>2</sup> [9]. Simple calculations show that for an integrated flux of  $10^{13}$  neutrons/cm<sup>2</sup> the total number of atomic collisions is of the order of  $10^9$  collisions /cm<sup>2</sup>, assuming a worst case  $10 \mu\text{m}$  epitaxial layer thickness. For MeV energetic neutrons, each primary collision induces a cascade of approximately 500 secondary displacements. The threshold energy for atomic displacements in silicon is 20 eV and the energy of the Primary Knock on Atom (PKA) is roughly 36 keV on

average, leading to around 500 atomic displacements (for the principle of the calculation see [10] and [11]). The number of primary displacements in the active region of a single pixel approaches 10000 at  $10^{13}$  neutrons/cm<sup>2</sup>. For integrated fluxes 100 times lower ( $10^{11}$  neutrons/cm<sup>2</sup>), the total number of generated defects below each pixel is then lower than 50000 ( $500 \times 100$ ) corresponding to an initial concentration of  $5 \times 10^{12}$  neutrons induced defects per cm<sup>3</sup>. The effect of neutron irradiation at this integrated flux is very low as it can be seen in Figure 2(a). This effect results from defect-clusters non-homogeneously distributed in a pixel. The total defect-cluster volume remains lower than the volume of the pixel's epitaxial layer below  $10^{13}$  neutrons/cm<sup>2</sup>. Limited extended-defect overlap occurs at this integrated flux level. This possibly results in a spread of the pixels leakage currents throughout the sensor and this could explain the observed pedestals dispersion. The pedestals dispersion could level off if the total defect concentration is drastically increased through irradiation. This should be checked experimentally.

### 7. Degradation of the charge collection efficiency

Detection of <sup>55</sup>Fe X photons measurements were made to measure the charge collection efficiency (CCE). The CCE is here defined as the ratio of the position (Most Probable Value of signal amplitude) of the peak corresponding to 9 adjacent-pixel clusters to the calibration peak (total collection of the charge in one single pixel). The calibration peak position does not vary under irradiation. The result is displayed in Figure 6. The charge collection efficiency is directly related to the electron transport properties in the silicon.

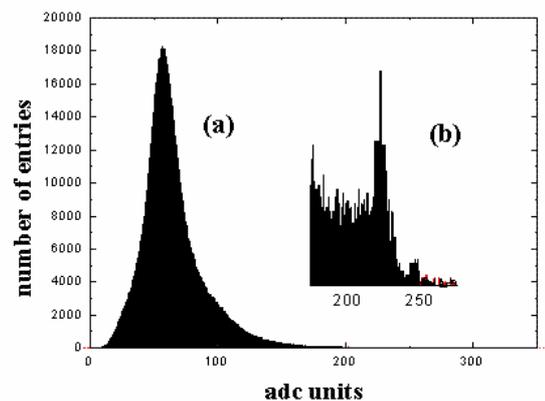


Figure 6: charge collection from 5.9 keV X photons at  $1.13 \times 10^{13}$  n/cm<sup>2</sup> (a) nine pixels cluster peak (b) calibration peak ((horizontal scale: 1 adcu=0.5 mV, vertical scale: arbitrary units).

Deep traps reduce the electron migration length and lower the average signal amplitude through various signal build up mechanisms. Simulations could help to evaluate quantitatively the effects of neutron-induced deep traps on the signal formation. Reduced charge collection leads to a shift of the cluster peak towards lower values. The charge collection efficiency plotted versus integrated neutron flux is given in Figure 7.

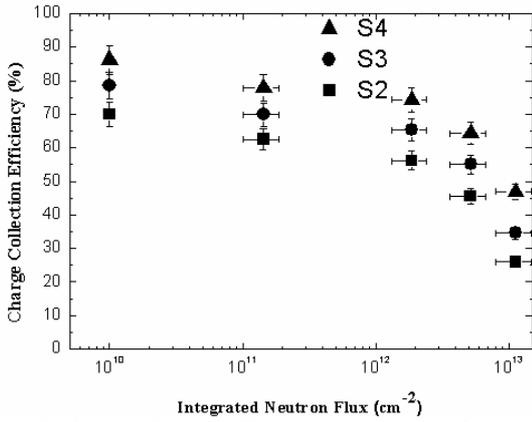


Figure 7: charge collection efficiency versus integrated neutron flux for the three sub-arrays studied (linear scales). The point at the left corresponds to an un-irradiated chip.

It is clear that the CCE drops for integrated fluxes above  $10^{12}$  n/cm<sup>2</sup>. This is due to charge transport degradation. Large detecting media dimensions compared to the migration length of the carriers result in a high sensitivity of the detector to traps [10]. Subsequently, as pixel clusters are larger than elementary pixels, their sensitivity to neutron irradiation could be higher than that of single pixels. The number of primary collisions in the epitaxial layer of a 9-pixel cluster is  $10^4$  for  $10^{11}$  n/cm<sup>2</sup>. This indicates that for integrated fluxes up to  $10^{11}$  n/cm<sup>2</sup> the effects should be limited. The CCE is more sensitive to neutrons than the pedestals.

### 8. Pixel leakage current and discussion

At this clocking frequency (1 MHz) the time interval between two readouts is about  $128 \times 1\mu\text{s} \times 16 = 2.048$  ms. When no events occur (no X photon hit) this is the time interval between which the leakage current is effective in changing the pedestals. For the highest integrated neutron flux and the largest diode (S4) the pedestal value is approximately 4 mV. This means that the slew rate is given by:  $dV/dt = 4 \text{ mV}/2.032\text{ms} = 1.97 \text{ V/s}$ . For the S4 sub-array of these chips the conversion factor is  $52 \mu\text{V/e}^-$ , equivalent to  $3.23 \cdot 10^{14}$  Volt/Coulomb. The equivalent capacitance is then  $3.09 \cdot 10^{-15}$  F. The leakage current in the sensing material is then given by:  $i=C(dV/dt) = 1.97 \times 3.09 \cdot 10^{-15} = 6.09 \cdot 10^{-15}$  A. This weak value shows that the recombination-generation current remains low.  $J=qW < N_t > \sigma_p \sigma_n v_{th} n_i / (\sigma_n + \sigma_p)$  is the current density in the diode due to recombination processes. Let us name  $W \sim 1\text{-}5\mu\text{m}$  the depth of the depletion region below the n+ electrode. If  $\sigma_n \sim \sigma_p \sim 10^{-15} \text{ cm}^2$  (neutral traps),  $v_{th} \sim 10^7 \text{ cm.s}^{-1}$ ,  $n_i \sim 1.45 \cdot 10^{10} \text{ cm}^{-3}$ , this gives  $J \sim < N_t > W \times 10^{-21} \text{ A/cm}^2$ . The concentration of traps can be computed with a current density of:  $J \sim 0.1057 \cdot 10^{-6} \text{ A/cm}^2$  assuming squared diode ( $2.4 \mu\text{m} \times 2.4 \mu\text{m}$ ) as being then:  $< N_t > \sim 9.03 \cdot 10^{13} / W \text{ cm}^{-3}$ . This gives an electrically active deep trap introduction rate  $K = < N_t > / \Phi$  in the range:  $7.9\text{-}1.6 \text{ cm}^{-1}$  (corresponding to  $W \sim 1\mu\text{m}\text{-}W \sim 5 \mu\text{m}$  respectively). This value should be compared to the value of  $50 \text{ cm}^{-1}$  that results from numerical estimations (§ 6), or to experimental values (e.g.

$\sim 5 \text{ cm}^{-1}$  in [12]). A defect annealing process similar to the one found in germanium [9] can be a reason for a lower experimental value. In an unirradiated sample the trap concentration deduced from a similar calculation is more than 4 times lower, the leakage current finding then its origin in native defects located inside the detector active region. This approach also gives us an estimation of the electron lifetime (§2) in the depleted region of the sensor at  $\sim 10^{13}$  n/cm<sup>2</sup>. This value is of the order of 1-5  $\mu\text{s}$ , and is useful for calculations and future MAPS simulations.

### 9. Conclusion and future work

The results show that for integrated fluxes lower than  $10^{12}$  neutrons/cm<sup>2</sup> the effects on the pedestals, the CCE and the temporal noise of these chips is low. These MIMOSA8 chips have encouraging characteristics with respect to displacement effects due to neutrons as preliminary measurements made on earlier and simpler MAPS had suggested[13]. This present work should be supplemented by a study of the clock frequency influence on the characteristics of these devices. Beam tests of irradiated chips could adequately complete this work on MAPS primarily designed for charged particle detection.

### Acknowledgments

The contribution of J.Briaud and co-workers at CERI (Orléans, France) where the irradiations were performed is acknowledged. An IN2P3 Orsay group kindly provided a few nickel samples used for dosimetry. We acknowledge the support of E. Delagnes (DAPNIA), the contribution of Y. Degerli (DAPNIA) and that of our colleagues in IPHC.

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