A Multigigahertz Analog Memory with Fast Read-out for the H.E.S.S.-II Front-End Electronics

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Abstract– **The H.E.S.S.-I front-end electronics is based on the ARS0 chip, a multigigahertz sampler and analog memory used as a level-1 circular buffer. In the future H.E.S.S.-II, the energy threshold will be decrease as low as 10 GeV. This will require a much higher acquisition rate capability and a larger dynamic range incompatible with the electronics developed for HESS-I. These constraints led to the development of the SAM (for Swift Analog Memory) chip to replace the ARS0. The SAM chip includes 2 analog memory channels, with a 256-cell depth each. The sampling frequency is adjustable up to 2GS/s. Thanks to the matrix structure of the analog memory, the readout-time of an event has been decreased by more than two orders of magnitude compared to the one obtain with the ARS0 chip. It permits to deal with the high expected rate of H.E.S.S.-II. The SAM input bandwidth and dynamic range are increased up to 250 MHz and more than 11 bits respectively.**

I. Introduction

The H.E.S.S. experiment is a new generation of ground based atmospheric Cherenkov detector located in Namibia and dedicated to gamma ray astronomy in the 100GeV-10TeV energy range. In its phase I (H.E.S.S.-I), it consists of an array of four 107 m^2 telescopes working in stereoscopic mode. For each telescope, the very compact camera, located at the focal plane, accommodates all the data acquisition electronics. The camera consists of 960 closely packed photomultiplier tubes (PMT). Its electronic read-out architecture [1] is based on the ARS0 chip [3] that allows digitizing the PMT signals at a GHz rate for moderate power consumption. The A-D conversion of the PMT signals is achieved inside the camera, so that very few cables come out from the camera. The first telescope has been taking data reliably since June 2002 and the four telescope set-up is fully operational since the end of 2003. In the second phase of the experiment (H.E.S.S.-II) [2], it is planned to add a 600 m2 telescope in the centre of the existing array, equipped with a 2048 P.M.T.s camera. In stand alone mode, its energy threshold will be in the 10 to 20 GeV range, connecting the energy range of H.E.S.S. to those of satellite experiments and giving access to new objects such as pulsars and AGNs at larger red-shift.

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The front-end electronics architecture of this new instrument will be very similar to the one of the first telescopes.

But, as the ARS0 chip cannot fulfill new requirements arising from the lowering of the energy threshold, a new sampling chip SAM (Swift Analog Memory) has been designed. This paper first discusses the specifications for this new chip, describes its architecture and presents measurement results on the SAM chip.

II. SAM Chip Description

A. H.E.S.S.-I front- electronics overview and its limitations.

The H.E.S.S.-I front-electronics, shown in Fig 1, is based on the ARS0 chip developed firstly for the ANTARES experiment.

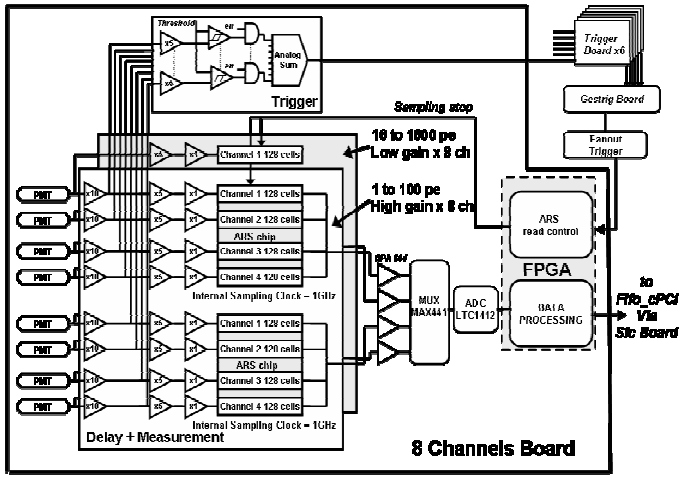

Fig. 1: Block diagram of the H.E.S.S.-I electronics.

The analog signal, coming from one of the 960 P.M.T.s of the camera is continuously stored at a 700 MHz sampling rate in the 128 analog memory cells of the ARS0 chip, used as a circular buffer, while it is compared to a threshold by a fast discriminator. The result of the discrimination, combined with those from the other channels is used to elaborate the level 1 trigger that is sent back to the front-end with 70ns latency. Whenever a final camera trigger occurs, the analog memory is frozen and a given number of cells Nf, typically 16, can be read back, starting from a cell located at a programmable offset Nd from the cell corresponding to the arrival time of the trigger. These analog read-back samples are converted by off-chip A.D.C. and the charge of the P.M.T. signal is computed by an FPGA located on the front end board. Then the

sampling in the circular analog memory is restarted, waiting for the next trigger. To cope with the large signal dynamic range of the photomultiplier, two channels with a gain ratio of 10, defined by external amplifiers, are used. This system has proven its excellent performances and high reliability during the three years of operation of the H.E.S.S.-I phase. However, as detailed below, some limitations prevent using the ARS0 for the next phase H.E.S.S.-II.

First, in H.E.S.S.-I, the ARS-ADC section is the major bottleneck in the acquisition data flow. The digitization of a 16 cells Cherenkov event takes 275 µs leading to a ~10% dead-time when the experiment operates at its nominal acquisition rate of 300Hz.

Then, as explained previously, the ARS0 limited analog input bandwidth of 80MHz broadens the 5ns-long PMT signal by more than a factor of two, forcing to use a quite long integration window resulting in a larger noise from the night sky background (N.S.B.).

B. *H.E.S.S.-II front-end electronics.*

Considering the excellent results of the H.E.S.S.-I DAQ and the very tight schedule to build H.E.S.S.-II, the design of the Front End electronics for the new telescope, shown in Fig. 2, is very similar to that of the existing telescopes. In particular, it is based on the same dual-gain architecture using fast analog circular memories.

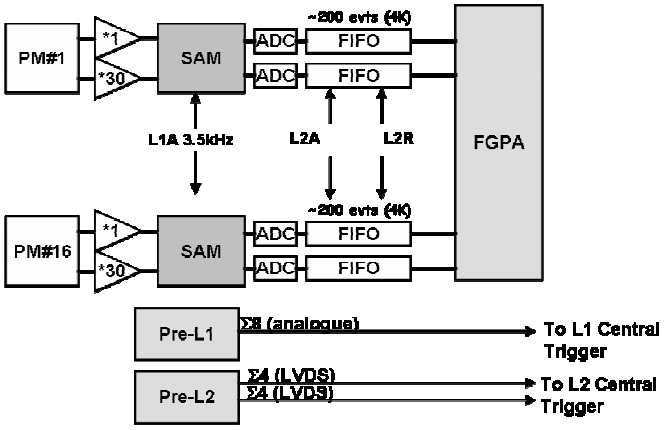

Fig. 2: Block diagram of the H.E.S.S.-II electronics.

However, because of the lower energy threshold: i) the expected trigger rate for each pixel of the H.E.S.S.-II camera is expected to be at least an order of magnitude higher than in H.E.S.S.-I , ii) the dynamic range of H.E.S.S.-II will extend up to 5000e- and iii) a FIFO buffer is added in order to manage a second level trigger and to smooth the trigger fluctuations. Since the two first requirements cannot be fulfilled by the ARS0, a new analog memory, named SAM, with the same functionality of the previous chip, but with improved performances, mainly concerning the readout speed and the dynamic range, had to be designed. The ratio between the two gains of a photomultiplier channel is increased in the range of 25 to 30 to cope with the dynamic range.

C. *Description of the SAM chip.*

The SAM chip, whose block diagram is shown in Fig. 3, uses the 3.3V CMOS AMS 0.35µm technology. Its area is only 11 mm^2 and integrates 60000 transistors.

It features only two channels, of 256 analog storage cells each, used to sample the high and low gain signals of a photomultiplier channel. This extended depth allows to cope with longer trigger latencies than in H.E.S.S.-I.

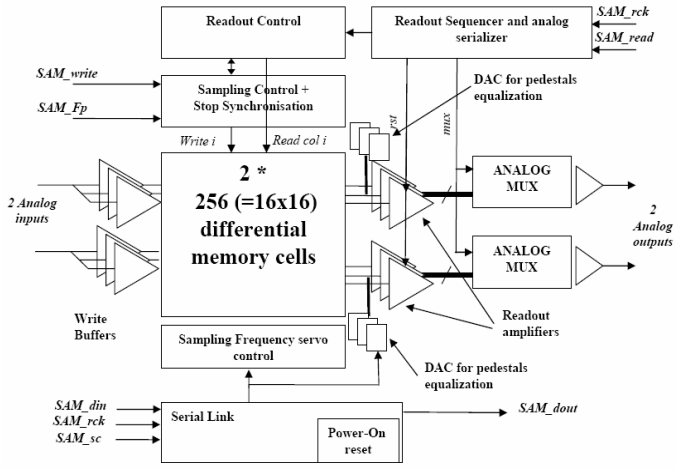

Fig. 3: Block diagram of the SAM chip.

As in the ARS, the high sampling frequency (Fs) of the SAM is obtained by a virtual multiplication of the lower frequency clock (Fp) using internally servo-controlled Delay Line Loops (D.L.L.). But, rather using the standard linear structure, each analog memory channel is configured as a matrix of 16 lines with 16 capacitors each, shown in Fig. 4. This structure was already used in the MATACQ chip described in [4]. In this structure, successive capacitors in the same column contain consecutive analog samples taken at 1/Fs whereas successive capacitors in the same line contain samples taken at 1/Fp=16/Fs intervals. The sampling timing is ensure by a 16-step D.L.L. associated with each column and which delay is servo controlled to 1/Fp. The input signal is splitted, using for each line, a voltage buffer feed the analog signal.. In each line, a readout amplifier permits to read back the analog information stored in the capacitors. During readout, the read amplifier outputs are time multiplexed toward an external A.D.C. Both the write and read operations are performed in voltage mode in the capacitors to ensure a total voltage gain robustness against parasitic elements or components mismatch.

The matrix architecture offers the following advantages compared to the standard linear sampling D.L.L. structure:

- Better analog bandwidth for the same power consumption dissipated in the input buffers.
- Lowest switching noise during the write phase as the switching time interval between two

consecutive memory cells on the same line is long (1/Fp).

- Lower readout noise. This noise contribution is, at the first order, proportional to 1+Cr/Cs where Cs is the capacitance of the storage element and Cr is the total capacitor of the readout bus connected to the negative input of the readout amplifier. Actually, Cr is smaller in a matrix structure, because the read busses are shorter than in the linear structure
- Faster readout time, as 16 consecutive capacitors are read simultaneously by the readout amplifiers.

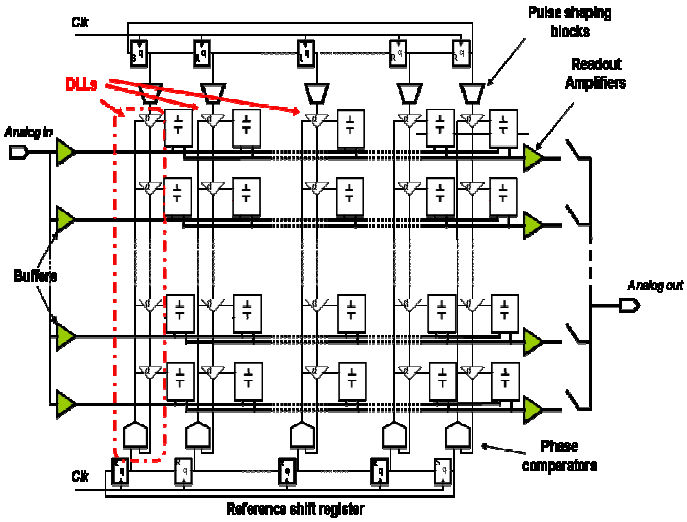

Fig. 4: Principle of the sampling D.L.L. matrix.

Several functions have been added or improved compared to the previous [3] and [4] chips:

- A functional block memorizing the position of the last cell written before the stop signal arrival and calculating the index of the first cell to be read back using the Nd value.
- A functional block selecting the 16 capacitors to be read in parallel. Actually, these capacitors are eventually spread on two consecutive columns, depending on the index of the first cell to be read,
- One 7-bit DAC for each line of the matrix to compensate the static offsets due to the use of amplifiers on each line in the matrix structure. These DAC must be set during a dedicated calibration phase without input signals.
- The D.L.L.s have been designed to avoid unlocking during readout which would introduce extra deadtime between acquisition.
- A slow-control serial link to program various parameters of the chip (Nd, DACs settings, test mode, biasing of the amplifiers…).

To decrease the effect of digital switching, each analog memory channel is actually fully differential and all the potentially noisy digital input or output chip signals are using LVDS standard.

III. Performances Measured On The SAM Chip.

The chip characteristics have been measured on a very first prototype of the H.E.S.S II front-end board. It includes two bi-gain channels (gain 1 and 25) each feeding a SAM chip, 4 ADCs, FIFOs, and a F.P.G.A. controller. For each channel, a fast discriminator allows auto-triggering. This setup was not designed to obtain the ultimate chip performances but to perform realistic measurements representative of the final front-end electronics.

The main performances of the SAM chip, summarized in Table I are matching the experiment requirements and our expectations.

The Chip has been characterized at 1 and 2 GSample/s but is still working for sampling frequencies higher than 2.5 GHz. The nominal sampling frequency used for H.E.S.S.-II will be 1GHz, so that all the characteristics and plots reported hereafter have been measured for this value.

The SAM chip has been operated using repetitive input signals at rate up to 800 kHz, reading back 16 samples by event. The chip behavior and its charge resolution were the same than at lower rate validating thus the robustness of the D.L.L. design.

The chip analog bandwidth is larger than 250 MHz, so that a 5.5ns pulse, simulating a H.E.S.S.-II photomultiplier signal, is widened to only 6ns as shown in Fig. 5. This allows using integration windows as short as 8ns and then to limit the noise due to Night Sky Background.

TABLE I
MAIN SAM MEASURED PERFORMANCES

NAME	Value	Unit
Power Consumption	**300**	**mW**
Sampling Freq. Range	**<1to 2.5**	**GS/s**
Analog Bandwidth	**~250**	**MHz**
Maximum event readout Frequency	**>800**	**kHz**
Read-out speed for Ncell cells to read	**90+ 90* cell**	**ns**
Fixed Pattern noise	**0.4**	**mV rms**
Total noise	**0.65**	**mV rms**
Maximum signal (limited by ADC range)	**2**	**V**
Dynamic Range	**>11.6**	**bits**
Crosstalk	**<3**	**per mil**
Integral non linearity	**< 1**	**%**
Sampling Jitter	**<40**	**ps rms**

Before any offset corrections, the cell-to-cell pedestal non-uniformity over the 256 cells of a channel is 2.5mV rms, which is quite large, as expected. After calibration, the line by line offset cancellation operation, taking benefit of the DACs associated to each line, reduce drastically this value to 0.4mV rms. This calibration remains valid for weeks. As the noise is 0.65mV rms and that the maximum signal is 2V, the dynamic range of SAM is 11.6 bit rms. Actually, the dynamic range is

limited both by the range of the used ADC and by the signal distortion appearing for the largest fast signals because of the limited write buffers slew rate.

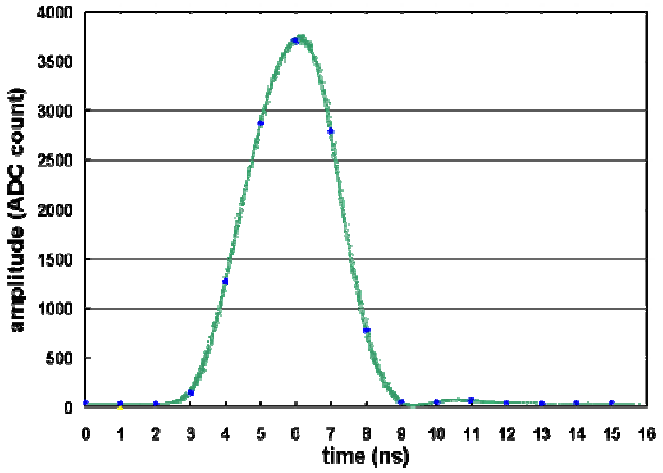

Fig. 5: Electrically simulated PMT pulse sampled at 1 GHz.. The blue dots are corresponding to a single shot acquisition. The Green dots are corresponding to 1000 asynchronous repetitive acquisitions superimposed.

As the two gains of a photomultiplier signal are treated the same SAM chip, the crosstalk between the two channels must be as low as possible. If not, the saturation of the high gain could induce non-linearity on the low gain. Actually, the crosstalk between the two channels inside the chip is very small (<0.3%). Its shape is derivative so that its integral within the time window used to compute the charge of the signal (8 to 12 ns) is not measurable (<0.1%).

A single photoelectron spectrum measured using a H.E.S.S.-II photomultiplier is plotted on Fig. 6. The very low noise allows reaching peak-over-valley ratio larger than 2.5.

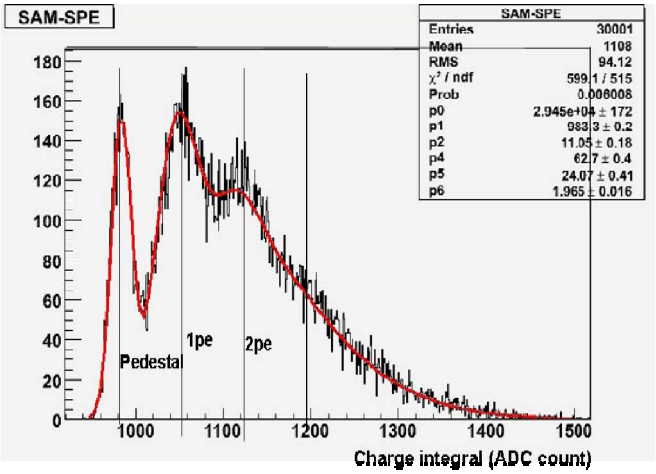

Fig. 6: Single Photoelectron spectrum measured with SAM connected to a H.E.S.S.-II photomultiplier. For this measure the tube gain was 1.5 larger than the nominal value.

The linearity of the bi-gain system, thus also including the effects of saturation of the highest gain, has been measured using electrical pulses, as those of Fig. 5, to simulate a photomultiplier signals. The Fig. 7 shows the charge integrated on a window of 12 SAM samples as a function of the input signal normalized in photoelectrons. The integral non-linearity characteristic plotted on Fig. 8 is obtained by calculating the relative residues to a linear fits on the same data. The integral non-linearity of the system remains smaller than +/-1% on a 1 to 5000 photoelectron range.

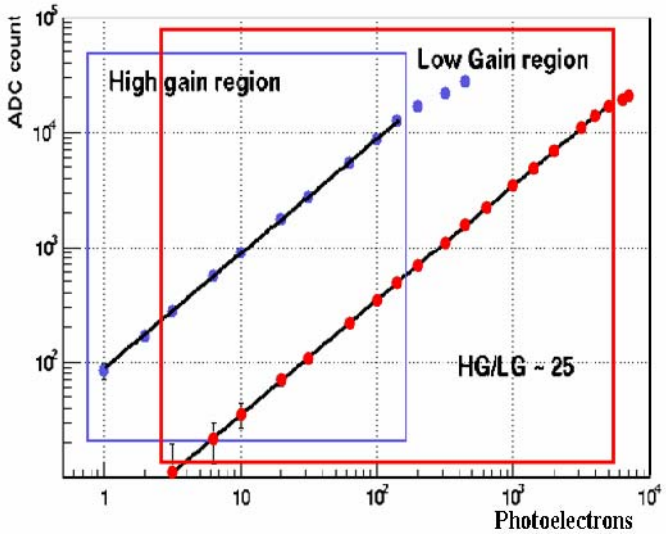

Fig. 7: Transfer function of the Bi-gain system including a SAM. The blue dots are for the high gain channel, the read ones are for the low gain channels. The error bars are corresponding to the rms value of each measurement.

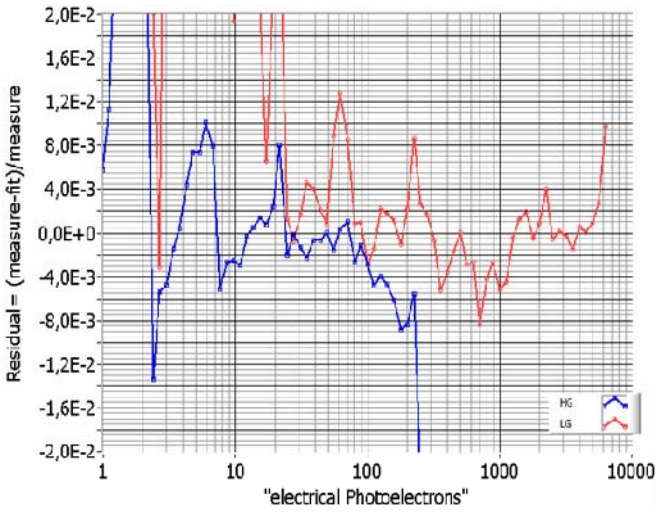

Fig. 8: Non-linearity characteristics for the data plotted on Fig. 7

The curve with blue dots on Fig. 5 is a single shot acquisition at 1 GHz sampling rate of an electrically simulated photomultiplier pulse. Such an acquisition has been repeated 1000 times. As the input pulse and the sampling clock are asynchronous, there is a 1ns peak-to-peak jitter between the start of the input signal and the first sample over the various acquisitions. For each acquisition, the phase between the sampling clock and the signal start has been computed using a

fit. This phase has been used to calculate the real time of the samples. All the samples, with time corrected by this method are plotted with green dots on Fig. 6. This is equivalent to the Equivalent Time Mode used by commercial oscilloscopes for repetitive signals. A maximum value of 40ps rms is derived from the measurement of the width of the resulting trace both on the rising and the trailing edges of the signal.

IV. Conclusions and Perspectives.

The SAM chip fulfils all the requirements of the H.E.S.S.-II front-end electronics. 6000 SAM chips have been manufactured to equip the H.E.S.S.-II telescope. A new chip, based on the SAM architecture but also integrating ADC and FIFO is currently under study for the next generation of Atmospheric Cherenkov Telescopes.

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