Development of Binary Readout CMOS Monolithic Sensors for MIP Tracking

Y. Değerli, A. Besson, G. Claus, M. Combet, A. Dorokhov, W. Dulinski, M. Goffe, A. Himmi, Y. Li, and F. Orsini

***Abstract*–Recently, CMOS Monolithic Active Pixels Sensors (MAPS) have become strong candidates for pixel detectors used in high energy physics experiments. A very good spatial resolution can be obtained with these detectors (lower than 5 microns). A recent fast MAPS chip, designed on AMS CMOS 0.35 µm Opto process and called MIMOSA16 (HiMAPS2), was submitted to foundry in June 2006. The pixel array is addressed row-wise. The chip is a 128 x 32 pixels array where 8 columns have analog test outputs and 24 have their outputs connected to offset compensated discriminator stages. The array is divided in four blocks of pixels with different conversion factors and is controlled by a serially programmable sequencer. Discriminators have a common adjustable threshold. The sequencer operates as a pattern generator which delivers control signals both to the pixels and to the column-level discriminators. This chip is the basis of the final sensor of the EUDET-JRA1 beam telescope which will be installed at DESY in 2009. In this paper, laboratory tests results using a ^{55}Fe source together with beam tests results made at CERN using Minimum Ionizing Particles (MIPs) are presented.**

I. Introduction

ONE of the goals of the EUDET-JRA1 project (Detector R&D towards the International Linear Collider) is to provide a test beam area with a high precision telescope by upgrading an existing facility in Europe at DESY near Hamburg [1]. An optimal determination of the spatial resolution of the device under test is among the most important tasks in this concept. To this end, a high precision beam telescope with up to six measurement planes and one plane for a device under test will be constructed (Fig. 1). Each measurement plane will be equipped with CMOS Monolithic Active Pixel Sensors (MAPS) that allows fully evaluation of the precision properties of new detectors. The telescope can be also operated inside a solenoid magnetic field of up to 1.2 T.

In the past, the first fast MAPS with on-chip signal discrimination designed for charged particle detection, the MIMOSA8 (HiMAPS1) chip, exhibits very encouraging performances [2][3]. Thanks to the double sampling architecture integrated inside each pixel, the temporal and fixed pattern noises of the sensor have been largely reduced. The input referenced temporal noise is only about 10 e^-. The first step towards final on-chip data sparsification has been realized by column level comparators which digitalize analog pixel signals into a 1-bit digital code. The readout speed reaches 13 µs/frame (~75000 frames/s) for analog outputs and 20 µs/frame (50000 frames/s) for digital outputs. With the 5 GeV electron test beam of DESY, performed in 2005, detection efficiency for Minimum Ionizing Particles (MIPs) is above 98% for both analog and digital outputs [3]. Then, a spatial resolution of ~7 µm on binary outputs was measured at CERN with 180 GeV pions, corresponding to Pixel_pitch/$\sqrt{12}$. All these encouraging results demonstrate that the circuit architecture of MIMOSA8 chip is a good candidate for high energy experiments where high speed and good spatial resolution are necessary. However, comparing to the high S/N (Signal-to-Noise ratio) acquired in laboratory tests with a ^{55}Fe source, the S/N of the central pixel is quite small in beam tests (<10). The reason is that the MIMOSA8 chip was realized using TSMC 0.25 µm digital process, where the estimated thickness of epitaxial layer is only about 6.5 µm. The total charge collected with this epitaxial layer is insufficient and it limits the maximum signal value.

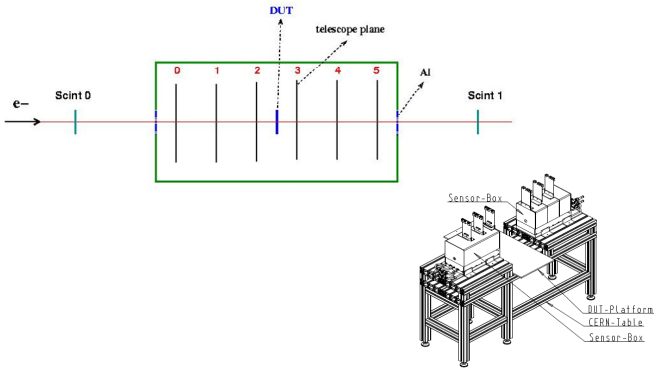

Fig. 1. Sketch of the EUDET-JRA1 beam telescope.

To improve the amount of total charge, a CMOS process with thicker epitaxial layer can be used. As a result, a new prototype, MIMOSA16 (HiMAPS2), using the same architecture as MIMOSA8, but improved pixels was realized in AMS 0.35 µm OPTO process with an epitaxial layer of about 14 µm. Moreover, in order to study the influence of the thickness of epitaxial layer on detection performance, another version of MIMOSA16 has been realized in the same process but with an epitaxial layer of about 20 µm.

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Y. Değerli, M. Combet, Y. Li, and F. Orsini are with CEA Saclay, DAPNIA/SEDI, 91191 Gif-sur-Yvette Cedex, France (e-mail: degerli@dapnia.cea.fr).

A. Besson, G. Claus, A. Dorokhov, W. Dulinski, M. Goffe, and A. Himmi are with IPHC, IN2P3/ULP, 23, rue du Loess BP 28, 67037 Strasbourg, France.

These chips are the basis of the final sensor of the EUDET-JRA1 beam telescope. We notice that the final sensors will have at least 500000 pixels and integrated zero suppression circuits.

II. Architecture of the Chip

As the main purpose of MIMOSA16 is to test and improve the performances of the architecture of MIMOSA8 by using a CMOS process with thicker epitaxial layer, only minimum modifications in the architecture have been made. The global architecture diagram chip is shown in Fig. 2a. The MIMOSA16 chip is an array of 128 rows by 32 columns of which 8 columns have analog test outputs and 24 columns are discriminated binary outputs with a common adjustable threshold. Analog outputs are used to evaluate the performance of different pixels. The pixel size is 25 µm x 25 µm. Three versions of this chip (M16_1, M16_2 and M16_3) are submitted for fabrication. Each chip is divided in sub-arrays with four types of pixels (S1-S4) with different charge collecting diode sizes and amplifier types. Table I summarizes the differences between these three versions of fabricated MIMOSA16 chips[1]. The only difference between M16_1 and M16_2 is the thickness of their epi-layers. The pixels of S3 (M16_1 and M16_2) have been designed with ionizing radiation tolerant design rules in order to study the radiation tolerance.

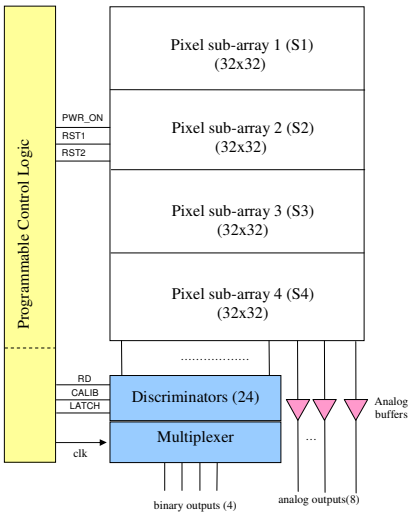
TABLE I
DESCRIPTION OF FABRICATED MIMOSA16 CHIPS

	Epi-layer thickness	Pixel Type			
		S1	S2	S3	S4
M16_1	14 µm	(1.7 µm)² diode *CS* amplifier*	(2.4 µm)² diode *CS amplifier*	(2.4 µm)² rad-tol diode *CS amplifier*	(4.5 µm)² diode *High gain amplifier with FB***
M16_2	20 µm	(1.7 µm)² diode *CS amplifier*	(2.4 µm)² diode *CS amplifier*	(2.4 µm)² rad-tol diode *CS amplifier*	(4.5 µm)² diode *High gain amplifier with FB*
M16_3	14 µm	(3.0 µm)² diode *CS amplifier*	(2.4 µm)² diode *CS amplifier*	(3.5 µm)² diode *CS amplifier*	(4.5 µm)² diode *High gain amplifier with FB and additional SF****

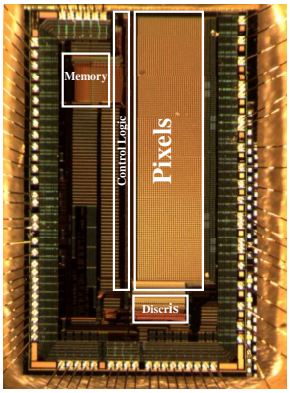
* CS: Common Source
** FB: Feedback
*** SF: Source Follower

The digital part generates and distributes the control signals necessary for the analog part. Thanks to the programmable sequencer, the timing patterns are loaded into the chip during the initial phase of programming. The outputs of 24 columns level discriminators are multiplexed by the serializer block.

[1] M16_1 and M16_2 are fabricated in the same time on an engineering run, while M16_3 is fabricated later on a different MPW run.



(a)



(b)

Fig. 2. (a) Architecture of MIMOSA16 CMOS sensor, (b) microphotography of the chip.

The column level discriminators and the programmable digital sequencer described in [2] are translated in AMS 0.35µm Opto process with only minor modifications. The process used for this chip offering analog options, in the discriminators MOS capacitors are replaced by poly-ploy capacitors for better linearity. The description of these blocs will not be repeated in this paper.

III. Pixels

The success of pixel design strongly depends on the efficiency of noise reduction. While the influence of shot noise is small thanks to high readout speed, the classical 3-T photodiode pixel suffers from the reset noise, temporal readout noise and pixel-to-pixel FPN (Fixed Pattern Noise). All these noises have to be reduced in the pixel in order to perform column level discrimination. To reduce the influence of the temporal readout noise, an amplifier has to be added and be placed very close to the detection diode. Moreover, the FPN results from the offset of the mismatches among the transistors and its reduction is also crucial for on-chip data sparsification.

Each transistor implemented on the analog signal path contributes to the pedestal variations. Considering the small signal level, special care is needed to remove these offsets while maintaining the target readout speed.

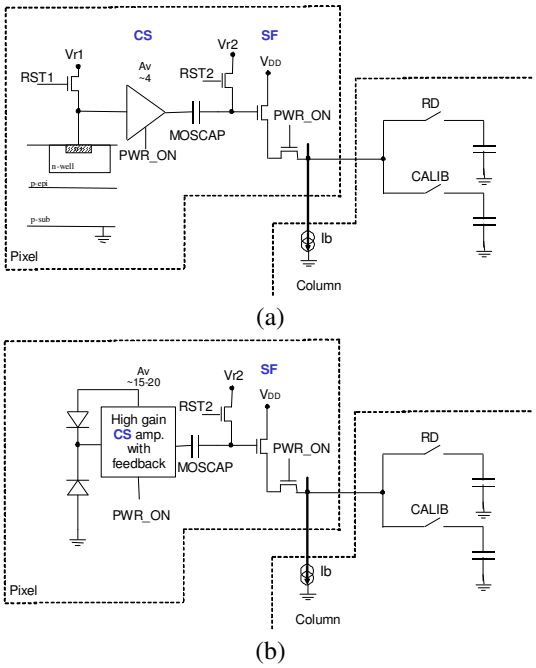


Fig. 3. Schematics of the pixel used in the MIMOSA16 chip, (a) pixel with basic Common Source amplifier, (b) pixel with high gain CS amplifier and feedback.

A. *Pixel with Basic CS Amplifier*

The pixel architecture is shown (Fig. 3a). A CS (Common Source) pre-amplifying stage is placed very close to the charge detection diode. The amplifier is based on a common source NMOS transistor with a diode connected NMOS transistor load, both saturated in strong inversion. The voltage gain is the ratio of the transconductances of these two transistors. The DC current bias of the amplifier is determined by the voltage across the charge collecting diode. A double sampling circuitry is made up of this CS preamplifier, a serially connected capacitor (MOSCAP) and two reset switches. The first switch (RST1) is used to reset the detection diode and the second one (RST2) is used to memorize on the capacitor the offset of the preamplifier and the reset level of the diode. A SF (Source Follower) and a row select switch are used to output the signal on the common data bus. RD and CALIB are column level commands and are used to memorize the output signal level and the reference level of the pixel output stage, respectively. The timing diagram and more details on this pixel can be found in [2][3].

While the damage of non ionising radiation can not be reduced by applying special layout design rules, the ionising radiation damage can be reduced by using enclosed geometry transistors and by using guard-rings. The enclosed geometry transistor thins down the field oxide to reduce the charge created by ionization. The guard-ring cuts the path of surface leakage current induced by positive charge build-up on oxide after irradiation. In MIMOSA 16, diodes with guard-ring structure is used in the pixels of sub-array S3 (M16_1 and M16_2). The size of diodes is the same as the diode size used in sub-array S2.

B. *Pixel with High Gain CS Amplifier and Feedback*

In this pixel, the reset transistor is replaced by a diode. The charge sensitive element is a two diode system, with an n-well/p-epi diode, collecting the charge available after particle impact, and a p-plus/n-well diode, providing a constant reverse bias of the first one.

In order to maximize signal-to-noise ratio of the pixel, the gain of the amplifier should be increased as much as possible. The performances of the basic CS amplifier used in the first pixel can be improved using additional transistors. The AC gain of the modified CS amplifier proposed in [4] is increased by a factor of two, but the DC operation point and DC gain are almost not changed, which makes the circuit more resistant to CMOS variations. In addition to this, negative feedback is used to stabilize the operation of point of the amplifier. More details on the amplifier used in this pixel can be found in [4][5]. This pixel also uses a CDS circuit with a serially connected clamping capacitor, a switch and a SF like the first pixel (Fig. 2b).

In the sub-array S4 of M16_3, to better polarize the MOS capacitor (MOSCAP), an additional SF is introduced between the amplifier and this capacitor. However, this additional SF will decrease the signal by 20% and hence may increase the noise, also one need to add a current source for the source follower, so the circuit becomes more complex.

IV. Laboratory Test Results

In order to determine the basic performances of the chip (temporal noise, FPN, conversion factor and charge collection efficiency), laboratory tests were performed on analog test outputs and discriminated binary outputs, with and without a ^{55}Fe source (5.9 keV peak).

A. *Analog Outputs*

Fig. 4 shows the input referred rms Temporal and Fixed Pattern Noises measured without source on a M16_2 chip as a function of the clock frequency up to 170 MHz. At high operating frequencies, the dominant noise being generated by the electronics and the kTC noise of the charge collecting diode being suppressed, no significant differences have been observed between the output noise levels of S1-S3. For the pixels with basic CS amplifier, the input referred noise is lower for the smallest diode (S1) when referred to the input. The increase of the Temporal Noise at low frequencies is probably due to the increase of low-frequency noise; and the increase of FPN above 100 MHz is due to the increase of time constants required to charge the auto-zeroing capacitors. Note that the chip is optimized to work at f_{CK}=100 MHz. The FPN

remains well below the temporal noise, as it is needed for on-chip data sparsification. The noise results obtained for M16_1 and M16_3, which are very close to the results of M16_2, will not reported in this section[2]. However, the noise levels of the most interesting sub-arrays will be given in the beam tests section together with other measured parameters.

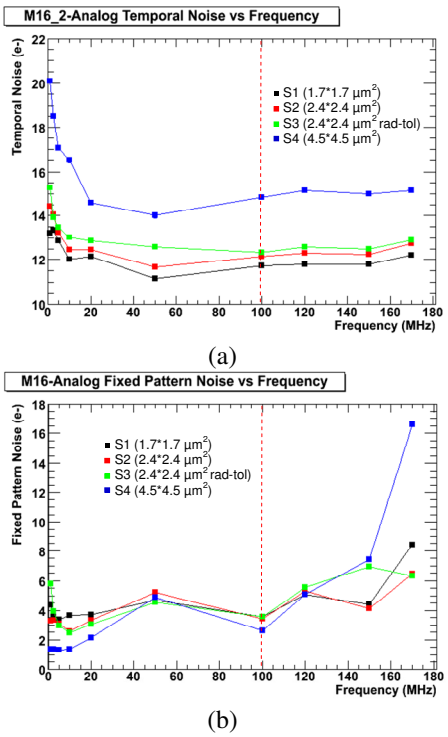


Fig. 4. Measured (a) temporal noise and (b) FPN versus clock frequency for the 4 sub-arrays of M16_2 chip.

Then using a ^{55}Fe source, Calibration Peaks, Cluster Peaks and Charge Collection Efficiencies (CCE) are evaluated. The distribution of hits for only one pixel, obtained at f_{CK}=100 MHz with a significant number of events recorded, is given in Fig. 5 for two sub-arrays of M16_2. The calibration peak of the source is clearly seen (~200 ADC Units for S2 and ~195 ADC Units for S4), but corresponds to relatively rare events, when photons deposit all their energy (5.9 keV) on a single diode or very near. The Charge-to-Voltage conversion Factors (CVFs) obtained for these two sub-arrays are ~61 µV/e$^-$ and ~59 µV/e$^-$ respectively.

In order to study main events of charge deposition, the charge distribution around a central pixel (where the charge is a maximum), was analyzed. Fig. 6 shows the total charge collection peak for clusters of 3x3 pixels for a M16_2 chip.

The ratio of the position of total charge collection peak over the position of calibration peak gives the Charge Collection Efficiency (CCE). The CCEs measured on M16_1 and M16_2 chips as a function of the clock frequency are given in Fig. 7. For the chip M16_2, this parameter is measured up to f_{CK}=170 MHz (~82000 frames/s) and no significant change is observed. CCE varies from 8% for S1 up to 52% for S4 (Fig. 7a); and for M16_1 chips, from 7% for S1 up to 66% for S4 (Fig. 7b).

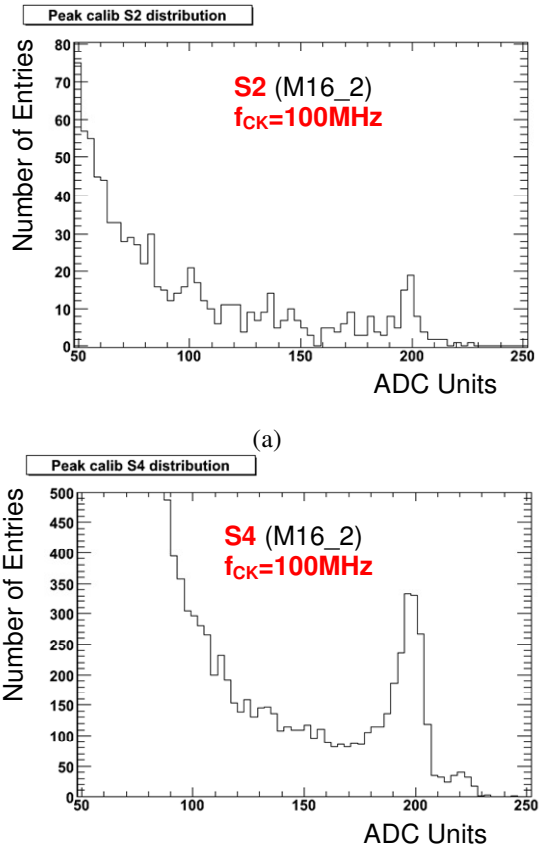


Fig. 5. Calibration distribution (number of hits versus signal magnitude) for one single pixel (no clusters) at a clock frequency of 100 MHz with the ^{55}Fe source, (a) for the S2 sub array (M16_2), and (b) for the S4 sub array (M16_2) (1 ADC Unit = 0.5 mV).

Note that the CCE is higher for M16_1 whose epi-layer thickness is smaller (14 µm). In fact, the epi-layer of this type of sensor being not fully depleted, in spite of more charges generated in the 20 µm epi-layer option (M16_2), more charges are diffused to neighboring pixels and less charge is collected in a cluster of 3x3 pixels, while the position of the calibration peak remains unchanged. So, the CCE of M16_2 is lower for clusters of 3x3 pixels.

From these laboratory measurements, it is clear that the diode sizes of S1-S3 are too small for this process and very little charge is collected. The diode size of S4 was much larger and hence the CCE was sufficient, however, this diode size have to be used with high gain amplifier, which has more complicated design and larger layout size.

To explore the simple amplifier circuit (like in S1-S3), a third chip, M16_3, have been submitted to fabrication with

[2] The lowest input referred temporal noise levels are measured on S1 of M16_1 and M16_2 (~9 e-), and the highest noise level on S3 of M16_3 (~19 e-).

simple amplifier and bigger diode sizes (see Table I). The sub-array S2 of this chip is identical to the S2 of M16_1 to get a reference. Unfortunately a difference in CCEs is observed on this chip with respect to M16_1, probably due to a different unknown doping profile of the wafer. The problem is still under investigation.

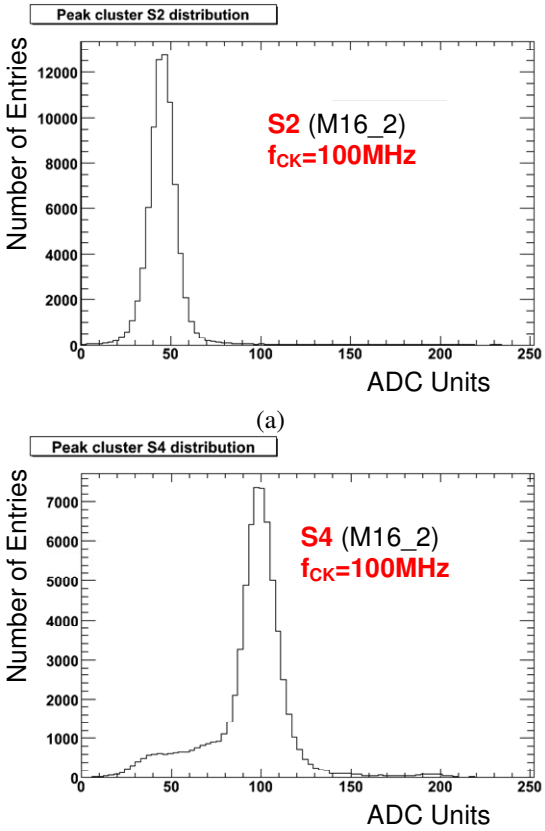


Fig. 6. Charge collection distribution obtained with a ^{55}Fe source after software reconstruction with 3x3 clusters at the clock frequency of 100 MHz (a) for the S2 sub array (M16_2), and (b) for the S4 sub array (M16_2) (1 ADC Unit = 0.5 mV).

B. Binary Outputs

The transfer curves for the global performance are obtained using the data acquisition system. One transfer curve is related to one pixel and the corresponding column-level discriminator. The transfer curves give the noise performance for both pixels and column level discriminators. Limited by the speed of the data acquisition system, the measurements are performed at f_{CK}=40 MHz. The curves are obtained without input signal by varying the external threshold voltage in a certain range. For each pixel, the average of 1000 events is calculated for each threshold value. Fig. 8 shows these normalized curves obtained on the whole pixels of two sub-arrays (S3 of M16_3 and S4 of M16_1). From these curves, one can estimate the mean systematic offset, the temporal noise and the FPN of the analog signal path (pixels & discriminators). Note that the temporal noise is smaller for S4 of M16_1 than the noise for S3 of M16_3.

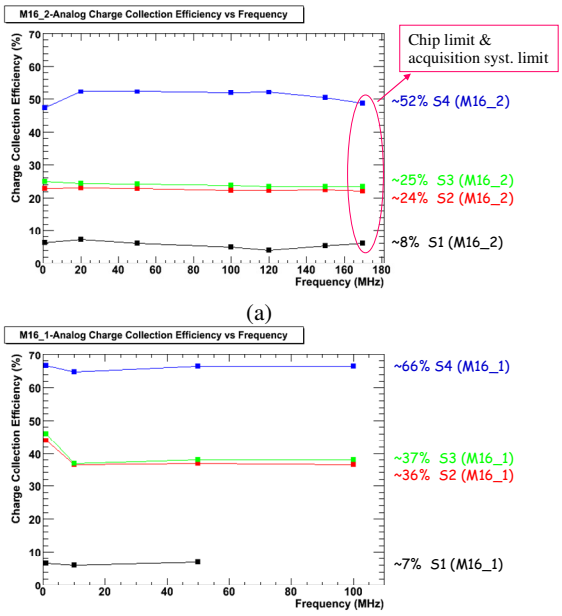


Fig. 7. Percentage of charge collected versus clock frequency for the 4 sub-arrays of (a) M16_2, and (b) M16_1. Clusters of 9 pixels were used.

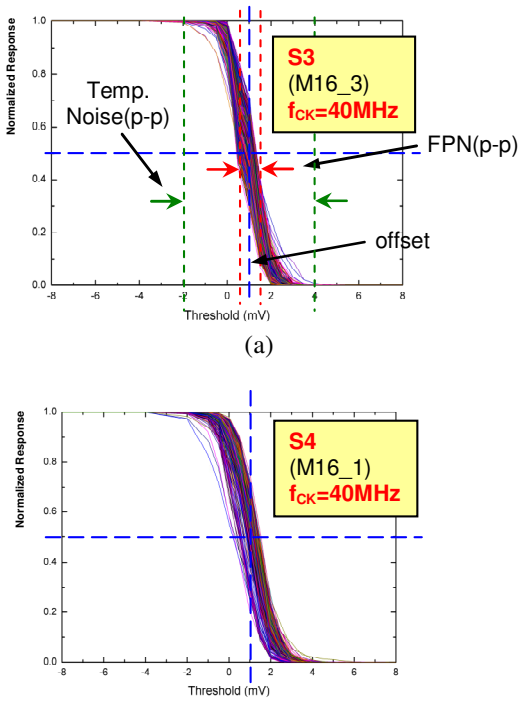


Fig. 8. Normalized number of counts versus discriminator threshold voltage for (a) S3 of M16_3, and (b) S4 of M16_1. The offset and the noise of the pixel & discriminator chain can be derived.

During beam tests, the threshold value applied is very important because it influences the detection efficiency and the fake hit rate (see next section). When there is no input signal, the random responses of a discriminator could be either "1" or "0" and the "1" is obviously caused by noise in this moment. By raising the threshold voltage, the probability of "1" caused

by noise can be reduced but the minimum input signal level will be greater on the contrast, reducing the sensibility of the discriminator. Thus, the detection efficiency will be drawn down. On the other hand, if the threshold value is two small, the unwanted "1" caused by noise increases and leads to an increase of fake hit rate. So that compromise has to be found between the noise performance and the sensibility of the discriminator. A preliminary study of different threshold values as a function of the pixels responses is carried out. As an example, the responses of three sub-arrays (S2, S3, S4) for M16_1 at V_{Th}=6 mV are shown in Fig. 9 with and without source (100 kEvents were recorded). We notice that with this threshold value, very few pixels are activated by noise and more hits are recorded on S4 (S4 having highest CCE).

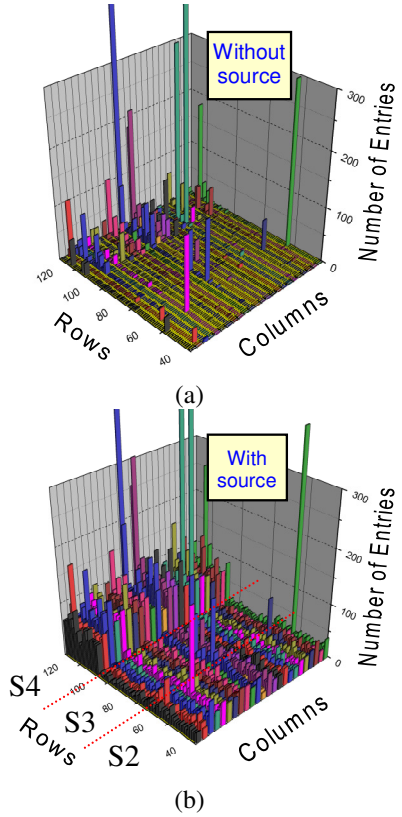


Fig. 9. Histogram (number of hits for each pixel) recorded on M16_1 (S2-S4) (a) Without sources, (b) With source. (f_{CK}=40MHz, Threshold voltage=6 mV). 100 kEvents were recorded in each case.

V. Beam Tests Results with MIPs

The three chips of MIMOSA16 series were tested with a 180 GeV/c positive pions beam in September 2007 at CERN. The set-up used and the types of measurements performed are already described in [3]. The measurements are performed at f_{CK}=40 MHz, due to the limitations of the acquisition system. Only preliminary test results on the analog and digital part will be presented here, as data analysis is still going on. A C++ based analysis software using ROOT interface under LINUX environment is used to analyze the experimental data. This software, called "MAF" (Mimosa Analysis Framework), has been developed by IPHC since 2003. No survey is done to make any preliminary alignment corrections, so the final alignment is made by software using particles tracks. The alignment procedure is a simple minimization algorithm based on the assumption that the particle trajectory is a straight line. After the alignment procedure of the MIMOSA16 chip with the 8 reference planes, the performances of the chip can be calculated offline.

As it is impossible to show all the results for the 12 sub-arrays (3 chips x 4 sub-arrays), only the 2 best sub-arrays (S4 of M16_1 and S3 of M16_3) are illustrated in the continuation.

The first result concerns the noise level: the typical temporal noise obtained in beam test conditions are shown in Fig. 10 for S4 of M16_1 (a) and S3 of M16_3 (b). Noise level is very similar to those obtained in laboratory for the two chosen sub-arrays (15 e^- and 19 e^- respectively).

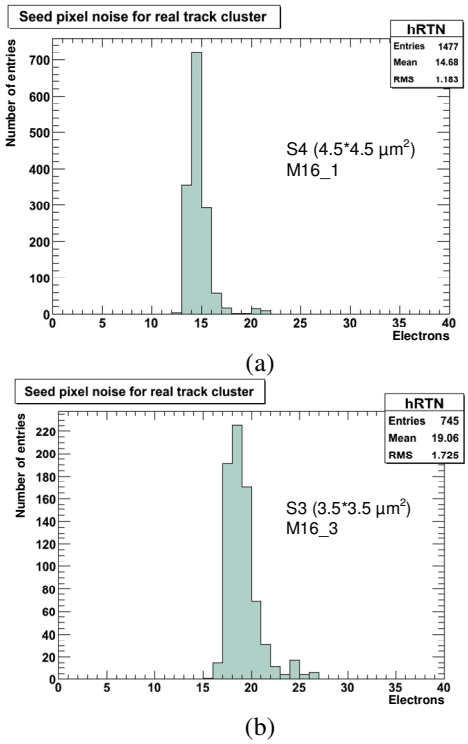


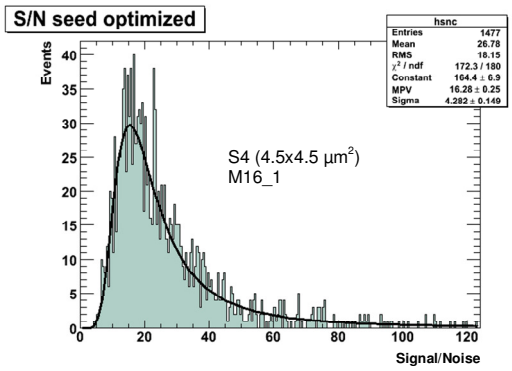
Fig. 10. Temporal noise measured in beam tests conditions for (a) S4 sub-array M16_1, (b) S3 sub-array of M16_3.

For the other M16_1 and M16_2 sub-arrays, the temporal noise is between 12e^- and 15e^-; and for the other M16_3 sub-arrays, between 13e^- and 20e^-. The temporal noise is slightly higher for the sub-arrays of M16_3 chip than the others because the sizes of the diodes chosen for this chip are a bit larger, and this increases the equivalent capacitance of the diode and thus the input referred noise. Anyway, this noise level is still very good.

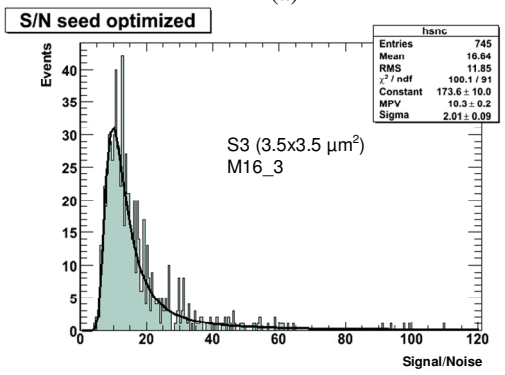
One of the most important parameter for these chips is the S/N ratio, which has to be as great as possible. This parameter has been improved with these new chips, compared to MIMOSA8 results [3]. This is mainly due to the thicker

epitaxial layer in MIMOSA16 and the increased in-pixel amplifier gain. Fig. 11 illustrates this improvement; the Most Probable Value of the S/N ratio is >16 for S4 of M16_1 and > 10 for S3 of M16_3. The results, in terms of S/N ratio, obtained with S4 of M16_1 (14 µm epi-layer) are very encouraging.

One remark concerns the S/N results obtained with M16_2 (20 µm epi-layer): the S/N ratio is equivalent to those obtained with M16_1, in spite of a thicker epi-layer for M16_2. In principle, a thicker epitaxial layer chip should provide a higher signal because the particle is crossing a larger amount of sensitive material. But in the other hand, being a diffusion based sensor, this could also result in a greater spread of the charge in neighboring pixels and in a lower charge collection efficiency because of charge recombination effect. Indeed, we notice a spread of the charge in the neighboring pixels in M16_2. For example, the total charge in a cluster of 3x3 pixels is higher in the case of M16_2 than for M16_1 (~700 e^- for a S4-3x3 cluster of M16_1, and >800 e^- for same S4 cluster size of M16_2), but keeping always the same charge inside the seed pixel (this is not illustrated here with figures), which proves that increasing the epi-layer thickness in this process is not necessarily a good solution. But increase of in-pixel amplifier gain is probably the best solution with this process to improve the S/N ratio.



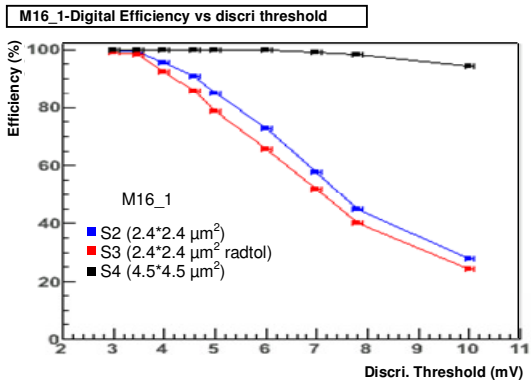
(a)



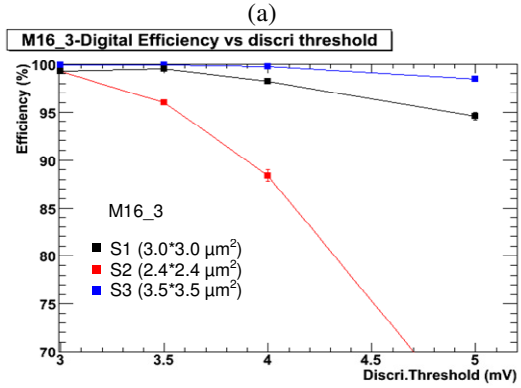
(b)

Fig. 11. Seed pixel S/N ratio distribution obtained on analog test outputs with MIPs at a clock frequency of 40 MHz: (a) S4 sub-array M16_1, (b) S3 sub-array of M16_3.

Another important parameter is the detection efficiency to MIPs, which is > 99.9%, with a fake hit rate ~2.10^{-4} for a discriminator threshold of +4 mV. This efficiency decreases only a little bit to 99.88% with a fake hit rate of ~10^{-5} (S4 of M16_1) and ~10^{-4} (S3 of M16_3) for a discriminator threshold of +6 mV (Fig. 12 and Fig. 13). This result proves that we are able to provide a chip with a very good MIP detection efficiency on a large range of discriminator threshold.



(a)



(b)

Fig. 12. Binary outputs detection efficiency as a function of the external threshold voltage of discriminators: (a) M16_1, (b) M16_3.

The hit multiplicity per pixel is also an important parameter for the digital part. To give an order of magnitude for S4 of M16_1, we found only ~2% of clusters with one pixel and ~10% of clusters with one pixel for a discriminator threshold of +4mV and +6mV respectively. Working at high discriminator thresholds, without degrading the detection efficiency is recommended.

Finally, the spatial resolution, without multiple scattering, is studied as a function of the discriminator threshold (illustration of the results on Fig. 14). In spite of a pixel pitch of 25 µm, the single point resolution obtained is < 5 µm for S4 of M16_1 and < 6 µm for S3 of M16_3 for a discriminator threshold of 5-6 mV. This value is well below the binary resolution reflecting the 25 µm pitch (7.2 µm). This result can probably be explained by the important charge collected in the pixels with this process and thus the barycenter of the CoG method is known with better precision.

Table II summarizes the most important parameters measured at CERN for the best two sub-arrays for a discriminator threshold value of +6 mV.

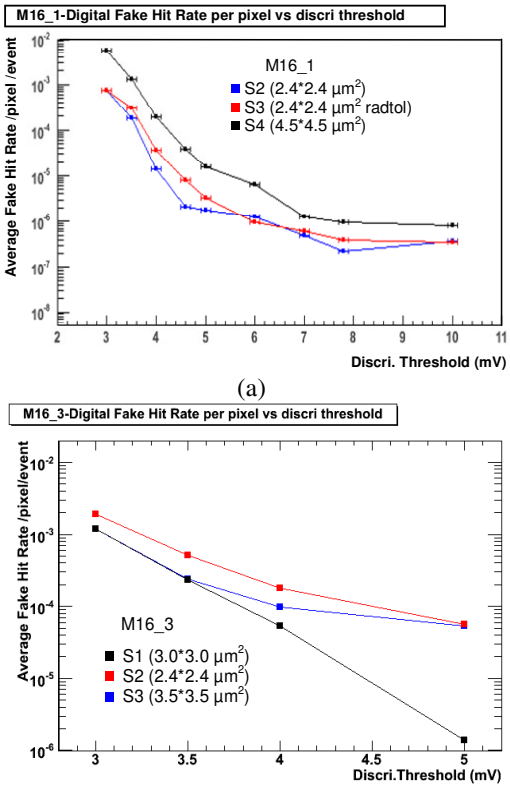


Fig. 13. Digital fake rate as a function of the external threshold voltage of discriminators: (a) M16_1, (b) M16_3.

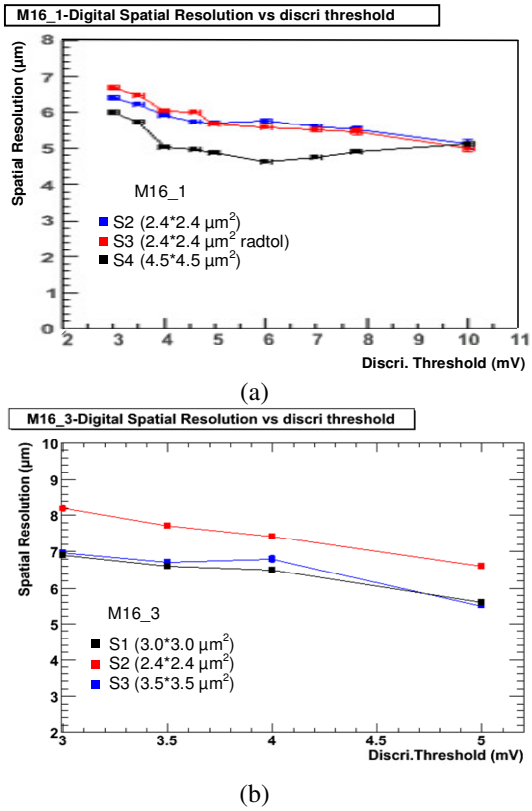


Fig. 14. Binary outputs spatial resolution as a function of the external threshold voltage of discriminators: (a) M16_1, (b) M16_3.

TABLE II
SUMMARY OF THE PERFORMANCES WITH MIPS FOR 2 SUB-ARRAYS

Sub-Array *(Discri. Threshold=4mV)*	S/N Ratio (MIPs)	Detection Efficiency to MIPs	Spatial Resolution (digital)	Fake Hit rate
S4 (M16_1)	> 16	99.96±0.03%	≤ 4.8 µm	2×10^{-4}
S3 (M16_3)	> 10	99.71±0.05%	≤ 6 µm	1.8×10^{-4}

VI. CONCLUSIONS

A higher detection efficiency and better spatial resolution than MIMOSA8 are obtained with this sensor with a discriminator threshold of ~ 4-6 mV. The columns architecture works very well and on-chip digital-to-analog coupling is well controlled. With these results, we checked that at least one pixel sub-array fully satisfies EUDET-JRA1 Beam Telescope requirements. Best results are obtained with sub-array S4 of M16_1 and S3 of M16_3 which have been realized on substrates with 14 µm epi-layer. In the case of 20 µm epi-layer option (M16_2), the charges diffuse more laterally on neighboring pixels (well beyond the seed pixel) and then the spatial resolution is slightly degraded.

Another very important conclusion of the work on this chip is that the increase of in-pixel amplifier gain improves S/N ratio and consequently the spatial resolution. In the near future, other chips will be designed developing this point. In the process AMS CMOS 0.35 µm Opto, diodes sizes bigger than $(3.5\mu m)^2$ have to be used to get a reasonable CCE.

For the third prototype with 14 µm epi-layer thickness, M16_3, a difference in charge collection efficiencies is observed in laboratory (with respect to M16_1); the problem is still under investigation.

Following the very encouraging results of MIMOSA16, a larger chip (MIMOSA22) with an active surface of ~25 mm^2 (576 x 128 pixels), smaller pitch (18.4 µm), with more optimized pixels, JTAG, and more testability is submitted to foundry at end of October 2007. This chip (IDC: Intermediate Digital Chip) is the last prototype before the final sensors of EUDET-JRA1.

REFERENCES

[1] T. Haas, "A pixel telescope for detector R&D for an international linear collider", *Nucl. Instrum. Meth. A*, vol. 569, no. 1, Dec. 2006, pp. 53-56.

[2] Y. Degerli *et al.*, "A fast monolithic active pixel sensor with pixel level reset noise suppression and binary outputs for charged particle detection", *IEEE Tran. Nucl. Sci.*, vol. 52, no. 6, Dec. 2005, pp. 3186-3193.

[3] Y. Degerli *et al.*, "Performance of a fast binary readout CMOS active pixel sensor chip designed for charged particle detection", *IEEE Tran. Nucl. Sci.*, vol. 53, no. 6, Dec. 2006, pp. 3949-3955.

[4] A. Dorokhov *et al.*, "NMOS-based high gain amplifier for MAPS", Talk given at *5th Int. Meeting on Front-End Electronics (FEE)*, 17-20 May 2006, Perugia, Italy.

[5] A. Dorokhov *et al.*, "Optimization of amplifiers for monolithic active pixel sensors", presented at *Topical Workshop on Electronics for Particle Physics (TWEPP)*, 3-7 Sept. 2007, Prague, Czech Republic.