AFTER, an ASIC for the Readout of the Large T2K Time Projection Chambers.

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***Abstract*— The T2K (Tokai-to-Kamioka) experiment is a long baseline neutrino oscillation experiment in Japan, for which a near detector complex (ND280), used to characterized the beam, will be built 280m from the target in the off-axis direction of the neutrino beam produced using the 50 GeV proton synchrotron of J-PARC (Japan Proton Accelerator Research Complex). The central part of the ND280 is a detector including 3 large Time Projection Chambers based on Micromegas gas amplification technology with anodes pixilated into about 125,000 pads and requiring therefore compact and low power readout electronics. A 72-channel front-end Application Specific Integrated Circuit has been developed to read these TPCs. Each channel includes a low noise charge preamplifier, a pole zero compensation stage, a second order Sallen-Key low pass filter and a 511-cell Switched Capacitor Array. This electronics offers a large flexibility in sampling frequency (50 MHz max.), shaping time (16 values from 100ns & 2µs), gain (4 gains from 120 fC to 600 fC), while taking advantage of the relatively low physics events rate of 0.3 Hz. Fabricated in 0.35 µm CMOS technology, the prototype has been validated and meets all the requirements for the experiment so that mass production will be launched at the end of 2007.**

***Index Terms*— Mixed analog-digital integrated circuits, Front-end electronics, CMOS.**

I. Introduction

The T2K (Tokai-to-Kamioka) experiment [1] is dedicated to the study of neutrino oscillations. An intense neutrino beam from the J-PARC (Japan Proton Accelerator Research Complex) facility in Tokai will be sent 295 km across Japan towards the Super Kamiokande detector in Kamioka in order to study how neutrinos change from one type to another. The ND280 detector complex, located at 280 m from the neutrino production target, will measure properties of the neutrino beams at the J-PARC site before the neutrinos have had a chance to oscillate into other flavors. This near detector complex consists of finely segmented detectors acting as neutrino targets and tracking detectors surrounded by a magnet to measure the neutrino beam energy spectrum, flux, flavor contents, and interaction cross-sections before the neutrino oscillation. One of the major parts of this detector is the tracker constituted by 3 Time Projection Chambers (TPC). These TPCs will measure the momenta of muons produced by charged current interactions in the detector, and it will be used to reconstruct the neutrino energy spectrum. The outer dimensions of each TPC (Fig. 1) are roughly 2.5 m x 2.5 m in the plane perpendicular to the neutrino beam direction, and 1 m along the beam direction.

Each TPC is read at each of its extremity by micro pattern readout endplates using the bulk Micromegas technology [2]. This Micromegas detector is made of a segmented Printed Board Circuit (PCB), used as the anode, on top of which a stainless steel micromesh is integrated using photolithography techniques. Each TPC end-plate is made of 12 Micromegas

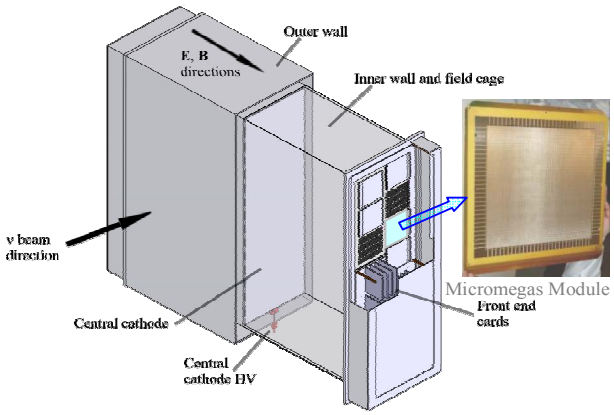

Fig. 1: global view of a TPC and of a 36 cm x 34 cm Micromegas readout module.

modules of 36x34 cm^2. The readout anode of each module is pixilated in 1728 pads of 6.9 mm x 9.7 mm. The readout of the total 125,000 pads of the 3 TPCs implied therefore the design of novel compact readout electronics. As it fits in the area enclosed by the magnet, these front-end electronics have to be compact and have low power consumption.

II. Outline of the TPC Electronics

The goal of the TPC detectors is to perform 3D tracking of charged particles and to measure their energy loss. For this purpose, the electronics will measure the charge collected by each pad. A centroïd calculation will permit to determine X and Y coordinates for each point of the track, whereas the Z coordinate will be given by the drift time of electrons to the endplate of the TPC. To measure these parameters, for each particle spill (every 3.5 s), each pad signal will be recorded over duration slightly larger than the maximum TPC drift time (few tens of microseconds). The overall electronics architecture has been optimized to handle and concentrate the

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resulting highly bursted data flow and to minimize cabling coming out from the detectors, taking benefit of the very low event rate (0.3 Hz in standard condition and up to 20 Hz for cosmic ray calibration). For this purpose, the electronics is based on an architecture derived from those developed for the former STAR TPC [3], but more compact and with better noise and power consumption performances, thanks to the use of modern technologies. The on-detector electronics, located inside the magnet, is based on a modular electronics unit, depicted in Fig. 2, reading one whole Micromegas module. This unit, connected directly to the anodes, is composed of 6 Front-End Cards (FECs) and one Front-End Mezzanine (FEM) card.

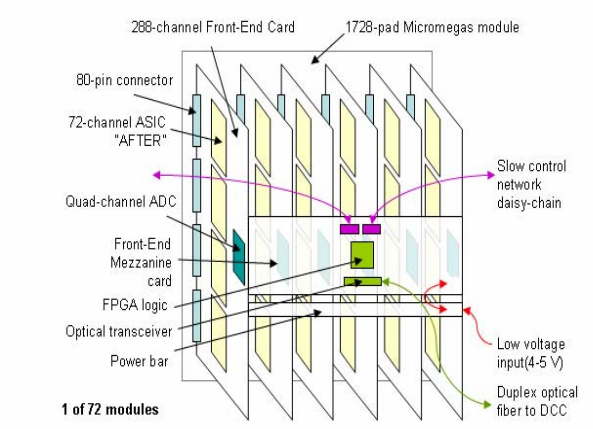

Fig. 2. TPC module readout electronics.

Each 288-channel FEC includes mainly input protection networks, 4 custom-made 72-channel "AFTER" front-end chip (ASIC For TPC Electronic Readout) and a commercial 12-bit quad-channel ADC. The ASIC collects and filters the detector signals and samples them continuously in an analog memory, based on a Switched Capacitor Array (SCA) until a trigger arrives. Then the analog data from all the channels of the chip is read back and multiplexed towards one of the four channel of the external ADC achieving thus a first 72-to-1 data concentration.

The FEM is a pure digital electronics card that controls up to 6 FECs, gathers event digitized by the FECs, performs optionally pedestal subtraction and zero suppression, and sends data outside the detector through a full-duplex gigabit optical link. Outside the detector, 6 Data Concentrator Cards (DCC) aggregate the data of the TPC endplates and send event fragments to a merger computer that performs a final data reduction and communicates with the experiment DAQ system via a standard network connection.

III. The AFTER ASIC

This section describes the architecture of the chip which has been optimized to match the main specifications and requirements reported in table I. The required dynamic range is 10 bits. The chip gain can be selected among 4 values to adapt the measurement range to the maximum charge delivered by the detector. This charge is ten times the charge delivered by the detector for a Minimum Ionizing Particle (MIP) that will depend on the detector parameters like gas mixture, voltage applied.

TABLE 1: MAIN REQUIREMENTS AND SPECIFICATIONS

Parameter	Value
Number of channels	72
Samples per channel	511
Dynamic Range	2 V / 10 MIPs on 12 bits
MIP charge	12 fC to 60 fC
MIP/Noise ratio	100
Gain	Adjustable (4 values)
"Detector" capacitor range	20 pF -30 pF
Peaking Time	100 ns to 2 µs (16 values)
INL	1% 0-3 MIPs; 5% 3-10MIPs
Sampling frequency	1 MHz to 50 MHz
Readout frequency	20 MHz to 25 MHz
Polarity of detector signal	Negative(T2K) or Positive
Test	1 among 72 channels or all

A. Architecture of the AFTER Chip

The AFTER chip (Fig. 3) is the central component of the FEC board. This chip, defined before the final choice of the detector, is very versatile, in order to accommodate various kinds of detectors and gas mixtures. It can even deal with both signal polarities depending on the choice of few external components. It performs a first concentration of the data from 72 inputs to only one analog output connected to an external ADC.

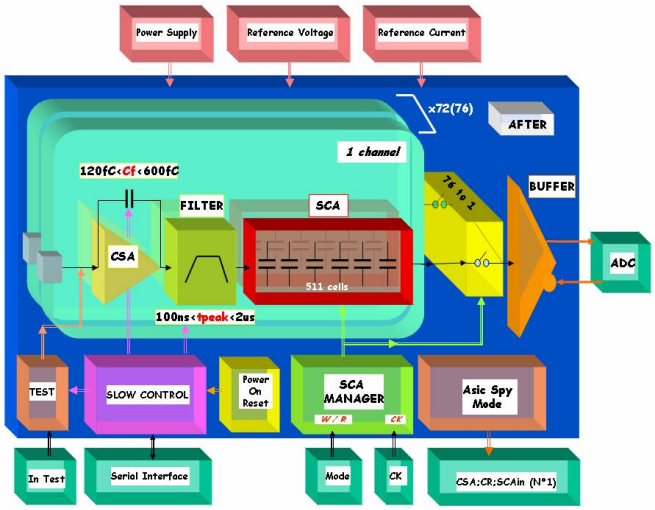

Fig. 3. Architecture of the AFTER chip.

Each channel comprises a front-end part dedicated to the charge collection and the shaping of the detector signal and a SCA that samples and stores the analog signal. Several parameters (gain, peaking time, test modes and chip control) are configured by slow control, using a custom serial 4-wire link. Two inputs are provided for calibration and the functional test of the 72 channels.

B. Architecture of the Front-End Part of the Channel

The front-end part (depicted on Fig. 4) is composed of: a

Charge Sensitive Amplifier (CSA), a Pole-Zero Cancellation (PZC) block, a $(R.C)^2$ filter and a Gain-2 amplifier. The CSA is based on single-ended folded cascode architecture [4]. It has been optimized for detector capacitances in the 20 pF - 30 pF range. The input transistor is a NMOS device (2000 µm / 0.35 µm) with a tunable current. The full charge range (120 fC, 240 fC, 360 fC or 600 fC) is defined by selecting the CSA feedback capacitor value (200 fF, 400 fF, 600 fF or 1 pF). The DC feedback of the CSA is achieved by an attenuating current conveyor [5] which is also used to realize the resistor setting the zero of the PZC stage.

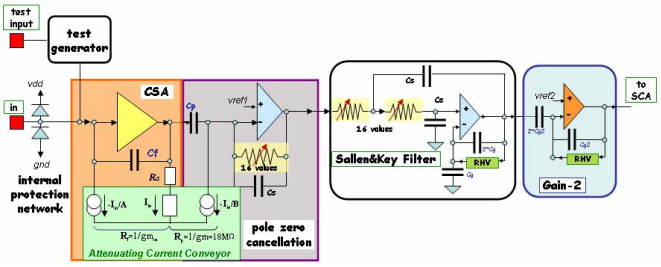

Fig. 4. Architecture of the front-end part of the channel

The PZC stage is used to cancel the long duration undershoots at the shaped output. It introduces a zero to cancel the low frequency pole of the CSA and replaces it by a higher frequency pole.

Associated with the PZC pole, the 2-complex pole Sallen-Key low-pass filter provides a semi-Gaussian shaping of the analog signal. The peaking time at the shaper output can be set among 16 values (from 100 ns to 2 µs) by using various combinations of resistors in the feedback network.

A last amplifier adjusts the voltage dynamic range of the chain (Gain of 2) to drive the analog memory.

C. *The Switched Capacitor Array*

The analog memory is based on a SCA structure using 4-switches memory cells similar to those described in [6]. It includes 72 effective channels plus 4 dummy channels (Gain-2 stage + SCA) which can be used for common mode or fix pattern noise rejection. Each SCA channel operates as a 511 cell circular analog buffer in which the signal coming out from each analog channel is continuously sampled and stored at a F_{wck} sampling rate (up to 50 MHz). Depending on the gas drift velocity, this frequency can be adjusted in order to cover the maximum TPC drift time with the 511 samples.

The sampling is stopped by the FEM when it receives an external trigger signal. Then, the 511 analog samples of each channel are sequentially read back and multiplexed at 20 MHz towards the output of the chip. This reading operation (Fig. 5) is performed cell by cell, starting from the oldest sample. For each cell, after 3 readout clock periods, required for analog data stabilization, the corresponding stored data of all the 76 channels are successively multiplexed towards the external ADC. At the end of the readout phase, the digital address of the last column read is converted into a series of analog samples. This address can be analyzed offline for control purpose. The readout of the full memory takes 2 ms, but it is possible to read only partially the 511-cell depth of the SCA.

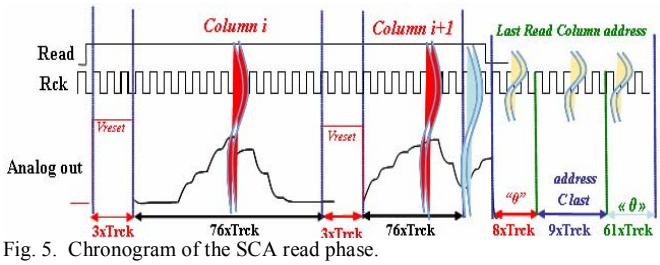

Fig. 5. Chronogram of the SCA read phase.

An on-chip fully-differential buffer drives one of the 4 inputs of the external ADC (Analog Devices AD9229). This buffer is designed to settle to 0.1% within 25ns. The input and output common mode voltages are adjusted with external passive components (same values for all chips).

D. *Chip Manufacturing, Layout and packaging.*

The AFTER chip has been fabricated in a 0.35 µm CMOS AMS process. The chip integrates 400,000 transistors, and as shown on Fig. 6, its area (7.8 mm × 7.4 mm) is mainly dominated by the SCA. The channel input pads are located on the right and left sides of the chip by group of 36 in order to make the chip assembling easier in a standard 160-pin LQFP plastic package. The main digital blocks, including the SCA manager, the clocks buffering and the slow-control interface are located in the bottom part of the chip.

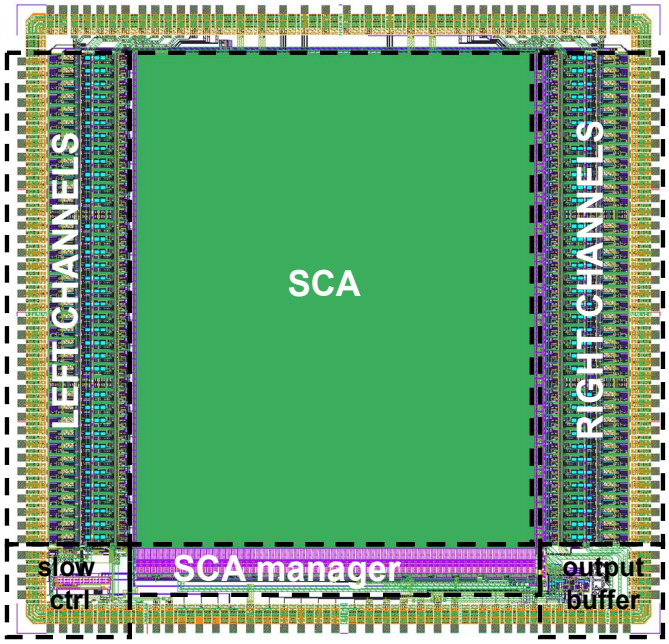

Fig. 6. AFTER chip layout.

IV. Test Results

More than a hundred chips have been characterized using test boards permitting also to validate the final FEC and FEM architectures. As in its final use in the experiment, the 12-bit ADC range was set to 2 V so that its LSB value was corresponding to 0.49 mV.

All the chip functionalities and its various modes of operation have been fully validated. The measured chip power consumption ranges from 6.2 mW to 7.5 mW per channel, depending on the bias current of the CSA (400 µA or 800 µA).

A. Signal Shape and Baseline Spread.

Fig. 7 shows the response of the AFTER chip to mid-range pulses injected through the test input for 4 different shaping times, and recorded using a 50 MHz sampling frequency. The 1.5% undershoot was expected from simulation because of the 2 complex poles of the Sallen-Key filter. The timing parameters of the pulses measured for various peaking times, reported in Table II, are consistent with the simulation results. In this table, T_{peak} is the signal rise time measured from 5% of the full amplitude to the peak, T_{fall} is the signal fall time measured from the peak to 5% and T_{FWHM} is the signal width measured at 50% of the signal amplitude.

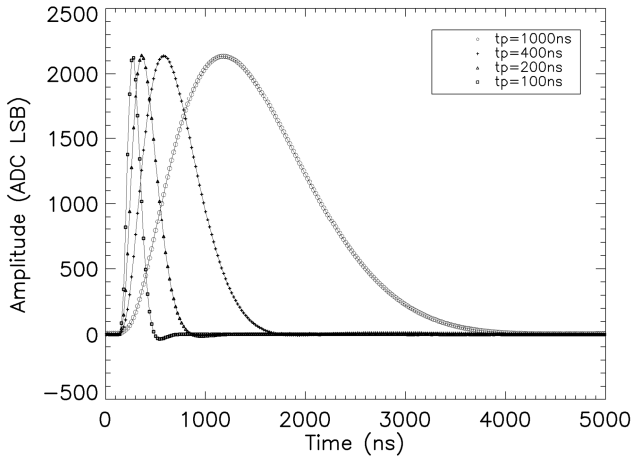

Fig. 7. 60 fC test pulses recorded by AFTER (120 fC range).

TABLE II: MEASURED TIMING PARAMETERS OF THE SHAPED PULSES

Shaping time (ns)	**T_{peak} (5%-100%) (ns)**	**T_{fall} (100%-5%) (ns)**	**T_{FWHM} (ns)**
100	111	182	150
200	185	552	287
400	387	823	631
1000	893	2118	1529
2000	1776	4037	2953

Inside a chip, the channel-to-channel baseline spread is within 160 to 300 LSBs peak-to-peak. The spread of the baselines over 50 chips is 360 LSBs peak-to-peak. These values are in good agreement with Monte-Carlo simulation results showing that this spread is dominated by the contribution the SCA readout part. Individual analog baseline adjustment is not required and the mean baseline will be set to 200 LSBs. This corresponds to a loss of the dynamic range of less than 10%.

B. Transfer Function and Linearity.

The chip has been characterized using pulses generated by a 14-bit DAC housed on the test board and injected to the chip calibration input through a calibrated external capacitance. The transfer functions of the chip have been extracted from characteristics as the one plotted on Fig. 8 which was obtained for a 100 ns peaking time and the 120 fC range. These transfer functions are very close to the simulated ones. They are summarized in Table III, for the four charge ranges available and for a shaping time of 100 ns that is the most sensitive one. Their spread measured over 122 chips is less than 2% rms. The CSA open loop gain, calculated from the measured transfer function versus input capacitance characteristic, is 3000. This is smaller than the 3700 simulated value, but not totally surprising as the simulated MOS transistor output impedance is generally overestimated.

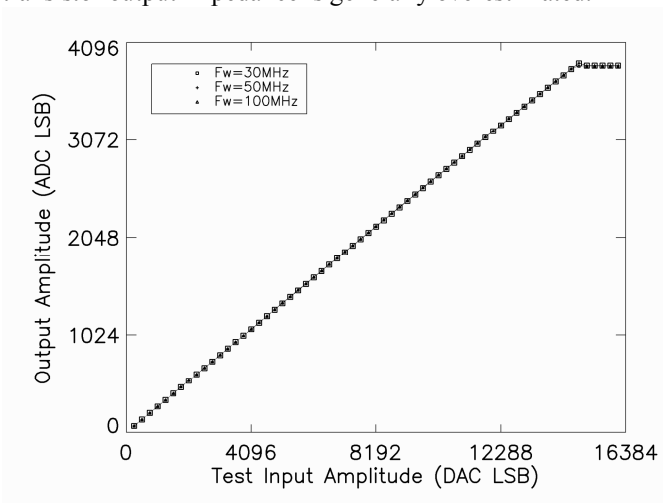

Fig. 8. Output amplitude versus test pulse amplitude measured for three SCA write frequencies (120fC range, 100ns peaking time).

TABLE III: AFTER TRANSFER FUNCTION (100NS SHAPING TIME)

Range (fC)	**Simulated value (mV / fC)**	**Measured value (mV / fC)**	**spread over 120 chips (% rms)**
120	18.5	18	1.7%
240	9.9	9.7	1.25%
360	6.6	6.67	1.15%
600	4.05	4.1	1.1%

The chip Integral Non-Linearity (INL), is calculated from the measured transfer function as the ratio of the residues to a linear fit of this data divided by the data, is smaller than 1.2% over the full chip dynamic range for the 120 fC range and 100 ns peaking time (Fig. 9), which is the least favorable configuration. For a 2 µs peaking time, the INL is improved to less than 0.5%. These values are much lower than the 5% specification.

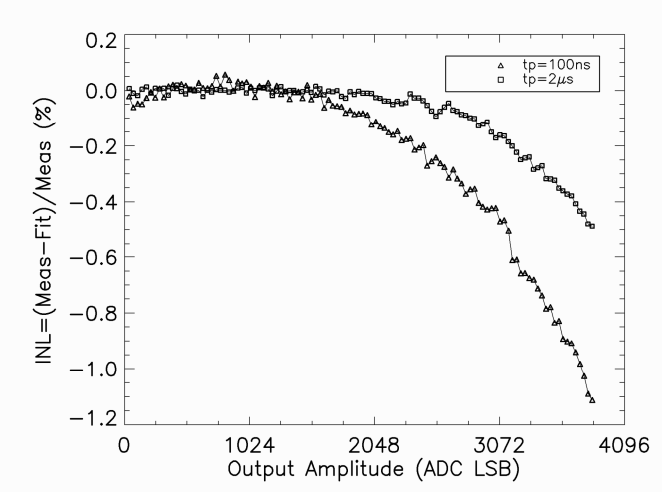

Fig. 9. Integral Non Linearity versus output amplitude for 100 ns and 2 µs peaking times (120 fC range)

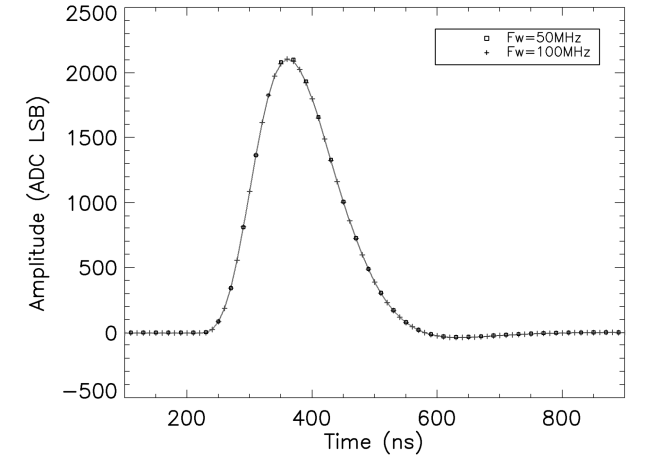

Fig. 10. Same single shot test pulse sampled at 50 MHz and 100 MHz (100 ns peaking time).

Although the chip has been designed for a 50 MHz maximum SCA sampling frequency, it has also been characterized at higher frequencies. As shown on Fig.10, pulses sampled at 50 MHz and 100 MHz can be perfectly superimposed. The chip transfer functions (Fig. 8) and the non-linearity curves (Fig. 11), measured at 30 MHz, 50 MHz and 100 MHz, are exactly the same. This shows the large speed margin of operation of the chip.

C. Chip Noise.

The chip Equivalent Noise Charge (ENC) has been measured for the various available peaking times and different input capacitors. The ENC can be theoretically expressed as the quadratic sum [4]:

$$ENC^2 = \frac{\alpha^2(I_{csa})\cdot(C_0+C_{in})^2}{t_p} + \gamma^2\cdot(C_0+C_{in})^2 + \beta^2 . t_p + D^2 \quad (1)$$

Where α stands for the series noise contribution (depending on the input transistor bias current), C_0 is the intrinsic input capacitor of the preamplifier, C_{in} is the added capacitor at the preamplifier input, t_p is the peaking time of the shaped signal, γ stands for the 1/f noise contribution, β stands for the parallel noise contribution and D is the second stage noise contribution.

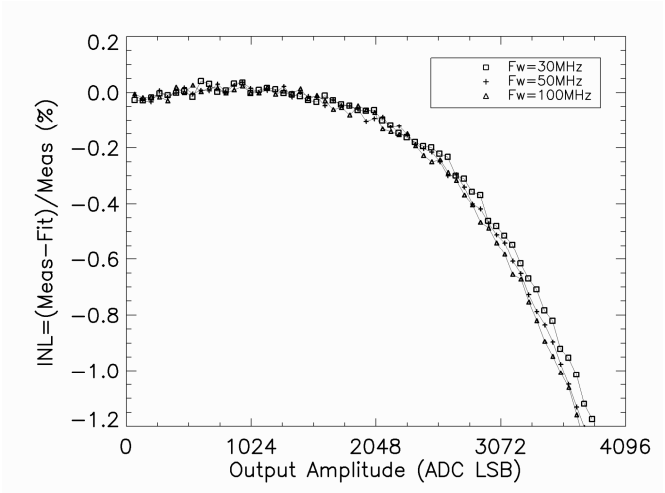

Fig. 11. Integral Non Linearity versus output amplitude for 100ns peaking time, 120fC range measured for three sampling clock frequencies.

The parameters of this expression have been extracted by fitting the measured data for the four charge ranges of the chip, and for two CSA bias currents. Both the ENC measured values and the fitted curves, which are perfectly matching the measurements, are shown on Fig. 12 for the 120 fC range. The extracted noise parameters are summarized in Table IV.

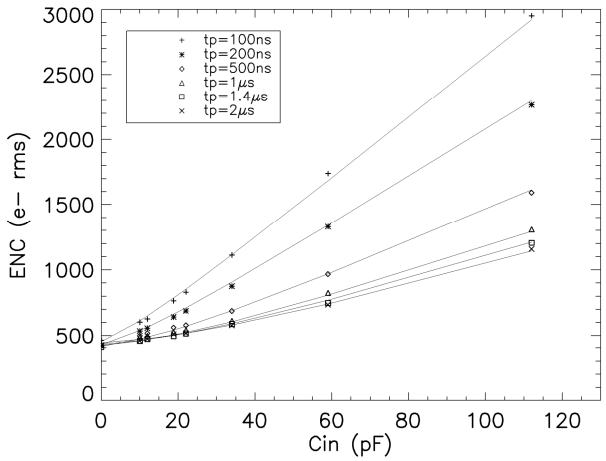

Fig. 12. ENC versus input capacitance for different peaking times (120fC range, I_{CSA}=800µA). The symbols are corresponding to measurements; the lines are corresponding to fit results.

As expected, the parallel noise is negligible and the second stage noise value scales with the charge range. This latest appears to be shared equally between SCA and shaper contributions. The 10 pF intrinsic input capacitor C_0 value is 3 pF larger than the simulated one. This extra capacitor is compatible with those added by the plastic package. The serie noise contribution is 10% larger than in simulation and is independent of the range. For 800 µA bias current, it corresponds to a 1.1 $nV/Hz^{1/2}$ CSA input transistor thermal white noise density. As expected, the 1/f noise is nearly independent on the current and on the charge range. However, its value is 80% higher than expected. Fortunately, this unexplained excess noise has nearly no impact for the T2K

experiment application for which the shaping time will be in the range of 200 ns to 400 ns.

TABLE IV: EXTRACTED NOISE PARAMETERS (QUADRATIC EXPRESSION)

Parameter	120 fC	240 fC	360 fC	600 fC	Unit
α(400 µA)	246	250	253	254	$e\text{-}.ns^{1/2}.pF^{-1}$
α(800 µA)	197	198	198	194	$e\text{-}.ns^{1/2}.pF^{-1}$
γ(400 µA)	*6.6*	*6.6*	*6.9*	*8*	$e\text{-}.pF^{-1}$
γ(800 µA)	6.66	6.9	7.5	8.6	$e\text{-}.pF^{-1}$
β	0	0	0	0	$e\text{-}.ns^{-1/2}.pF^{-1}$
C_0	10	10	10	10	*pF*
D	385	730	1070	1760	*e-*

For users's convenience, it is usual to approximate linearly the ENC versus C_{in} characteristic. Linear parameterizations, valid only for input capacitances in the 15 pF - 40 pF range, are given in Table V for the four charge ranges and various peaking times, in the case of a 800 µA CSA bias current.

TABLE V: EXTRACTED NOISE PARAMETERS (LINEAR APPROXIMATION)

		100 ns	200 ns	500 ns	2 µs	Unit
120 fC	*Offset*	350	370	415	404	*e-*
	Slope	22.2	14.6	7.8	5.3	*e-/pF*
240 fC	*Offset*	690	700	775	750	*e-*
	Slope	13	8.5	4.5	3.1	*e-/pF*
360 fC	*Offset*	1015	1050	1135	1092	*e-*
	Slope	10.7	5.6	3	2.8	*e-/pF*
600 fC	*Offset*	1700	1740	1817	1780	*e-*
	Slope	6.5	3.2	3.3	1.8	*e-/pF*

D. *Crosstalk inside the Chip.*

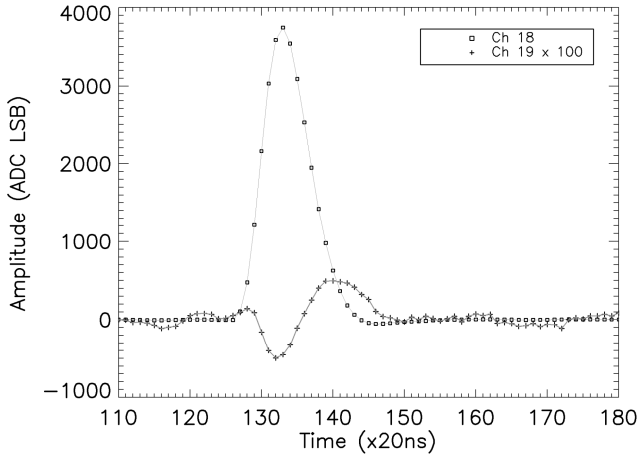

Fig. 13. Full dynamic range test input signal pulsed on channel 18 and crosstalk signal recorded on the neighbour channel 19, magnified by 100. (120 fC range, 100 ns peaking time).

Crosstalk between channels in a TPC must be minimized as it deteriorates both the charge and position resolutions. To measure it, a large amplitude test signal is injected in a single channel whereas the others are recorded. As shown on Fig. 13 the crosstalk signals are differentiated. For the 120 fC range and 100 ns peaking time, the crosstalk magnitude, plotted on Fig. 14, is smaller than +/- 0.4% and at first order inversely proportional to the distance of the pulsed channel. The Crosstalk measured for other peaking times and ranges are similar. This crosstalk is intrinsic to the chip and does not take into account couplings at the detector level.

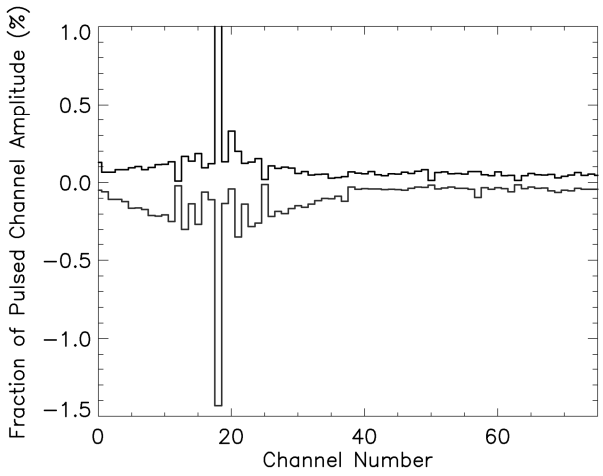

Fig. 14. Relative amplitudes (negative and positive) measured on all the channels of a chip referred to the amplitude of the pulsed (18) channel (100 ns peaking time, 120 fC range).

E. *Effect of Leakage Current.*

As the readout of the SCA takes 2 ms, the analog data stored in capacitors can be corrupted by leakage currents. The leakage effect has been characterized by varying the time between the write and read operations. As the effect of leakage current for a 2 ms storage time was to small to be measured accurately, measurements have been performed for a 35 ms storage time. The values obtained for 35 ms have been divided by 17.5 to extrapolate the effect corresponding to a 2 ms storage time.

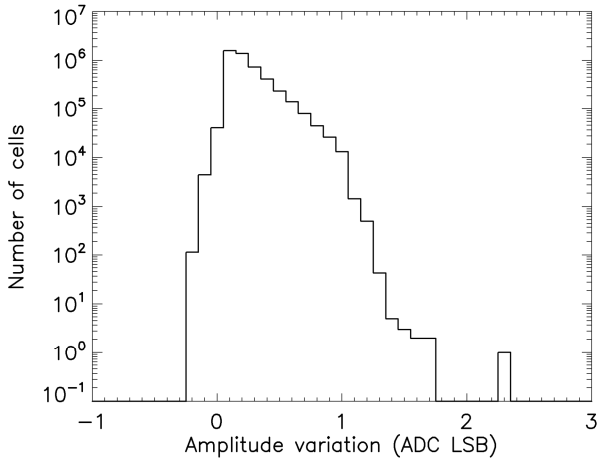

Fig. 15. Distribution of the voltage droop on storage cells after a 2 ms storage time.

The voltage droop distribution measured over all the cells of 122 chips is plotted on Fig. 15. It is very asymmetric, with a mean value of 0.19 LSBs. Nearly all the cells (99.95%) are exhibiting less than 1 LSB droop (corresponding to a 55fA current) and the maximum measured droop is 2.2 ADC LSB. For a worst case cell with 1 LSB droop, read randomly within a 2 ms interval, the readout voltage spread will be 0.29 LSB

rms which is totally negligible compared to the 2.5 LSB rms second stage noise. The leakage current will be measured anyway during production tests so that chips with droop larger than 1 LSB within 2 ms will be rejected.

V. Measurements on the Chip in its Final Environment

A. Noise measurements of the chip mounted on the FEC.

On the FEC, each AFTER chip is associated to a connector and each signal input is ac-coupled to the anode and protected against detector sparks by the network depicted on Fig.16. The PhotoMOS, common to a group of 144 channels (2 AFTER chips) permits to disconnect this group of channel in case of short circuit in the detector. As shown on Fig. 17, the routing capacitance and all these extra-elements are increasing the noise.

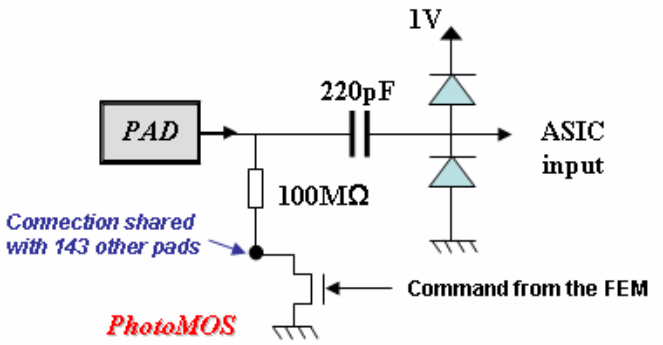

Fig. 16. AC-coupling to the detector and external protection network against sparks.

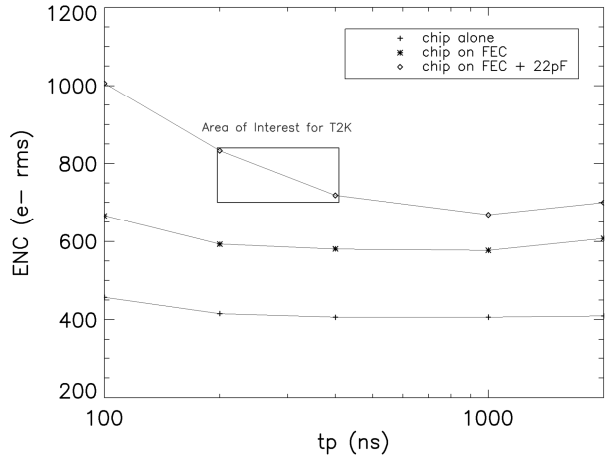

Fig. 17. Comparison of the ENC versus peaking time characteristic for the chip alone, mounted on the FEC and with extra 22 pF to simulate the detector (120 fC range, CSA bias current= 800 µA).

An ENC measurement performed with extra 22pF capacitors, simulating the detector, connected to the each FEC input is reported in the same figure. In the worst case, for a peaking time of 100 ns, the ENC is 1000 e- rms and is reduced to 850 e- rms in the 200 ns - 400 ns range, planned for the T2K operation.

B. Noise Measurements with detectors.

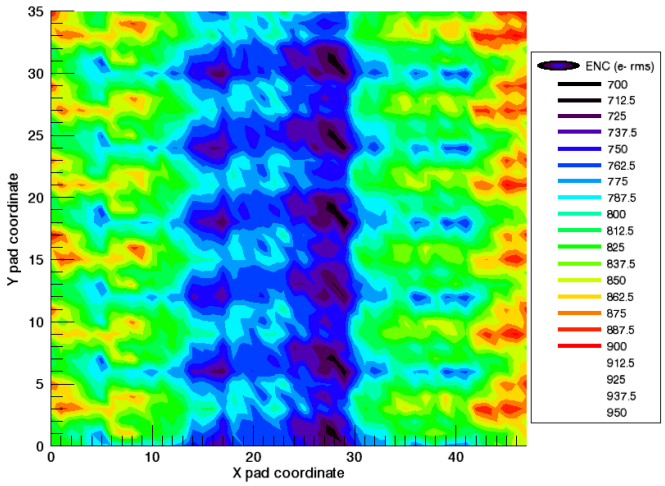

Fig. 18. ENC map measured with a Micromegas detector. (100 ns peaking time, 120 fC range, 800µA CSA bias current).

FECs have been mounted on a prototype Micromegas endplate. Fig. 18 shows a map of the ENC in the detector measured in the 120 fC range for the worst case 100 ns peaking time. The mean ENC over the detector is 810 e- rms with a spread of +/- 100 e- rms. The noise spread between channels, which presents a very regular pattern is mainly due to differences in routing on the detector from the pad to the connector, and therefore in parasitic capacitances. The detector capacitance value has been evaluated from these noise measurements. Its mean value is 12 pF with a minimum of 7 pF and a maximum of 17 pF, quite smaller than our estimations. Under these conditions the chip dynamic range is close to 10 bits.

C. Measurements with particles.

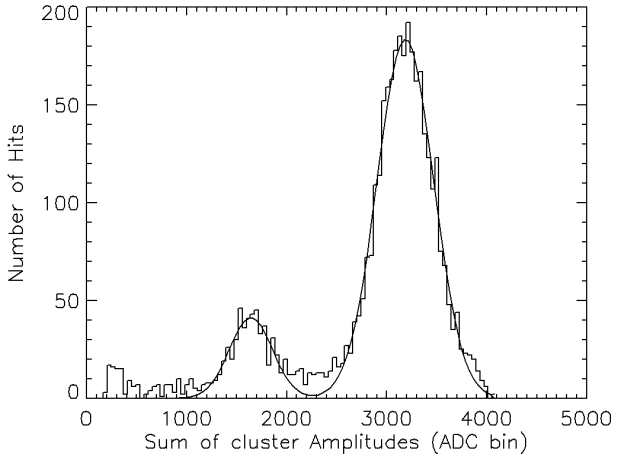

Fig. 19. ^{55}Fe Spectrum acquired with AFTER (200 ns peaking time, 120 fC range, 20 MHz sampling frequency).

A Micromegas detector, read by AFTER chips, has been used to detect photons of a ^{55}Fe source. During data taking, noise levels were very stable and similar to those obtained in the electronics laboratory. The spectrum (Fig 19) exhibits a very good 8.5% resolution for the 5.9 keV line, limited by the detector itself. Because of ac coupling between the detector

and the electronics, a crosstalk corresponding to the ratio of the interpad capacitance over the ac-coupling capacitance is expected in addition to the intrinsic crosstalk in the AFTER chip reported in section IV.D. This has been evaluated using the data obtained with the ^{55}Fe source. First, the events hitting only a given pad were selected. The charges measured on two neighbour pads surrounding the hit pad are reported as a function of the charge of the central pad in Fig. 20. This graph shows a very good correlation between the measured charges giving the evidence of a 1.2% crosstalk effect. This is consistent with a 2.5 pF parasitic capacitor between neighbour detector channels. This crosstalk magnitude is depending from pad to pad but 1.2%, which is an acceptable value for T2K, is the maximum measured value. The charge distribution measured on a neighbour pad is plotted on Fig. 21 shows a clear image source spectrum measured on the main pad (with charge scaled down by a factor 80) and with a quite good resolution (12% rms). As the crosstalk signal charge is roughly 1 fC, it corresponds to 750 e- rms and give an evidence of the low noise level.

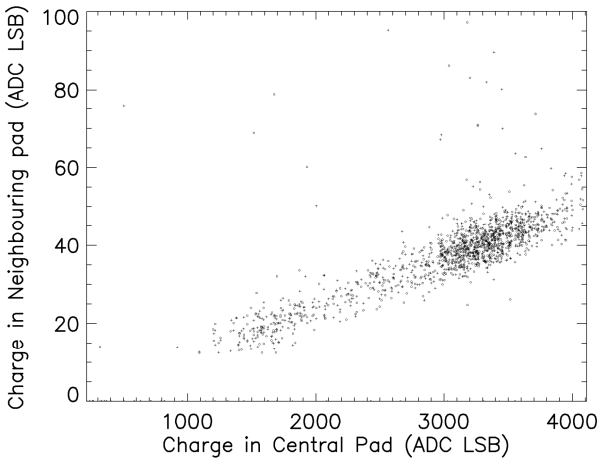

Fig. 20. Correlation graph between charges measured on two neighbour pads and charge on the main pad.

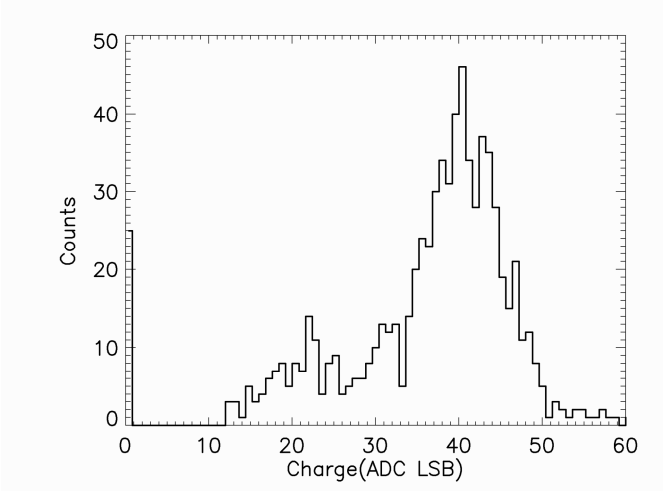

Fig. 21. Charge distribution measured for a neighbour pad.

A Micromegas endplate detector, fully instrumented with AFTER electronics (including 6 FECs and one FEM), has also been tested in September 2007 with cosmic rays in the former HARP [7] field cage at CERN. The detector and its very compact electronics have operated continuously during two weeks very stably. Noise levels were similar to those measured in-lab. These tests and the associated results are discussed in [8].

VI. Conclusion

AFTER, a low noise front-end ASIC has been designed to read the endplate detector of the TPC of the T2K experiment. This very versatile circuit has been extensively tested and characterized. It fulfils the T2K experiment requirements and exhibits a noise of 800 e- rms for a 100 ns peaking time when connected to the detector and for a power consumption of less than 8 mW/channel. 4000 AFTER chips will be manufactured for the T2K experiment before the end of 2007. Its low cost and its large number of tuneable parameters make it useable for other experiments with low rates or for detector testing.

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