Intermediate Digital Chip Sensor for the EUDET-JRA1 High Resolution Beam Telescope

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Abstract– **A high resolution beam telescope, based on CMOS Monolithic Active Pixels Sensors (MAPS), is being developed within the EUDET collaboration, a coordinated detector R&D program for a future international linear collider. A very good spatial resolution < 5 µm, a fast readout time of 100 µs for whole array and a high granularity can be obtained with this technology. A recent fast MAPS chip, designed on AMS CMOS 0.35 µm Opto process and called MIMOSA22, was submitted to foundry in October 2007. MIMOSA22 has an active area of 26.5 mm^2 with a pixel pitch of 18.4 µm arranged in an array of 576 rows by 136 columns where 8 columns have analog test outputs and 128 have their outputs connected to offset compensated discriminator stages. The pixel array is divided in seventeen blocks of pixels, with different amplification gain, diode size, pixel architecture and is addressed row-wise through a serially programmable (JTAG) sequencer. The sequencer operates as a pattern generator which delivers control signals both to the pixels and to the column-level discriminators. Discriminators have a common adjustable threshold, with internal DAC, controlled by the JTAG. MIMOSA22 is the last chip (IDC-Intermediate Digital Chip), before the final sensor of the EUDET-JRA1 beam telescope, which will be installed at the 6 GeV electron beam line at DESY in spring 2009. In this paper, laboratory tests results on analog and digital parts are presented. For this purpose, a ^{55}Fe source is used for calibration of pixels. Test beam results, obtained with a 120 GeV pions beam at CERN in summer 2008, are also presented. In the last part of the paper, a new chip MIMOSA22-bis, with radiation tolerant pixel architectures (evolution of MIMOSA22) will be discussed.**

I. Introduction

Under the EUDET-JRA1 (European detector R&D towards the International Linear Collider) project is developed a high resolution beam telescope based on Monolithic Active Pixel Sensors (MAPS) [1]. This telescope will be composed of up to 6 sensor planes and may be placed in a magnetic field up to 1.2T. Main requirement for the telescope is to reach a spatial resolution of < 5 µm in binary readout mode. Such a performance has already been obtained for the sensor with the test chip MIMOSA16 [2]. This paper describes the next generation sensor MIMOSA22, the Intermediate Digital Chip of the project and the last one before the final EUDET sensor, called MIMOSA26. MIMOSA22 specific goals are the validation of fast readout architecture developed in MIMOSA16 at real large scale, the extraction of an optimal pixel design, and an improvement of the chip testability (JTAG, bias DAC, output pads, etc…).

II. Evolution from MIMOSA16 to MIMOSA22

MIMOSA16 was produced in 2007, in AMS 0.35 µm Opto process with epitaxial layer of 14 µm, a pixel pitch of 25 µm and on-chip signal discrimination, designed for charged particle detection. This chip exhibited very encouraging performances [2]. With its double sampling architecture integrated inside each pixel, the input referenced temporal noise was only between 12 and 15 electrons. The column level comparators, which digitalize analog pixel signals into a 1-bit digital code, had a readout speed of 160 ns per row [2]. Previous beam test results with the 120 GeV pions beam at CERN, performed in 2007, showed detection efficiency for Minimum Ionizing Particles (MIPs) above 99.9%, with a fake hit rate ~2.10^{-4} for a discriminator threshold of +4 mV [2]. In spite of a pixel pitch of 25 µm, the spatial resolution obtained was about 5 µm for at least one of the sub array and for a discriminator threshold of 4-5 mV.

The promising experimental results of MIMOSA16 have confirmed the choice of the technology for the final detector (i.e pixel architecture and process). Thus an improved design, MIMOSA22, was realized with the main goal to keep the performance proven with the test chips within a large active area, surrounded by the embedded electronics needed for the interface with the EUDET Telescope. In addition, MIMOSA16 exhibits signal to noise ratio (S/N) of the seed pixel about 16 for the best sub-array and less than 10 for the others due to too small diode size and too low in-pixel amplification. The new chip MIMOSA22 tries to eliminate this weakness by improving the pixel architecture. Finally, MIMOSA22 is the last prototype before the full size sensor. As a result, the schematic and the layout have been especially designed to be stretchable to the final sensor size.

III. MIMOSA22 Architecture

MIMOSA22 is based on an array of pixels covering 26.5 mm^2 commanded through a row-wise sequencer and

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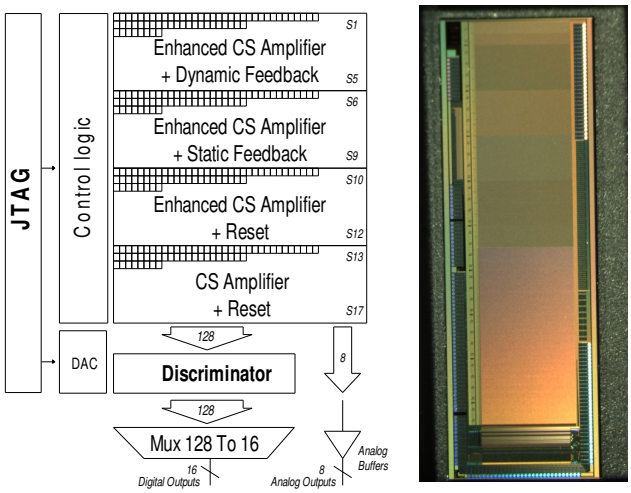
surrounded by embedded electronics for slow control and data processing (see Fig. 1). The array is composed of 576x136 pixels divided in seventeen sub-arrays – including test structures and reference pixels - with different amplification gains, diode sizes and pixel architectures as summed up in the Table 1. The pitch of the pixel was reduced compared to MIMOSA16 from 25 µm to 18.4 µm. The digital commands sent to pixels are synchronous with the 100 MHz nominal clock frequency and lead to a readout of the full array in less than 100 µs. For test purpose, 8 columns - out of 136 - are connected to analog outputs whereas the 128 others are on-chip digitized with column discriminators. At the end of the read-out chain, the digitized data are multiplexed on 16 outputs.



(a) (b)

Fig. 1. (a) MIMOSA22 CMOS sensor architecture. (b) Microphotograph of the chip.

TABLE 1 : CHARACTERISTIC OF THE SEVENTEEN SUB-ARRAYS (INCLUDING TEST AND REFERENCE PIXELS).

	Diode area	Architectures	Diode Biasing Circuit: Reset	Diode Biasing Circuit: Static Feedback	Diode Biasing Circuit: TVFB
Main array	15.2 µm²	standard	CS, ECS		CS, ECS
		RadTol	CS, ECS		CS, ECS
	14.6 µm²	standard		ECS	ECS
		RadTol		ECS	ECS
Reference pixels & Test structures	11.6 µm²	standard			ECS
	12.3 µm²	standard	CS		
	15.2 µm²	standard	CS		
	19.4 µm²	standard		ECS	
	20.4 µm²	standard			ECS

RadTol : Diode with Poly-Si ring to remove the surrounding thick oxyde
CS : Common Source Amplifier
ECS : Enhanced Common Source Amplifier
TVFB: Time Variant Feed-Back

In order to be fully compatible with the beam telescope requirements MIMOSA22 includes on-chip 15 digital to analog converters (DAC) for current and voltage references and a standard JTAG slow control interface.

A. Analog to Digital Channel

The readout scheme of charges deposed in epitaxial layer follows the architecture firstly proposed in [3], [4] and validated on the AMS 0.35µm CMOS Opto process by M16 [2]. The voltage induces by the charges collected through a Nwell/p-epi diode is amplified in each pixel by a first amplification stage, decoupled from the column driver by a double sampling (DS) circuit based on a clamping capacitor (see on Fig. 2).

Row by row, the pixels are connected to end column discriminators which assume the function of analog to digital conversion. A second DS stage (correlated in this case), seated in the discriminator circuit, removes the pixel to pixel offsets introduced by the second amplifier stage and lets the use of a common threshold for all the discriminators. The M16 test results have shown that the double "DS" strategy reduces the Fixed Pattern Noise (FPN) of the whole array into a 1 mV standard deviation which is compatible with the dynamic range of the discriminators.

The complete digital sequence is done in 16 clock cycles. The fast readout is guarantied by the rolling shutter activation scheme and a double selection switches: pixels are grouped into sub-sections of 16 rows in order to reduce the column capacitance added by the individual contribution of pixel's switch.

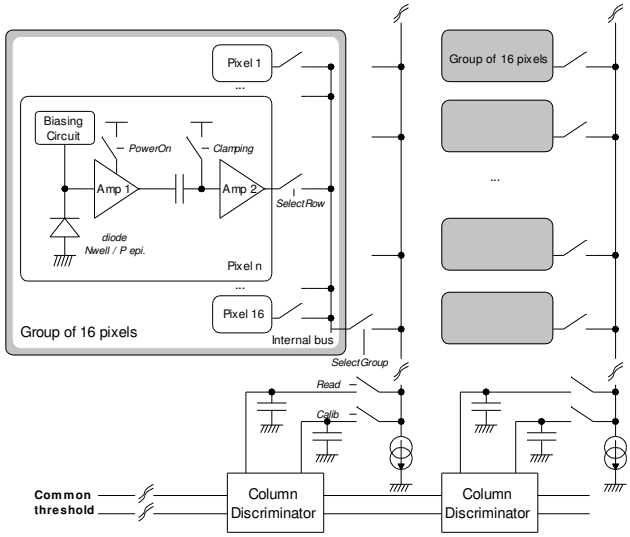


Fig. 2. Double "DS" and group strategy for fast readout and end column discriminator common threshold

B. Pixels Sensing and Amplification Scheme

Correct digitization is dependant of S/N ratio inside pixel which is itself strongly dependant of the front stage i.e. diode size, biasing scheme and amplifier gain.

The main difficulty in pixel amplifier design is the exclusive use of NMOS type transistors due to parasitic collecting diode

introduced by Nwell box of PMOS type transistors and the small size of the pixel. Four main biasing and amplification circuit are tested in MIMOSA22 (see Fig. 3). The first amplifier scheme is based on a common source amplifier and a reset circuit for sub-array S15 to S17, it is one of the reference designs from MIMOSA16. The second schematic uses the same biasing circuit but increases the gain of the amplifier thanks to an enhanced common source described in [5], [6] (sub-array S10 to S14). The third pixel architecture keeps the enhanced common source but removes the dependency of an external reference voltage by connecting the reset voltage to an internal node: during the reset phase, the amplifier is in a "gain one" feedback configuration (sub-array S1 to S5). This is the Time Variant Feed-Back (TVFB) architecture [5]. The last pixel architecture is based on an enhanced common source amplifier and a so call "self-bias" (SB) circuit done through a p-diff /n-well diode connected in a continuous feedback configuration (second reference design from MIMOSA16, sub-array S6 to S9).

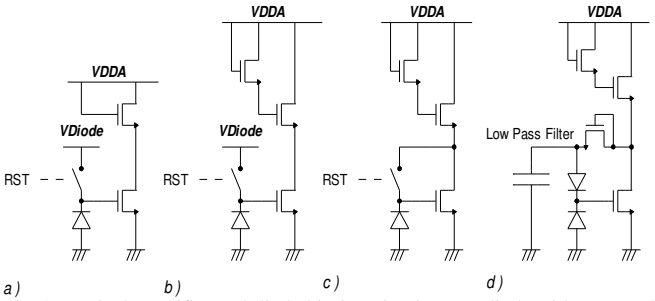


Fig. 3. In pixel amplifier and diode biasing circuitry: (a) diode with reset and common source amplifier, (b) diode with reset and enhanced common source, (c) diode with TVFB and enhanced common source, (d) diode with static feedback and enhanced common source.

IV. Laboratory Tests Results

Basic performances of the chip as the input referred Temporal Noise (TN), Fixed Pattern Noise (FPN), Charge Conversion Factor (CVF) and Charge Collection Efficiency (CCE) for analog and digital outputs are obtained in laboratory by using a ^{55}Fe source, which delivers a 5.9 keV photons peak. All laboratory tests are performed at the nominal frequency of 100 MHz, which means a readout time of 92.5 µs per frame.

A. Analog Outputs Characterization

The pixel noise observed in the best performing sub-arrays ranged typically from 10 to 14 e^-. The noise values obtained with these pixels of the two main architecture types (self-biased feedback diode and reset diode with standard common source amplifier) are summarized in Table 2, for a cooling temperature of 15°C, translating in a temperature of 20°C at the chip surface. The comparison between many and different measurements involves a measurement accuracy on TN of typically ± 0.3 e^-. In fact, at high frequency (100 MHz), the dominant noise is generated by the electronics only, whereas the kTC noise of the charge collection diode is suppressed by DS (Double Sampling).

We notice that the pixels with TVFB (S1-S5, S11 and S14) don't work well for the moment, due to a bad polarization of the in-pixel amplifiers after reset.

The most significant noise variations are due to the capacitance of the sensing diode (S8, with a diode size of 19.36 µm^2, is noisier than S9, with a diode size of 11.56 µm^2), and also from the (non-)radiation tolerant design (S7 versus S6 and S12 versus S10). In particular, the comparison between the TN values of S6 and S7 shows that the radiation tolerant design increases the noise of the self-biased pixels by about 1 e^- ENC. This is due to the polySi ring added around the sensing diode which increases slightly the total capacitance.

Overall, the noise performance of several pixel designs is very satisfactory. Self-biased pixels (S6-S9) and reset pixels (S10-S17) exhibit nearly the same TN value.

TABLE 2 : LABORATORY TESTS RESULTS FOR ANALOG OUTPUTS

Sub-array	*Diode Surface (µm²)*	*Temporal Noise (e^-)*	*CCE (3x3 pixels)*	*CCE (5x5 pixels)*	*CVF (µV/e^-)*	*Diode biasing type*	*RadTol diode*
S6	*14.62*	*12.4*	*74%*	*87%*	*53.1*	*SB*	*yes*
S7	*14.62*	*11.2*	*74%*	*88%*	*57.0*	*SB*	*no*
S8	*19.36*	*12.6*	*79%*	*90%*	*54.3*	*SB*	*no*
S9	*11.56*	*10.7*	*70%*	*85%*	*59.5*	*SB*	*no*
S10	*15.21*	*12.7*	*74%*	*87%*	*54.9*	*RST*	*yes*
S12	*15.19*	*12.0*	*75%*	*88%*	*56.6*	*RST*	*no*
S13	*15.21*	*13.5*	*72%*	*84%*	*51.8*	*RST*	*yes*
S15	*15.19*	*12.5*	*73%*	*85%*	*53.3*	*RST*	*no*
S16	*15.19*	*13.4*	*76%*	*89%*	*43.1*	*RST*	*no*
S17	*12.50*	*12.4*	*71%*	*86%*	*46.1*	*RST*	*no*

SB: Self-Bias; RST: Reset

Using the ^{55}Fe source, calibration and cluster peaks are studied in order to calculated CVF and CCE values. Calibration peak corresponds to relatively rare events, when photons deposit all their energy (5.9 keV, corresponding to 1640 e^-) on a single pixel (called seed pixel). CVF is then deduced from the calibration peak position (Fig. 4). The CVF obtained varies between 40 and 60 µV/e^-, according to the size of the diode and to the gain of the pre-amplifier.

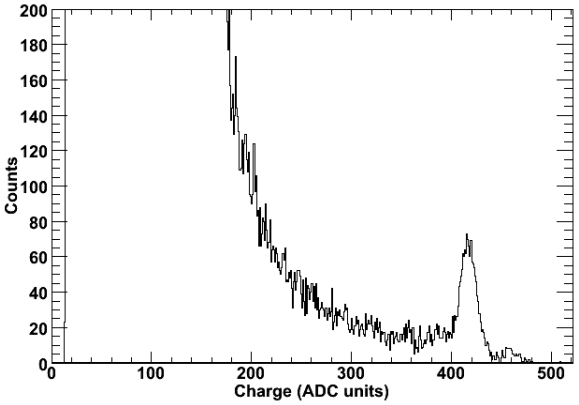


Fig. 4. Signal distribution for the seed pixel of sub-array S12 (number of hits versus signal amplitude) at 100 MHz clock frequency, obtained by calibration with a ^{55}Fe source (1 ADC Unit = 0.22 mV).

The CCE is extracted from the ratio between the charge collection peak position in a cluster of 3x3 or 5x5 pixels (Fig. 5) and the calibration peak position. CCE values are almost 75% for a 3x3 cluster and 88% for a 5x5 cluster (see all results on Table 2), and differ only little for a cluster 5x5 by an amount of 5% from one pixel architecture to another one. The CCE are estimated with a typical uncertainty of ± 0.5 %. In addition, we check that CCE is almost unaffected by the chip temperature change in a range of 20°C up to 35°C (ambient temperature).

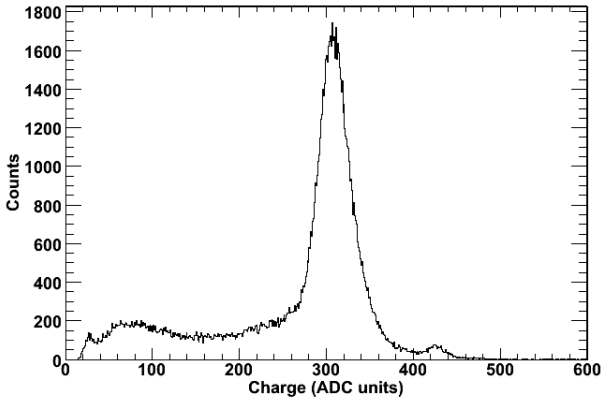


Fig. 5. Signal distribution in a cluster of 3×3 for sub-array S12 (number of hits versus signal amplitude) at 100 MHz clock frequency, obtained with a ^{55}Fe source (1 ADC Unit = 0.22 mV).

B. Digital Outputs

For the digital part, the study consists to analyze separately the 128 discriminators alone in one hand (pixels outputs are disconnected) and the 73728 pixels + 128 discriminators in the other hand. This way to proceed allows separating properly the noise contribution coming from the discriminators and the noise coming from the complete columns (pixels + discriminators). In both cases, transfer functions are obtained by changing the external threshold voltage via the programmable internal DAC by JTAG. Systematic offset, TN (mean value of noise) and FPN (sigma value of systematic offset) of discriminators are extracted from these measurements by applying an error function *erf* fit on transfer curves.

Distribution obtained is illustrated on Fig. 6 for discriminators only. The observed TN amounts to ~ 0.35 mV, while the threshold dispersion translates into a FPN of ~ 0.25 mV. These results are similar with those obtained with M16 prototype, which was equipped with the same discriminators.

The threshold scan is repeated with discriminators connected to the pixels (Fig. 7). The dispersions observed combine the pixel and discriminators noise contributions. The measurements results are illustrated in Fig. 7, which displays the measurements made with sub-array S12. TN increases to 0.6 mV, corresponding to 11 e^- and FPN is 0.3 mV, corresponding to 5 e^-. These values match well the requirements. The noise results obtained with the digital chain is compatible with ones obtained for the analog part.

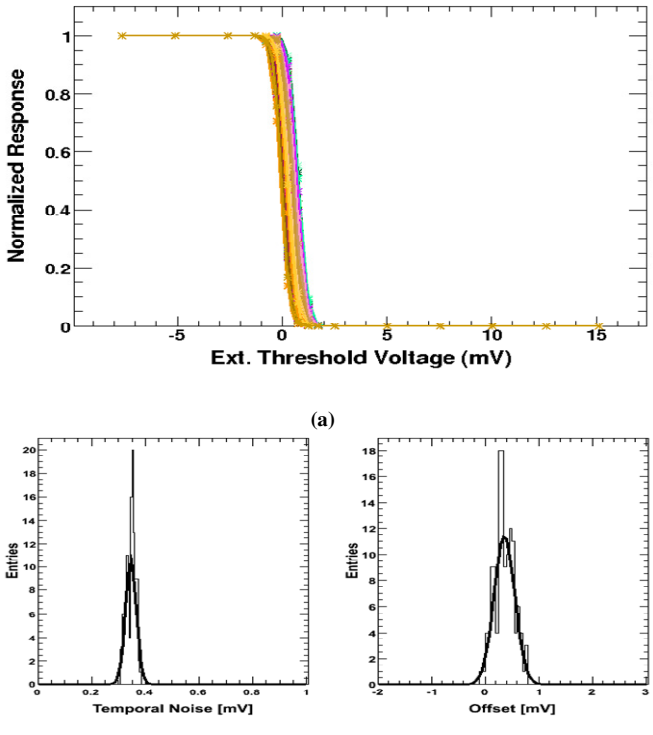


Fig. 6. (a) Transfer functions of the 128 discriminators when applying a threshold voltage scan at their outputs, (b) Temporal Noise distribution, and (c) extracted FPN value.

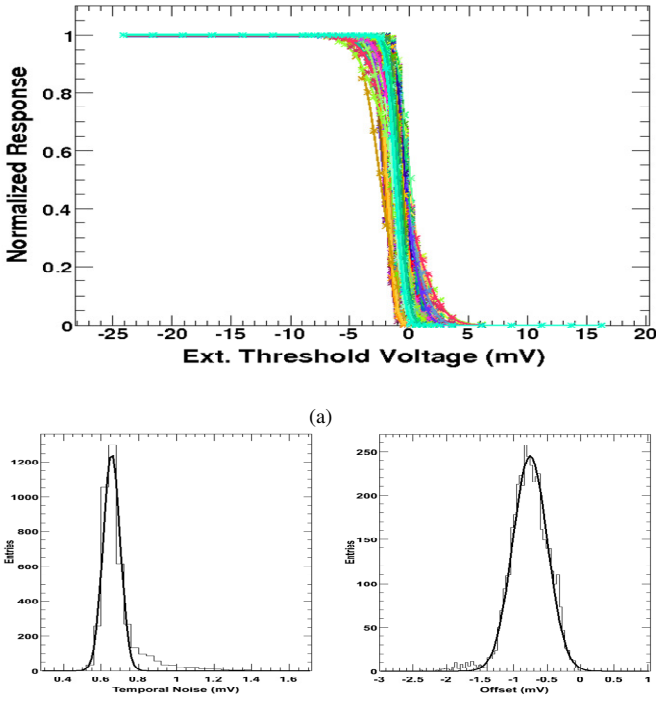


Fig. 7. (a) Transfer functions of the 128 discriminators connected to the pixels arrays when applying a threshold voltage scan at their outputs, (b) Temporal Noise distribution, and (c) extracted FPN value.

V. MIMOSA22 BEAM TESTS RESULTS WITH MIPS

A test beam campaign has been performed in August 2008, at CERN-SPS with a 120 GeV pions beam. Due to poor beam spills and dead time, only 2 chips (a standard one and an irradiated one at 150 kRad) have been studied during this period, and measurements were concentrated only to the promising sub-arrays S6 to S10, S12 and S13.

The setup used and types of measurements performed are already described in [4]. All measurements have been performed at f_{CK}=100 MHz, with an USB DAQ for the tested chip MIMOSA22. A C++ based analysis framework, developed by IPHC and extensively used since many years, using ROOT interface under LINUX environment, has been used. No survey is done to make any preliminary alignment corrections, so the final alignment is made by software using particles tracks. The alignment procedure is a simple minimization algorithm based on the assumption that the particle trajectory is a straight line. After the alignment procedure of the chip with the 8 reference planes, the performances of the chip can be off line calculated. Due to the high energy beam, multiple scattering is negligible.

A. Analog Tests Outputs

Detection performances of the analog part are studied. The analog part of the chip allows measuring the Signal-to-Noise ratio (S/N) for MIPs. Noises obtained with beam are compatible with values obtained in laboratory, i.e. comprise between 10 e^- and 14 e^- ± 0.1 e^-. Fig. 8 illustrates as an example the TN value obtained in test beam conditions for S6. The typical S/N values are measured between 16 (S13) and 21 (S8). This is an improvement compared to the previous chip MIMOSA16. This is due in part to the lower noise of the pixel, and also to a better CCE of MIMOSA22 (enhancement of the common source amplifier). Fig. 9 illustrates the S/N for S6 corresponding to 17.6.

Detection efficiency is also very satisfactory. It reaches 99.9% for all sub-array tested (by applying a standard cut on the seed pixel with a S/N>4). All the results obtained with the analog part are summarized in Table 3.

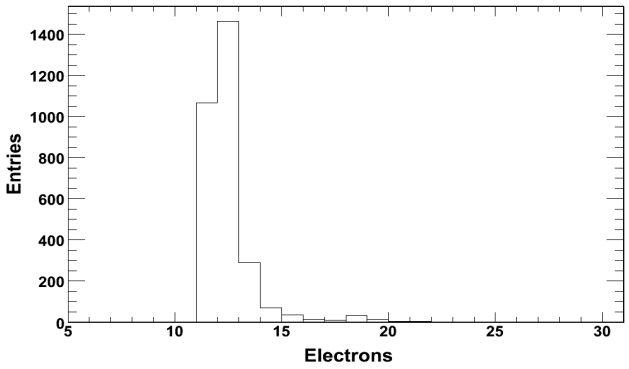


Fig. 8. Temporal Noise measured in beam tests conditions for sub-array S6, obtained on analog test outputs with MIPs at f_{CK}=100 MHz. The mean value is 12.4 ± 0.1 e^-.

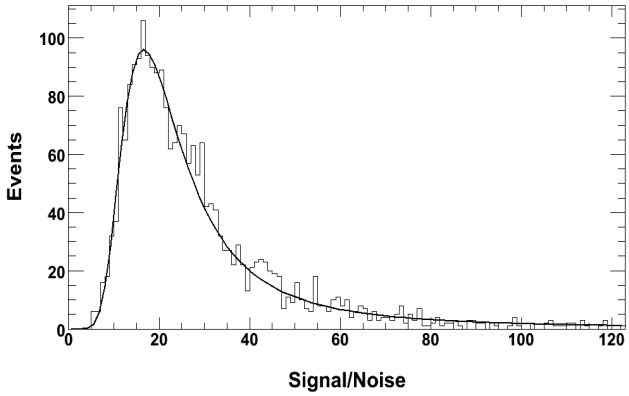


Fig. 9. Seed pixel S/N distribution for sub-array S6, obtained on analog test outputs with MIPs at f_{CK}=100 MHz. The MPV value is 17.6 ±0.2.

B. Digital Outputs

Performances of the digital part are characterized by three driving parameters: Detection Efficiency, Fake Hit Rate and Spatial Resolution. A scan of the discriminator threshold value (in mV or translated in S/N cut) allows finding the optimal threshold voltage range. For instance, by increasing discriminator threshold voltage, one improves the Fake Hit Rate, whereas the Detection Efficiency can be much degraded.

We remind that Detection Efficiency is defined as the ratio between tracks found in the telescope and hits found in the chip sensor. At low thresholds (2-3 mV), we find an efficiency usually between 99.9% and 100%. Up to 6 mV, the efficiency is kept above 99% for at least 4 different pixels architecture, which is largely satisfactory for the final telescope. Beyond this threshold value, the efficiency starts to decrease significantly as expected. Fig. 10 shows the efficiencies of sub-arrays S6 up to S13 for different discriminators threshold S/N cuts (conversion to mV depends on TN and Offset of the sub-array concerned).

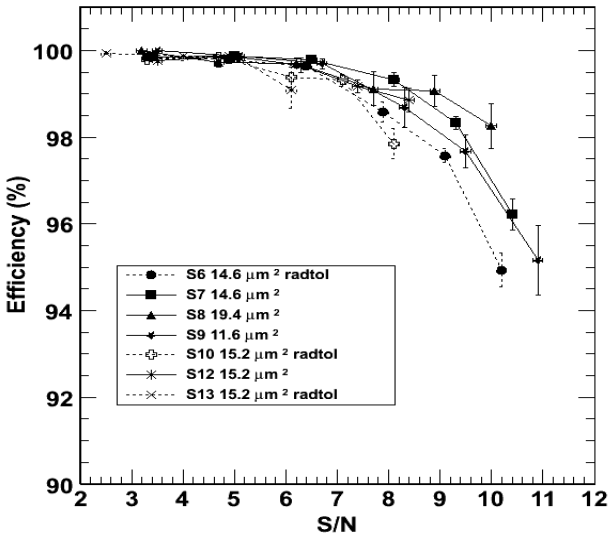


Fig. 10. Detection Efficiency of binary outputs as function of the S/N threshold cut of discriminators for sub-arrays S6 up to S13.

TABLE 3 : SUMMARY OF THE PERFORMANCES OF MIMOSA22 CHIP WITH MIPS FOR ANALOG OUTPUTS (@F_{CK}=100MHZ)

Sub-Array	*S6*	*S7*	*S8*	*S9*	*S10*	*S12*	*S13*
Detection Efficiency	*99.93% ±0.05%*	*99.95% ±0.04%*	*100.00% +0/-0.30%*	*100.00% +0/-0.14%*	*99.87% ±0.09%*	*100.00% +0/-0.08%*	*100.00% +0/-0.07%*
Input Referred Noise (e^-)	*12.5±0.1*	*11.6±0.1*	*12.3±0.1*	*10.6±0.1*	*13.6±0.1*	*12.1±0.1*	*14.0±0.1*
S/N (seed, MPV)	*17.6±0.2*	*18.5±0.2*	*20.9±1.1*	*19.5±0.5*	*16.5±0.3*	*18.2±0.3*	*16.0±0.3*

Fake Hit Rate is considered as the probability for one pixel and for one event to pass accidentally the discriminators threshold, while there is no MIPs crossing the pixel in the event. Practically, to estimate the Fake Rate, one uses test beam data with a reconstructed track going through outside the acceptance of the chip. This leads to a conservative estimate since fortuitous particle hits are still possible depending on beam intensity. In particular, when the discriminator threshold voltage is high, fake hits might be real hits, that the reason why the curve can reach a plateau at high thresholds.

Fig. 11 illustrates the Fake Hit Rate versus the discriminators S/N threshold cut for sub-arrays S6 up to S13. This parameter seems a little bit larger than for MIMOSA16, but it is still acceptable with the order of magnitude of 10^{-4} to 10^{-5}.

The third important parameter is Spatial Resolution. In case of a 1-bit discriminator, the spatial resolution expected is pitch/$\sqrt{12}$ = 5.3 µm. In practice, we use the multiplicity of the cluster (larger than 1) to improve the resolution. A simple center of gravity method is applied to compute the reconstructed position in MIMOSA22. The difference between this position and the reconstructed position of extrapolated telescope track gives the residual. Single point resolution is found to be ~ 3.5 µm for all sub-arrays tested (as expected).

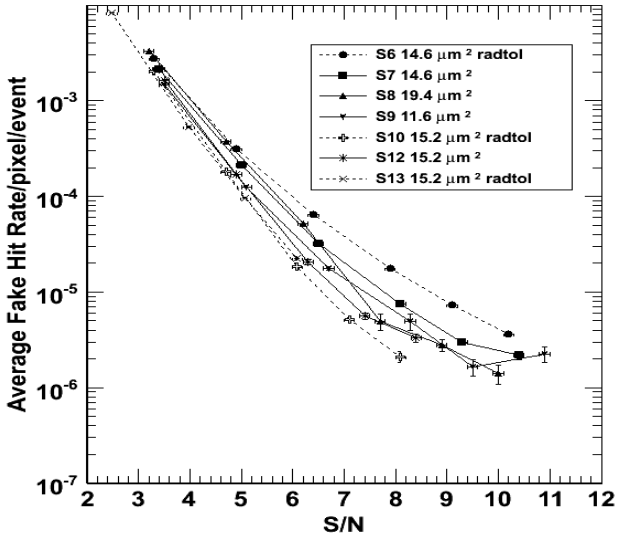


Fig. 11. Fake Hit Rate of binary outputs as function of the S/N threshold cut of discriminators for sub-arrays S6 up to S13.

To summarize, the main results of this beam test campaign shows very satisfactory detection performances in terms of Detection Efficiency, Noise, S/N, Fake Hit Rate and Spatial Resolution. Few pixel architecture (diode size, amplification scheme, and even progress on radiation tolerant diode design) are validated. Moreover, no problem of non-uniformity is observed over the chip surface, a real large scale detector is validated.

VI. RADIATION TOLERANCE: MIMOSA22-BIS CHIP

Radiation tolerance can be a concern for the future of the EUDET telescope [7]. Indeed, even if the annual dose at DESY is estimated to be lower than ~3.5 kRad/year, the doses expected in other machines (CERN, FermiLab), can reach an order of magnitude of ~100 kRad. Accordingly to these specifications, it was important to assess the radiation tolerance behavior of our architecture. For this purpose, a new chip, MIMOSA22-bis, has been designed in July 2008, and tested in beam in October 2008, with the main following objectives: check robustness of pixel operation against steering parameter values, optimize combination of parameters driving S/N value, and optimize the pixel design against ionizing radiation damage using enclosed layout (ELT) for some critical transistors. The main characteristics of some RadTol pixel sub-arrays of this chip are summarized in Table 4.

TABLE 4 :CHARACTERISTICS OF SOME MIMOSA22-BIS RAD-TOL PIXEL SUB-ARRAYS

Sub-array	*Diode Surface (µm²)*	*Diode biasing type*	*Ampl. type*	*Feed-back*	*RadTol diode*	*Enclosed Layout Transistor (ELT)*
S2	*11.32*	*SB*	*ECS*	*static*	*yes*	*no*
S4	*14.62*	*SB*	*ECS*	*static*	*yes*	*feedback transistor*
S5	*14.62*	*SB*	*ECS*	*static*	*yes*	*No*
S13	*15.21*	*LOG*	*CS*	*no*	*yes*	*biasing transistor*

SB: Self-Bias; LOG: NMOS transistor with Gate-Drain terminals shorted

Fig. 12 illustrates the Detection Efficiency versus S/N cut before and after irradiation at 150 kRad. Very good performances, in terms of noise, CCE and Detection Efficiency are preserved. Performances of reference sub-array in MIMOSA22 (S6) and MIMOSA22-bis (S5) are identical.

The detailed architecture and complete test results of this chip will be presented later in a separate paper.

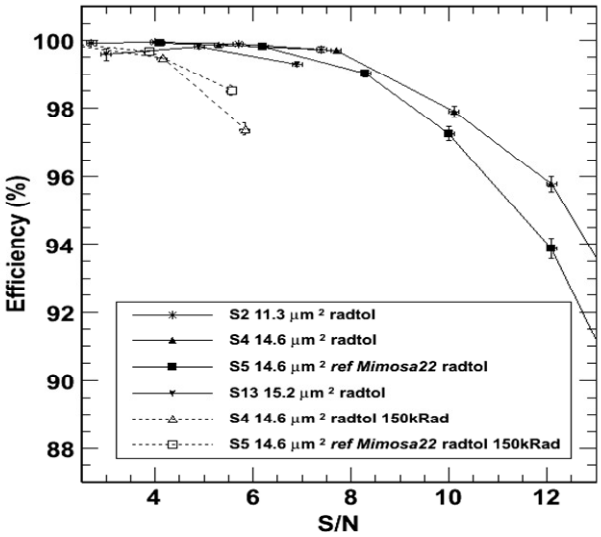


Fig. 12. MIMOSA22-bis binary outputs: Detection Efficiency as function of the S/N threshold cut of discriminators for sub-arrays S1 up to S13 for a non-irradiated chip and for an irradiated chip at 150 kRad.

VII. Conclusions

Parallel column architecture with discriminators output is validated for MIPs detection on a real large scale (128 column of final length). The readout frequency is ~104 frames/s. Pixel noise is ~10 to 14 e^-, with a S/N ratio ~16-21. Detection Efficiency is > 99.5% with a Fake Hit Rate of 10^{-4}-10^{-5}. The single point spatial resolution is ~3.5 µm. In parallel to the MIMOSA22 chip tests, a zero-suppression circuit (∅–circuit, called SUZE) has been validated [8] for 128 columns at a readout frequency greater than the nominal frequency. Radiation tolerant pixel architecture has been also assessed.

The final EUDET sensor, MIMOSA26 (combining column parallel architecture with zero-suppression circuit), will have an active surface of 1152 columns of 576 pixels (21.2×10.6 mm^2). This chip will be an extension of MIMOSA22 and ∅–circuit from 128 columns to 9×128 columns.

The design of MIMOSA26 is actually under progress and it will be submitted mid-November 2008, and sensor tests are expected to start in January 2009.

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