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High resolution photon timing with MCP-PMTs: a comparison of commercial constant fraction discriminator (CFD) with ASIC-based waveform digitizers TARGET and WaveCatcher.

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***Abstract* – There is considerable interest to develop new time-of-flight detectors using, for example, micro-channel-plate photomultiplier tubes (MCP-PMTs). The question we pose in this paper is if available waveform digitizer ASICs, such as the WaveCatcher and TARGET, operating with a sampling rate of 2-3 GSa/s can compete with 1GHz BW CFD/TDC/ADC electronics. We have performed a series of measurements with these waveform digitizers coupled to MCP-PMTs operating at low gain and with a signal equivalent to ~40 photoelectrons. The tests were done with a laser diode on detectors operating under the same condition as used previously in SLAC and Fermilab beam tests. Our measurement results indicate that one can achieve similar resolution with both methods. Although commercial CFD-based electronics are readily available and perform very well, they are impractical to implement on a very large scale, necessitating custom electronics. In addition, analog delay line requirements make it very difficult to incorporate CFD discriminators in ASIC designs.**

INTRODUCTION

The possibility to use fast MCP-PMTs with 10μm holes and a 1cm-thick quartz radiator to produce Cherenkov light (see Fig.1) to achieve high resolution TOF counters poses the question of what readout electronics to use. The traditional method is to use a constant-fraction-discriminator (CFD), coupled to a high resolution TDC, and an ADC to correct residual amplitude-dependent timing dependence ("time walk"), which the CFD does not entirely remove [1]. With such methodology we have achieved a timing resolution of σ ~14ps per counter in both test beam and laser bench tests [1] (see also Fig.2). The MCP-PMT was operated at a low gain[1] of 2-3x10^4 in these tests. This is a crucial point as MCP-PMT aging and rate issues become less severe at lower gain. However one has to offset this handicap by having a thicker radiator to produce more photo-electrons. In the test beam we used a 1cm-thick quartz radiator with Al-coated cylindrical sides, which yields a number of photoelectrons, Npe ~20-35, producing a total charge of N_{total} > 5-8x10^5 avalanche electrons, which is the necessary minimum to obtain good timing resolution.[2] One wants to keep the total avalanche charge as low as possible for a safe operation of the MCP when considering aging effects in a high rate environment, while still getting a good timing resolution. The quartz radiator produces fast a Cherenkov signal, which is an essential ingredient to achieve good timing resolution. As is shown in Fig.1, one could also inject a fast laser diode light pulse[3] into the MCP through the quartz radiator, and determine the timing resolution under this condition. In the laser tests we could vary number of photoelectrons, as shown in Fig.2, by adding Mylar attenuators. For the waveform digitizing electronics tests we have selected Npe ~40.

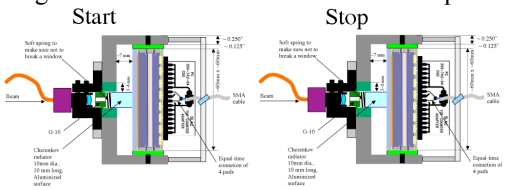


Fig. 1 The prototype setup, based on two nearly identical Burle/Photonis MCP-PMTs with 10μm MCP holes, used for timing measurements in this paper. The detector setup is the same as used in a Fermilab beam test [1].

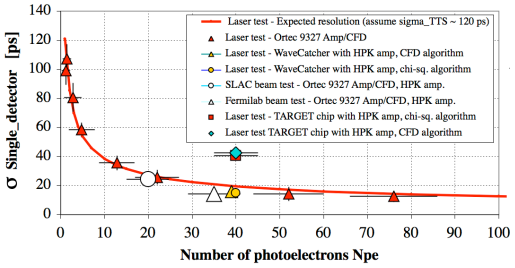


Fig. 2 A graph shows all results presented in this paper with the setup shown in Fig.1. It includes SLAC and Fermilab beam test results (large open circle and triangle) and laser tests with Ortec CFD, and waveform digitizers Target and WaveCatcher. Important point is that the MCP-PMTs operated at low gain in this test.

This work supported by the Department of Energy, contract DEAC02-76SF00515, and DOE Advanced Detector Research award DE-FG02-08ER41571, and by the French P2I research consortium (Physics of the Two Infinites) on the theme called "miscellaneous highly specialized programs" under the name "Development of analog multi-GigaHertz acquisition systems".

[1] Low gain operation was chosen to eliminate single photoelectron background at SuperB, so that the detectors would be sensitive only to charged particle tracks.

[2] Expected timing resolution with a threshold type of electronics is: $\sigma_t = \sigma_{noise}/(dS/dt)_{thresh} \sim t_r/(S/N)$, where σ_{noise} is the rms noise, $(dS/dt)_{thresh}$ is the derivative of signal evaluated at the threshold, t_r is the pulse rise-time and S/N is a signal-to-noise ratio.. Therefore the rise-time t_r and S/N are crucial variables to get a good timing resolution. One can lower the gain only if the noise is correspondingly smaller.

[3] PiLas is a laser diode made by Advanced Laser Diode Systems A.L.S. GmbH, Berlin, Germany. In this test we used a 407nm laser diode.

The new electronics method to be used for high-resolution timing is based on waveform digitizers utilizing analog memories. In this paper we are asking whether the 2.5 GSa/s TeV Array Readout GSa/s Electronics with Trigger (TARGET) [2-4] and the 3.3 GSa/s WaveCatcher [5] ASIC-based waveform digitizers, can compete with a 1GHz BW CFD timing technique, which was represented by the Ortec electronics[4] in our case. The complete specs of both digitizers are shown in Appendix I.

Fig.2 shows a summary of all results. One can see that the WaveCatcher waveform digitizing test result is consistent with the beam and laser test results, which both used the Ortec 9327CFD, TAC588, and 14bit ADC114 electronics.

Fig.3 shows two possible applications of results presented in this paper for so called "pixilated" TOF detector.[5] The Cherenkov radiator consists of the quartz cubes, each optically isolated by Aluminum reflective coating of sides. The stepped face solution on Fig.3b will suffer from worse resolution near edges.

The pixilated TOF detectors were proposed for the SuperB endcap application [6], and therefore we have chosen this particular operating point for the comparison. One should stress, however, that a choice of some other operating point may need to retune this study, as pulses shapes may change, for example, because one may require much higher gain to detect single photoelectrons. We have chosen this example because we had good existing results from the Fermilab test beam, as well as many good reference laser tests with the CFD/TAC/ADC electronics.

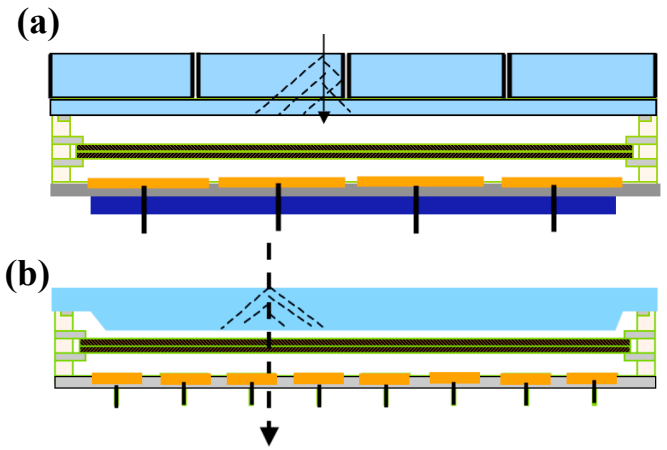


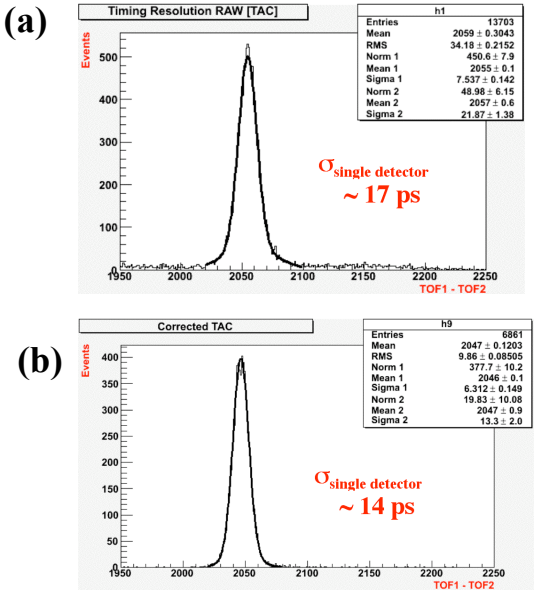
Fig. 3 (a) Photonis Planacon MCP-PMT with pads arranged into 16 macro-pixels. The radiator consists of 16 cubes, each one optically isolated from others by aluminum reflective coating. (b) Radiator is part of the stepped-face MCP-PMT widow. Here one has to deal with the charge sharing.

TIMING METHODS

A. Beam test and laser test results with CFD/TDC/ADC

Figure 4 shows results from a 120 GeV/c proton beam at Fermilab [1]. Fig.3a shows the results for all events without any ADC cut or CFD time-walk correction. Fig.3b shows the final resolution of $\sigma_{single\_detector}$ ~14ps per counter, corresponding to tighter cuts on the MCP-PMT pulse heights, shown in Fig.4c, and the time-walk correction to the CFD timing, shown on Fig.4d. The electronics for this test is shown in Fig.5a. The results clearly indicate that one has to be careful losing photoelectrons, and that the CFD needs to be corrected for the time-walk to achieve the ultimate resolution. Beam test results from the SLAC and Fermilab tests are entered to Fig.2.

Fig.2 also shows the laser diode lab test results with the same detectors with the same gain and electronics (see Fig.5b), but with a different laser diode (635nm). The laser tests used a 80:10:10 fiber splitter to get the signal into two detectors at the same time. The single detector resolution is obtained by dividing the measured resolution by √2. The laser diode optics produced a 1 mm spot on the MCP face. Fig.2 shows the measured resolution as a function of the number of photoelectrons[6] (Npe) at low gain for the CFD arming thresholds of –10 mV, the CFD walk (zero-crossing) threshold of +5 mV and MCP-PMT voltages of 2.28 & 2.0 kV respectively, and compares it with a prediction.[7] The prediction agrees well with the data if we assume that the transit time spread (the resolution for a single photoelectron) is σ_{TTS}(extrapolated to Npe = 1) ~120 ps; such a large value of σ_{TTS} is consistent with our choice of low gain operation in order to be linear for signals of up to Npe ~30-50, where we measure $\sigma_{Single\_detector}$ ~20 ps, see Fig.2.



[4] Ortec 9327 Amplifier/CFD (1GHz BW), TAC588, and 14bit ADC114 electronics, plus an additional ADC correction of the CFD timing..

[5] Present cost of a detector wall, made of ~550 Planacon detectors, is too expensive. Hopefully such detectors could be affordable in future.

[6] Laser diode light was attenuated by Mylar asttenuators ands Npe was determined by several methods: (a) scope, (b) ADC measurement, and (c) statistical arguments.

[7] **Laser test:** $\sigma \sim \sqrt{[\sigma^2_{MCP\text{-}PMT} + \sigma^2_{Laser} + \sigma^2_{Electronics}]} \sim$
$\sim \sqrt{[\sigma_{TTS}/\sqrt{N_{pe}})^2 + \sqrt{((FWHM_{Laser\_diode}/2.35)/\sqrt{N_{pe}})^2 + (\sigma_{Electronics})^2]}$.

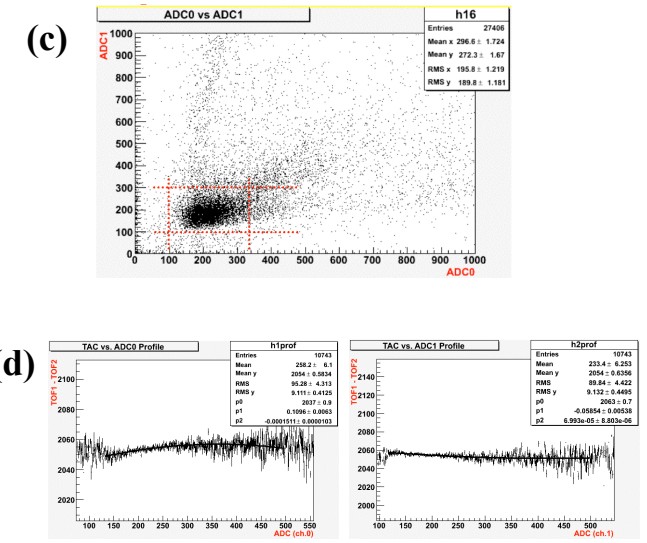


Fig. 4 (a) The single-detector resolution obtained in a 120GeV proton beam at Fermilab with the Photonis MCP-PMT. Both detectors had MCP holes of 10 μm dia. No off-line correction to the CFD timing, and accepting all events. (b) The same result, but applying time-to-ADC correction to the CFD timing, and applying tight ADC cuts, as shown in (c) and (d).

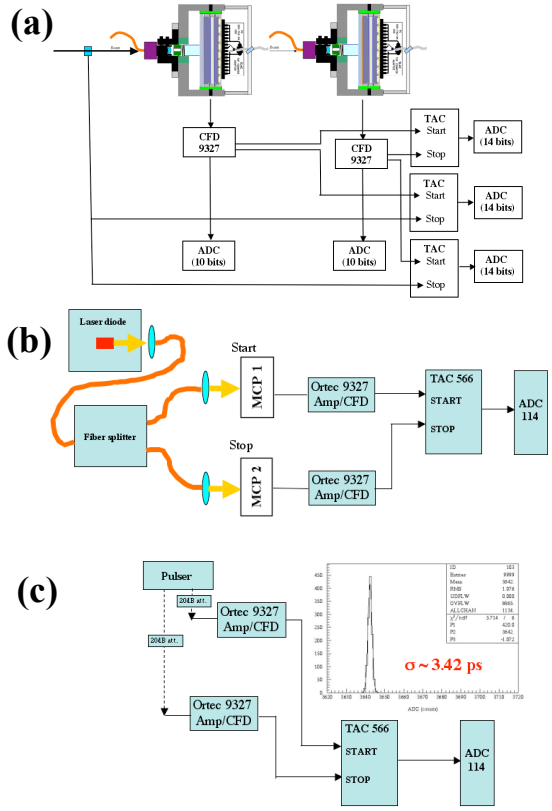


Fig. 5 (a) CFD-based electronics setup used in the Fermilab beam test, employing a small trigger counter (see Figs. 4a,b,c,d). The detector was connected to the Ortec 9327 CFD via a short 6-inch long SMA cable. Time between start and stop signals was measured by the Ortec TAC 566 and a 14 bit Ortec ADC 114. It was found that this arrangement was not good enough to remove time walk, and it was necessary to add another ADC. to correct the time-walk. This ADC was coupled to a 9327 CFD monitor signal via additional amplifier. (b) CFD-based setup used for the laser tests (see Fig.1). (c) Electronics calibration with the CFD-based electronics. The single detector electronics resolution $\sigma_{electronics} = \sigma_{two\_detectors}/\sqrt{2}$ ~3.42ps is the best performance, to our knowledge.

B. The laser test setup for the waveform analysis

The laser bench setup with the waveform digitizing electronics used two Hamamatsu C-5594-44 1.5 GHz BW amplifiers with 63x gain,[8] coupled to each detector via a 6-inch long SMA cable. Fig.6 shows a detector setup with two amplifiers. The laser diode operated at a wavelength of 407 nm, and the light was split by a 80:10:10 fiber splitter to get the signal into two detectors at the same time.

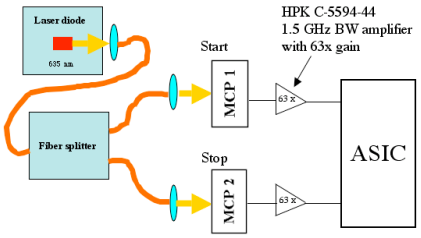


Fig. 6 MCP-PMT detector with Hamamatsu amplifiers and the waveform digitizing electronics, either the Target chip or the WaveCatcher board..

C. Timing results with the WaveCatcher ASIC board

The USB WaveCatcher board is suited for acquisition of fast analog signals over a short time window. The current version is based on the SAM chip [7]. This ASIC, designed in the AMS CMOS 0.35μm process, integrates two channels of ultrafast differential analogue memories of 256 cells each arranged in a matrix structure relying on a CEA/IRFU and IN2P3/LAL common patent [8]. The chip performs the sampling of analogue data at a rate up to 3.2GS/s, defined by an internally servo-controlled delay line loop. Sampled data is stored in an array of capacitors which can be fully or partially read back and digitized by an external ADC operating at a moderate conversion frequency (10MHz).

The WaveCatcher board, measuring 149x77 mm², is USB 2.0 driven at a 12Mbits/s rate. Its very low power consumption (< 2.5W) allows it to be powered by the sole USB bus.

It performs the digitization over 256 points of 2 DC-coupled analog channels of bandwidth above 500MHz over 12 bits at a sampling frequency (Fs) switchable between 400MHz, 800MHz, 1.6GHz and 3.2GHz. This offers a sampling depth ranging from 80ns at 3.2GS/s up to 640ns at 400MS/s. It also includes on each channel a pulse generator for reflectometry measurements and the possibility to perform signal charge integration (direct measurement of the charge of a PM signal for instance). In the latter case, the sustainable trigger rate can rise up to a few tens of kHz.

The input analog ranges can be individually offset thanks to 16-bit DACs over the full ±1.25V dynamic range, thus taking benefit of the maximum SNR whichever the shape of the signal.

The trigger signals can be generated inside the board (there is an individual discriminator with a 16-bit DAC threshold on each input, internal random trigger) or outside (software trigger, external trigger input). The board trigger can also be

[8] Fermilab beam test did not use the Hamamatsu 63x amplifier [1].

sent to the external world through the LVCMOS trigger output. So, different boards can easily be synchronized. Moreover, trigger rate counters are implemented, thus permitting to measure said rates independently of the readout of the event.

The board can also be used as a TDC for high precision time measurement between two signals. Said signals can be present either on the same input channel, or on two different channels, and their distance must be smaller than 16 clock periods (one clock period = 5ns@3.2GS/s up to 40ns@400MS/s). Sampling time precision is better than 10 ps rms at 3.2GS/s.

Power is taken from USB, but the board can also be powered with a +5V external supply through a standard 2.1mm jack plug. Although the standard default connectors are BNC, SMA or LEMO connectors can be mounted instead.

Fig.7a shows a WaveCatcher board used in these tests. It was used with a sampling rate of 312.5ps/bin and the full front-end BW of 500MHz. Fig.7b shows a "scope-like" software interface developed for this waveform digitizer to setup this measurement.

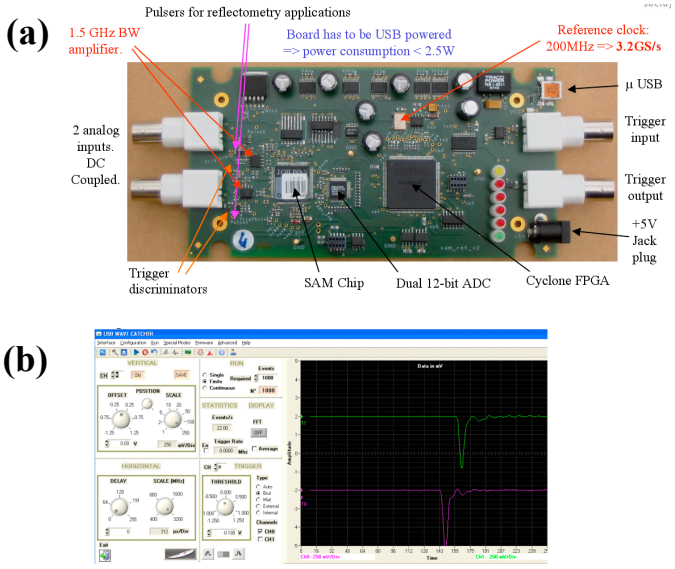


Fig. 7 (a) WaveCatcher test board used in this paper (b) Scope-like software interface for the WaveCatcher board.

In order to obtain the best measurements in terms of timing measurement, it is necessary to correct the effect of integral non-linearity (INL) in time of the analog memory, which is typically a necessary correction with these types of digitizers. The effect is described in Fig.8a: the sampling points (blue points) which should be equidistant are actually not, and therefore the real signal (black) may turn into the fake one (dashed blue).

The INL effect has to be calibrated out, and therefore a method using only a good-precision sine wave generator[9] has been developed to measure the error in the sampling instants: a well-chosen sine wave (135 MHz, 500mV rms as shown on Fig.8b) is used as a source of segments crossing the mid scale of the dynamic range. These segments are assimilated to straight lines. Using a sufficient statistics, the mean length of the segments directly gives the differential non-linearity (DNL) in time, whereas the jitter on their length gives the jitter on the measurement time. Integrating the DNL and rescaling it with the clock period gives the Integral Non Linearity in time (time INL). The INL correction, which is very stable over long term, can be used to correct the position of the samples of an event to their actual location in time in two different ways: either re-creating equidistant samples (green crosses on Fig.8a) thanks to a second order Lagrange polynomial interpolation (for instance if the signal has to be fully displayed on screen or used for a FFT), or just using the real time position of the few points (red points on Fig.8a) needed for the ongoing measurement (like precise time measurement with CFD method as described below).

The effect of this correction is very significant. For the WaveCatcher board, the DNL distribution was 7.5ps rms before the calibration, and 0.33ps rms after. Similarly, the INL distribution was 16.9ps rms before the calibration, and 1.15ps rms after.

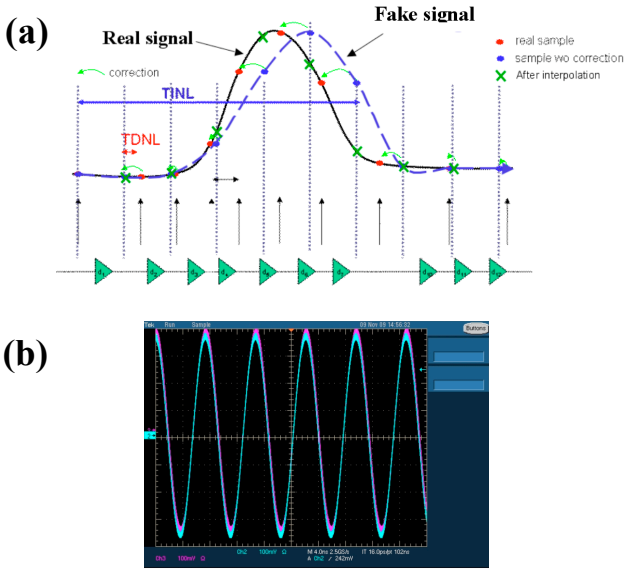


Fig. 8 (a) Difference between the real and distorted pulse shape is caused by DNL (a differential non-linearity) time shifts. Total accumulated time shift is called INL (a integral non-linearity) (b) A 135 MHz sine wave used to determine the DNL and INL constants for the Wave Catcher.

The laser was adjusted to 100Hz frequency for these tests (see Fig.6), the MCP-PMT voltages to 2.21 and 2.1kV to operate at a gain of 2-3x10^4, and the laser intensity adjusted to give a similar charge as in the Fermilab test [1]. The WaveCatcher took data with 312.5ps/bin; the first analysis step was to perform a spline interpolation, which worked with either 1ps or 10 binning (at the end it was determined that the 10ps binning is sufficient). Fig.9 shows the MCP-PMT pulses, as measured by the WaveCatcher board with the spline fit with an interpolation step of 10ps bins, and by a 1GHz BW scope. Two timing methods were employed. (a) The first one, shown on Fig.10a, is a software CFD method, which consists of normalizing the pulses to the same peak and using a constant-

[9] High precision 8656B HP gate sine wave generator, 0.1-999MHz

fraction threshold, usually set to 18-22% of the peak amplitude. (b) The second method is called a reference timing. In this method one determines first a reference pulse shape (see Fig.10b). The pulse to measure is then stepped through the chosen reference pulse, and one calculates a χ^2 including a certain number of bins; this needs to be tuned to get the best performance. One can use, for example, a second order polynomial to fit only the leading edge of the average pulse profile of normalized pulses (see Fig.11). Fig.12 shows the χ^2 values as a function of the timing step, and resulting time distributions corresponding to a χ^2-minimum. Figs.13a&b shows final results of the timing distribution between start & stop TOF counters for both (a) the reference timing method and (b) the CFD method. We quote a final resolution per single counter by dividing the fitted result by √2. One can see that the χ^2 method yields a better timing resolution than the CFD method. The crucial variable to obtain a good resolution with the χ^2 method is number of bins used in the χ^2. We found the best resolution with 190 10ps-long bins.

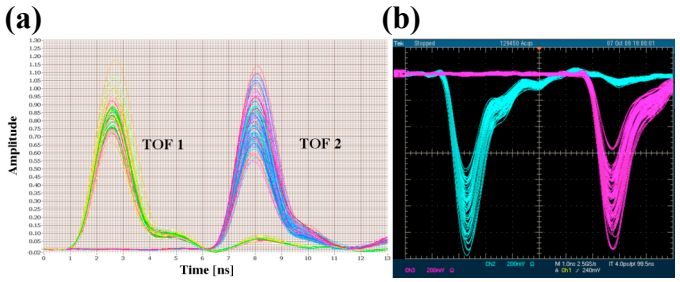


Fig. 9 Laser-generated pulses corresponding to Npe ~40, which is a charge approximately equivalent to the Fermilab beam test [1]: (a) spline-interpolated WaveCatcher chip pulses (inverted), (b) the same measurement by the Tektronix 1GHz BW scope,.

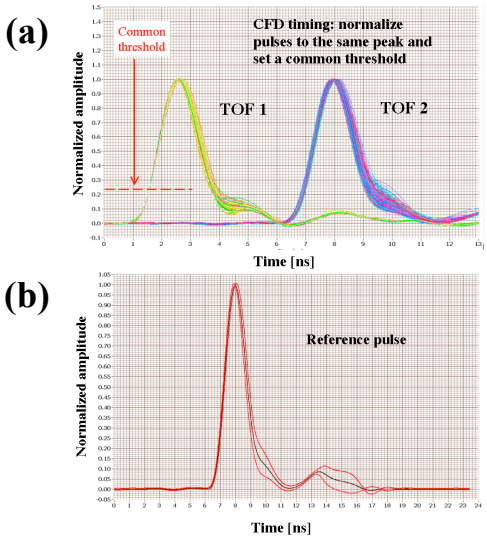


Fig. 10 (a) Normalize the WaveCatcher pulses to the peak amplitude. Set a threshold 22% of peak amplitude to perform a CFD timing. (b) Average pulse shape used for the reference timing chi-sq algorithm (black is average, red shows ± 2 sigma contour).

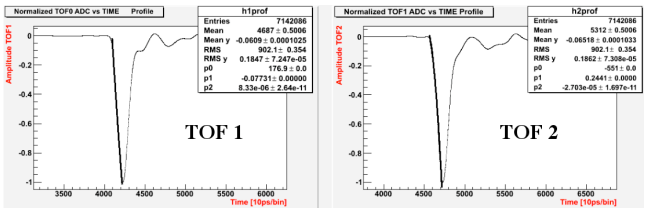


Fig. 11 A reference pulse for the χ^2 timing, formed from a second order polynomial fit to the leading edge of the average pulse shape profile; the fit is used as a reference pulse in the χ^2 timing in Fig.13a.

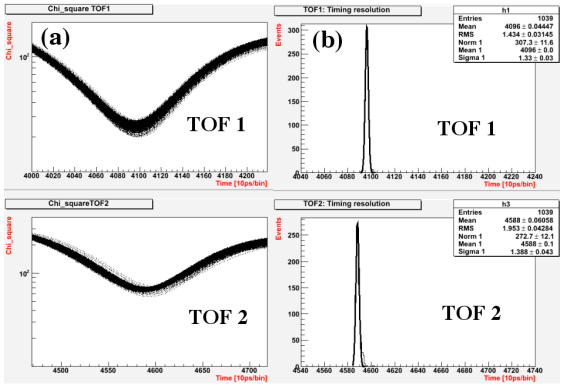


Fig. 12 WaveCatcher board: (a) χ^2 as a function of time to find the best timing point. (b) Resulting time distribution for two single channels corresponding to χ^2 - minimum.

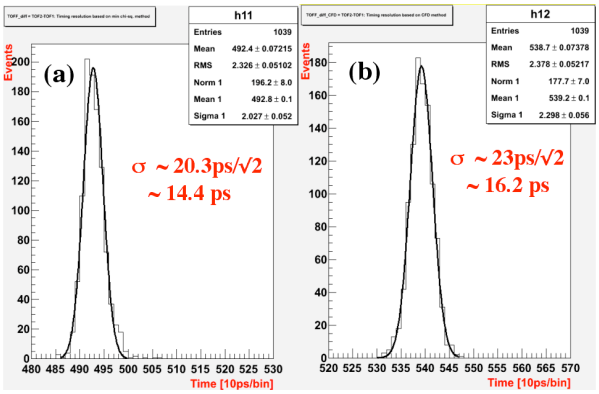


Fig. 13 Laser test result with the WaveCatcher board: (a) Timing resolution with the chi-sq algorithm using the reference pulse of Fig.11 with 10ps-long bins. (b) The timing resolution with the CFD algorithm, where the threshold is set to 15% of the peak amplitude.

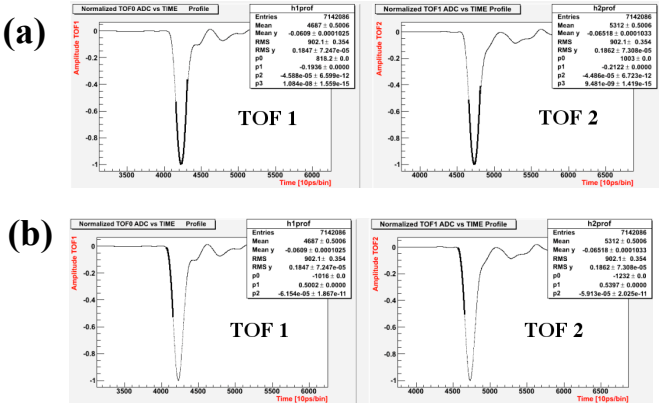


Fig. 14 A reference pulse for the χ^2 timing, formed from: (a) A third order polynomial fit to the pulse peak of the average pulse shape profile; the fit is used as a reference pulse for the χ^2 timing in Fig.15a. (b) A second order polynomial fit to the very beginning of the leading edge of the average pulse shape profile; the fit is used as a reference pulse for the χ^2 timing in Fig.15b.

It is not a'priori obvious which portion of the pulse carries the highest precision. What enters here is not only the S/N ratio of each sample (see footnote 11), but also the fluctuations in the MCP amplification. Since we do not have a reliable MCP MC simulation program at present, we have decided to explore this question empirically. Figure 14 shows two additional methods to create the reference pulse for the χ^2 method: (a) peak region only and (b) the very beginning of the leading edge only. In each case an optimum number of bins used in the χ^2 calculation had to be retuned. Figure 15 shows the result: doing timing with the very beginning of the leading edge carries the slightly higher precision. The resolution is almost ~0.9ps better than if we use the peak region only, and ~0.4ps better than if we use the entire leading edge. All these χ^2 timing methods are better than the CFD timing, which yielded a resolution of ~16.2 ps (see Fig.13b).

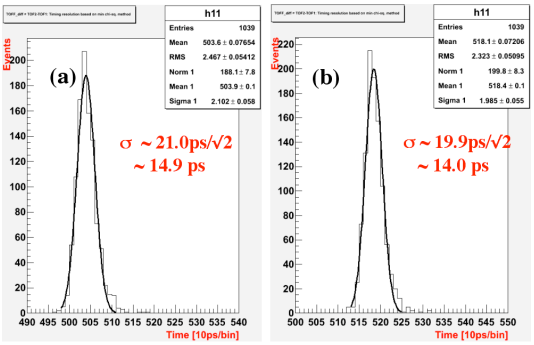


Fig. 15 Laser test result with the WaveCatcher board: Timing resolution with the χ^2 algorithm using the reference pulse made using (a) the peak region (see Fig,14a), (b) the very first portion of the leading edge (see Fig.14b).

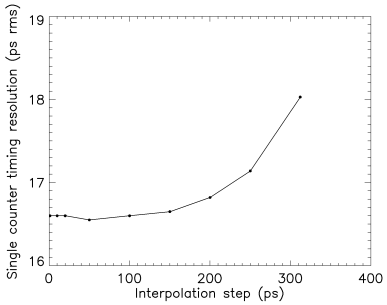


Fig. 16 CFD-based single counter timing resolution as a function of interpolation step in the spline fit ($\sigma_{single\_detector} = \sigma_{double\_detector}/\sqrt{2}$).

Although it is appropriate to investigate various methods of timing in the R&D stage, in the final application one has to worry about the speed of the algorithm. From this point of view we believe that the CFD-based software algorithm is a very good candidate for future large-scale applications with the waveform sampling electronics as it is much faster than the χ^2-method. However, even the CFD-based algorithm has to be optimized for speed while preserving the performance. In all results so far we used an interpolation step of 10ps. In Fig.16 we vary the spline interpolation period from 1ps to 312ps (312ps means no spline interpolation at all), while keeping the CFD algorithm the same. This is equivalent to a simulation of the system with various sampling frequencies. We can see that for interpolation period between 1 and 100ps the time resolution is unchanged, for 150ps the increase is very small and at last, without spline interpolation (312.5ps) the timing resolution value remains good: $\sigma_{single\_detector}$ ~ 18.1 ps. From this we conclude that applying this very simple algorithm, which is easy to integrate inside a FPGA (finding a maximum & linear interpolation between two samples, i.e., without a use of the spline fit), already gives very good results (only 10% higher than the best possible resolution limit, and even no loss if the chip was able to sample at a 6GS/s sampling rate).

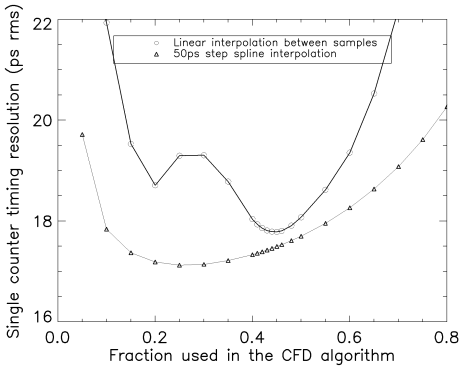


Fig. 17 CFD timing using full computing power with a spline fit with 50ps interpolation step (open triangles), and a simple FPGA algorithm with linear interpolation (open circles, see also footnote 8).

Figure 17 shows a comparison of the resolutions obtained using an ideal CFD calculation using a full computing power and using a simpler method, which can be easily implemented in FPGA firmware[10]. The ideal method, applied on data corrected from timing INL, as described previously, gives a $\sigma_{single\_counter}$ ~17.2ps for a CFD fraction in the range of 0.2 to 0.3. If the INL correction is not applied, the resolution worsens to 27.3ps. The simplest algorithm, applicable for FPGA firmware, gives only ~8.5% worse result than the complex method.

Data taken over a period of three months using the same timing calibration data gives the same timing resolution performances. This validates the high stability of the timing INL pattern already noticed.

D. Timing with the TARGET ASIC chip

Fig.18a shows a TARGET ASIC chip card used in these

[10] Algorithm: (a) For each sample, the data are first corrected from timing INL by associating a corrected time Tc(j) to each sample j thanks to a lookup table (b) after a pedestal subtraction, find the pulse and its amplitude M, (c) determine the two samples with index j and j+1 between which the waveform cross the M.F level (F is the fraction), (d) approximate the waveform by a simple straight line. The timing is then given by: Time = Tc(j)+ (Tc(j+1)-Tc(j))*MF/(V(j+1)-V(j)). Using this method I find a single counter resolution of 18.6ps rms (for F= 0.23).

tests. Fig.18b shows a block diagram of the TARGET ASIC together with the FPGA chip providing control signals. The TARGET chip used in this test was run at a sampling rate of ~450ps/bin. The analog BW into the storage array is approximately 150 MHz for this test. After an on-chip terminator, the analog signal is copied to the matrix of 8 storage rows of 512 samples for each of the 16 input channels. Each of the rows may be independently addressed to initiate a storage cycle. Within each Switched Capacitor Array (SCA) storage cell is a capacitor and a comparator. Conversion of these stored samples is done using a Wilkinson ADC method, where the stored voltage is converted into a transition time of the in-cell comparator due to an applied voltage ramp. Encoding is performed by measuring the time interval between the start of the ramp and the comparator output transition. In a simple form of time-to-digital conversion, this interval is measured by counting the number of high-speed clock cycles taken [4,5].

Fig.18c shows a "scope-like" software interface used with this waveform digitizer to setup this measurement.

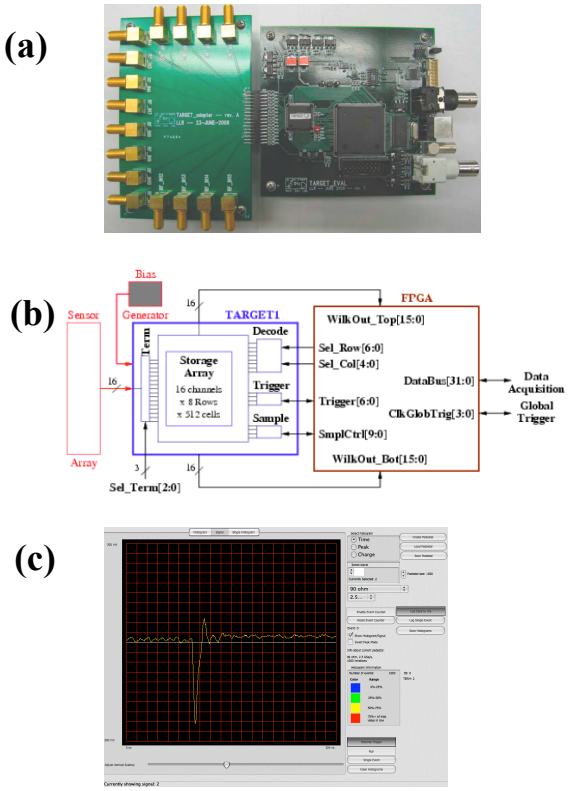


Fig. 18 (a) Test board to evaluate its performance. (b) The TARGET ASIC chip block diagram. (c) Scope-like software interface for the Target chip

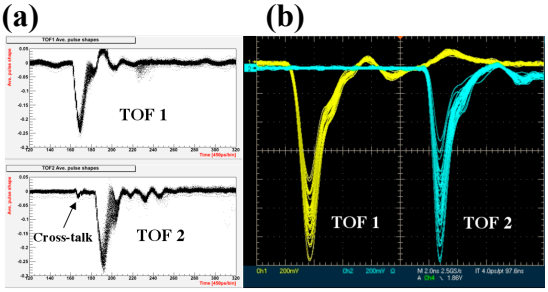


Fig. 19 The laser-induced waveform pulses, as measured in (a) Target chip and (b) a 1GHz BW scope, correspond to Npe ~40, which is approximately equivalent to the Fermilab beam test [1].

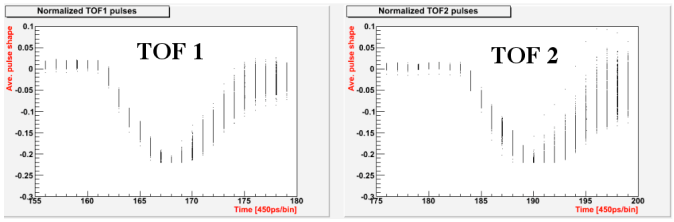


Fig. 20 Normalized pulses, which were used for the CFD-based algorithm. A pulse peak was found by a parabola fit to top region of the pulse.

The laser was run at 10Hz in this test, the MCP-PMT voltages at 2.2 and 2.1kV, and the laser intensity adjusted to give a similar charge as in the Fermilab test [1]. The Target chip took data with ~450ps/bin. The first analysis step was to perform the spline interpolation with 10ps-bins. Fig.19 shows the MCP-PMT pulses, as measured by the Target chip and a scope for a condition used in the Fermilab beam test [1].

There are two timing methods we employed. The first one is a software CFD method, which consists of normalizing the pulses to the same peak and using a constant-fraction threshold, usually set to 18-22% of the peak. We used a parabola fit the small region near the pulse peak to find the optimum maximum amplitude, which was used for the normalization. Fig.20 shows the normalized pulses, which were used in the CFD algorithm. The second method is called a reference timing. In this method one finds first a reference pulse shape, in this case a fit to leading edge of average pulse profile of normalized pulses – see Fig.21 for an example of such fits. The reference pulse is then stepped through a given normalized pulse, and one calculates a χ^2 using a number of bins, which needs to be tuned. We found that the optimum tune of the number of samples is 40-60 of 10ps-long bins, which corresponds to a time interval equivalent to the length of the pulse leading edge. Fig.22 shows a χ^2 tune as a function of the timing step, and a resulting time distribution corresponding to a χ^2-minimum. Fig.23 shows the final result of the timing distribution between start & stop for both the CFD and χ^2 timing methods. We quote a resolution per counter by dividing the fitted result by √2. One can see that the reference timing is slightly better.

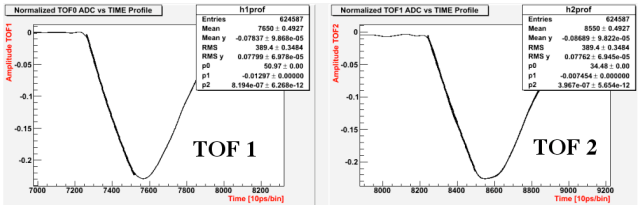


Fig. 21 A fit to a profile leading edge of pulse profiles used in the reference timing method. Although, one fits only the leading edge for highest accuracy, in the χ^2 calculation, we use a larger number of bins than just a leading edge range (in this case: 380 10ps-bins) to improve the statistical accuracy.

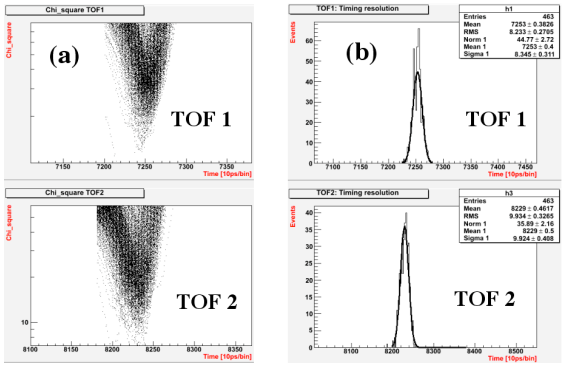


Fig. 22 (a) χ^2 as a function of time. (b) Resulting time distribution for two single channels corresponding to χ^2 - minimum.

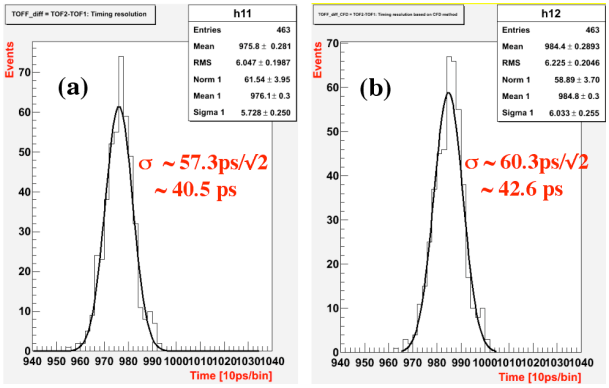


Fig. 23 Laser test result of the timing distribution between start & stop for both the (a) CFD and (b) χ^2 timing methods with the Target chip. We quote a resolution per counter by dividing the fitted result by √2.

The TARGET chip is triggered, which means that in these types of laser tests, the pulse always appears in the same position in the memory. Therefore, we did not expect the INL correction to have a large effect. Indeed our data analysis confirms this expectation.

One should add that the front end of the Target chip is slower than that of the WaveCatcher (see Fig.24). This may contribute to the better performance of the WaveCatcher in our tests.

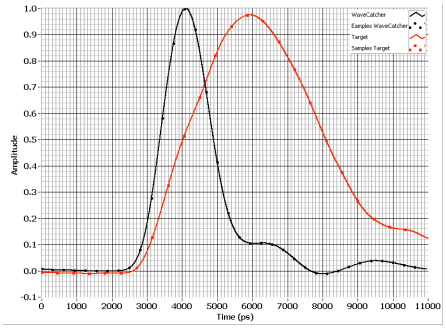


Fig. 24 Average pulse shapes of the pulses from the TARGET chip and WaveCatcher board (the same Hamamatsu amplifier used in both tests). Faster rise time of the WaveCatcher is due to its higher FE bandwidth – see Table 1. The detector amplifier is the same for both chips.

We propose a simple formula[11] for evaluation of the χ^2 method timing resolution with waveform sampling. Although one has 4-6 samples on the leading edge, only samples near peak have higher weight as the S/N ratio is highest. This probably explains why the χ^2 method is only slightly better than the CFD method.

CONCLUSION

We conclude that when MCP-PMTs are operated under the same conditions, waveform digitizing timing results using the WaveCatcher board are consistent with a combination of Ortec 9327CFD, TAC588, and 14bit ADC114 electronics. The TARGET chip results are worse due to (a) lower bandwidth and (b) a worse S/N ratio (see Table 1). We also conclude that a spline fit-based CFD method yields a worse result than all χ^2 timing methods with several reference pulses. Among various χ^2 timing methods, which use different portions of a pulse, the best timing resolution was obtained using timing based on the very beginning of the leading edge of the pulse. The CFD-based software algorithm is a very good candidate for future large-scale applications as it is much faster than the χ^2-method. Searching for a simple and fast algorithm without a spline fit, which would be suitable for implementation in an FPGA, we determine that finding a maximum and using linear interpolation between two samples already gives very good results (within ~8% of the best resolution limit).

The fact that we found waveform digitizing electronics capable of measuring timing resolutions similar to that of the best commercially-available Ortec CDF/TAC/ADC electronics is, we believe, a very significant result. It will help to advance the TOF technique in the future.

We should add that similar conclusions about the excellent timing possible with waveform digitizing techniques was shown in Ref.9, where the authors compared simulations with measurements using a 18GHz BW scope with 40GSa/s sampling.

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[11] Expected timing resolution with a χ^2 timing method with the waveform sampling is: $\sigma_t = 1/N\{\sum[\sigma_{noise}(i)/(dS/dt)_{thresh}(i)]\} \sim t_r\ 1/N\{\sum[1/(S_i/N_i)]\}$, where N is number of samples, $\sigma_{noise}(i)$ is the rms noise contribution from the i-th, $(dS/dt)_{thresh}(i)$ is the derivative of signal evaluated at each sample i, t_r is the pulse rise-time and S_i/N_i is a signal-to-noise ratio evaluated at the i-th sample. Therefore the rise-time t_r and S/N are crucial variables to get a good timing resolution.

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Table 1: Comparison of two waveform digitizers

Parameter	TARGET	Wave Catcher
Number of channels	16	2
Resolution	9 bits	12 bits(board) >12.5 bits (chip)
Conversion time	<500 ns/32 samples	100 ns/one sample
Termination	90 Ω, 1kΩ, 10kΩ	>50 Ω (board) > 1 MΩ (chip)
Power consumption	<10 mW/ch.	<2.5 W (board) <300 mW(chip)
Sampling rate	1-2.5 GSa/s	0.4 to 3.2 GSa/s
Sampling bin in this test	~450 ps/bin	312.5 ps/bin
S/N ratio in this test *	~50-60	~450
Chip's front end BW in this test	~150 MHz	500 MHz
Storage depth (samples/channel)	4096	256
Trigger rates	Up to 50 kHz	Up to 30 kHz
Encoding	Wilkinson	On board ADC
Cross-talk to nearest channel	~10% **	<0.5%
Readout time (ASIC->FPGA)	16 µs for 48/64 cells over 16 channels	~30 µs for 256 cells over the two channels
External interface	USB 2.0	USB 2.0

Note: * The noise is a baseline noise measured before the pulse. Signal is defined as the average of the signal peak.
** Large cross-talk is due to the inductive coupling in wire bonds.