OVERVIEW OF LIQUID ARGON FRONT END ELECTRONICS

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The ATLAS Liquid Argon Front End rad-tolerant electronics chain is described, and the main requirements that have led to today's architecture are discussed. Performance characteristics of the rad-soft prototype system, based on results obtained from about 6000 read-out channels installed in the test beam, are presented. During the past year, significant progress has been made in the transition to rad-tolerant electronics, which is based on a number of ASICs both in DMILL and DSM technology. Initial measurements on the prototype of the final version of the front-end board are presented.

1. Introduction

The LHC environment sets strong constraints on the ATLAS calorimetry and on its electronics. The very high energy and luminosity of LHC require a large number of channels with a large dynamic range and operating at high frequency. The Liquid Argon technique is used for all electromagnetic calorimeters (electromagnetic barrel and end-cap calorimeters, presampler and forward calorimeter) and the hadronic end-cap calorimeters adding up to a total of $\sim$180000 electronic channels to be read[1]. Common electronics is used everywhere except the very front-end where the HEC uses cold preamplifiers. This standardisation minimizes design effort and will facilitate maintenance.

Most of the elements of the system are now in the production phase and boards are ready to undergo the final tests. In this note, an overview as well as the status of the system are given.

2. Requirements

The signal delivered on the detector electrodes is a triangular shaped current with a fast rise time ($\sim$ 1ns), decreasing linearly to zero at the end of the

drift time of ionization electrons in liquid argon ($\sim$ 450 ns in a 2 mm gap at 10 kV/cm electric field). A typical value of the current is 2.8 μA/GeV for the EM calorimeters. This signal is delivered on the detector impedance which can be modeled, to a very good approximation, as a pure capacitance.

The main requirements for the read-out electronics can be summarized as:

- The dynamic range to be covered is as least of 16 bits as the energy to be measured can be as large as 3 TeV and the mean energy deposited in a single cell coming from pile-up interactions is of 50 MeV.
- The physics goals to be reached need a good energy resolution (for the electromagnetic calorimeters) $\frac{\sigma_E}{E} \sim \frac{10\ \%}{\sqrt{E}} \oplus 0.7\ \%$. In order to keep the constant term below 0.7 %, the contribution of the calibration to this term should be less than 0.25 % over the whole energy range.
- Since the energy of a cluster is the sum of many cells, the coherent noise over many cells should be kept small. It is required that the coherent noise per cell should be less than 5 % of the level of the incoherent noise.
- Cells should be summed in trigger towers of granularity $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ and the result sent to the Level-1 processor.
- The read-out system should sample at 40 MHz; to this end a pipeline with a depth of at least 2.5 μs should be provided; in addition a large derandomizing buffer and a fast read-out should allow for a maximum Level-1 trigger rate of up to 75 kHz.
- Since the system will be located in a region of limited access, it needs to be highly reliable. In addition, although radiation levels at that location are not very large (10^{12}n/cm^2/yr; 10^{10} ionizing particles/cm^2/yr) the electronics needs to be radiation tolerant. A number of ASICS (Application Specific Integrated Circuits) have been designed in DMILL and DSM rad-tolerant technologies.

3. System Design

In Figure 1 a schematic view of the front-end and read-out electronics is shown. This figure shows the logical flows of information and the different boards with the important components. The sensitive analog electronics is on detector, in a front-end crate (FEC) attached to the cold to warm feedthrough. This crate is on top of the warm feedthroughs, in the crack between the barrel and the end-cap to provide an extension of the cryostat Faraday cage. This should protect the readout electronics against external electromagnetic radiation and minimize pick-up noise. In addition, this location keeps the warm part of the signal and calibration cables to a minimum length, minimizing the associated

attenuation and noise. The front-end crate houses the following type of boards:

- The Front-end board amplifies and shapes the analog signals, sums cells within layers to prepare the input for the tower builder board, stores the signals in analog memories waiting for the Level-1 trigger decision, digitizes the selected pulses and transmits the digital results on optical fibers.
- The Calibration board generates pulses with a precision of 0.2 %;
- The Trigger Builder board does the final analog summation of the different layers in depth to form trigger towers and to transmit the analog signals to the Level-1 cavern for digitisation and processing.
- The Control board receives and distributes the 40 MHz clock, the Level-1 accept signal and other signals to configure and monitor the boards in the crate.

The limited space in the FEC constrains the access and power dissipation and cooling. As already said, radiation levels at that location are not very large however the electronics needs to be radiation tolerant. ATLAS has defined standard Radiation Tolerance Criteria (RTC) that all components need to pass in order to qualify. The criteria are defined taking into account the expected dose after 10 years of LHC running increased by a large safety factor. These doses in the FEC are the following:

- NIEL (non ionizing energy loss) test with neutrons at the level of 1–3.6 10^{13}n/cm^2;
- TID (total ionising dose) test with X-rays with a dose of 50 to 330 krad, depending on the component to be tested;
- SEE (single event effects) at the level of 7.7 10^{11}h/cm^2/yr;

4. Front End System

4.1. *Front End Board*

The Front End Board deals with 128 channels in 16 groups of 8 channels. Each group contains 2 four-channel preamplifiers, 2 four-channel shapers, 2 twelve-channel analog memories (SCA, Switched Capacitors Arrays) and one 12-bit ADC.

The preamplifiers amplify signals above noise level. They need to accept the whole signal dynamic range ($\geq$16 bits) and deal with high speed inputs requiring them to have a low input impedance. There are two types of preamplifiers. The warm bipolar hybrids preamplifiers (electromagnetic calorimeter) are more than 50 % produced and the overall noise performance is $e_n = 0.4$ nV/$\sqrt{\text{Hz}}$;

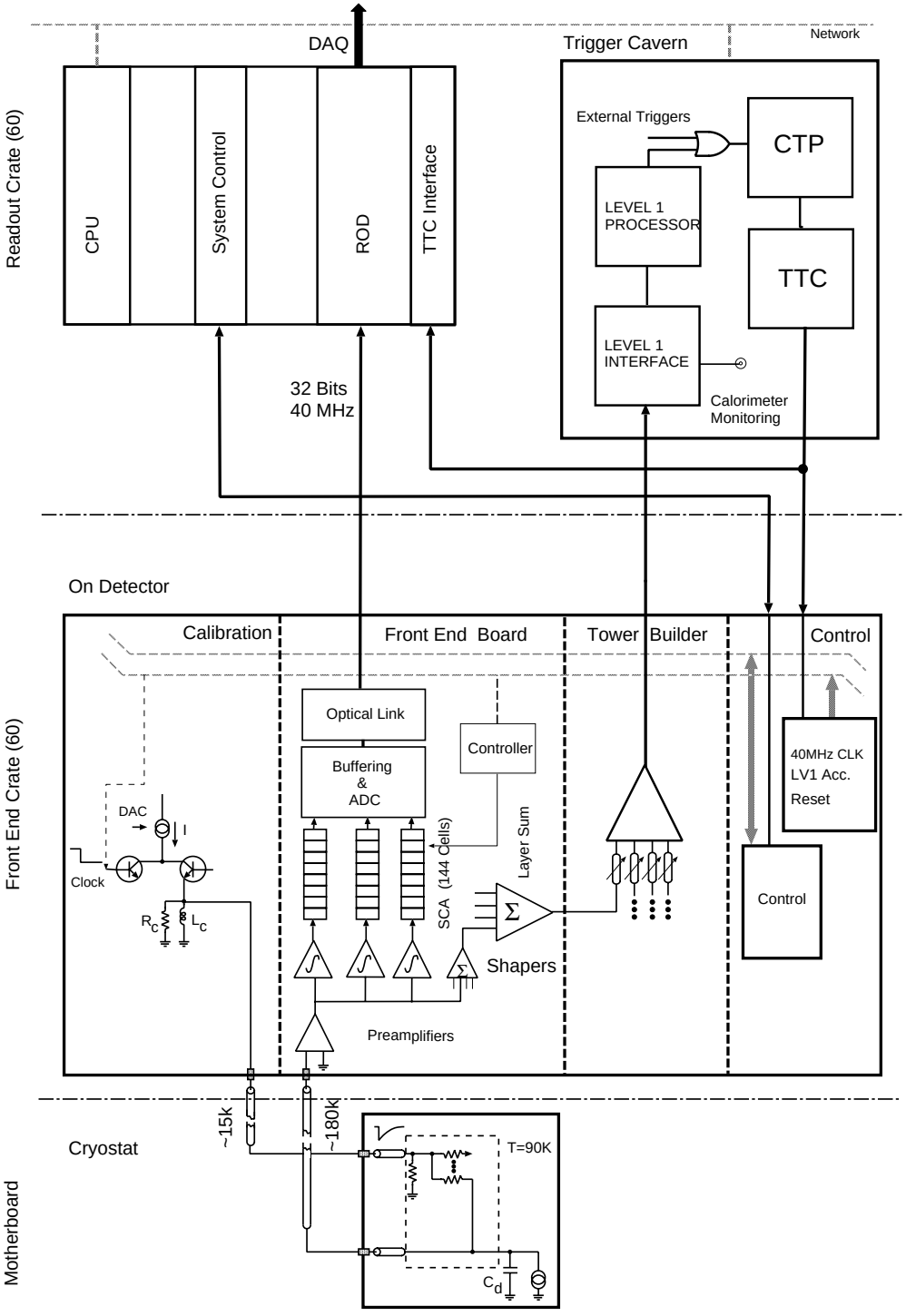

Figure 1. Block diagram of the front-end electronics. The drawing shows warm preamplifiers in the front-end board which are present for the electromagnetic and forward calorimeters. For the hadronic end-cap calorimeters, the preamplifiers are located in the liquid argon.

i_n = 6 pA/$\sqrt{\text{Hz}}$. For the cold Ga As monolithic HEC preamplifiers the production and testing is now completed giving a yield of 84 %. The circuits have been tested up to 3 kGy and 10^{14} N.

The AMS bipolar shapers (rad tolerant by design) limit the system bandwidth to match the 40 MHz sampling frequency. A bipolar filter CR(RC)^2 is adopted to remove the signal tail and limit the bandwidth. In order to optimize the electronic noise and the pile-up noise at high luminosity of the LHC, the time constant (τ = 13 ns) has been optimized to minimize the total noise. In order to achieve a 16 bit dynamic range in a linear scale, 3 ranges are used to split the dynamic range. The noise is of 390 μV for the medium gain (850 and 250 μV for the high and low gain). The integral non-linearity has been measured to be less than 0.2 %. The full production is now completed.

Signals from the shapers are stored in a circuit using Switched Capacitors Arrays (SCA). The SCA chip contains 16 analog channels. Among them, 12 are used to store the signal coming out from the shaper; the 4 others store a reference level. During the read-out operation, an off-chip amplifier subtracts the closest reference channel from each signal channel. This offers a noise rejection ratio improvement larger than a factor 4 during the simultaneous read and write operations of the chip. Two prototypes of the circuit were carried out: a CMOS version intended for the test beam electronics and the final version in DMILL technology. The performances of both prototypes have been measured on test bench and are summarized in Table 1. The DMILL chip was irradiated with 3 kGy and 2 10^{13}N/cm^2. No measurable change was observed after both irradiations.

The analog pipelines are followed by a 12bit 5 MHz ADC (AD9220)[a] which digitizes the output of two SCA after a level 1 trigger. The gain of the signal is either chosen automatically by the hardware (free gain) or the digitization of one, two or three gains can be programmed.

4.2. *Calibration Boards*

The calibration boards are in charge of generating 0.1 % precision pulses. In order to minimize the spurious injected charge, a static low-offset (10μV) operational-amplifier has been developed. The DAC is in rad hard DMILL technology. The uniformity has been measured to be 0.11 % and the crosstalk

[a] Analog Devices, 1 Technology Way, Norwood, MA 02062, USA

Table 1. Summary of the measured SCA performances.

Noise	300 μV
fixed sequence noise	< 0.2 μV
dynamic Range	13.3 bits
cell to cell variation	$< 0.02\%$
drift	< 3mV/ms
integral non linearity	$< 0.1\%$

less than 0.1 % as can be seen from Figure 2. The board has undergone irradiations up to level of 2 kGy and 10^{14} N.

4.3. *Tower Builder Board*

The Tower Builder Board is in charge of the analog summation of the different depth layers to form the trigger towers. Before summing the signals from different layers, the peaking times need to be adjusted by correction poles and the gains need to be normalized. In order to have accuracies of a few ns in time and a few % in amplitude, a good prediction of the components is needed, implying a good knowledge of the electronic chain and of the detector. To align the pulses, very specially designed programmable delays lines are used. The noise per trigger tower at the output of the trigger chain has been measured to be $\sim$ 300 MeV and the saturation behavior is understood and within requirements. The board has been irradiated with 2 kGy and $3\,10^{13}$ N. The boards are now validated for production.

4.4. *Controller Board*

The Controller Board loads, updates and checks the different registers and parameters for all the different front-end boards. A special 10 Mb/s bus has been designed, the SPAC bus, with read and write lines doubled for safety. The final boards will be ready in October 2002.

4.5. *Optical link*

The optical link will transfer the Front End Board data to the Read Out system. The chosen link is the HP Glink, a radiation resistant Gigabit ethernet speed digital Optical link. A lot of effort has been put in developing a system with a low error rate[2]. Extensive radiation studies were performed with irradiations of 3 kGy and $5\,10^{13}$ N. The single event effects were of 0.47 bit flip per link and per hour which corresponds to 8 hours of dead time in 10 years of LHC running.

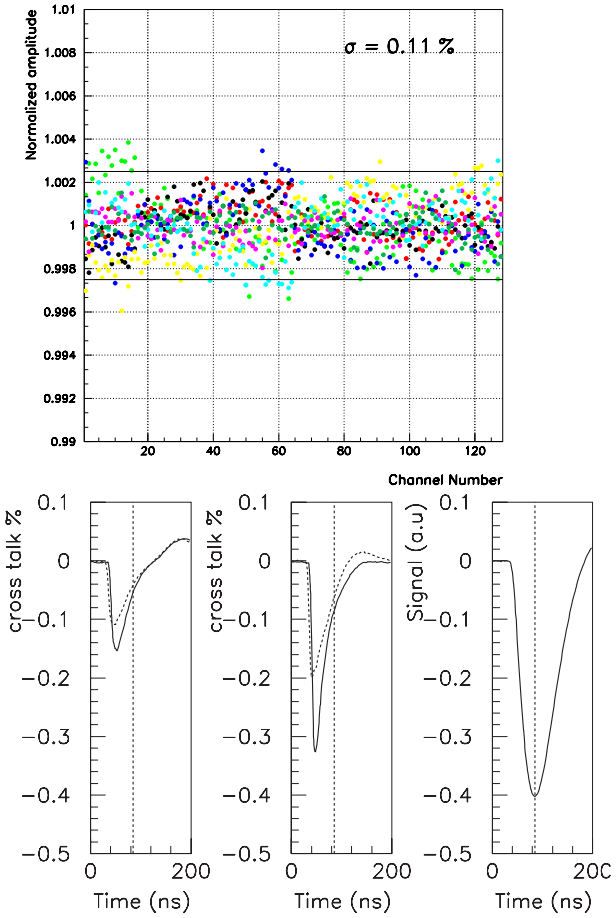

Figure 2. The top plot shows the amplitude of the calibration pulse for the 128 channels. The different colors show the 11 tested boards. The bottom plot shows the pulsed channel in arbitrary units (most right), the response in the neighbor (center) and the next to neighbor (left). The pulses are shown with a vacuum cable (full lines) and with no vacuum cable (dashed lines).

5. Test beam results

Final electronics have been tested on test beam during the past two years. For the electromagnetic calorimeter one pre-series module and 4 series mod-

ules have been tested with final electronics using 6000 channels, 50 front-end boards, 12 calibration boards and 1 Tower Builder Board. The boards have all functionalities but are not completely rad-hard. The noise per standard electron cluster has been measured to be 140 MeV (high gain) and 240 (medium gain). The coherent noise is $\sim 5-7\%$ and the power dissipation 0.7 W per channel. The automatic gain selection has been tested (the lower threshold only since the electron energy is limited to 245 GeV) and is behaving as expected. Full test beam results can be found elsewhere in these proceedings[3].

For the Hadronic End Cap 12 pre-series modules and 24 series have been tested on test beam using 400 cold channels[4,5].

6. Conclusion and perspectives

The successful use of more than 6000 front-end channels in test beam with full functionalities show the validity of the technical choices and have proven that the prototypes fulfill the required specifications (except for radiation criteria).

A test of the full system crate with final radiation hard boards is scheduled for the fall 2002. This test will provide further measurements (coherent noise, system stability, timing jitter...) qualifying the system for the production phase.

The next major steps are expected for April 2003 with the production of the 1650 FEBs, in October 2004 with the complete assembly and finally, installation is scheduled in February 2005.

Acknowledgments

I would like to thank the organisers and staff of CALOR02 for the nice atmosphere of the Conference. Thanks to P. Borgeaud and B. Mansoulié for their help preparing this talk and for the careful reading of this note.

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