Monolithic Active Pixel Sensors With In-Pixel Double Sampling Operation and Column-Level Discrimination

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***Abstract*—Monolithic active pixel sensors constitute a viable alternative to hybrid pixel sensors and charge coupled devices for the next generation of vertex detectors. Possible applications will strongly depend on a successful implementation of on-chip hit recognition and sparsification schemes. The task is tough, first because of very small signal amplitudes ($\sim$ mV), which are of the same order of magnitude as natural dispersions in the transistor threshold voltages, secondly because of the limitation to use only one type of transistor over the sensitive area. This paper presents a 30×128 pixel prototype chip, featuring fast, column parallel signal processing. The pixel concept combines in-pixel amplification with double sampling operation. The pixel output is a differential current signal proportional to the difference between the reference level and the charge collected. The readout of the pixel is two-phase, matching discrimination circuitry implemented at the end of each column. Low-noise discriminators feature autozero functionality.**

The details of the chip design are presented. Difficulties, encountered in the first attempt to address on-line hit recognition, are reported. Performances of the pixel and discriminator blocks, determined in separate measurements, are discussed. An important part of this paper consists of results of first tests performed with soft X-rays from a ^{55}Fe source.

***Index Terms*—APS, CMOS APS, double sampling, image sensors, particle detector, pixel detectors, system-on-chip.**

I. Introduction

BECAUSE of physics requirements, the need of precise vertex measurements makes a high-resolution vertex detector (VXD) an essential part of the experiment apparatus. One of the options considered for VXD construction in a future linear collider is a monolithic active pixel sensors (MAPS)-based detector. The ability of MAPS realized in a CMOS process, to provide charged particle tracking has been demonstrated with the Minimum Ionising Particle Mos Active Pixel Sensor (MIMOSA) chips family (see, e.g., [1]. The results were obtained on a series of small scale and 1 million pixel large prototypes that were designed exploiting a classical three-transistor (3T) pixel configuration.

The use of MAPS in particle physics [2] will strongly depend on a successful implementation of an on-chip hit recognition and sparsification scheme. This is not a trivial task, because of very small signal amplitudes, in the range of millivolts, which are of the same order of magnitude as transistor threshold variations of a CMOS process. The solution consisting in storing of reference values for each pixel is impracticable, because of waste of active area due to the large memory required. Therefore, the correction for offset, performed during every access to the pixel, has been adopted. The offset correction, called calibration, consists in reading empty data from the analog readout, including the pixel circuitry, chain with a short-circuited input. A new column-based, low power, offset compensated (autozeroed) multistage comparator has been developed completing the pixel design [3]. A planned final detector would include an array of identical pixels with their addressing, signal processing within the chip, sparsification, and data transmission circuits. The design of the MIMOSA VI chip, focusing the interest of this paper, is a first step toward construction of high performance detection system integrated on chip. Additionally, the fabrication goal of the MIMOSA VI chip was to test the possibility of the in-pixel sampling and storing signals from two different time slots. This could be the first step for further extension of the number of memory cells aiming at multiple and fast signal sampling during the train time in the collider.

II. Pixel Design

Novel ideas, optimizing charge sensitive elements (CSEs) for a vertex detector environment and new pixel configurations with signal amplification and double sampling operation, have been recently proposed [4]. In this new CSE, the charge generated in the lightly doped, undepleted volume is collected by the n-well/p-epi (n-well/p-sub) diode, as it was proposed for 100% fill factor devices in visible light applications [5]. The reverse bias is provided in a continuous way via a $\mathrm{p}^{++}/\mathrm{n}-\mathrm{well}$ diode. This one is forward biased with a leakage current of

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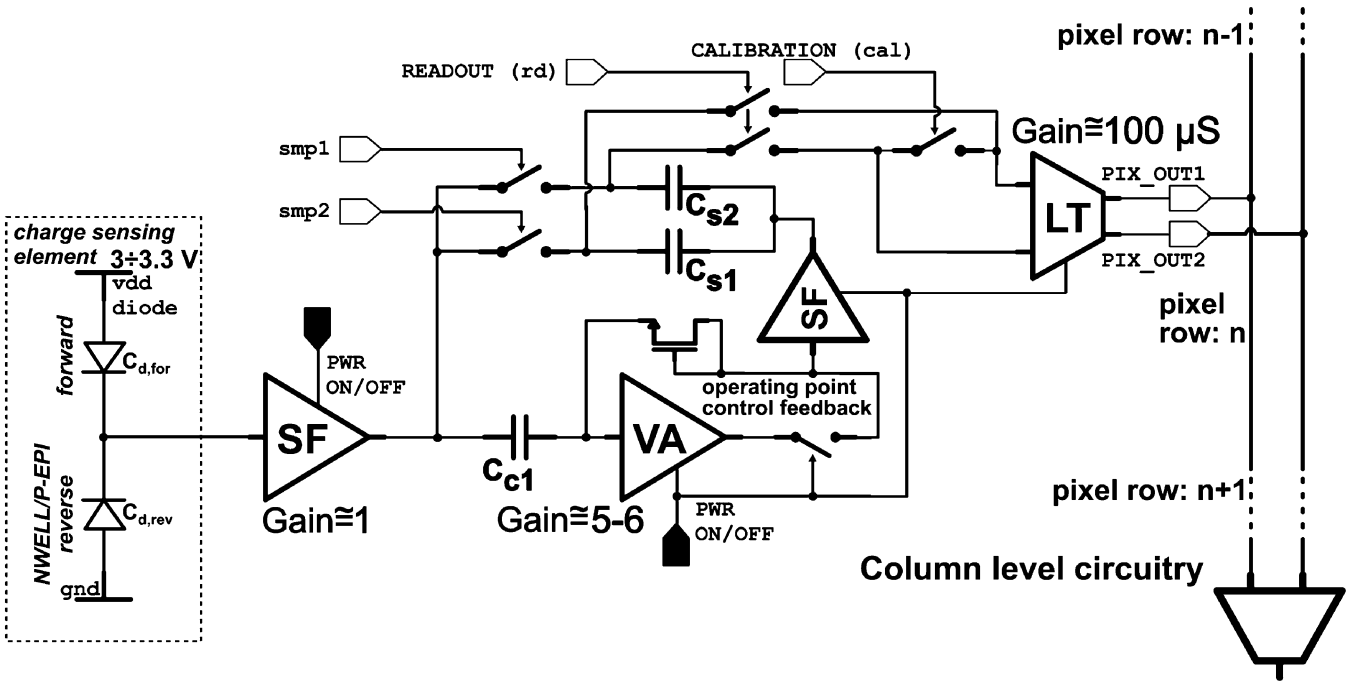

Fig. 1. MIMOSA VI pixel concept based on autoreverse polarization of charge collecting diode, where SF, VA, and LT stand for source follower, voltage amplifier, and linearized transconductance pair, respectively, and the column level circuitry includes signal discrimination and multiplexing of resulting signals.

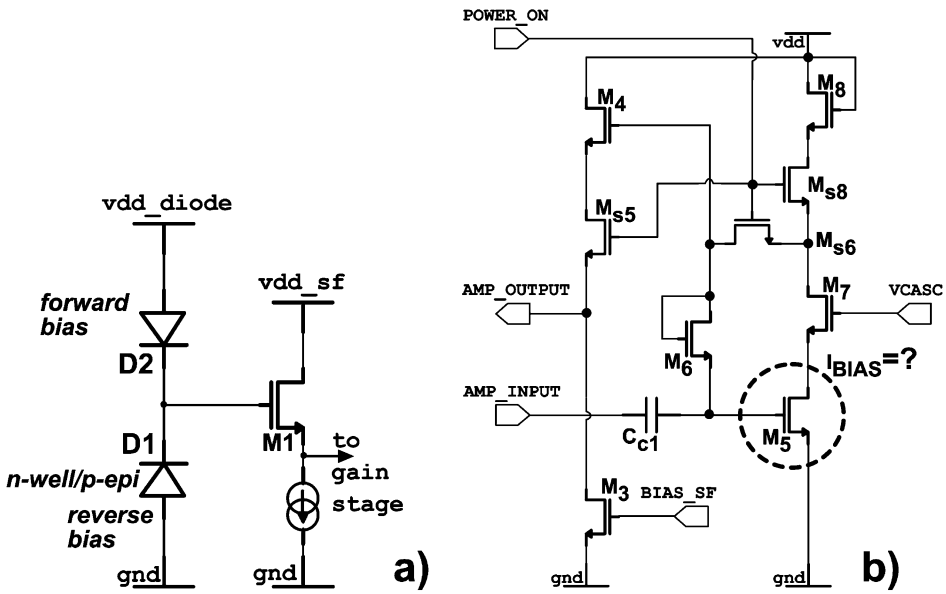

Fig. 2. Schematic diagrams: the charge sensitive element with auto-reverse polarization (a), all NMOS in-pixel amplifier (b) (storage capacitors, placed in the feedback path of the amplifier, are not shown).

the charge collecting diode. The temporal response of CSE is leakage current independent. CSE is ac-coupled to all NMOS transistor amplifiers featuring the voltage gain of five to six. This is a switched power amplifier, optimizing power consumption of the chip. The block diagram presenting the pixel concept is sketched in Fig. 1. The double sampling operation is achieved using two storage capacitors, C_{s1} and C_{s2}, placed in the feedback path of the amplifier. The ac-coupling capacitor is C_{c1}. The output stage of the pixel is built with a linearized differential stage with a transconductance of 100 μS, providing differential output current.

The calibration and offset cancellation of the analog chain is achieved by short-circuiting the input of the differential stage. The schematic diagrams of the charge sensitive element and of the in-pixel amplifier are shown in Fig. 2.

III. Comparator Design

A single comparator is shared by all pixels in one column with the pixel outputs switched sequentially to the front-end of the comparator. The simplified architecture of the offset compensated comparator developed is shown in Fig. 3. The width of

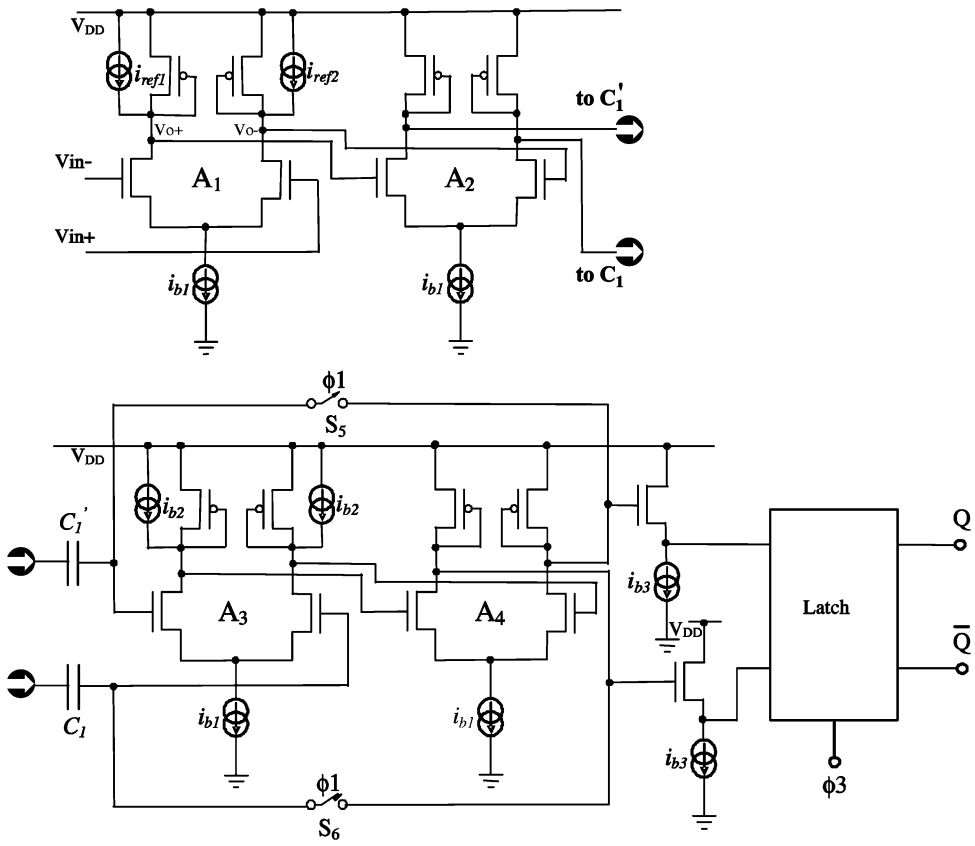

Fig. 3. Schematic diagram of the offset compensated comparator.

the comparator, achieved in a careful layout design, matches the 28 μm pixel pitch. To speed up the comparator, each gain stage is realized using two cascaded low gain amplifiers shown at the top of Fig. 3. The two output source follower buffers are used to reduce the kickback effects of the latch. All the switches are realized using PMOS transistors, with corresponding dummy switches reducing charge injection. The reference levels, necessary for the threshold voltage settings, are injected in form of currents $\mathrm{i_{ref1}}, \mathrm{i_{ref2}}$, as shown in Fig. 3. The comparator has a fully differential architecture, allowing improvement of power supply rejection ratio, reduced substrate coupling problems, and charge injection in switches.

The timing diagram for the comparator is inscribed into the readout sequence of the pixel. Its simplified form is presented in Fig. 4. During τ_1 (*CALIBRATION* phase), the threshold level (proportional to $\mathrm{i_{ref1}}-\mathrm{i_{ref2}}$), after conversion from current to voltage, is amplified and stored in the capacitors $\mathrm{C_1}$ and $\mathrm{C_1'}$. The pixel offset voltage is applied on the gates of the input amplifier and the amplified value is stored in the capacitors together with the amplifier offsets for later correction. The transistors of current sources shown in Fig. 3 normally deliver $\mathrm{i_{ref1}}$ and $\mathrm{i_{ref2}}$ currents which are of different values, defining the threshold level. During τ_3 (*READOUT* phase), currents $\mathrm{i_{ref1}}$ and $\mathrm{i_{ref2}}$ are made equal, allowing subtraction of mismatches. The amplified input signal is then compared to the threshold level and the resulting logical state is latched.

The output current of the pixel is converted back to voltage at the input of the comparator by means of two triode-region-operated transistors, not shown in Fig. 3, with gate voltages imposed from outside of the chip. Thus, the conversion factor, referred to the input of the comparator, is adjustable and varies from $10\mu\mathrm{V/e^-}$ to $100\mu\mathrm{V/e^-}$.

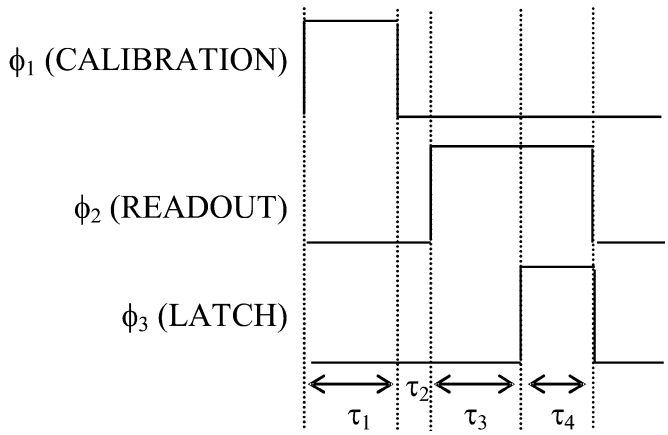

Fig. 4. Timing for the comparator, τ_1-calibration phase, τ_2-dead time between calibration and readout/comparison, τ_3-comparison phase, τ_4-result latch.

Four different designs of discriminators, i.e., T0, T1, T2, and T3, were implemented on the MIMOSA VI chip for genuine test purposes. T0 and T1 have identical designs[1] based on four differential stages of gain and a dynamic latch; T2 comprises three differential gain stages and a dynamic latch, while T3 features a static latch. Separate test results of T3 can be found in

[1]Identical comparators T0 and T1 allow observing the mismatch between them.

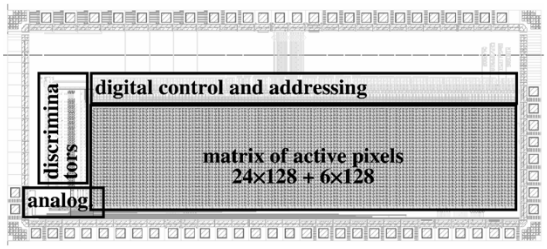

Fig. 5. Layout of the MIMOSA VI prototype.

TABLE I
MAIN PARAMETERS OF THE MIMOSA VI CHIP

MIMOSA VI				features		
performances of chip designed				noise ENC: ~20 e⁻, conversion gain: 6.5 nA/e⁻ pixel pedestal variations: ~120 e⁻		
discriminator performances						
τ_1 ns	τ_2 ns	τ_3 ns	τ_4 ns	noise inp.ref.	offset inp. ref.	power
90	15	45	30	~85 μV_{rms}	negligible	~200 µW
75	12.5	62.5	25	~100 μV_{rms}	~300 µV	~200 µW
60	15	45	30	~100 μV_{rms}	~800 µV	~200 µW

[3]. The layout dimensions of the comparators T0 and T1 are 28×300 μm^2.

IV. MIMOSA VI CHIP DESIGN

The MIMOSA VI chip, fabricated in a 0.35 μm CMOS process with 4.2 μm epitaxial layer, features an array of 30×128 pixels, where 24 columns are connected to the discrimination stages for binary readout and the remaining six columns are connected, via simple current amplifiers, directly to output pads. The latest makes access to the analog data possible. The pixel pitch is 28 μm and pixels with two diode sizes, i.e., 4.0×3.7 μm^2 (3.5 fF) and 5.0×4.7 μm^2 were designed. The layout of the prototype is shown in Fig. 5. The clock frequency used to drive the matrix of pixels is 30 or 40 MHz, depending on whether the readout of a single pixel is done in the mode with six or eight clock cycles, respectively.

V. ESTIMATION OF CHIP PERFORMANCES

The chip has been extensively tested. The electrical performances of constituent blocks were examined independently, i.e., pixels in the subarray, for which direct analog outputs are available, and the comparators in the test structures, placed aside the main array. The tests of the whole systems, comprising the discrimination stages and array of pixels, were not performed, due to unexpected pixel-to-pixel pedestal variations. The dispersions, which were referenced to the equivalent input signal of one hundred and a few tens of electrons equivalent noise charge (ENC), were observed despite subtraction of the reference value. The qualitative description of dispersions and the analysis explaining their origin are discussed in the following sections. The summary of estimated chip parameters is given in Table I.

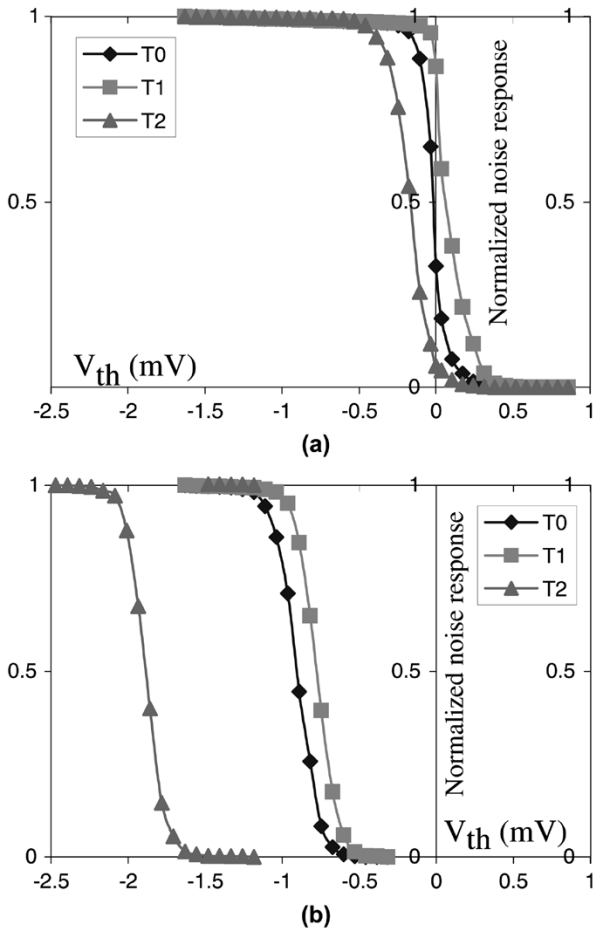

Fig. 6. The normalized noise response of the comparators versus threshold voltage with the inputs at the same reference voltage. (a) $f_{ck} = 33$ MHz, $\tau_1 = 90$ ns, $\tau_2 = 15$ ns, $\tau_3 = 45$ ns, $\tau_4 = 30$ ns and (b) $f_{ck} = 33$ MHz, $\tau_1 = 60$ ns, $\tau_2 = 15$ ns, $\tau_3 = 45$ ns, $\tau_4 = 30$ ns.

A. Discriminating Stage

The functionality of comparators was studied with a clock of up to 80 MHz. The residual offset below 1 mV was achieved with a clock frequency of 40 MHz. This translates to an effective 5 MHz frequency for the full processing. The power consumption was measured to be in the order of 200 μW at 40 MHz. The design goals for discriminators were met. Two examples of the normalized noise response of the comparators, measured for different timing conditions versus threshold voltage, are shown in Fig. 6. The curves plotted in Fig. 6 allow calculating the temporal noise taking their derivatives. Its value is below a few hundreds of microvolts rms referred to the input. It was shown that the precision of the calibration depends strongly on the calibration time τ_1. This is due to relatively large storing capacitors C_1 and C_1' (400 fF) (see Fig. 3), which have to be charged. Therefore, reducing τ_1 leads to an increase of the residual offset, which remains below 1 mV as long as τ_1 is above 60 ns. The definitions of τ_2, τ_3, and τ_4 are given in Fig. 4.

B. Pixel

The pixel performances were simulated using the integrated simulation environment under CADENCE, while the temporal noise has been examined in the time domain with

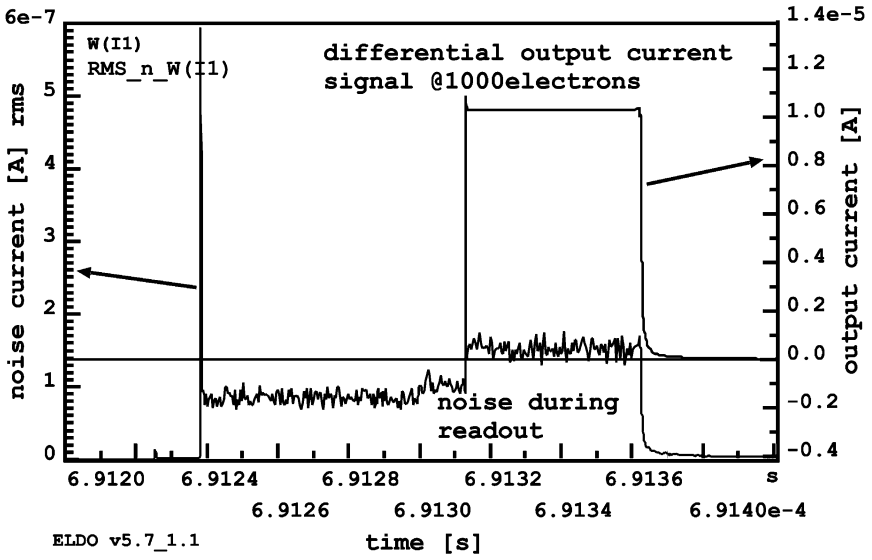

Fig. 7. Differential current rms noise during a pixel readout cycle (left axis), for a differential current signal (right axis) corresponding to 1000 e^- collected.

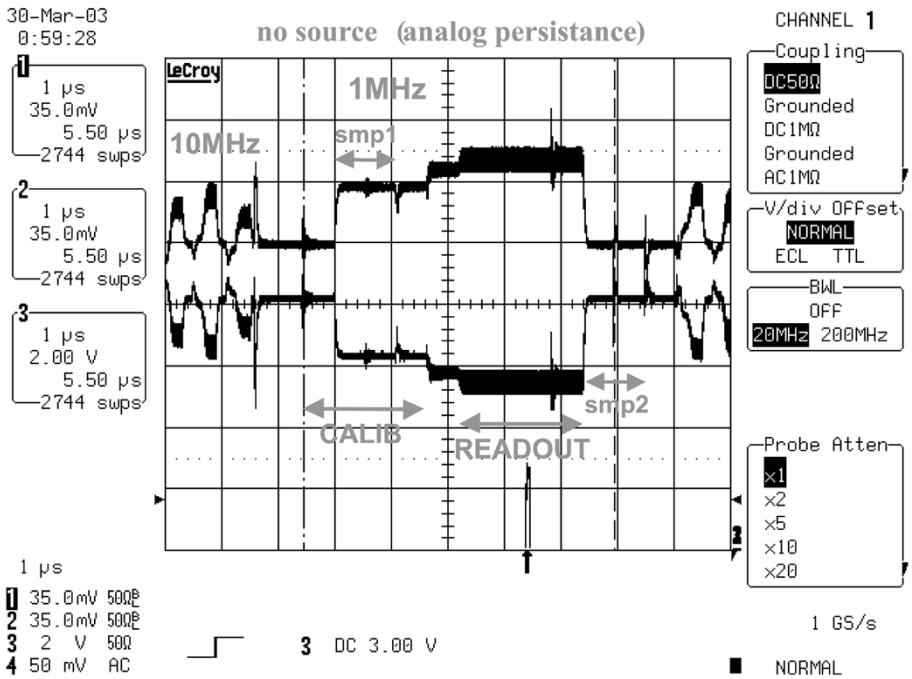

Fig. 8. Oscilloscope view of the raw output from one column of pixels.

the ELDO simulator. The results of noise simulation are shown in Fig. 7. The plots show differential current rms noise during a pixel readout cycle and the differential pixel output current corresponding to the collection of 1000 e^- on the n-well/p-epi diode. The pixel sensitivity in the order of 10 nA/e^- and an average noise value of 152 nA (rms) corresponding to $\sim$15 e^- ENC during the *READOUT* phase were simulated. The noise level estimated in the transient noise simulations with ELDO can be compared with the measured value presented in Table I.

The pixel parameters were estimated in tests of the six columns of pixels with the analog outputs directly available. The tests were performed at a readout clock frequency of 10 MHz, which was limited by the readout circuitry external to the chip. Fig. 8 shows an oscilloscope view of the raw output from one column of pixels. The differential current was converted to voltage on two 825 Ω resistances and the resulting signal amplified by a factor of five.

Two waveforms in Fig. 8 correspond to the difference of currents transmitted in a differential mode to the data acquisition system, where analog-to-digital converters (ADCs) were seated.

The waveform shows access to the consecutive pixels. The access to the pixel presented in the central part of Fig. 8 was slowed down to 1 MHz of clock frequency, allowing distinguishing respective phases [2] during the access to the pixel. The smp1 time is used to store a new value of signal on one of the sam-

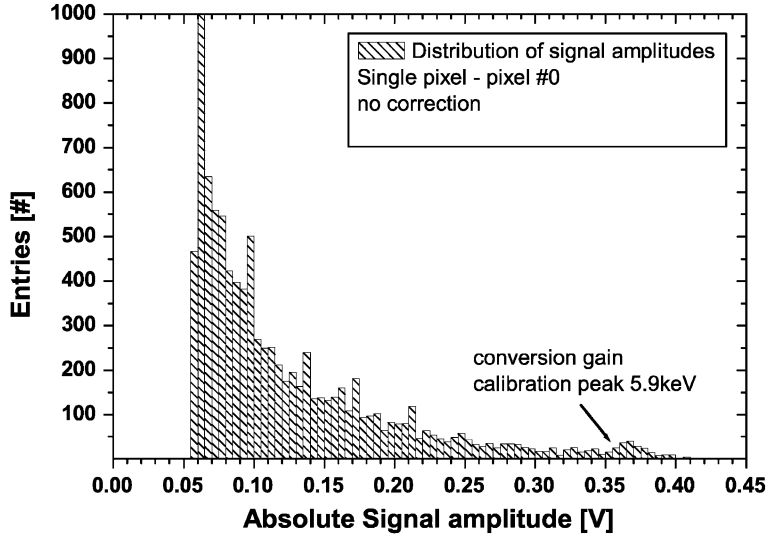

Fig. 9. Hit histogram for a single pixel exposed to a ^{55}Fe source.

pling capacitances. The sampled signal is subtracted from the reference signal taken during the smp2 phase of the precedent readout cycle.

The detection performances of the MIMOSA VI chip have been first assessed with soft X-rays by exposing the chip to a ^{55}Fe source. The tests were performed on individual pixels, selected randomly from the matrix. The measurements lead to the estimation of the pixel conversion gain. An example of the hit histogram measured on a single pixel is shown in Fig. 9.

The test setup was based on two synchronized VME data acquisition cards (DACs) working in parallel. The cards, equipped with four fast ADC channels each, allowed acquiring signals from the six analog outputs available on the chip. The DAC card is equipped with a set of configurable digital inputs/outputs. One of them was used to set the digital readout pattern. The programming sequence was delivered to the chip together with the readout clock and the reset signal.

The test setup with DAC cards was primarily used in tests aiming at estimation of pixels parameters like pedestals, noise, and their variations between pixels. However, a digital 8-bit oscilloscope was used in tests with the X-ray source. The choice was dictated by the poor hit statistics per single pixel due to the relatively fast readout. A simple LabView based program, allowing connection to the oscilloscope, was used for on-line selection and storing on disk only those events with signals above specified threshold level. The system was triggerless, i.e., the readout was running continuously with the full frame readout time, also referenced as a detector integration time, of 77 μs.

The efficiency in reducing pixel-to-pixel pedestal variations, using calculation of signals difference between the *READOUT* and *CALIBRATION* phases was demonstrated. Fig. 10(a) and (b) presents distributions of signals sampled during both phases of the access to the pixel. Next, Fig. 10(c) and (d) shows the distributions of the calculated difference and of the variance of the difference, respectively. The units used are ADC units. The value of pixel-to-pixel pedestal variations amounts to $\sim$160 ADC units before taking difference between both signals and drops to $\sim$19 ADC units after. The average pixel-to-pixel pedestal variations are thus suppressed more than five times. However, the residue is still nonnegligible, translating to $\sim$100 $\mathrm{e}^{-}(1\sigma)$ of an equivalent input signal. Unfortunately, the nonfully compensated dispersions hampered the possibility of setting the comparator threshold level in a common way for all pixels from one column. The average level of noise over the whole matrix of pixels amounts to $\sim$3.5 ADC units ($\sim$20 e^{-} ENC) after subtraction of signals for the *CALIBRATION* and *READOUT* phases.

The observed pixel-to-pixel pedestal variations required more detailed theoretical and simulation studies. However they could not be reproduced in Monte Carlo SPICE simulations using available models of mismatch variations. Important observation from these analyses was the fact that the variation of the parameters of active components does not give rise to the dispersions observed.

VI. Study of Pixel-to-Pixel Pedestal Variations

The device modeling and layout extraction rules provided by the design-kit, used for the chip design, were too limited to allow tracing down the origins of the observed dispersions.[2] After excluding the mismatches of active components in Monte Carlo SPICE simulations, the rise of dispersions has been attributed to the variation of parasitic capacitances. These interline and line-to-substrate capacitances (metal–metal, metal–floating diffusion, metal–poly) introduce coupling between lines with switching signals and sensitive nodes of the circuit. Modeling parasitic couplings is extremely difficult: first, due to the mentioned incompleteness of the extraction model; secondly, parasitic capacitances, influencing pixel behavior, barely exceed a few tens of aF. The modeling is a very subtle task, since the

[2]For example, extraction of parasitic capacitances to POLY2 was not included in the design-kit.

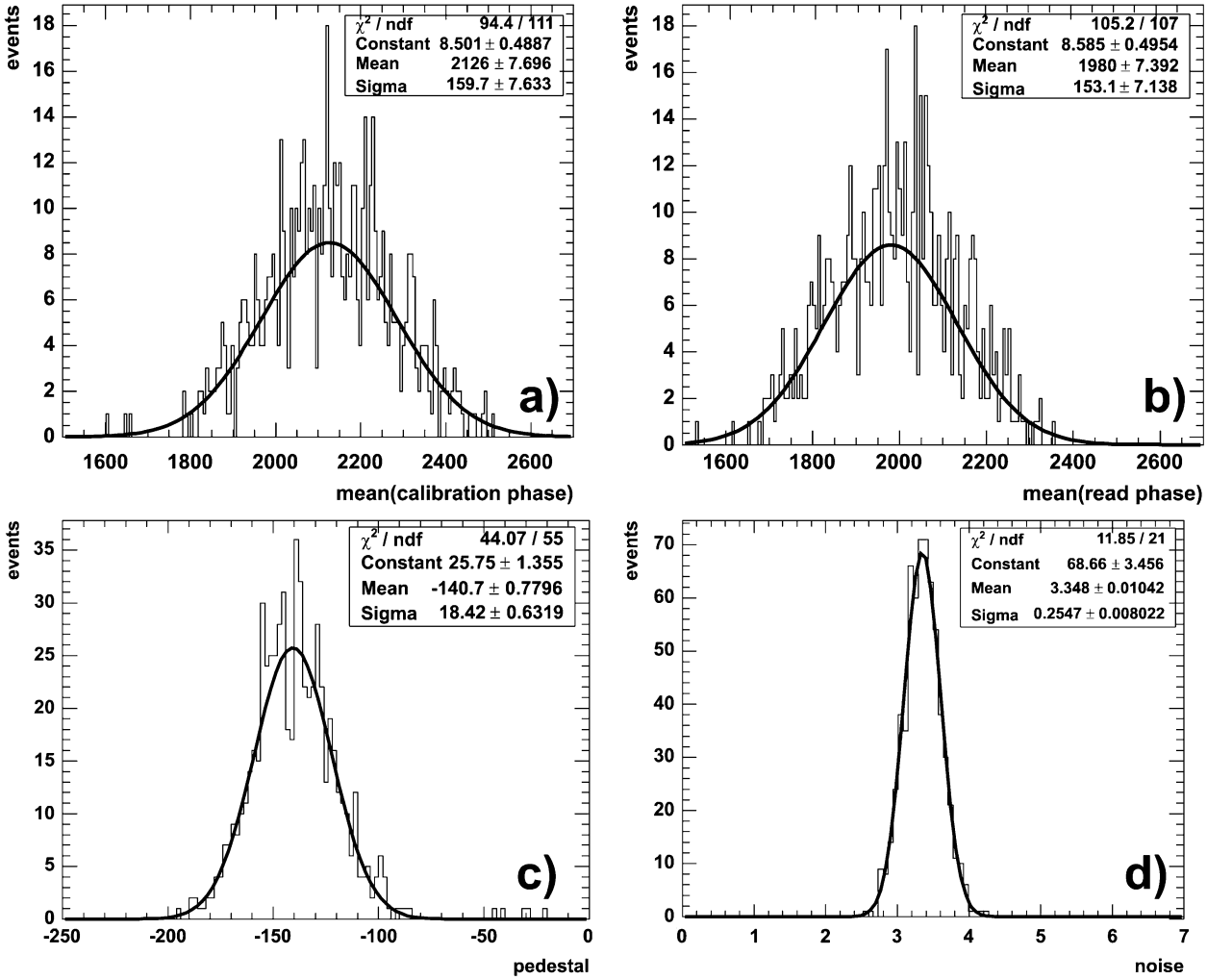

Fig. 10. Distributions of signals sampled during the (a) *CALIBRATION* and (b) *READOUT* phases and (c) of the resulting difference, and (d) the mean variance of the difference signal (all expressed in ADC units without absolute signal calibration).

variations of parasitic capacitances are unknown and difficult to estimate. An "intuitive" approach was applied to carry out parasitic coupling analyses.

Applying this "intuitive" approach, the effects observed in tests could be reproduced and the quantitative results were compatible with the measurements. As an illustration of the analysis, Fig. 11 shows an example of possible parasitic coupling with digital lines within the pixel area. The sensitive nodes are terminals of the two sampling capacitors C_{s1} and C_{s2}.

The excerpt of the pixel layout, illustrating the situation depicted in Fig. 11, is shown in Fig. 12. The layout was designed in a careful symmetrical way, but variations in parameters, like isolation oxide thickness or metal line width, perturbate this symmetry, resulting in signal dispersions.

The results of the transient simulations of signal dispersions due to coupling through the sets of different parasitic capacitances are shown in Fig. 13. The figure displays four chosen plots of the differential output current of a single pixel considering different coupling ways. Fig. 13(a) shows the influence of the parasitic coupling capacitances for their nominal values, estimated from the design kit, when added consecutively into the

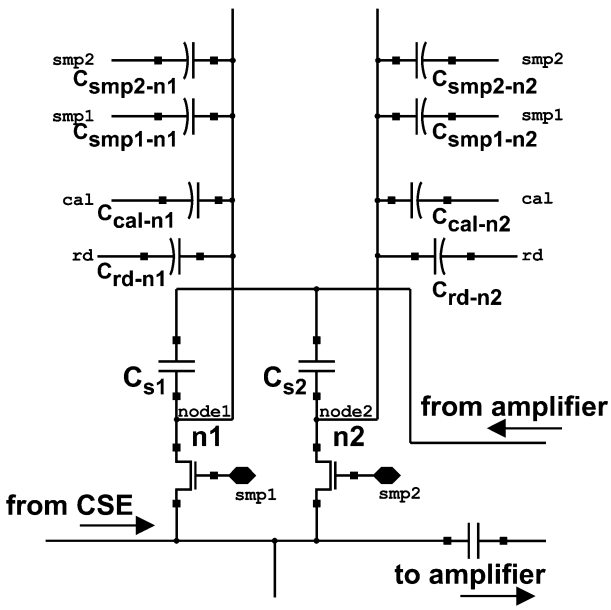

Fig. 11. Example of parasitic coupling with digital lines within pixel.

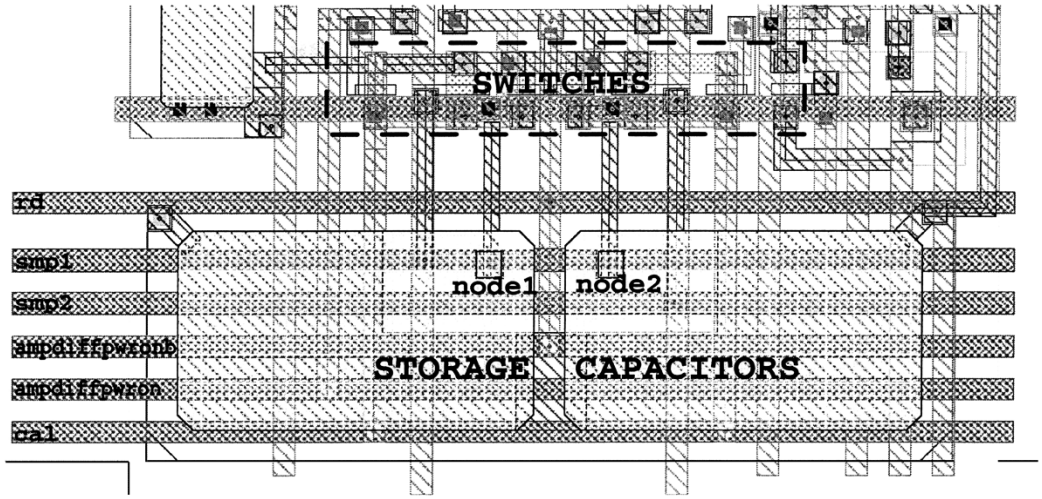

Fig. 12. Part of the pixel layout showing storage capacitances, sampling switches, and digital control lines passing over sampling capacitances, corresponding to the schematic view shown in Fig. 11.

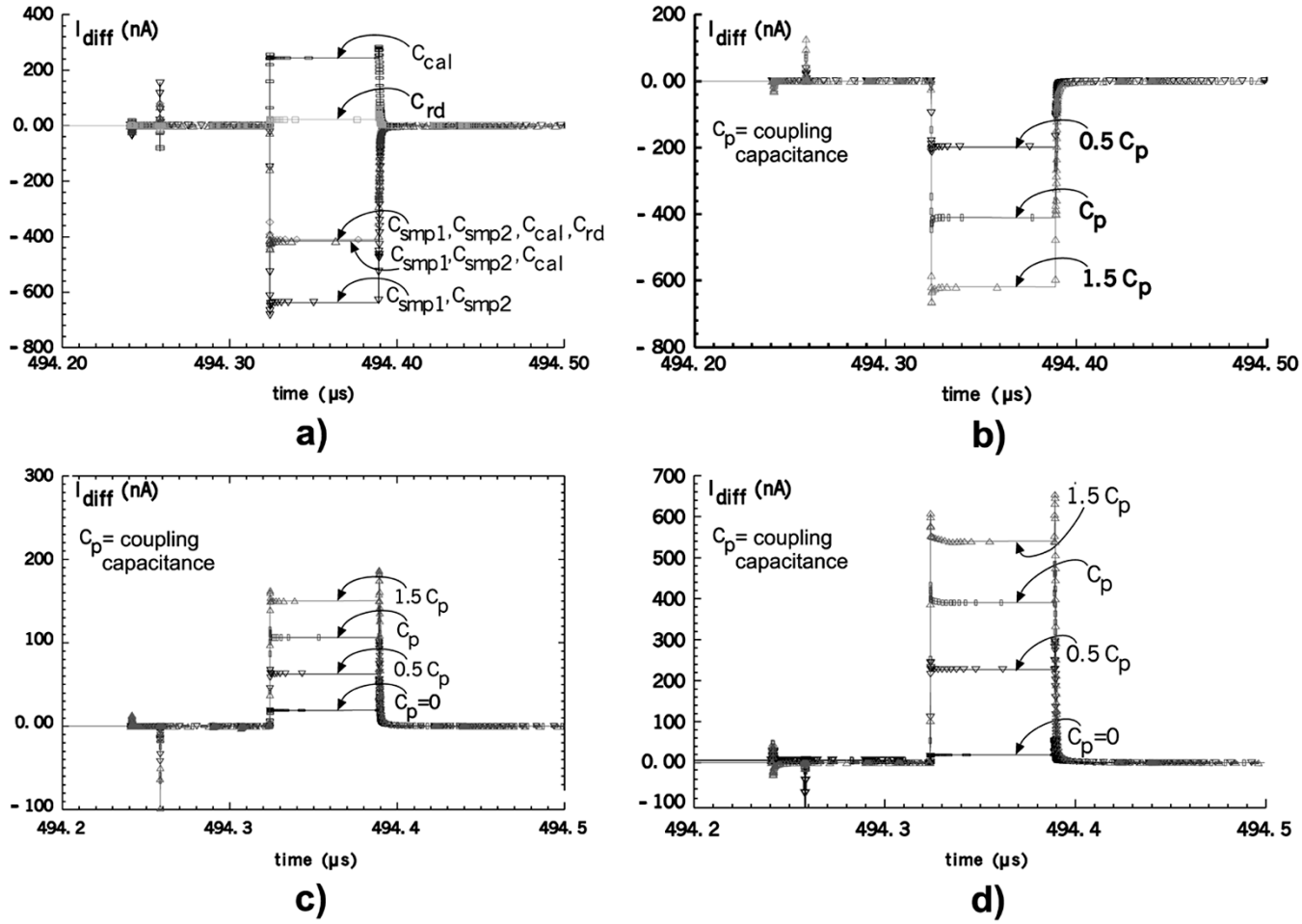

Fig. 13. Simulation results of signal dispersions due to coupling through sets of different parasitic capacitances. The differential output current of a single pixel is shown. *Effects:* (a) digital control lines and two sensitive nodes of storage capacitors $C_{cal-n1} = C_{cal-n2} = 65$ aF, $C_{rd-n1} = C_{rd-n2} = 65$ aF, $C_{smp1-n1} = 745$ aF, $C_{smp1-n2} = 360$ aF, $C_{smp2-n1} = 745$ aF, $C_{smp2-n2} = 360$ aF; (b) digital control lines and 2 sensitive nodes of storage capacitors, when varying all parasitic capacitors in the same direction (by $\pm 50\%$ of extracted values); (c) two analog nodes, i.e., input of the amplifier and the internal node of differential amplifier (step from 0 V two $\sim$1 V), when the differential amplifier is switching on), parasitic capacitance is only of 20 aF (two adjacent M1 lines of 0.7 μm long); (d) digital line (READ) at the proximity of the charge collecting diode, parasitic capacitor extracted $\sim$150 aF).

simulation. Following curves in Fig. 13 show the influence of varied coupling capacitances and different sources of coupling onto the output current. Assuming realistic dispersion level of parasitic capacitance, the results are quantitatively in agreement with measurements.

VII. Results Summary

The important design features and main parameters extracted from the first measurements of MIMOSA VI are summarized in Table I. Noise levels reported correspond to the calculated difference between the levels in *CALIBRATION* and *READOUT* phases, as simulated with ELDO. The pixel dispersions are referred as to the pixel-to-pixel pedestal variations between the dc levels for the two phases in the pixel readout cycle.

VIII. Conclusion and Perspectives

The MIMOSA VI chip features the first step toward the development of a smart MAPS based vertex detector. The functionality of the column-based comparators has been demonstrated. The possibility of in-pixel integration of double sampling operation allowing reduced intrinsic pixel-to-pixel output level dispersions has also been ascertained. The limited efficiency of the current implementation of zero-suppression is attributed to the parasitic stray and substrate capacitances. Improvement can be achieved by careful circuit and layout studies. This includes increasing of the gain of the in-pixel amplifier to about ten or more, reducing the number of control lines, replacing the input in-pixel source follower by direct ac-coupling to the charge sensitive element, special care about fully symmetrical layout of critical parts, and minimized coupling by pushing away "truculent" lines.

Despite the drawback of high pedestal dispersions, the MIMOSA VI chip validated the possibility of in-pixel sampling and storing signals from two different time slots. The number of memory cells can be extended in future circuits, allowing multiple and fast signal sampling inside beam bunch trains. The stored information (snapshots) can be read out between trains at lower speed. This approach would allow dealing with high occupancy in some experiments.

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