Monolithic active pixels with in-pixel amplification and reset noise suppression for charged particle detection in a 0.25µm digital CMOS process

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In this report, new all-NMOS pixel architectures suitable for charged particle detection are presented. These pixels achieve high charge-to-voltage conversion factors (CVF) using a few number of transistors inside the pixel. The first pixel architecture uses a preamplifying stage close to the detector and a simple double sampling circuitry to store the voltage level of the detector after reset called reset level. The double sampling removes the offset mismatches of amplifiers and the reset noise of the detector. Offset mismatches of the source follower are also corrected by a second double sampling stage. A differential version of this pixel is also presented.

The classical 3-T photodiode pixels need few modifications to be used for future linear colliders like TESLA. The maximum achievable CVF is limited to ~20µV/e^- with n-well/p-epi diodes in mainstream CMOS technologies. This is not sufficient to overcome the residual pixel-to-pixel and column-to-column fixed pattern noise (FPN). To obtain higher CVF, the detector signal must be amplified *closest to the detector*. Also (correlated) double sampling is required to suppress reset noise of the diode capacitance and pixel-to-pixel offset non-uniformities, which would be of the order of the signal generated by an impinging particle.

Recently, some methods are presented in the literature to reduce or remove the reset noise of 3-T photodiode pixels [1]-[7]. While these methods are theoretically efficient, they need often long durations of the reset for a good reduction of noise, and in practice present high FPN due to the increased number of transistors and capacitors used for the pixels.

The reset noise suppression method, proposed in [1] and shown in Figure. 1, consists of the use of a serial capacitor, a switch, and a source follower to store the reset level of the detector capacitance in the pixel. This pixel could be used for charged particle tracking, if some issues are addressed [8]. In fact, the high readout rates required in TESLA (a few tens of µs) and the 100% fill-factor property of the pixel with an n-well/p-epi diode [9] give the opportunity to store easily the reset level of the detector on an in-pixel analog memory. The first pixel presented here is based on this architecture (Figure. 2), but several important changes were made to the pixel presented in reference [1]:

1. A simple n-well/p-epi diode with reset transistor like a detector is used [9], instead of a photodiode with readout floating capacitor separated by a transfer gate. In fact, as the transfer transistor operates in the sub-threshold regime, a charge transfer problem occurs in this pixel [10] [11]. Very long integration times are needed for an efficient transfer, which are not possible in our application.

2. To increase the CVF, a *simple* common-source (CS) stage with diode-connected NMOS load as the first amplifying stage is used instead of the first source-follower (SF).
3. In order to save power consumption, the CS stage is switched instead of continuous bias of the SF.
4. To remove the offset voltages of the output SF, its offset is sampled externally during the measure of reset level of the detector on the in-pixel serial capacitor.
5. To increase the readout speed, the gate voltage of the output SF's bias transistor is switched. This limits signal variations on the column bus by avoiding the bus capacitance discharge

The key points of the design are followings:

- The reset transistor should remain in linear region for a fast reset,
- The MOS capacitor should remain in inversion for linearity,
- The CS stage should remain in appropriate operating region,
- The second switch transistor should remain in linear region for a fast reset,
- The SF should remain in appropriate operating region.

Three versions of this pixel are designed with different CVFs: 40µV/e^-, 50µV/e^-, and 60µV/e^-. To obtain higher CVFs, the reset level of the detector should be reduced considerably.

The main temporal and FPN sources of this pixel are well known:

- All the noises generated by the first switch transistor (thermal noise, low-frequency noise, channel charge injection, clock feed-through etc.) and sampled to the detector capacitance are removed through in-pixel correlated double sampling (CDS) circuitry.
- The offset of the CS stage is removed through CDS. It should be noted that the CDS doubles its thermal noise (power) [12], and the 1/*f* noise is not removed. However, as a high CVF is obtained close to the detector, input referred noise should still remain small.
- The thermal noise generated by the second switch and sampled to the MOSCAP is not removed, but this noise is small compared to the other temporal noises. The charge channel charge injected by this switch and the clock feed-through are removed through double sampling (not correlated)[1], if the reset level of the input of the SF after RST2 is constant for successive resets in the same pixel. This is the case if a "clean" power supply for the pixel is provided.
- The offset and 1/*f* noise of the SF are suppressed through column-level CDS. The thermal noise (power) is doubled.

[1] It is also possible to suppress the charge injected by this switch and the clock feed-through through real CDS with a modified timing. However, this modified timing could lower the readout speed due to the larger signal swings on the column bus.

The second architecture is the differential version of the first (Figure. 3). In fact, it is the pixel-level implementation of the “conventional” column-level readout circuitry of CMOS active pixel sensors [13] [12]. In the original architecture, as an NMOS source follower is used in the pixel, PMOS source followers are used to buffer the reference and signal levels of the pixel. This is not possible in our application. Fortunately, the common source amplifier gives the required level shift which makes possible the use of NMOS source followers. The advantage of this architecture is a better immunity to power supplies disturbances and to injected charges of the switches, which are crucial in this application. The disadvantages are the increased complexity, increased power dissipation, and a lower speed. Also, the reset level of the detector must be reduced considerably which limits the dynamic range.

References

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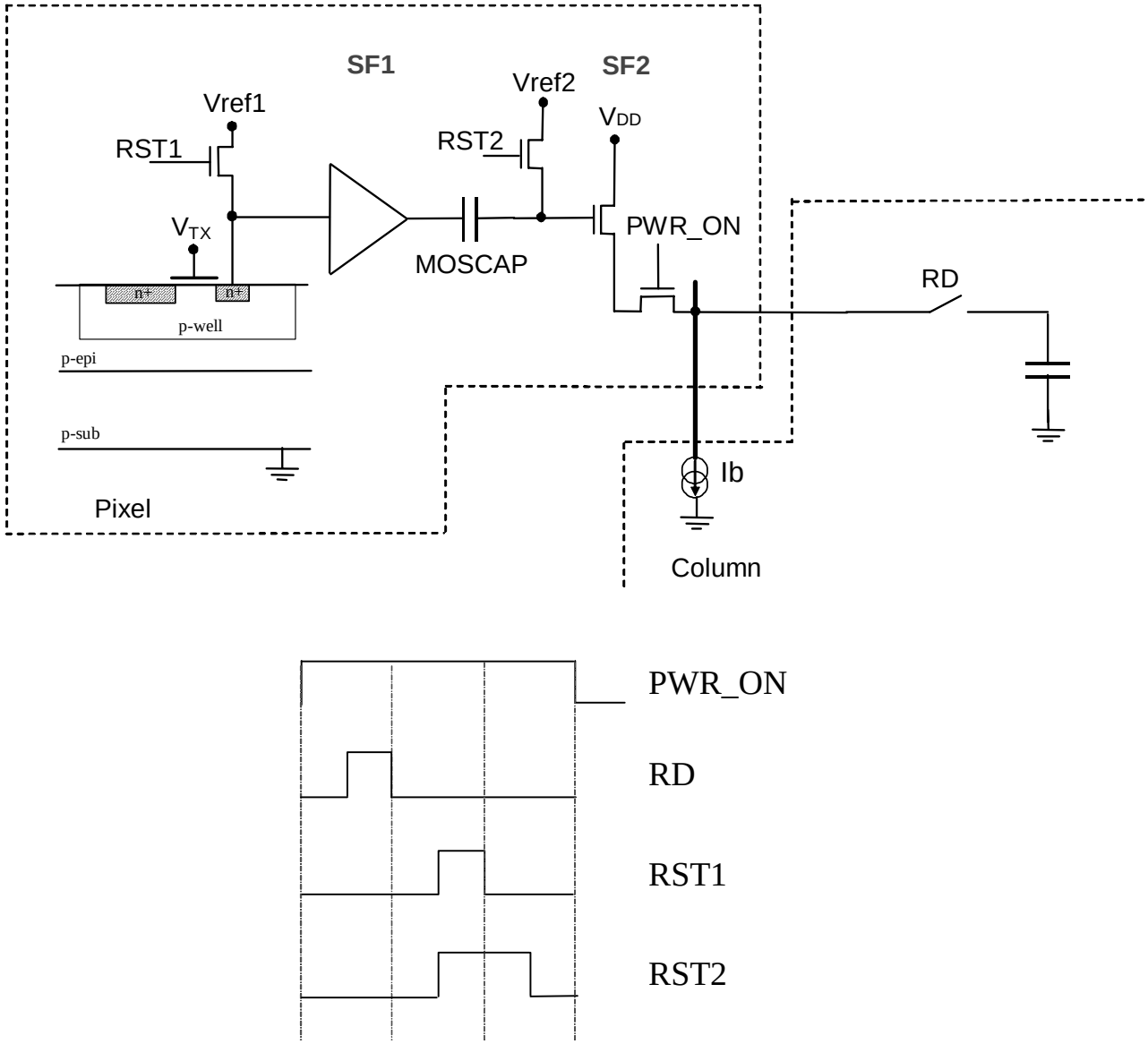
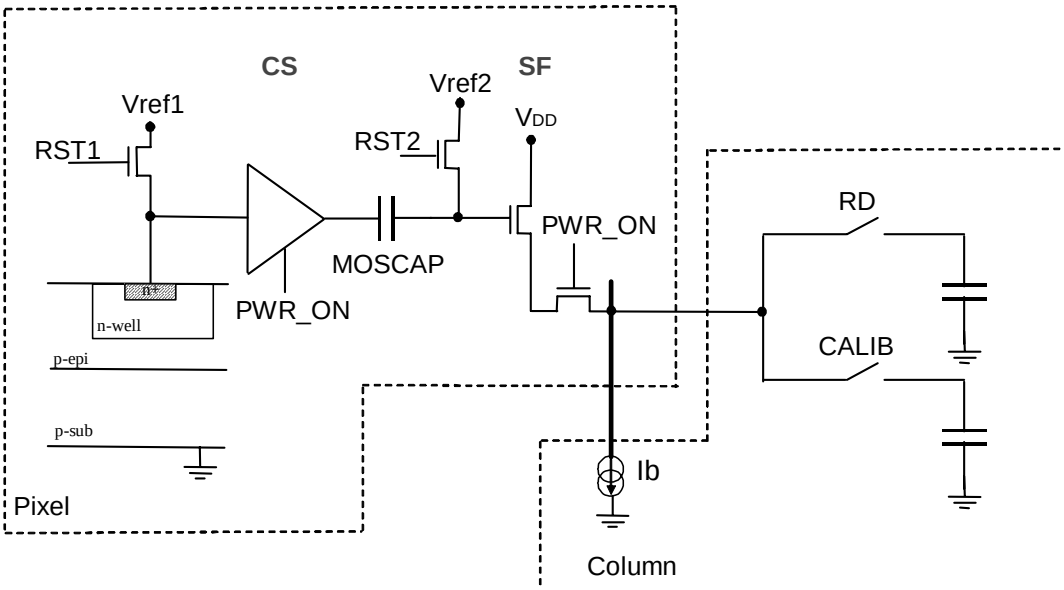
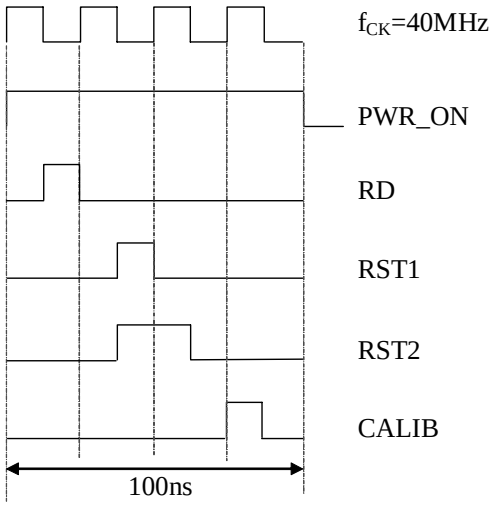
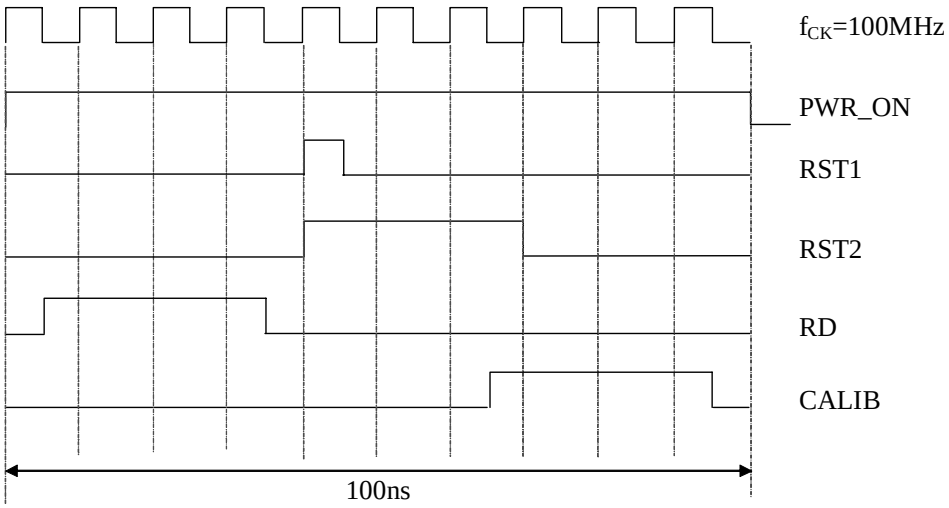


Figure 1 : (a) Schematic of the pixel presented in [1], (b) related timing (not to scale). Note that the offset variations of SF2 are not corrected.





(b)



(c)

Figure 2 : (a) Schematic of the proposed first pixel and, (b) related timing (clocking stimuli) with f_{CK}=40MHz, and (c) related timing with f_{CK}=100MHz.

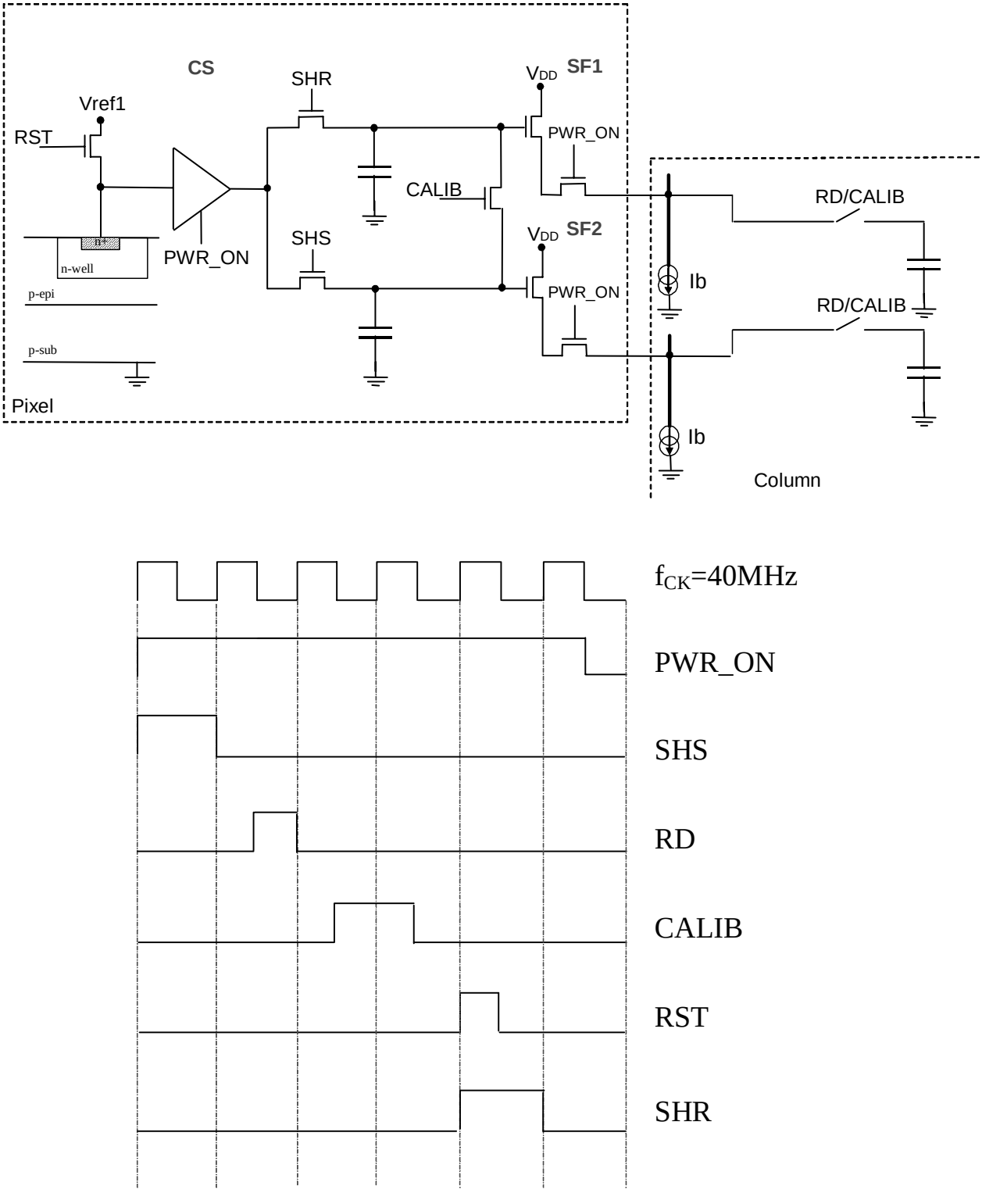


Figure 3 : (a) Schematic of the differential version of the proposed pixel and, (b) related timing (clocking stimuli).