VHDL DESIGN AND SIMULATION OF A FAST BEAM LOSS INTERLOCK FOR TTF2

A. Hamdi, M. Luong, CEA-Saclay, Gif sur Yvette, France
M. Werner, DESY, Hamburg, Germany

Abstract

The TTF2 fast beam loss interlock provides different modes of protection. Based on the differential beam charge monitoring over a macropulse, a pulse slice or bunch-by-bunch, the signal processing time should be as short as the bunch repetition period (110 ns). The signal delivered by the toroid-like inductive current transformer always shows an envelope droop due to its self-inductance to resistance ratio. When the macropulse length is comparable to this ratio, the charge of each bunch must be derived from the difference of the top to the bottom level on the signal. This necessity combined to the various protection modes leads to a digital implementation. All the processing functionalities are designed with VHDL for a Xilinx FPGA. Because the interlock involves other control signals in addition to the toroid signal with specific shapes, which cannot be easily reproduced for the design validation before the TTF2 completion, VHDL provides meanwhile the possibility for an exhaustive validation of the system with a software test bench including all timing information.

INTRODUCTION

In the TTF linac, the high average beam power (72 kW) and the small beam size (< 1 mm) require a very fast detection of beam loss in order to avoid any accelerator systems damages. Two techniques have been considered. The first one uses the measurements of electromagnetic radiation induced by the interaction of the electrons with the matter based on photo-multipliers and secondary emission multipliers. The second uses a non-destructive direct measurement of the beam current by means of 2 inductive transformers (toroids) placed at a given distance and their comparison. Both techniques are integrated in a beam inhibit system with a dedicated control architecture [1]. The principle of the latter technique, even quite obvious, requires a complex implementation for several reasons. Bunch by bunch charge comparison should be performed in less than 110 ns. Because of the inductive nature of the toroid, the DC component of the beam signal is not converted, resulting in a droop at the output of the toroid for a long macropulse. Therefore, a double sampling of the signal at the top and the bottom is necessary to measure the charge of each bunch. The fast response of the toroid with a FWMH of 25 ns shows a very narrow peak, which requires an accurate sampling (top) with an automated calibration process. Furthermore, several protection modes should run simultaneously [1]. This implies a parallel implementation synonymous to large resource consumption on the FPGA, likely to make the placement and routing critical with regard to the signals timing. Interfacing to the embedding beam inhibit system is another aspect of such a design.

HARDWARE DESCRIPTION

Low capacitance and inductance transformers deliver the toroid signals. Preamplifiers with a maximum 40 dB gain allow a calibration ratio of 500 mV/nC. Since the bunch charge in the linac could reach 3 nC [2], the 14 bits ADC input dynamic range was set to ± 2 V. Fast arithmetic operations needed by the different protection modes are performed in the FPGA (Figure 1). Programmable and static delays chips generate the synchronisation triggers. FPGA configuration data are programmed to an ISP-PROM through the JTAG port, then, transferred to the FPGA in a master serial mode at initialisation.

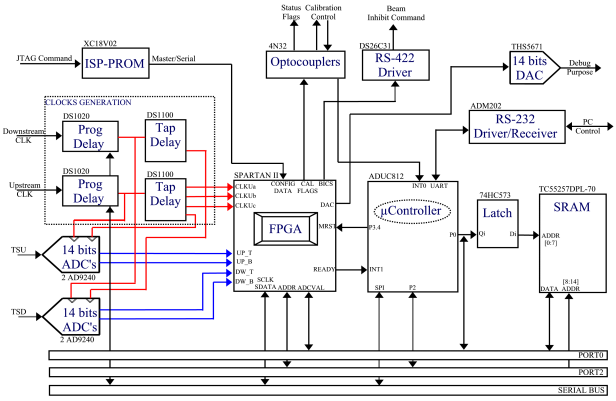

Figure 1 : Parts and interconnections of the system

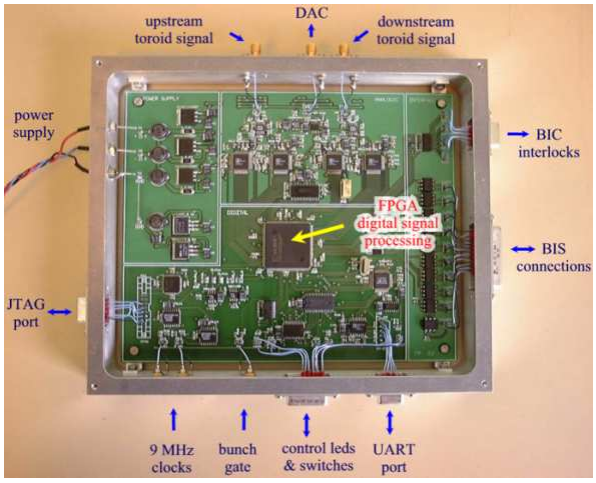

Figure 2 : Inputs and outputs on the physical board

A Xilinx Spartan II FPGA has been chosen for its input compatibility with 5 V signals and its PQFP packaging, which eases the PCB design and signal probing in the debugging process (Figure 2). The microcontroller (ADuC812) ensures the slow but more elaborate computations needed by the calibration in a single shot mode with a period of 200 ms. It makes also an interface for the alarm threshold settlings through a standard RS-232 port, either to a standalone laptop computer or a VME board integrated in the accelerator control system. Calibration request and acknowledgement as well as status flags are linked to the distributed control system (DOOCS) with opto-coupler galvanic isolation while the alarm signals are sent to the beam interlock concentrator (BIC) with a RS-422 interface. The 14 bits DAC can be used in the commissioning stage if necessary.

SOFTWARE IMPLEMENTATION-VHDL

The software design is organised into different functional modules interconnected to each other as shown in Figure 3. Each of them includes a set of smaller blocks implemented in VHDL and connected at a schematic level. The BTC module converts the ADC straight binary output to a twos complement coding. All operations involve only integer arithmetic for faster execution. The module ACQUISITION, ADDRESS DECODER and PARAMETER INTERFACE manage the communication between the FPGA and the microcontroller as well as the calibration process in which this communication is essential. An abnormal situation occurs when the bunch gate (BG) is missing and bunch charge measured at the upstream toroid exceeds a minimum threshold, the same in a reverse case. Such situations trigger an alarm through the charge validation mode. The other modes refer to the transmission based protection modes [1]. After each macropulse, the protection system resets automatically with the corresponding AUTORESET module.

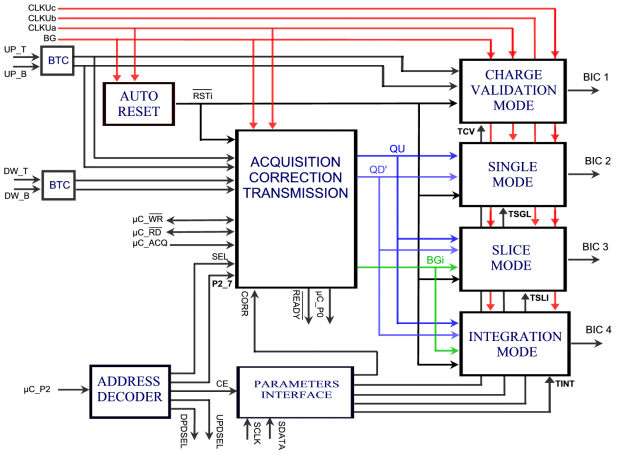

Figure 3 : Software organisation into functional modules

Signals synchronisation

The cables that carry the signals from the toroids, which may be distanced by more than 200 m, are arranged to have roughly the same length in order to keep the same dispersion. The downstream signal should arrive with a delay : $\Delta t = N\ T_{bunch} + \delta$, where N is an integer, T_{bunch}, the bunch repetition period and δ the cable cut tolerance, limited to 30 ns, which will be compensated by the programmable delay during the automated calibration. Digital data are synchronised inside the FPGA with shift registers accounting for the N integer periods and the ADC pipeline latency of 3 periods.

Automated calibration

The toroid signal is sampled with a programmable delay sweep set by the microcontroller, which receives the digitised data and decides the optimal delay for the maximum measured bunch charge (U1-U2, or D1-D2) after averaging (Figure 4). Standard deviation gives an evaluation of the noise or the beam current fluctuation. Each acquisition is triggered by ACQ signal. The latch freezes the data and sends a READY acknowledgement. The data are multiplexed byte by byte on the P0 port to be read by the microcontroller. The monostable function necessary for timing purpose here and elsewhere in the design is implemented by a counting process. The LD block represents a level sensitive latch.

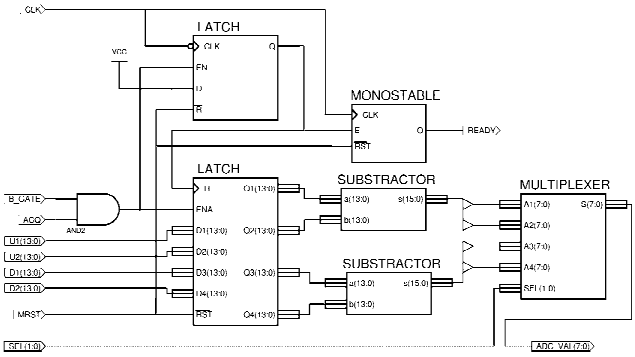

Figure 4 : Communication for automated calibration

Single bunch mode

This mode (Figure 5) compares for each bunch the charge loss between the upstream and downstream toroid. If this latter exceeds a given threshold in percentage (TSGL), an alarm is generated.

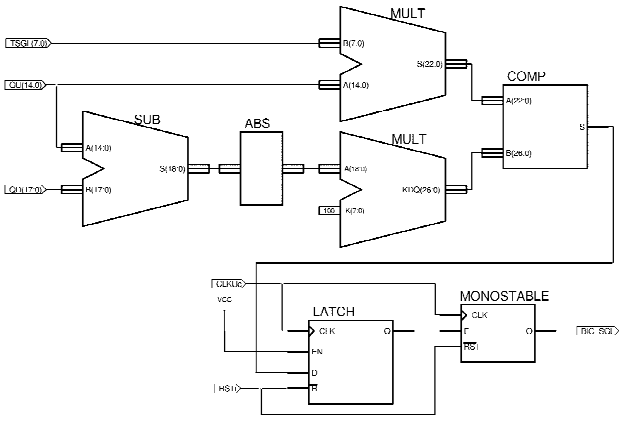

Figure 5 : Implementation of the single bunch mode

The ABS operator envisages the case of strong beam loss where the downstream toroid receives an electron shower, producing then a higher amplitude signal at its output. This is also a beam inhibit condition.

Slice and integration mode

These two modes are quite similar; they are dedicated to medium and low loss detection with medium threshold (TSLI in %) and low threshold (TINT in nC) by integrating the losses over a moving slice of S bunches or over the whole macropulse of M bunches. The beam inhibit conditions are given respectively by :

$$100\ S \sum_{i-S}^{i} \left| QU_i - QD_i \right| > TSLI \sum_{i-S}^{i} QU_i \ \ and \ \ \sum_{0}^{M} \left| QU_i - QD_i \right| > TINT$$

Figure 5 shows the implementation of the slice mode for S = 29. The counter prevents the logic to trigger an alarm during the first S bunches of a macropulse. Otherwise a single bunch mode behaviour with a much lower threshold is obtained.

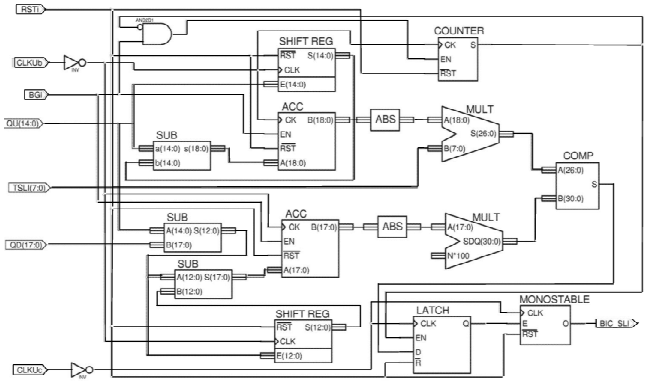

Figure 5 : Implementation of the slice mode

SIMULATION RESULTS

Results are presented for the more critical modes in term of linac protection and implementation complexity.

Single bunch mode

The bunch gate signal (first marker, Figure 6) is synchronised with the analog toroid signals at the input of the system. Because of the latency of the ADC (3 periods), it is delayed by N+3 periods (N = 1) to be synchronised with the digitised values of toroid signals (Up and Dw). An integer value of 5000 represents 2.5 nC. The test scenario simulates a beam loss higher than the threshold (25%) on the second bunch of the macropulse measured on the downstream toroid. The second and third marker indicates respectively the time when first and second bunch charge is compared, while the last marker locates the triggering of the beam interlock on the rising edge of the CLKUc signal.

Slice mode

In this scenario, the sum of the relative losses over a slice length at the beginning of the macropulse does not exceed the threshold (1%). Inside the zoomed area (blue rectangle), linear increasing losses are simulated, which exceed the threshold at the location of the second marker. An interlock is then generated. The distance from the first marker to the second defines a slice of S bunches.

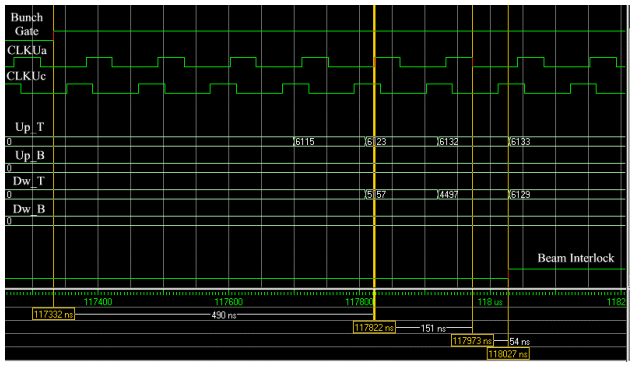

Figure 6 : Single bunch mode simulation result

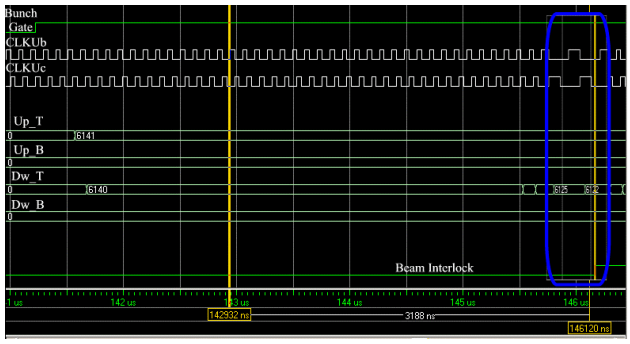

Figure 7 : Slice mode simulation result

CONCLUSION

A short description of the hardware as well as the software implementation for the transmission based beam loss protection on the TTF II linac has been given. Simulations with VHDL testbenches demonstrated all the functionalities of the system accounting for the post-place and route propagation delays in the FPGA at 9 MHz bunch repetition rate. The design can even be pushed to 13 MHz to check for the timing margin. The hardware has been validated using toroids T1 and T2 [1] for the "charge validation mode" and the "single bunch mode" in a short macropulse operation at Desy. A more detailed description can be found in reference [3].

REFERENCES

[1] D. Nölle et al, "The Beam Inhibit System For TTF II", Proceedings of DIPAC 2003, Mainz, Germany

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[3] A. Hamdi, "Conception et Réalisation d'un Système Numérique Rapide pour la Protection d'un Accélérateur Linéaire", Dissertation, Conservatoire National des Arts et Métiers, Paris, France.