A Fast Monolithic Active Pixel Sensor with Pixel Level Reset Noise Suppression and Binary Outputs for Charged Particle Detection

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Abstract—In order to develop precision vertex detectors for the future linear collider, fast active monolithic active pixel sensors are studied. Standard CMOS 0.25 µm digital process is used to design a test chip which includes different pixel types, column-level discriminators and a digital control part. In-pixel amplification is implemented together with double sampling. Different charge-to-voltage conversion factors were obtained using amplifiers with different gains or diode sizes. Pixel architectures with DC and AC coupling to charge sensing element were proposed. As far, hits from conversion of ^{55}Fe photons were registered for the DC-coupled pixel. Double sampling is functional and allows almost a complete cancellation of fixed pattern noise.

I. INTRODUCTION

IN the next generation of linear colliders required for future high energy physics experiments, such as the Next Linear Collider (NLC), the Japanese Linear Collider (JLC) and the TeV Energy Superconducting Linear Accelerator (TESLA), precise vertex detectors will be necessary to study the Higgs mechanism. Secondary vertex measurements make a high-resolution vertex detector a necessary part of the detecting system. Precision vertex measurements will be a step forward. Improvements in the spatial resolution are requested making the use of Active Pixel Sensors (APS) an attractive alternative to Hybrid Pixel Sensors (HPS), chosen for the forthcoming Large Hadron Collider (LHC) experiments, both in terms of electronic/detector integration and material thickness. Precision vertex measurements will be a requirement. There has been significant progress done by the IReS/LEPSI-Strasbourg group in the use of the monolithic active pixel sensors (MAPS) for the detection of Minimum Ionizing Particles (MIP) [1]. An array of active sensors with a

readout circuitry is integrated in a monolithic structure of a silicon chip. These sensors are designed with standard CMOS technology and have significant advantages over Charge Coupled Devices (CCDs). Two exemplary strong points of MAPS are the high radiation hardness and the flexibility of the readout architecture design. In this paper the chip design with new all-NMOS pixel architectures with integrated correlated double sampling (CDS), suitable for charged particle detection is presented.


(a)

(b)
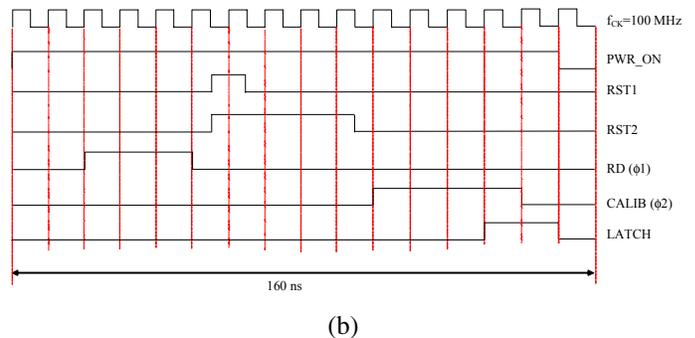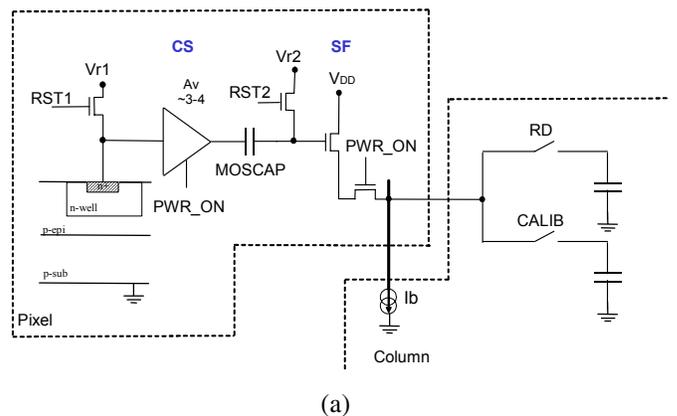
Fig. 1. (a) Schematic of the proposed DC-coupled pixel and, (b) related timing (clocking stimuli) with f_{CK}=100 MHz. RD, CALIB and LATCH signals are used by the column readout circuitry.

The classical 3-T photodiode CMOS active pixels need some modifications to be used for aggressive readout time scenarios in future vertex detectors of high energy physics experiments. The maximum charge-to-voltage conversion factor (CVF) achievable is limited to ~20 µV/e⁻ with n-well/p-epi diodes in mainstream CMOS technologies. This is not sufficient to overcome the residual pixel-to-pixel and column-to-column fixed-pattern-noise (FPN). In order to implement on-line data sparsification some in-pixel amplification of the signal is required for higher CVF. The amplifier has to be placed as close as possible to the detection diode for the optimum noise performance. The correlated sampling processing (CDS) can be performed on the amplified signal with less risk of deterioration of the noise performance. The CDS processing implemented in-pixel is required to suppress the reset noise and pixel-to-pixel offset non-uniformities. The latest are typically of the order of the signal generated by an impinging particle. The first step towards the on-chip data processing was the MIMOSA6 chip [2]. The design showed the usefulness of the two memory cells implemented in pixel for signal extraction taking the difference of the samples latched in two time intervals. In this previous design residual pixel-to-pixel FPN was too important to use effectively discriminators implemented on the chip. Those were tested separately assessing their good performances.

II. PIXEL DESIGNS

A. DC-Coupling Pixel Design

The pixel design with DC-coupling of the amplifier to the charge sensing diode is the basis of the chip design described in this paper. This pixel architecture, derived from [3] and proposed in [4], uses a common-source (CS) preamplifying stage placed closest to the detector, and double sampling circuitry with a serial capacitor, a switch, and a source follower (SF) combination to store the reset level of the detector (Fig. 1a). This reset level is memorized until the next readout of the pixel during which it is eliminated by subtracting from the signal. The short interval between readouts in this application give us the opportunity to store easily the reset level of the detector in the pixel. Offset mismatches of the amplifiers are also suppressed as a result of the double sampling process. The threshold voltage mismatches of the SFs are successively corrected by a second double sampling process performed at the column level.

The voltage V_{RD}, sampled by the readout circuitry during the RD phase, is the signal which also comprises the offset of the SF stage. The voltage V_{CALIB}, sampled during CALIB phase, is the offset of SF stage. The useful signal is the difference between these two levels, free from the reset noise and offset mismatches of the CS and SF stages.

This pixel achieves high CVF using only 8 transistors in the pixel. The amplifier is based on the NMOS transistor common source architecture with NMOS transistor diode connected load, both operated in strong inversion. The total voltage gain

is the ratio of the transconductances of the current source transistor and the load one. The DC current bias of the amplifier is determined by the voltage across the charge collecting diode. Further pixel design details can be found in [4]. SPICE simulations show that the pixel can be read in 100 ns. In the timing shown in Fig. 2b, additional 40 ns for discrimination and 20 ns to simplify the digital part of the whole chip were added.

B. Optional AC-Coupling Pixel Design

The pixel design with the direct AC-coupling of the amplifier to the charge sensing diode was used as a test structure for the current chip design. The pixel architecture uses an auto-reverse polarized charge collecting diode [5], in-pixel amplifier AC-coupled to the charge sensitive element and circuitry for CDS (Fig. 2a). The CDS circuitry is similar to that used in the DC-coupled pixel version. The charge sensitive element is a two diode system, with an n-well/p-epi diode, collecting the charge available after particle impact, and a p-plus/n-well diode, providing a constant reverse bias of the first one.


(a)

(b)

Fig. 2. a) Schematic of the proposed AC-coupled pixel, and b) principle of the direct AC coupling of the auto-reverse polarized charge sensitive element and the amplifier.

(a)

(b)

MAPS chip

(c)
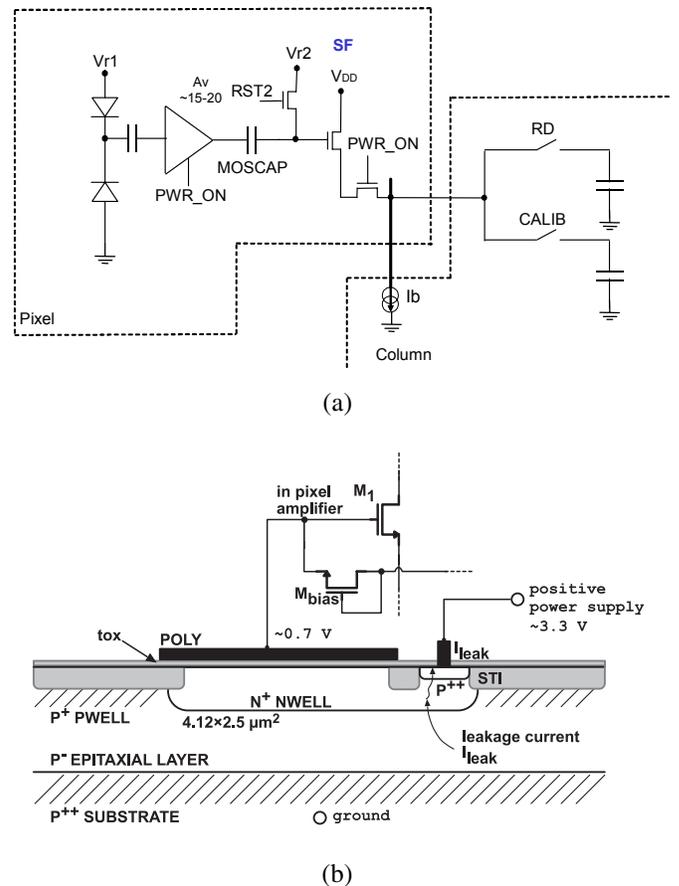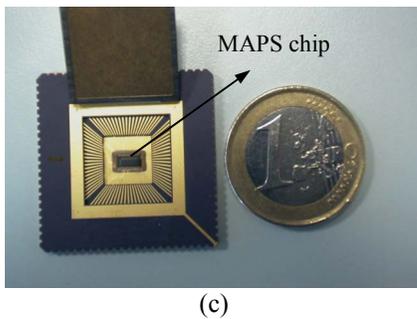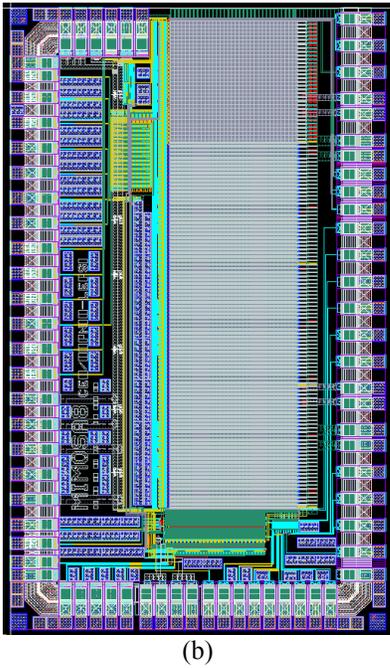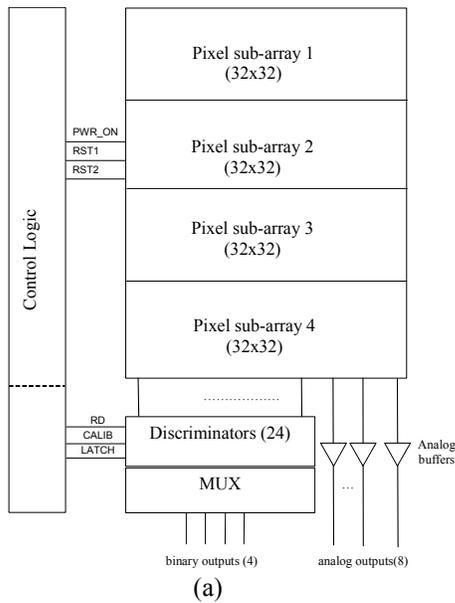
Fig. 3. a) Block diagram, b) layout and c) photography of the realized prototype chip.

The signal of the charge sensitive element is delivered to the amplifier via the series capacitance obtained by placing the polysilicon plate over the n-well area, as it is shown in Fig. 2b. The gate oxide is used providing a high value of the coupling capacitance. The signal is then amplified with a voltage gain about 15-20, aiming at total CVF about 150 µV/e$^-$.

The principle of the direct AC coupling of the auto-reverse polarized charge sensitive element and the amplifier is shown in Fig. 2b. The choice of AC-coupling instead of DC-coupling allows independent bias of the input transistor in the amplifier from the potential settled on the n-well region during the detector operation. At the same time, the n-well diode is polarized with the maximum voltage available in the technology process bearing the optimization of the charge collection process. Since the second pixel does not use reset transistor for the diode, the CDS is used to extract the signal in subtraction from the reference level. The reference level for each new measurement is the state from the previous readout cycle.

III. ARCHITECTURE OF THE CHIP

A test chip was designed using a 0.25 µm CMOS digital process available through MOSIS. The chip consists of four sub-arrays of 32x32 pixels each, 24 column-level discriminators for signal sparsification, a fully programmable digital sequencer and output multiplexers for binary outputs, as it is shown in Fig. 3. The pixel pitch is 25 µm. The bottom three arrays contain the DC-coupling pixel type. The three arrays were designed aiming at different values of CVFs with different diode sizes. The first array from the top of the chip is built with the AC-coupling pixel type.

The chip readout is organized in columns processed in parallel. The first 24 columns are connected to discriminators, multiplexed onto 4 outputs. The last 8 columns of 32 are not connected to discriminators. Their analog outputs can be observed directly on the output pads. These direct outputs were used for testing of pixels with the results presented in the latter part of the paper. An additional output of the eights column of the group of columns with analog outputs allows to examine internal point of the amplifier before the clamping capacitance used for CDS processing.

The digital part includes two circuits. One is the digital control circuit, which is fully programmable and generates the patterns necessary for addressing, resetting and double sampling of the signals in pixels in a column parallel way. The rows are selected sequentially using a multiplexer every 16 clock cycles. The pattern is loaded to the chip serially during a programming phase at low frequency. The second circuit realizes a temporal multiplexing of the binary outputs signals (column discriminators) at a frequency value half that of the main clock frequency.

The design of comparators is based on an auto-zeroed amplifying stage and a dynamic latch, as it is shown in Fig. 4. They are an improved version of the previous design MIMOSA6 presented in [6][2]. The architecture was modified to use MOS capacitors instead poly-poly linear capacitors, because the fabrication process used does not feature this type of capacitors. To obtain a good linearity, a care had to be taken

to bias the capacitors in the accumulation regime. Level shifters before capacitors were used for this purpose. Thanks to the MOS capacitors, which have small dimensions, the size of the comparators is the same as the ones used in the previous design (220 μm x 25 μm).

The discriminators substract V_{RD} from V_{CALIB} for each pixel, and compare it with the reference differential voltage $\Delta Vref = Vref1 - Vref2$.
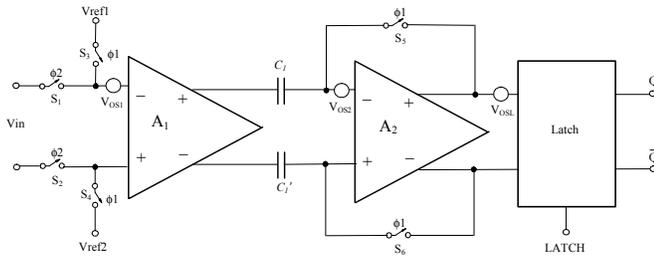

Fig. 4. Bloc diagram of the offset compensated comparator.

IV. TEST RESULTS

Two kinds of measurements were performed on the chip. At the first step, the analog outputs were tested with a digital oscilloscope. The digital part generates a signal synchronized with the access to the first row of the pixel array. The analog signal from a single, selected column was examined using this synchronizing signal. It was possible to observe the signal of one single pixel in this way. During the tests with the oscilloscope, the clock operating frequency was of the order of 10 MHz, allowing clearly observing different phases (the first readout, reset of the charge collecting diode, reset of the clamping capacitance, second readout – calibration in the pixel access). At the latter step, measurements with main clock frequency of up to 100 MHz were also successfully performed. A thorough study of the analog outputs was made. The arrays of pixels with the DC-coupling were tested at the beginning as the basic option. The tests of the matrix containing pixels with AC coupling were also started. Experiencing some problems during the tests of AC-coupling pixels, the results of the DC-coupling option are presented in this paper only. The tests of the AC-coupling will be continued.

Fig. 5 shows the direct analog output signal observed. Note that the 2 levels for each pixel (V_{RD} and V_{CALIB}). The black part is the pedestal and the grey lines correspond to the signal. The useful signal is the difference between these two levels. Tests without the source showed that the double sampling could eliminate offset dispersions of the in-pixel amplifying stage. The offset dispersions of the source follower output stage are to be corrected later by the column readout circuitry (discriminators). The two samples were recorded for each pixel and then subtracted offline, resulting in dispersions level less than 1 mV. The typical consumption of each pixel is reduced to 60 μA (the pixel dissipates only when it is powered-up).
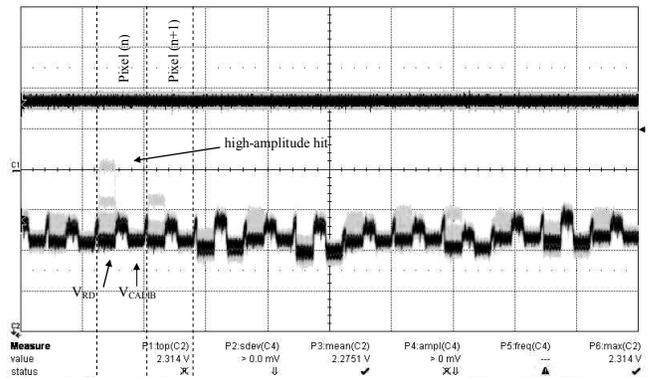

Fig. 5. Output analog signal from 12 pixels of a column recorded on a scope (50 mV/div.). The useful signal for each pixel is the difference between these two levels, normally extracted by the column readout circuitry. A high-amplitude hit is clearly detected on pixel (n) during the read phase, corresponding to full energy deposition of the X photon. Other hits appear distinctly.

The ability to detect ionising radiation was tested with soft X ray photons from a [55]Fe source in a second step. A 9.8 mCi [55]Fe source was placed in the dark box at approximately 1 cm of the chip with no material in between. After 15 minutes of the acquisition time, the hits could be seen on the oscilloscope as jumps on the output signal during the RD phase, as it is shown in Fig. 5 and 6. The conversion factors for different pixel architectures were grossly estimated from the maximum signal observed[1]. A good agreement comparing to ones simulated was obtained. The conversion between the measured voltage and the charge collected by the diode was estimated knowing the energy of the photons from the source to be 5.9 keV for the dominating emission mode, corresponding roughly to 1600 e⁻. The knowledge of the CVF allows estimating of noise, which does not exceed 20 e⁻ ENC for the worst case, i.e. the pixel with lowest CVF (@f_{CK}=100 MHz and with a measurement bandwidth of 200 MHz). The results obtained in this way can be only be considered as preliminary, allowing however demonstration of good ionising radiation detection capabilities, with low noise and low pixel-to-pixel DC level dispersion, of the new pixel architecture. The results obtained in tests are summarized in Table I.

The signal for an [55]Fe source is higher than the one which would be expected for a MIP (an average of 80 e⁻/μm x 6 μm = 480 e⁻), so the tests of the MIPs detection will be the next step forward. The good signal to noise ratio shows MIP detection should be possible. Beam tests are expected to clarify this issue.

The binary outputs were all proved functional.

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[1] The calibration is done, assuming that maximum signal observed for the exposition time correspond to the events of the photon impacts with conversion taking place in the n-well volume or in the depletion zone of the charge collecting diode, where the full quantity of the generated charge is collected within one pixel.
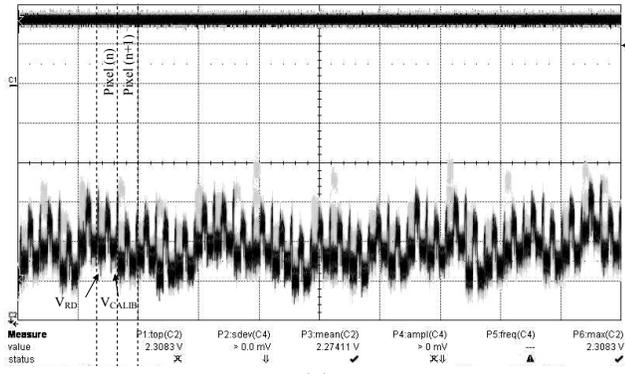
(a)
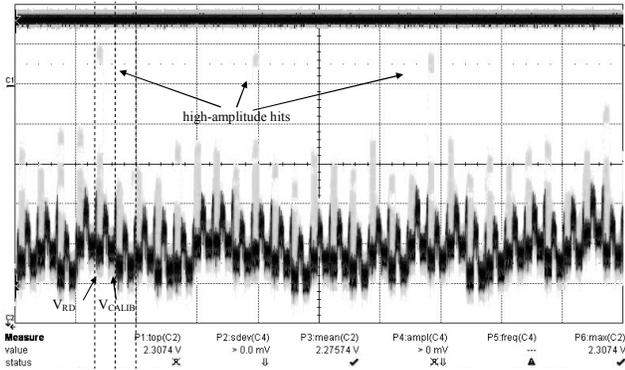
(b)

Fig. 6. Output analog signal from 32 pixels of a column recorded on a scope (20 mV/div.) a) with few small-amplitude hits, and b) with multiple high-amplitude hits.

V. CONCLUSIONS

The new method with series connection of the clamped capacitance used in the pixel design for double sampling enables the offset of each pixel to be literally eliminated. The prototype detector, consisting of 128 rows, can be read out and discriminated within 20µs with this design. Taking into account the temporal noise level and the residual FPN, the detection of MIPs should be possible using this technique. The small value of the residual pixel-to-pixel DC-level variation paves the way to the efficient on fly discrimination of signal during the readout of the detector, leading to the on-line data sparsification. The on-line sparsification is an issue for the layers L1 and L2 of the vertex detector in a future linear collider, where the high hit occupancy is expected. The feasibility of in-pixel double sampling with pre-amplification was successfully established. Implementation of the on chip analog to digital conversion and full data processing with digital hit reconstruction is still another future challenge.

The next step for the characterization of the chip will be to make statistical measurements on analog and binary outputs using a fast data acquisition system currently under development.

VI. ACKNOWLEDGMENT

VII. REFERENCES

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