IDeF-X V1.0: Performances of a New CMOS Multi Channel Analogue Readout ASIC for Cd(Zn)Te Detectors.

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***Abstract*–The evolution of the CdTe detectors properties (leakage current, capacitance, geometry) requires a continuous improvement of the electronic frond-end in terms of geometry, noise, and power consumption. This is why our group is working on a new modular spectro-imaging system based on CdTe detectors coupled to dedicated full custom readout ASICs, named IDeF-X for Imaging Detector Front-end. We present the most recent version of IDeF-X which is a sixteen channels analogue readout chip for hard X-ray spectroscopy. It has been processed with the standard AMS 0.35 µm CMOS technology. Each channel consists of a charge sensitive preamplifier, a pole zero cancellation stage, a variable peaking time filter and an output buffer. IDeF-X is designed to be DC coupled to detectors having a low dark current at room temperature and is optimized for input capacitance ranging from 2 to 5pF.**

I. Introduction

THE development of the IDeF-X front-end ASIC includes several steps from its first version as a set of stand-alone preamplifier prototypes [1] to a complex multi-channel (32 to 256) circuit for high-pixel density CdTe readout. The final device (ASIC + detector) is planned to be used in large area cameras (100 to 1000 cm²) for space borne astrophysics, either on focusing telescope (e.g. SIMBOL-X [2] and MAX [3]), operating with hard X-rays (4 to 150 keV) or gamma-rays (511 and 847 keV), or on a large area position sensitive detector of a coded aperture telescope (4 to 600 keV) (e.g. ECLAIRs [4]).The first ASIC, named IDeF-X V0 [1] was designed to evaluate the AMS 0.35µm CMOS technology and to choose the best suited charge sensitive preamplifier (CSA) design. This first chip has been fully characterized. The noise results permit its use in very high resolution spectroscopy (0.5 to 1 keV FWHM) applications. Moreover, the demonstrated radiation hardness of this technology up to more than 200 krad make it suitable for spatial applications and encouraged us to use it for the new chip.

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II. IDeF-X V1.0 ASIC design

IDeF-X V1.0 chip is a complete 16 channels analogue front-end. Each channel is fully independent. The design is optimized for low input capacitance (2 to 5pF) and low dark current (1pA to 1nA) hard X-ray detectors used in the energy range from 4 keV up to 300 keV. Each channel includes a CSA, a pole zero cancellation stage (PZC), two second order Sallen & Key (SK) type filters, and an output buffer.

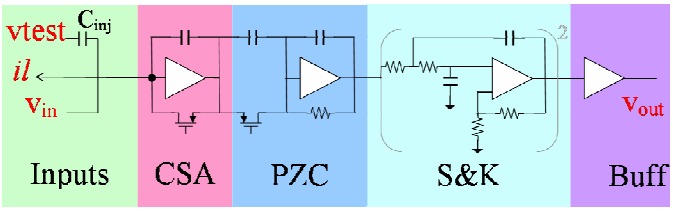

Fig. 1. Schematic of the channel: A test input allows calibrated charge injection. A current input makes it possible to inject a leakage current in the channel. The injected charge is converted into voltage by the CSA. The ouput of the CSA is connected to the Sallen & Key type filters via a pole zero cancellation stage.

The CSA is inherited from the previous IDeF-X V0 [1]. It is based on a classical "folded cascode amplifier" with a PMOS type input transistor. The continuous reset system is done by a feedback PMOS transistor operating in the subthreshold region. The current that flows through the channel of this transistor is the leakage current of the detector. The PZC stage is used to avoid long duration undershoots at the output. Moreover it amplifies the signal at the output of the CSA and allows optimized DC coupling by minimizing the influence of the dark current on the gain. The PZC stage is based on reference [5]. The fourth order shaper includes two second order SK low pass filters with tunable shaping times. The SK structure can operate a second order filter with only one active device (amplifiers, OTA). Its power consumption is therefore optimized in comparison with classical filters. The tunable shaping time is done by the commutation of series resistors in the filters. The ASIC is equipped with a test input *vtest* used to inject a calibrated charge through the on-chip injection capacitance C_{inj} placed in front of every channel. Finally, in order to simulate a detector current or to compensate a reverse detector current, each channel includes a

tunable current source *il*. The main characteristics of IDeF-X V1.0 are summarized in table 1.

TABLE I
IDEF-X V1.0 MAIN CHARACTERISTICS

PARAMETER	VALUE
CHIP SIZE	2355 µm × 4040 µm
NUMBER OF CHANNEL	16
POWER SUPPLY	3.3V
POWER DISSIPATED	2.26 mW/channel
GAIN	200mV/fC at 6µs peaking time
DYNAMIC RANGE	-40000 to 40000 e^- (0 to 176 keV for CdTe)
SHAPING TYPE	unipolar
PEAKING TIMES (IN µS)	0.5 / 0.9 / 1.5 / 2.4 / 3 / 4 / 4.5 / 6

III. EQUIVALENT NOISE CHARGE MEASUREMENTS (ENC)

A. Measurement setup

The first characterization of the circuit consists in measuring the ENC of each channel as a function of the peaking time (τ_{peak}). To perform the measurements, three test boards have been designed (Figure 2). First, the polarization board allows biasing, configuration, injection and response measurements. The polarization board is a standard printed circuit board (PCB) designed in a standard epoxy material (FR4). Second, the chip board carries the ASIC. To reduce excessive noise due to dielectric losses and capacitve load, the chip board is fabricated with glass-Teflon and the chip is directly mounted on the board by wire bonding (no package).

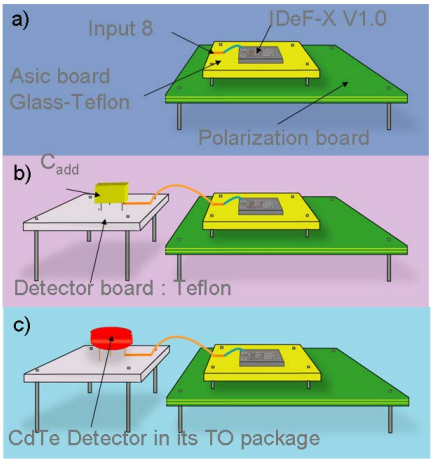

Fig. 2. Setup configurations: Config (a) The ASIC is directly mounted on a glass teflon board (the chip board) to avoid excessive noise due to parasitic capacitance and dielectric losses. Config (b) The input (channel #8) of IdeF-X V1.0 is connected to the detector board. An additional capacitance can be connected to the input #8. Config (c) A single pixel detector (CdTe Schottky biased under 330V at 22°C) in its TO package (2pF) is connected at the input of the ASIC.

Third, the detector board is used to connect a single pixel to the input of the ASIC. The detector board is also fabricated with Teflon for noise reduction purpose. The detector board can be connected to one of the ASICs input on the ASIC board with a simple enamel wire.

A calibrated signal is injected at the test input. The channel outputs are connected to external multiplexers, ADC and acquisition station. In this configuration, we measure simultaneously the amplitude and the noise of the channels. To keep the paper clear, we report in the following only results obtained on the channel #8, which behaves like all other channels but which is also equipped with intermediate test points at every analogue stages (CSA, PZC, SK and Buffer).

The ENC versus peaking time is plotted in Figure 3 using three different setup configurations (Figure 2): First, the ASIC board is not connected to the detector board config (a). Second, the ASIC board is connected to the detector board without any detector (config (b) with C_{add}=0) Third, the two boards are connected together and a CdTe monopixel detector (4.1mm×4.1mm×0.5mm equipped with a Schottky contact at the anode and a guard ring at the cathode: 1 mm guard ring surrounding the 2×2 mm² pixel) biased under 330V is plugged in the detector board config (c). The lowest ENC in the three configurations are reached at τ_{peak} =6µs. As expected, the best ENC is obtained at the highest peaking time because of the very low parallel noise (no leakage current).

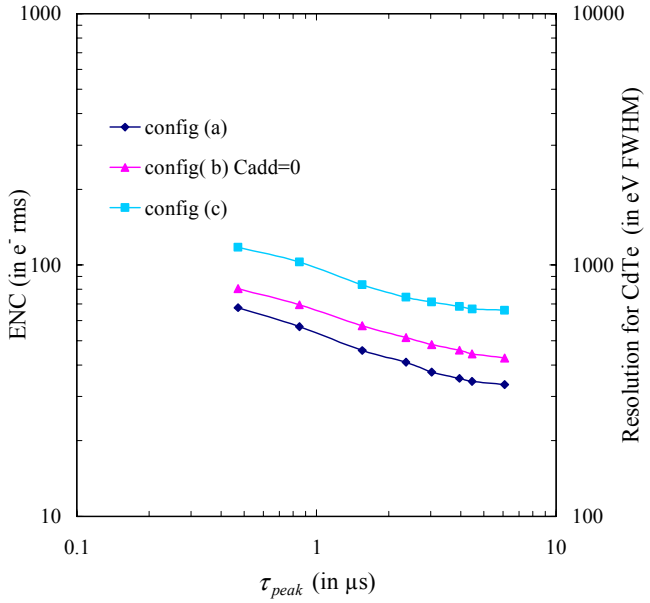

Fig. 3. Influence of the setup configuration on the noise performances. ENC=f(τ_{peak}) with the three different setup configurations. The minimal ENC of 35e^- rms is reached at the highest peaking time (6µs) when no detector board is connected to the input of the channel. The detector and its board bring parasitic noise essentially by capacitve effect.

The minimal ENC is obtained in the config (a) where the capacitance at the input of the channel is the lowest. The first setup configuration is used to measure the intrinsic performances of the circuit, i.e. the floor noise of the design. The ENC floor is found to be 35 e- rms. This result is in

excellent agreement with the previous IDeF-X V0 chip characterization [1], where the floor noise was found to be 33 e- rms. We derive from these measurements that the noise contribution of the additional stages in the channel (PZC and SK shapers) is negligible. The minimal noise measured in the config (b) is 42 e^-. The two ENC versus τ_{peak} curves in config (a) and config (b) are quite parallel, it demonstrates that the additional noise in config (b) is essentialy due to capacitive effect. In the case of config (c), we found a minimal ENC of 66 e^-. It is the noise floor with this type of detector in this kind of package (the detector capacitance is evaluated to 0.7 pF and the capacitance of the TO package to 2pF) at 22°C. At short peaking times (less than 3µs), the curve is parallel to the two other ones, the additional noise is only due to the capacitance of the detector and the one of the TO package. At longer peaking times, the additional noise is due to the dielectric losses and to the leakage current of the detector. The curves are no more parallel.

B. *ENC vs. additional input capacitance*

In order to predict the performances of the chip connected to a detector, we need to study the influence of the input capacitance on the noise behavior of the circuit. Moreover, this measurement allows us to understand the contribution of the setup. For those measurements, we use the config (b) and we plug a set of additional parasitic and calibrated capacitances on the detector board at the input of channel #8.

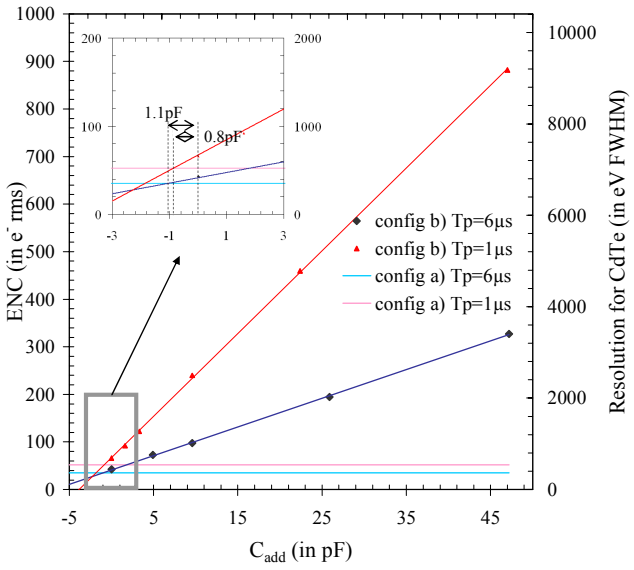

Fig.4. Influence of the input additional capacitance. As expected, the lowest sensistivity of the chip to the input capacitance on its noise performance is obtained at the highest peaking time: at 6µs, the slope is evaluated to 6e^-/pF. The comparison of this plots with the ENC values obtained in config (a) is done to extract the parasitic capacitance of the detector board.

The measurements are obtained without any leakage current (*il* < 1 pA) minimizing the parallel noise. For each additional input capacitance, we measure the ENC at two different peaking time values. At a given peaking time, the ENC is a linear function of the additional input capacitance (Figure 4), and we found:

$$ENC(at\ \tau_{peak} = 6\ \mu s) = 42\,e^- + 6\,e^-/pF$$
$$ENC(at\ \tau_{peak} = 1\ \mu s) = 66\,e^- + 17.5e^-/pF$$

As expected, the minimal ENC is obtained at the highest peaking time: the theoritical expression of the ENC at the output of the shapers is [6]:

$$ENC^2 = C_{tot}^2\left(\frac{\alpha_d}{\tau_{peak}} + \alpha_{1/f}\right) + \alpha_{//} \cdot il \cdot \tau_{peak}$$

Where :

- $C_{tot} = C_{board} + C_{add} + C_{in}$
- C_{in} is the total capacitance into the chip at the input of the CSA plus the capacitance on the ASIC board.
- C_{board} is the capacitance of the detector board.
- α_d is a parameter that depends on the filter order as well as the transconductance of the input transistor of the CSA. $\alpha_{1/f}$ is a parameter that depends on the filter order as well as technological parameters and the area of the input transistor $\alpha_{//}$ is a parameter that depends on the filter order.
- *il* is the leakage current injected at the input of the CSA.

When no leakage current is present at the input of the channel (*il* < 1 pA) the noise is dominated by the *1/f* and the thermal noise of the CSA input transistor. The *1/f* noise is independent of τ_{peak} while the series noise decreases with τ_{peak}. As a result, the minimal ENC is reached at the highest values of τ_{peak}.

To estimate the parasitic capacitance of the detector board itself, we can compare this plot to the ENC value found with config (a) at the same peaking time. In the case of config (a), C_{board}=0, so we have C_{tot}=C_{in}. The same calculus can be done at the two peaking times:

At τ_{peak} = 6 µs we find C_{board} = *(42-35)/6 = 1.1 pF* and at τ_{peak} = 1 µs we find C_{board} = *(66-52)/17.5 = 0.8 pF*. The most realistic value of C_{board} is obtained at τ_{peak} = 1 µs where the series and the *1/f* noises are dominant. At τ_{peak} = 6 µs we extract an over esimated capacitance because of a small contribution of dielectric losses to the total noise.

C. *ENC vs dark current*

The leakage current of the detector is the second key parameter which limits the spectral response (parallel noise) after the total capacitance (including detector capacitance) at the CSA input (series and *1/f* noise). In order to estimate the best spectral resolution achievable with IDeF-X coupled to a

detector, we need to study the influence of the leakage current on the noise behavior. To do so, we use the calibrated current source *il* to simulate the dark current of the detector. The *il* current calibration is operated by measuring the signal fall-time at the output of the CSA, which is inversely proportional to the current through the reset transistor as described in ref. [1]. The ENC measurements have been done with and without additional capacitance (C_{add} = 2.4 pF, ie. C_{tot} ~ 5.5 pF). For each leakage current, we determine the minimum value of the ENC vs. τ_{peak} characteristics (ENC_{min}). ENC_{min} is reported as a function of the injected leakage current *il* in Figure 5 and the fitted curves are plotted by using the theoritical expression as follows (2):

$$ENC_{\min}^2 = 2\sqrt{\alpha_d \cdot \alpha_{//} \cdot C_{tot}^2 \cdot il} + \alpha_{1/f} \cdot C_{tot}^2 \qquad (2)$$

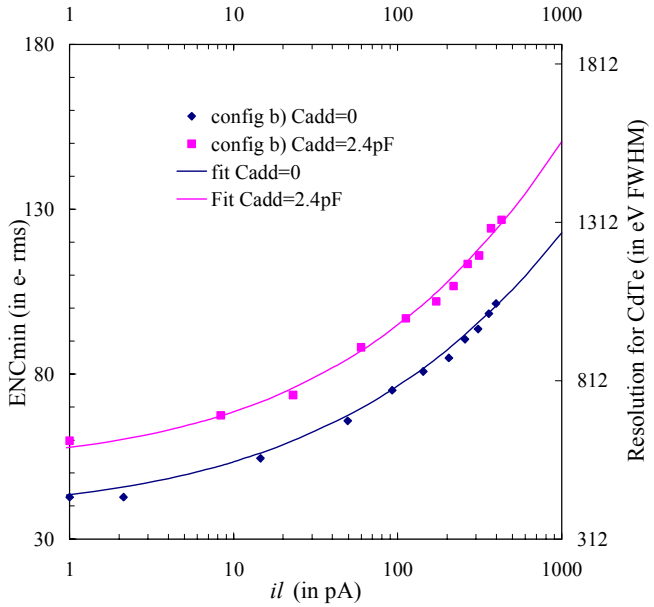

Fig.5. ENC_{min} as a function of input leakage current for two different additional input capacitances: measurement results and fits using (2). For a leakage current lower than 10pA, the minimal ENC is almost constant. At higher leakage currents the parallel noise is no more negligible and the minimal ENC increase with the dark current.

There are two different regions of interest in this plot:

- At very low dark current (*il* < 10 pA), the minimal *ENC* is reached at the highest peaking time. For these $\tau_{peakeak}$ values, the *1/f* noise is dominant and the leakage current has no significant influence.
- For higher leakage currents (10 pA < *il* < 500 pA), the minimal ENC is reached when the series noise and the parallel noise are equal and higher than the *1/f* noise. The slope factor $\delta\ ENC / \delta\ il$ is 1/4.
- For "very high" leakage currents (*il* > 500 pA), the theoretical minimal ENC can not be reached because the smaller τ_{peak} values of IDeF-X V1.0 is not short enough. The noise is dominated by the parallel noise, the slope factor tends to ½, and (2) is no more applicable.

IV. Spectroscopy Measurements

IDeF-X V1.0 has been evaluated by performing measurements at room temperature with CdTe detector. We have connected a 4.1mm×4.1mm×0.5mm CdTe (ACRORAD) equipped with a Schottky contact at the anode and a guard ring at the cathode (1 mm guard ring surrounding the 2×2 mm² pixel). The detector was biased at 330V (config c). The spectrum of figure 6 has been acquired using τ_{peak} = 6 µs with an ^{241}Am source.

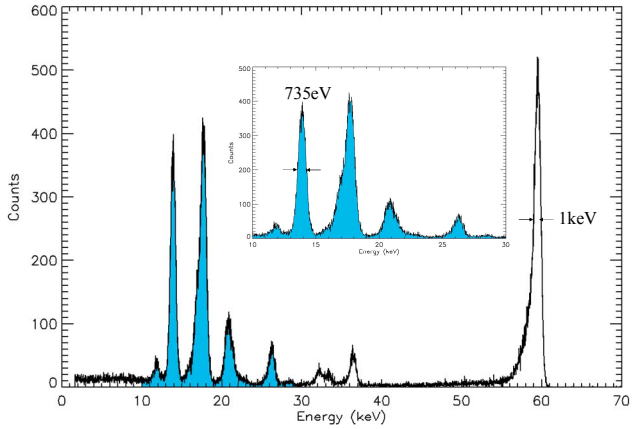

Fig.6. Spectrum of an ^{241}Am source obtained with a 4.1 × 4.1 × 0.5 mm^3 CdTe detector equipped with a Schottky contact at the anode. The cathode is 2 × 2 mm² pixel surrounded by a 1 mm guard ring. The detector is biased under 330 V at 22°C and is connected to the channel #8 of IDeF-X V1.0 at a 6µs peaking time. The best spectrum is obtained at the highest peaking tume becauqse of the very low leakage current of the detector.

We found the best spectrum at the highest peaking time value. This is consistent with the very low leakage current (less than 50 pA) measured on the detector at 330V at room temperature. The energy resolution was found to be 1 keV FWHM at 59.5 keV and 735 eV FWHM at 13.9 keV. The energy resolution at 13.9 keV is in excellent agreement with the theoritical value of 737 eV obtained by combining the electronic noise of 66 e- and the statistical fluctuation of pair creation in the CdTe assuming a Fano factor of 0.2. This result is slitlghy different from the data figuring in section III.A since in this case, the Fano factor has not been considered. Finally, the very low energy threshold value of 1.7 keV makes this chip suitable for applications at very low energy for astrophysics [4].

The spectral response is better than the one obtained with our first IDeF-X V0 chip. This is due to the optimization of the setup configuration and especially the optimization of the connection between the ASIC and the detector. The contribution of the setup to the total noise has been minimized by using materials with very good dielectric properties.

V. Conclusion

The IdeF-X V1.0 is a very low noise multi channel integrated circuit. It is optimized for the readout of low capacitive (2-5pF) and low dark current (~ 1 pA to few nA) Cd(Zn)Te detectors or pixel arrays for future X- and gamma-ray astronomy space missions. The noise performances of this chip are very promising since the floor ENC was found to be 35 e^- rms. We have studied its behavior with respect to the total input capacitance and leakage current. Today, these very satisfactory performances are only limited by the excessive parasitic capacitance and dielectric losses in the substrate of the detector (TO package). In the near future, we will use IDeF-X V1.0 to perform spectroscopy measurements with other types of Cd(Zn)Te detectors, especially with pixelated detectors. In addition, we will achieve measurements at lowest temperature to optimize the resolutions by minimising the contribution of parallel noise.

VI. References

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