# Performance of a Fast Programmable Active Pixel Sensor Chip Designed for Charged Particle Detection

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***Abstract*–We report on the performance of the MIMOSA8 chip. The chip is a 128 x 32 pixels array where 8 columns have analog direct outputs and 24 have discriminated outputs. The array is divided in four blocks of pixels with different conversion factors and is controlled by a serially programmable sequencer. MIMOSA8 is a representative of the CMOS sensors development option considered as a promising candidate for the Vertex detector of the future International Linear Collider (ILC). The readout technique, implemented on the chip, combines high spatial resolution capabilities with high processing readout speed. Data acquisition, providing control of the chip and signal buffering, linked to a VME system was made on the 8 analog outputs. Analog data, without and with a $^{55}$Fe X ray source, were acquired and processed using off-line analysis software. From the reconstruction of pixel clusters, built around a central pixel, the charge spread is limited to the closest 25 pixels and almost all the available charge is collected. The position of the total charge collection peak (and subsequently the charge-to-voltage conversion factor) stays unaffected when the clocking frequency is increased even up to 150 MHz (13.6 µs readout time per frame). The discriminators, placed in the readout chain, have proven fully functional. Beam tests have been made with high energy electrons at DESY (Germany) to study detection efficiency.**

## I. INTRODUCTION

DEVELOPMENTS in future high energy physics will include the construction of an e+e- international linear collider (ILC) [1]. This machine together with adequate detectors will allow precision, model independent measurements at sufficiently high energy and luminosity. Higgs and fundamental interaction studies may be done with this machine, with a reduced background compared to the LHC experiments [2]. Thus, this machine should be a priority for the next decades of particle physics research.

Precision vertex measurements will be mandatory for the detectors of the ILC. This makes the design of vertex detectors a challenge. New technologies are to be developed and tested, for which speed, radiation tolerance, power dissipation and integration are to be evaluated and, if needed, significantly improved.

The future vertex detector should offer a better spatial resolution than present day vertex detectors based on Hybrid Pixel Detectors, and should be faster than CCDs. The aim of the MAPS development program is to obtain spatial resolution roughly equal to 1-2 µm, with a readout time for each frame below 20 µs. This will involve very small pixels (20 µm pitch for the first layer) and thinning the silicon substrate to reduce multiple scattering.

MAPS have the competitive edge over CCDs for radiation tolerance, mainly because they are based on random access of each pixel avoiding charge transfer. The electric charge is converted into an electric signal 'in situ' on the photodiode of each pixel, all of them containing an amplifying element. Up to now MAPS seem to be the most serious candidates for the first and second detection layers of the future vertex detector of the ILC.

## II. DESIGN AND ARCHITECTURE OF THE MIMOSA8 CHIP

The MIMOSA8 device characterized here is a monolithic chip comprising a 128 x 32 pixels array, a fully programmable sequencer and 24 binary outputs. The outputs are discriminated with a common adjustable threshold and time multiplexed. The 8 remaining outputs are analog. In a move to meet speed requirements the 32 columns are read in parallel, using an external clocking. The chip is divided in sub arrays with four types of small pixels that have different conversion factors (S1: 110 µV/$e^-$, S2: 66 µV/$e^-$, S3: 60 µV/$e^-$, S4: 50 µV/$e^-$). For further details on the architecture of this chip see our previous work [4]. The MIMOSA8 was fabricated with TSMC 0.25 µm CMOS digital technology with an epitaxial layer thickness of the order of 8 µm. In order to reduce power consumption the power supply of the pixels in a row is only switched on for the row that is being read.

The new aspects of the pixel have already been described in [4]. To summarize: in pixel voltage amplification has been successfully implemented together with local CDS based on a concept familiar to CCD designers [5], this being based on one capacitor and a few transistor switches. This scheme proved to be successful up to now and has allowed some good preliminary measurement results [4]. The readout of each row is based on a scheme requiring 16 clock cycles, with a designed optimal clocking frequency of 100 MHz. The clocking chronogram is used for both the pixel and the discriminator.

The analog outputs are used to study the pixels individually, and to characterize their pedestal, temporal noise and the

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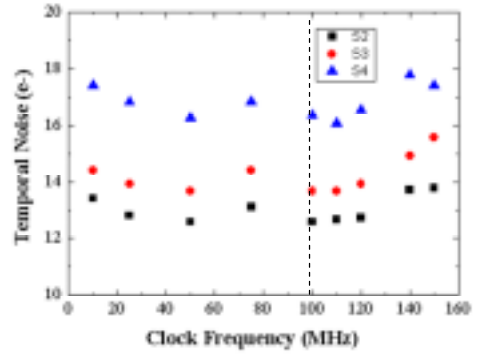
charge collection efficiency of the pixels. The digital outputs have been used to characterize the full one-bit digital chain and to evaluate the discrimination efficiency. Up to now the comparators have been tested thoroughly, these being auto-zero circuits very effective in reducing offset dispersion [6].

## III. Measurement Results

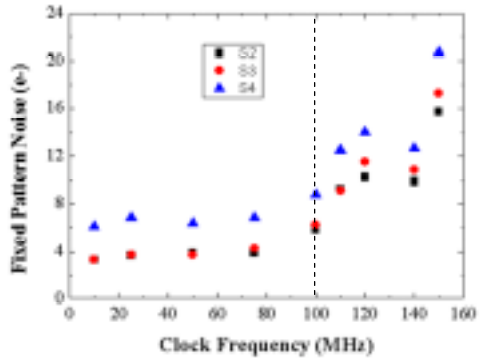
The results of the extended tests done on the pixel array with and without exposure to a $^{55}$Fe X ray source (energy peaks: 5.9 keV and 6.4 keV) are presented here. The acquisition of data was done with a VME system analog-to-digital conversion cards that record the analog outputs of the array. The chip was linked to DAQ by two dedicated boards designed to control the chip and to provide signal buffering for transmission. Data obtained were analyzed off-line using dedicated software. The data were taken and analyses carried out, first without source, to determine pedestals' dispersion (spatial noise or Fixed Pattern Noise - FPN) and their distribution on the chip and to measure the (temporal) noise level. In a second step data from the analog and digital outputs were taken with the source on. The S1 sub-array based on an architecture, different from the other arrays, was not characterized here.

### A. *Analogue Data on Single Pixels*

Fig. 1(a) indicates that the temporal noise remains stable up to 100 MHz clocking frequency. The FPN behaves similarly with a sharp increase above 100 MHz (Fig. 1(b)). This is satisfactory as the chip was optimized for 100 MHz clocking.



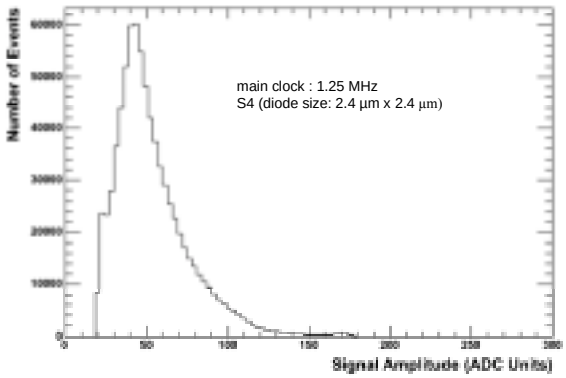

(a)



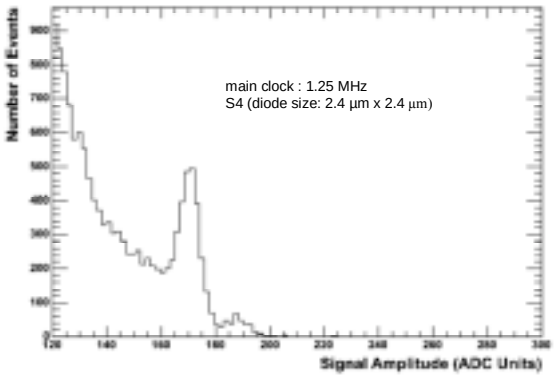

(b)

Fig. 1. Temporal noise (a) and FPN (b) versus clock frequency for the 3 sub-arrays.

The 8 columns with analog outputs underwent tests with a $^{55}$Fe 10 mCi source. Fig. 2 shows the signal corresponding to single pixels. For all spectra a cut at low energy has been made to reduce the influence of temporal noise. The calibration peak of the source is clearly observed in Fig. 2 (b) (~1600e-=170 ADC Units), but corresponds to relatively rare events, when photons deposit all their energy directly on one diode or very close. This is the reason why the calibration peak has low amplitude. As calibration events are rare, a low clocking frequency is needed to obtain a clear peak. The dominant broad peak Fig. 2 (a) which appears in the spectrum is due to events generating a charge between several diodes. This is the most probable case. The charge is shared on two or more pixels, inducing events of lower magnitude. Other events occur when part of the charge is created in the substrate. A fraction of the charge is then lost and the signal amplitude reduced. X rays (6 keV) also interact in the epi-layer by Compton diffusion. An electron is generated with a lower energy thus inducing a lower electrical charge. This contributes to the left background in the spectrum observable in many spectra.




(a)



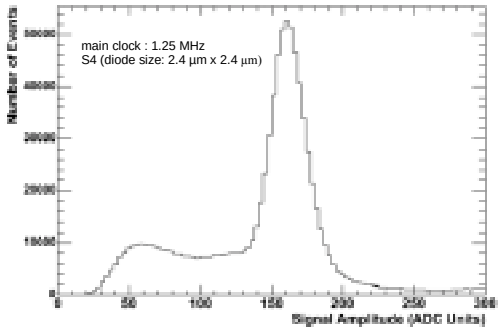

(b)

Fig. 2. Histogram of the events recorded on one single pixel (no clusters) at a clock frequency of 1,25 MHz with a $^{55}$Fe X ray Source: (a) total spectrum, (b) truncated spectrum (S4 sub array). The calibration peak is clearly observed in (b).

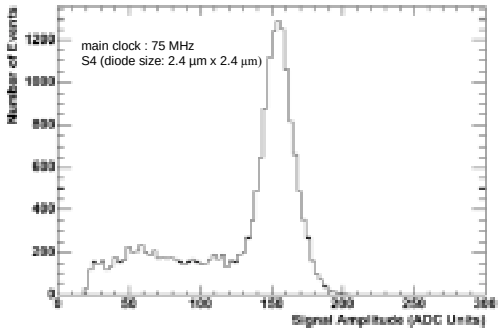
### B. *Clusterization method: 3x3 Pixels and 5x5 Pixels*

In order to study the charge distribution pixel clusters were analyzed. The software analysis allows studying different cluster sizes (3x3 or 5x5) built around the central pixel. This

analysis shows that the charge spread is limited to the closest 25 pixels and almost all the available charge is collected. Fig. 3 shows the *total charge collection peak* for clusters of 5x5 pixels in the S4 sub-array. The charge collection efficiency (CCE) is defined here as the ratio of the position of the total charge collection peak to the calibration peak. It varies from 83% for S2 sub-array up to 95% for S4 sub-array at the single clock frequency of 1.25 MHz (Fig. 4).




(a)




(b)

Fig. 3. Total charge collection peak for the largest diode size at different frequencies (a) 1.25 MHz (b) 75 MHz. Clusters of 25 pixels have been used.

The MIMOSA8 design was originally made to ensure functionality up to 100 MHz of the main clock frequency. The total charge collection peak remains unaffected by clocking frequency (Fig. 4) up to 100-150 MHz for 25 pixels clusters. In addition the shift in position of this peak at low frequencies may be attributed to the effect of the dark current of the photodiode.

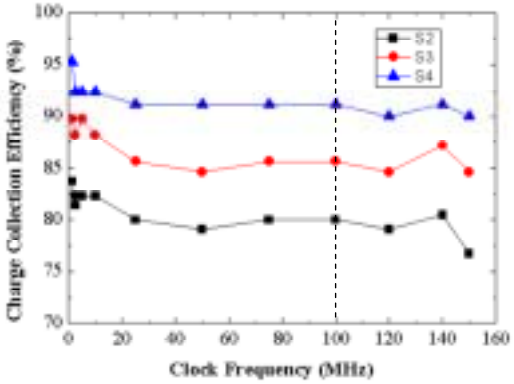



Fig. 4. Percentage of charge collected versus clock frequency for the 3 sub arrays of pixels. Clusters of 25 pixels were used.

There should be subsequently no change in the conversion factor and the charge collection efficiency up to 150 MHz clocking frequency.

### *C. Digital Outputs: Comparison with Analog Data*

In a second part of the in-lab tests, the one bit digital outputs were tested, in order to assess their functionality. Tests were carried out without and with source.

The offset distribution of the test discriminators has been evaluated on different chips. The maximum dispersion between discriminators has a value below 1 mV.

In a second step the offset distribution of the pixels discriminator readout on a single chip was analyzed (Fig. 5). This was done for S2, S3, S4 sub-arrays. The average offset is 1 mV at 40 MHz. Measurements of temporal noise give a value of 0.9 mV rms and a fixed pattern noise of 0.3 mV rms.

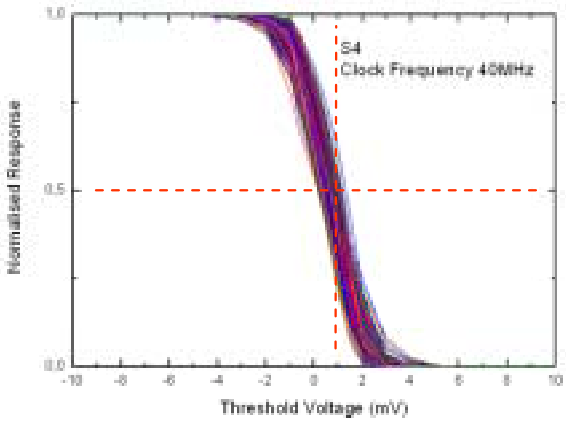



Fig. 5. Number of counts (normalized) versus discriminator threshold voltage. The offset and the temporal noise of the pixel/discriminator chain can be derived. Each curve corresponds to one pixel associated to a column discriminator. The offset dispersion can also be estimated. The clock frequency is 40 MHz.

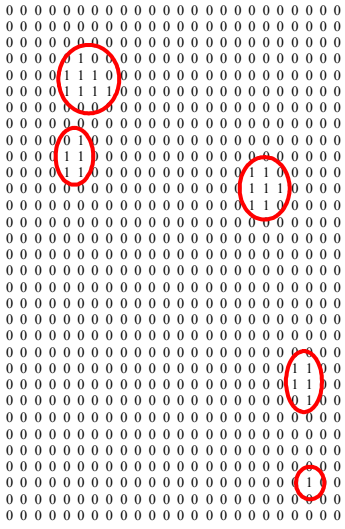
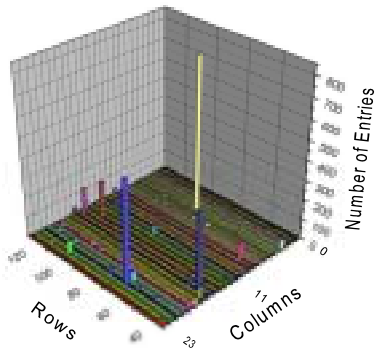
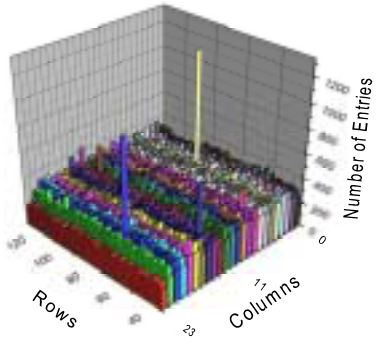


Fig. 6. Example for a sub-array of pixels with the digital values of their outputs (1: pixel hit, 0: no hit). This data was recorded with the X ray source on. Clusters of hits distinctly appear. The clock frequency is 7.5 MHz.

The analysis of the digital outputs (24 columns) with X ray exposure leads to an array of 1 (hits) and 0 (no hits) as represented in Fig. 6, for a single frame. Note that noise can induce non-physical hits. Increasing the discriminator common threshold can limit the influence of noise. Cluster of 1 are present and may be used for hit position determination. In this case discrimination is equivalent to one-bit analog to digital conversion.




(a)




(b)

Fig. 7. Histogram (number of hits for each pixel) for the array. (a) without the source, (b) with the source. The conditions are: clock frequency: 7.5 MHz, threshold voltage of the discriminators: +8 mV. 100k events were recorded in each case.

In Fig. 7 the threshold was set a high enough value to cut all the spurious hits due to noise. In spite of this in (a) some noisy pixels appear even with the high threshold voltage used. However the number of these pixels remains very low. Fig. 7 (b) shows that the discrimination is fully functional for this chip.

### *D. Minimum Ionizing Particles: Beam Tests Results*

We have made beam tests on the MIMOSA8 with a silicon strip based telescope which allows, with adequate data processing, the determination of the detection efficiency. The beam consists of electrons produced at DESY (Hamburg, Germany). The energy of the electrons is approximately 5 GeV. The analog outputs were tested together with the digital ones. The use of a high precision telescope (a few µm/plane) can, in principle, allow the estimation of the intrinsic spatial resolution of the MIMOSA8 detector. However due to multiple scattering at this energy, the spatial resolution is significantly degraded. It should be of the same order of magnitude of that measured on previous chips (< 5 µm). Data analysis process is based on C++ and root framework. Very encouraging results have been obtained for the detection efficiency of all sub-arrays. The seed pixel noise is between 11e- and 13 e-, which is compatible with laboratory's measurements for all sub-arrays studied.

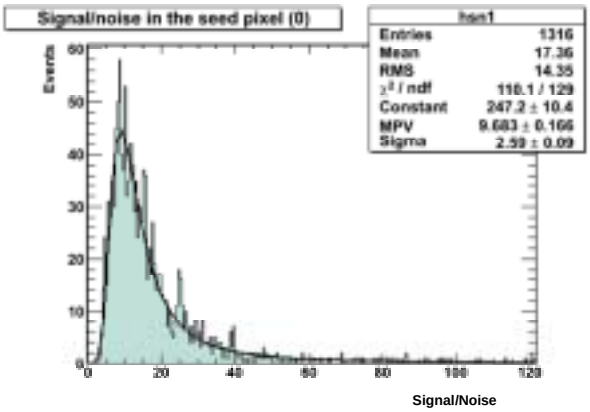
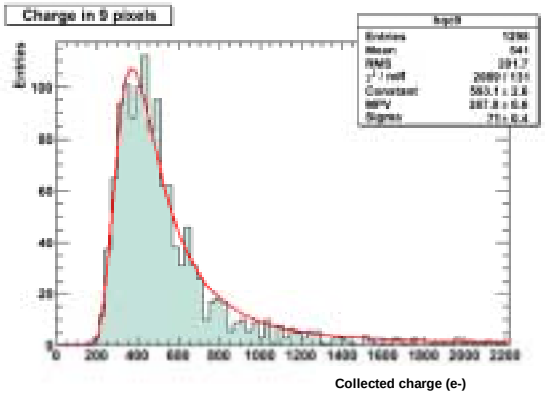
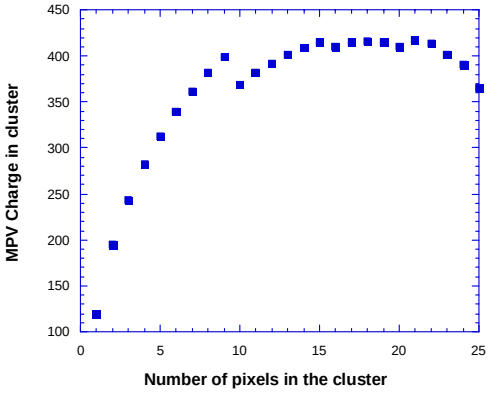



Fig. 8. Distribution of the ratio signal to noise for the seed pixel.

Fig. 8 indicates that the signal to noise ratio in this experiment has a maximum value around 10 MPV (Most Probable Value) which is a result compatible with the limited thickness of the epitaxial layer (< 6 µm) in this process. It should, however, be much improved to meet future requirements.




(a)




(b)

Fig. 9 (a). Distribution of the collected charge (in electrons) for pixels clusters of 9 pixels. (b). Total charge (Most Probable Value) (in electrons) as a function of the number of pixels in the cluster.

Fig. 9 shows that a cluster of 9 pixels is a good compromise for the cluster size. No significant gain in the collected charge may be made by increasing the size of the cluster. Indeed, as the sub-array is quite small for the analog part, beyond a 3×3 cluster, we start to take into account noisy pixels which reduce the total charge.

The detection efficiency is defined here as the ratio of physical hits in the sub-array studied to the number of reconstructed tracks in the telescope. Present analysis show that the detection efficiency of the S3 sub-array attains 98% depending on the signal to noise ratio cut made on the seed pixel (Fig. 11). These results are somehow satisfactory, but should be improved in the future.

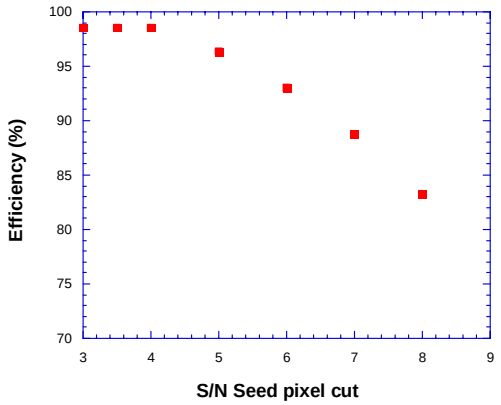



Fig. 11. Analog outputs: detection efficiency plotted versus Signal to Noise ratio cut on the seed pixel.

The digital outputs have also been characterized. Fig. 12 shows the detection efficiency versus discriminator threshold S/N cut. These data are consistent with the analog results. A detection efficiency higher than 95 % can be obtained even when a significant threshold voltage or a cut on Signal to Noise ratio is required. For reasonable low S/N value, an efficiency of 98% is obtained for all sub-arrays.

The present beam tests have proved that MIMOSA8 chip has good detection characteristics.

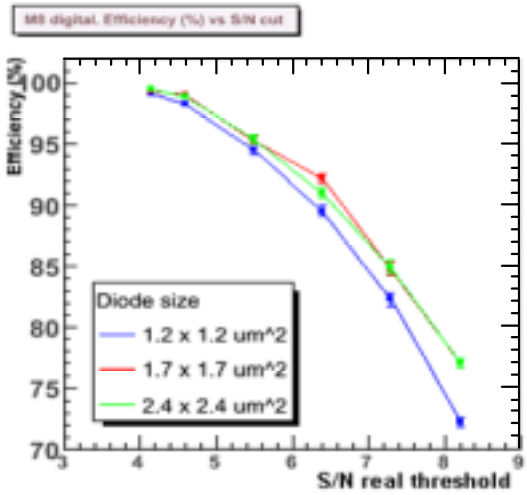



Fig. 12. Detection efficiency for increasing diode sizes as a function of the discriminator net S/N threshold on Seed pixel for the digital outputs.

## IV. Conclusions and Prospects

The results obtained show that the MIMOSA8 chip is a successful prototype of a fast CMOS pixel detector suitable for the inner part of the µVertex ILC detector. Future designs will be based on its analog and digital architecture. Tolerance to fast neutrons is also under study. These results will allows us to determine how the charge collection efficiency is affected by the displacement damage and how to possibly reduce this sensitivity. In a near future column analog to digital conversion could be implemented in order to optimize spatial resolution by improved computation.

MIMOSA8 shows that a big step forward in development of MAPS detectors used in high energy physics experiments is the integration of a high precision and fast circuitry for column parallel processing of signals, together with in pixel signal amplifying and processing.

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