# Design of the ANTARES LCM-DAQ Board Test Bench using a FPGA-based System-on-Chip approach

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**Abstract**

System-on-Chip (SoC) design approach consists in using state-of-the-art FPGA devices with embedded RISC processor cores, high-speed differential LVDS links and ready-to-use multi-gigabit transceivers allowing development of compact systems with substantial number of IO channels. Required performances are obtained through a subtle separation of tasks among closely cooperating programmable hardware logic and user-friendly software environment. We report about our experience in using the System-on-Chip (SoC) approach for designing the production test bench of the off-shore readout system for the ANTARES neutrino experiment.

*Key words:* System-On-Chip, SoC, FPGA, real-time, data acquisition systems
*PACS:*

## 1. Introduction

The use of platform FPGAs has become extremely attractive in designing high performance data acquisition (DAQ) systems for High Energy Physics experiment. FPGA-based System-on-Chip (SoC) architectures can achieve higher integration levels in low-power low-cost electronic systems by embedding RISC and DSP cores, on-chip memory blocks, busses and peripheral devices, multi-gigabit transceivers, steadily increasing quantities of programmable logic cells and supporting various differential or single-ended IO standards. By using existing large family of synthesizable IP (Intellectual Property) blocks combined with readily available software drivers and libraries, the SoC approach allows for rapid development of hardware and its prompt adaptation to a large variety of applications. Integration of application-specific logic blocks designed by users is facilitated by well-defined master and/or slave interfaces to peripheral busses of embedded processors. The paper reports on a FPGA-based SoC design for a flexible test bench for the off-shore read-out system of the ANTARES neutrino experiment [1]. Another application concerning a selective read-out processor (SRP) for the CMS electromagnetic calorimeter at LHC can be found in [2]. With this application we illustrate rapid development of a reliable functional test bench system.

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## 2. FPGA-based SoC Architectures

For our development we opted for devices from the Xilinx Virtex-II Pro FPGA family [3] which examplifies all the System-on-Chip features. In addition to the field programmable logic cells, these FPGA integrate hardware cores such as embedded processor (up to PowerPC405) that are able to run at 300MHz clock frequency and up to 20 RocketIO multi-gigabit transceivers (MGT). The bandwidth between the instruction/data cashes and adjacent block RAMs, where code software and data are stored, can be as high as 6.4 Gbit/s. Depending on their size, the devices integrate up to 8 Mbit of SRAM storage organized in 18 kbit true dual ported memory blocks of configurable depth and width.

The processor and transceiver cores are connected to the familiar programmable elements and routing resources of the Virtex-II FPGA fabric: configurable logic blocks with combinatorial, synchronous and distributed storage elements; digital clock managers, dual-port memories, multiplier blocks and general purpose IO bancs supporting most popular single-ended and differential I/O standards.

Development environment for the Virtex-II Pro FPGAs ranges from the low level VHDL description to the high level operating system layers and lets the hardware/software functionality to be tailored to the specific needs of applications. The IBM CoreConnect (`http://www-3.ibm.com/chips/products/coreconnect/`) technology provides versatile bus architecture for connecting the embedded processor with onchip instruction and data memory and several peripheral devices such as UARTs, Ethernet controllers as well as user defined logic blocks.

## 3. Test bench for the ANTARES LCM-DAQ board

The ANTARES (Astronomy with a Neutrino Telescope and Abyss environmental RESsearch) experiment is a large neutrino telescope designed to operate at a depth of 2500 m in the Mediterranean Sea. This detector will search for high energy cosmic neutrinos coming from extra-galactic sources and will hopefully allow for discovering dark matter signatures. It consists of a large 3D array of photomultipliers, arranged in 12 lines of about 300 m high, each of them carrying 25 storeys. To each node of this detector corresponds a Local Control Module (LCM) containing variety of electronic boards. The entire detector is linked to shore through an electro-optical cable.

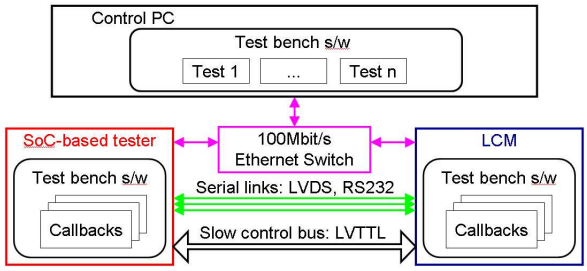


Fig. 1. ANTARES LCM-DAQ board test bench architecture

A test bench has been designed to assure production quality of some 350 LCM-DAQ boards located in LCMs. The LCM-DAQ board communicates through several interfaces. The RS485 and RS232 serial links send control commands to and gather information from instrumentation boards (temperature, compass, acoustics...). High speed LVDS links interact with four data acquisition boards populated by Analogue Ring Sampler (ARS) ASICs. An LVTTL bus is used for slow control and a 100 Mbit/s Ethernet interface is used to send collected data to shore. The LCM-DAQ board contains a FPGA for ARS data processing coupled to a on-board PowerPC processor running the VxWorks real-time OS.

The test bench architecture consists of 3 interacting systems: a LCM-DAQ board under test, a SoC-based tester board and a PC controlling all the tests (Fig. 1). The testing board, emulating the LCM-DAQ environment, is actually a Memec development kit with the 2vp30 Virtex2Pro FPGA. The versatility of the FPGA IO banks and readily available IP cores for Ethernet and RS485 / RS232 serial links greatly simplified the development of interfaces with the LCM-DAQ board. An embedded PowerPC processor runs Linux with

a NFS root file system on the Control PC. We have used slightly modified U-Boot free software (`http://u-boot.sourceforge.net/`) to boot the OS, and the BusyBox (`http://www.busybox.net/about.html`) project, which provides tiny versions of many common UNIX utilities into a single small executable, as a size-optimized root file system. The PowerPC and the peripheral busses are cadenced at 200 and 66 MHz.

The tests are divided into 3 sets: hardware tests of some components on the LCM-DAQ board (e.g. programming of the FPGA); emulation of ARS board (slow control communication and data flow with the ARS boards, simulation of trigger signaling); emulation of communications with others physical sensors (thermal, acoustical). For each of the LCM-DAQ functionality to test we have developed a corresponding IP core and a specialized C++ callback function.

Adopted SoC approach allowed us to trade complexity of IP cores against the complexity of corresponding software. Most of these IP cores became very simple to design because we only had to access FPGA registers in the read/write mode executing test sequences in software. The ARS data transfer tests, however, required development of high speed IP cores.

To test the slow control communications between the LCM-DAQ board and ARS boards, we developed an IP core emulating the presence of the 12 ARS ASICs and handling the SPI (Serial Peripheral Interface) protocol. The embedded processor on its turn receives and interprets the slow control command and eventually responds on them according to the developed C++ software.

Running Linux on the embedded platform made possible to reuse the ANTARES DAQ software framework, via a simple cross-compilation step. The control PC, the LCM-DAQ board and the tester board run C++ applications implementing a control state machine from the ANTARES RunControl software. The PC sends commands to LCM-DAQ and tester boards through the ControlHost message passing interface (`http://www.nikhef.nl/ruud/HTML/choo_manual.html`) keeping the boards perfectly synchronous with the state machine. The test bench operations are launched through a C++ GTK-based GUI which sends commands through a message passing server to each of the 3 interacting machines and generates for each LCM-DAQ board a test bench report used to populate the ANTARES quality control database.

The test bench allows for hot-swapping of the LCM-DAQ boards. It takes 15 minutes to accomplish a complete test. The production test bench is already in use since March 2005. By the end of september 2005, 150 LCM-DAQ boards were manufactured, tested and, thus, ready for integration.

## 4. Conclusion

Let us emphasize by the light of our experience the main advantages of using a SoC approach for the LCM-DAQ board test bench design. First, we avoid dedicated hardware developments for prototyping by adapting the commercially available hardware allowing rapid progress in firmware/software design. The developments takes benefits from the availability of a large variety of synthesizable IP cores with supporting software libraries, drivers and embedded operating systems. The SoC design greatly simplifies the testing and integration of the application cores by using the test code running on the embedded processor. Finally, the ANTARES test bench developments lay a good ground for KM3NeT research and developments, more precisely the design of a new version of the LCM-DAQ boards where the ARS FPGA and the on-board PowerPC will be integrated within a single platform FPGA.

## References


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