IDeF-X V1.0: a new sixteen-channel low noise analogue front-end for Cd(Zn)Te detectors

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Abstract

Joint progress in Cd(Zn)Te detectors, microelectronics and interconnection technologies open the way for a new generation of instruments for physics and astrophysics applications in the energy range from 1 to 1000 keV. Even working between –20 and 20°C, these instruments will offer high spatial resolution (pixel size ranging from 300 × 300 µm² to few mm²), high spectral response and high detection efficiency. To reach these goals, reliable, highly integrated, low noise and low power consumption electronics is mandatory. Our group is currently developing a new full-custom detector front-end ASIC named IDeF-X, for modular spectro-imaging system based on the use of Cd(Zn)Te detectors. We present the most recent version of IDeF-X which is a sixteen channels analogue readout chip for hard X-ray spectroscopy. It has been processed with the standard AMS 0.35 µm CMOS technology. Each channel consists of a charge sensitive preamplifier, a pole zero cancellation stage, a variable peaking time filter and an output buffer. IDeF-X is designed to be DC coupled to detectors having a low dark current at room temperature and is optimized for input capacitance ranging from 2 to 5pF.

Keywords: ASIC; Analogue front-end electronics; CdTe; CdZnTe; Hard X-ray spectroscopy; Gamma-ray spectroscopy

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1. Introduction

The evolution of the Cd(Zn)Te detectors properties requires a continuous improvement of the electronic front-end in terms of geometry, noise, and power consumption. This is why our group is currently developing a new modular spectro-imaging system based on Cd(Zn)Te detectors coupled to dedicated full-custom readout ASIC, named IDeF-X (Imaging Detector Front-end). The development of the IDeF-X front-end includes several steps from the set of stand-alone Charge Sensitive preAmplifiers prototypes (CSA) [1] to a complex multi-channel circuit for high-pixel density Cd(Zn)Te detectors readout. The final device (ASIC+Detector) is planned to be used in large area cameras (100 to 1000 cm^2) for space borne astrophysics, either on focusing hard X-ray telescope (e.g. SIMBOL-X [2], ranging from 4 to 150 keV), or on a large area position sensitive detector of a coded aperture gamma-ray telescope (e.g. ECLAIRs [3], ranging from4 to 600 keV). The IDeF-X chip family is realized using the standard AMS CMOS 0.35 µm technology. The encouraging results obtained with our previous chip named IDeF-X V0, allowed us to validate the use of this technology for our needs and to select one CSA design well suited to our future applications involving Cd(Zn)Te detectors [1]. Moreover, we demonstrated that our CSA design was tolerant to the ionizing dose higher than 200 krad, which makes it compliant for space environment. In this paper, we present the most recent version of IDeF-X chips family. It is a sixteen channels analogue readout chip intended for use with low capacitive and low dark current detectors.

This paper is structured as follows: Section 2 presents the IDeF-X V1.0 ASIC design. Section 3 presents the equivalent noise charge measurements (ENC) and discussion of the influences of the input capacitance and detector dark current on the noise performances. In the end, section 3 describes the spectral response when the chip is connected to a low capacitance and low dark current CdTe Schottky detector.

2. IDeF-X V1.0 ASIC design

IDeF-X V1.0 chip is a complete 16 channels analogue front-end. Each channel is fully independent. The design is optimized for low input capacitance (2 to 5pF) and low dark current (1pA to 1nA) hard X-ray detectors used in the energy range from 4 keV up to 300 keV. Each channel includes a CSA, a pole zero cancellation stage (PZC), a fourth order Sallen & Key (SK) type shaper, and an output buffer. The CSA is inherited from the previous IDeF-X V0 [1]. It is based on a classical "folded cascode amplifier" with a PMOS type input transistor. The continuous reset system is done by a feedback PMOS transistor operating in the subthreshold region. The current that flows through the channel of this transistor is the leakage current of the detector. The PZC stage is used to avoid long duration undershoots at the output. Moreover it amplifies the signal at the output of the CSA and allows optimized DC coupling by minimizing the influence of the dark current on the gain. The PZC stage is based on reference [4]. The fourth order shaper includes two second order SK low pass filters with tunable shaping times. The SK structure can operate a second order filter with only one active device (amplifiers, OTA). Its power consumption is therefore optimized in comparison with classical filters. The tunable shaping time is done by the commutation of series resistors in the filters. The ASIC is equipped with a test input used to inject a calibrated charge through the on-chip injection capacitance placed in front of every channel. Finally, in order to simulate a detector current or to compensate a reverse detector current, each channel includes a tunable current source *il*. The main characteristics of IDeF-X V1.0 are summarized in table 1.

3. Results

3.1 Equivalent noise charge measurements (ENC)

3.1.1 ENC measurements setup

The first characterization of the circuit consists in measuring the ENC of each channel as a function of the peaking time (τ_{peak}). To perform the measurements, two test boards have been designed. First, the

polarization board allows biasing, configuration, injection and response measurements. The polarization board is a standard printed circuit board (PCB) designed in a standard epoxy material (FR4). Second, the chip board carries the ASIC. Three chip boards have been designed to study the influences of the setup (JLCC parasitic capacitance, connectors, PCB parasitic capacitance and dielectric losses) on the noise behavior of the chip. To reduce excessive noise due to dielectric losses, the chip boards are fabricated with glass-Teflon: on the first one (CB1), the chip is mounted in a JLCC carrier soldered on the board. On the second board (CB2), the chip is directly mounted on the board. In the last board (CB3), the chip is also mounted on the board but the inputs are not wire bonded to the PCB.

A calibrated signal is injected at the test input. The channel outputs are connected to external multiplexers, ADC and acquisition station. In this configuration, we measure simultaneously the amplitude and the noise of the channels. To keep the paper clear, we report in the following only results obtained on the channel #8, which behaves like all other channels but which is also equipped with intermediate test points at every analogue stages (CSA, PZC, SK and Buffer).

The lowest ENC with the three boards are reached at τ_{peak} = 6 µs. The results are summarized in table 2. As expected, the best ENC is obtained with the CB3 board where the inputs of the chip are totally disconnected from the setup - no bonding at the inputs. This board is used to measure the intrinsic performances of the circuit, i.e. the floor noise of the design. The ENC floor is found to be 35 e^- rms. This result is in excellent agreement with the previous IDeF-X V0 chip characterization [1], where the floor noise was found to be 33 e^- rms. We derive from these measurements that the noise contribution of the additional stages in the channel (PZC and SK shapers) is negligible. The noise measured on CB2 and CB1 at τ_{peak} = 6 µs was found to be 55 and 100 e^- rms respectively.

3.1.2 ENC vs. additional input capacitance.

In order to predict the performances of the chip connected to a detector, we need to study the influence of the input capacitance on the noise behavior of the circuit. Moreover, this measurement allows us to

understand the contribution of the setup. For those measurements, we use the CB2 board. At the input of channel #8 we solder a set of additional parasitic and calibrated capacitances (figure 2). The measurements are obtained without any leakage current (*il* < 1 pA) minimizing the parallel noise. For each additional input capacitance, we measure the ENC at two different peaking time values. At a given peaking time, the ENC is a linear function of the additional input capacitance (figure 3), and we found:

$$ENC(at\ \tau_{peak} = 6\ \mu s) = 52e^- + 6\ e^-/pF \qquad \text{and} \qquad ENC(at\ \tau_{peak} = 1\ \mu s) = 111e^- + 17.5\ e^-/pF$$

The same characterization on the CB1 board leads exactly to the same noise sensitivity to the parasitic capacitance. As expected, the minimal ENC is obtained at the highest peaking time: the theoritical expression of the ENC at the output of the shapers is :

$$ENC^2 = C_{tot}^2\left(\frac{\alpha_d}{\tau_{peak}} + \alpha_{1/f}\right) + \alpha_{//} \cdot il \cdot \tau_{peak} \qquad \text{(eq. 1)}$$

Where $C_{tot} = C_{board} + C_{add} + C_{in}$; C_{in} is the total capacitance into the chip at the input of the CSA ; α_d is a parameter that depends on the filter order as well as the transconductance of the input transistor of the CSA ; $\alpha_{1/f}$ is a parameter that depends on the filter order as well as technological parameters and the area of the input transistor ; $\alpha_{//}$ is a parameter that depends on the filter order ; *il* is the leakage current injected at the input of the CSA.

When no leakage current is present at the input of the channel (*il* < 1 pA) the noise is dominated by the *1/f* and the thermal noise of the CSA input transistor. The *1/f* noise is independent of τ_{peak} while the series noise decreases with τ_{peak}. As a result, the minimal ENC is reached at the highest values of τ_{peak}. To estimate the parasitic capacitance of the board itself, we can compare this plot to the ENC value found with the CB3 board at the same peaking time. In the case of the CB3 board, the input is not wire bonded to the board, so we have C_{tot}=C_{in}. The same calculus can be done at the two peaking times:

At τ_{peak} = 6 µs we find C_{board} = *(52-35)/6 = 3 pF* and at τ_{peak} = 1 µs we find C_{board} = *(111-60)/17.5 = 2.9 pF*

The fact that we found the same board capacitance at the two peaking times demonstrates that the parallel noise and the noise due to dielectric losses can be neglected.

3.1.3 ENC vs. leakage current

The leakage current of the detector is the second key parameter which limits the spectral response (parallel noise) after the total capacitance (including detector capacitance) at the CSA input (series and *1/f* noise). In order to estimate the best spectral resolution achievable with IDeF-X coupled to a detector, we need to study the influence of the leakage current on the noise behavior. To do so, we use the calibrated current source *il* to simulate the dark current of the detector. The *il* current calibration is operated by measuring the signal fall-time at the output of the CSA, which is inversely proportional to the current through the reset transistor as described in ref. [1]. The ENC measurements have been done with and without additional capacitance (C_{add} = 2.2 pF, ie. C_{tot} ~ 5 pF). For each leakage current, we determine the minimum value of the ENC vs. τ_{peak} characteristics (ENC_{min}). ENC_{min} is reported as a function of the injected leakage current *il* in figure 4 and the fitted curves are plotted using the theoritical expression as follows (eq.2):

$$ENC_{\min}^2 = 2\sqrt{\alpha_d \cdot \alpha_{//} \cdot C_{tot}^2 \cdot il} + \alpha_{1/f} \cdot C_{tot}^2 \qquad \text{(eq. 2)}$$

There are three different regions of interest in this plot:

– At very low dark current (*il* < 10 pA), the minimal *ENC* is reached at the highest peaking time. For these τ_{peak} values, the *1/f* noise is dominant and the leakage current has no significant influence.

– For higher leakage currents (10 pA < *il* < 500 pA), the minimal ENC is reached when the series noise and the parallel noise are equal and higher than the *1/f* noise. The slope factor $\delta ENC / \delta il$ is $1/4$.

– For “very high” leakage currents (*il* > 500 pA), the theoretical minimal ENC can not be reached because the smaller τ_{peak} values of IDeF-X V1.0 is not short enough. The noise is dominated by the parallel noise, the slope factor tends to $1/2$, and eq. 2 is no more applicable.

3.2 Spectroscopy measurements

IDeF-X V1.0 mounted on the board CB1 (JLCC package) has been evaluated by performing measurements at room temperature with CdTe detector. We have connected a 4.1×4.1×0.5 mm^3 CdTe (ACRORAD) equipped with a Schottky contact at the anode and a guard ring at the cathode (1 mm guard ring surrounding the 2×2 mm² pixel). The detector was biased at 300V. The spectrum of figure 5 has been acquired using τ_{peak} = 6 µs with an ^{241}Am source. We found that the best spectrum was obtained at the highest peaking time. This is consistent with the very low leakage current (less than 50 pA) measured on the detector at 300V. The energy resolution is 1.68 keV FWHM at 59.5 keV and 1.3 keV FWHM at 13.8 keV. Finally, the very low energy threshold value of 2.7 keV makes this chip suitable for applications at very low energy for astrophysics [3].

The spectral response is similar to the one obtained with our first IDeF-X V0 chip. Today, these satisfactory performances are limited by the setup, and especially by the excessive parasitic capacitance and dielectric losses in the substrate of the detector. In the near future, improvements of the setup will help to reach much better performances. We expect for this detector type (~ 50 pA) and a total additional input capacitance less than 2 pF, energy resolution between 0.8 and 1 keV FWHM at 60 keV (see figure 4).

4. Conclusion

The IdeF-X V1.0 is a very low noise multi channel integrated circuit. It is optimized for the readout of low capacitive (2-5pF) and low dark current (~ 1 pA to few nA) Cd(Zn)Te detectors or pixel arrays [5] for future X- and gamma-ray astronomy space missions. The noise performances of this chip are very promising since the floor ENC was found to be 35 e^- rms. We have studied its behavior with respect to the total input capacitance and leakage current. We derived from these measurements that the chip connected to Cd(Zn)Te crystals will permit to reach very high spectral response, between 0.8 and 1 keV FWHM at 60 keV.

5. Acknowledgment

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References

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Table 1

Parameter	*Value*
Chip size	2355 µm × 4040 µm
Number of channel	16
Power supply	3.3V
Power dissipated	2.26 mW/channel
Gain	200 mV/fC at 6µs peaking time
Dynamic range	-40000 to 40000 e^- (0 - 176 keV for CdTe)
Shaping type	unipolar
Peaking times (in µs)	0.5 / 0.9 / 1.5 / 2.4 / 3 / 4 / 4.5 / 6

Table 2

Test board name	*IDeF-X Configuration*	*ENC at 6µs (in e^- rms)*
CB1	Packaged in JLCC carrier	100
CB2	Directly wire bonded on board	55
CB3	Chip input pads not bonded	35

Figure 1

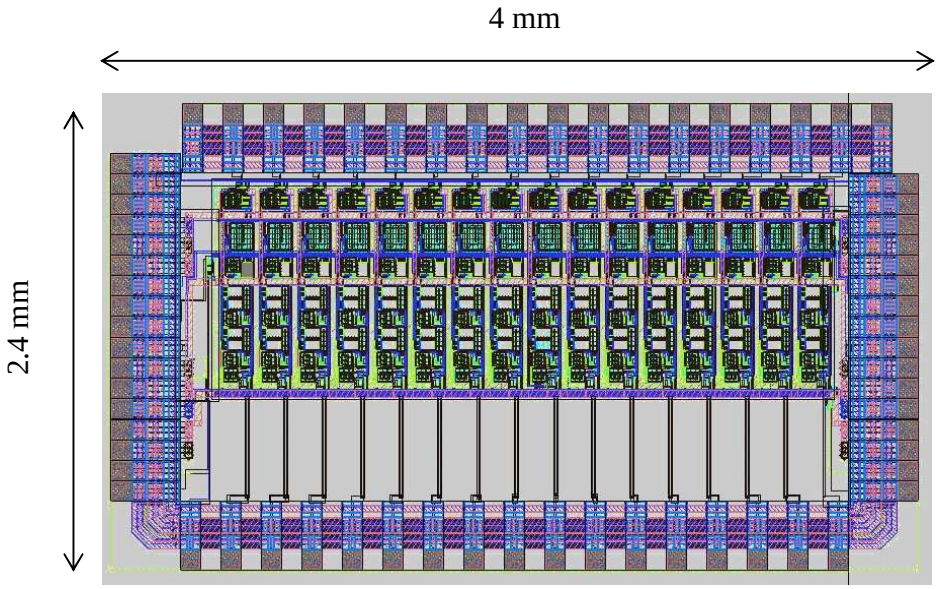

Figure 2

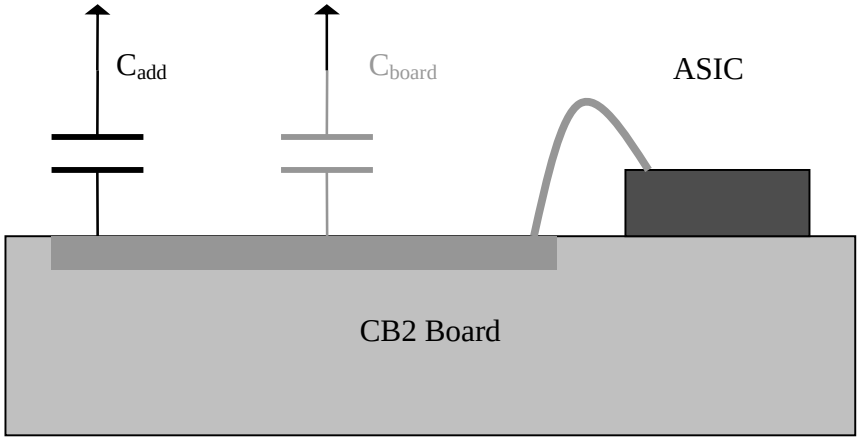

Figure 3

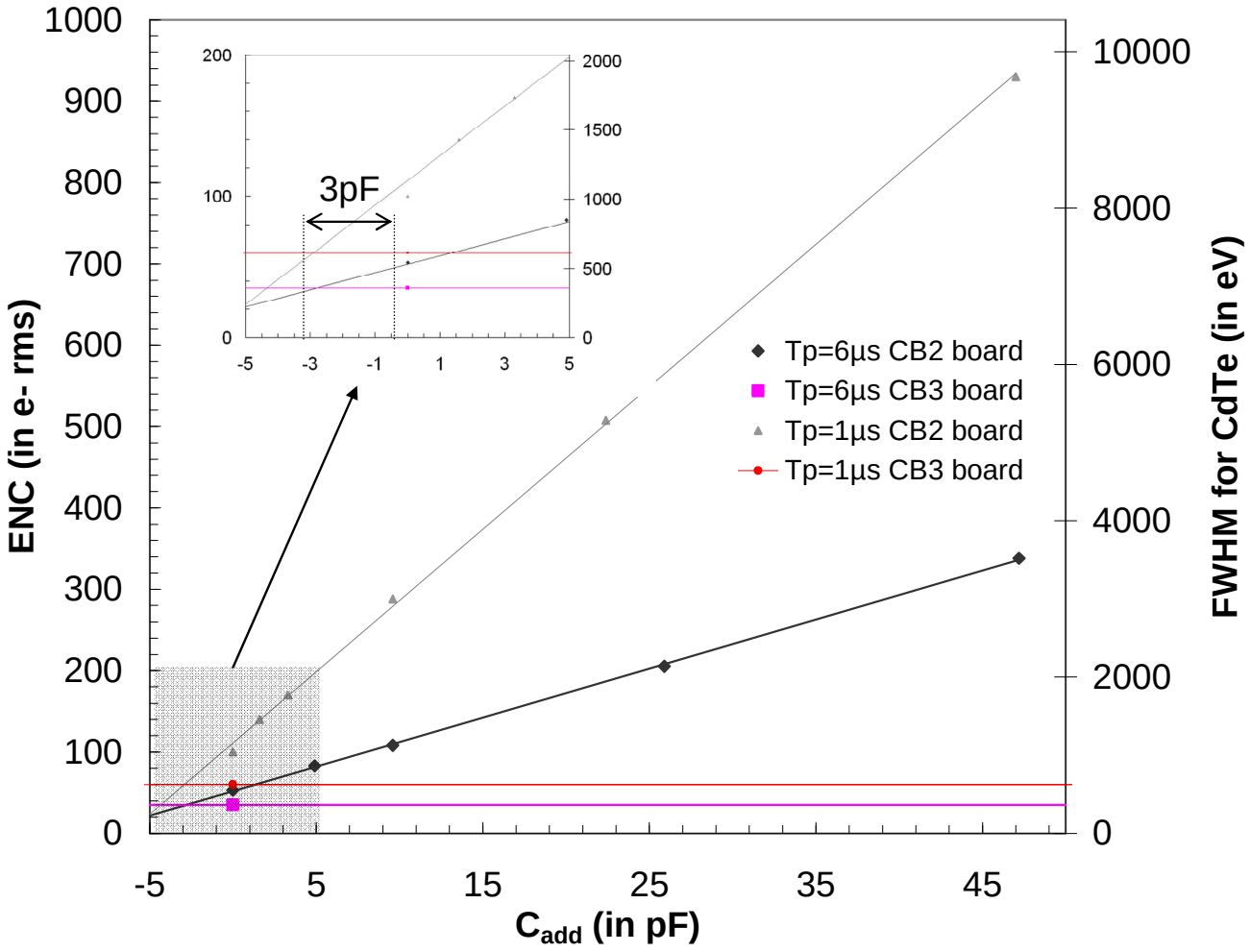
ENC (in e- rms)
FWHM for CdTe (in eV)
C_add (in pF)
3pF
Tp=6µs CB2 board
Tp=6µs CB3 board
Tp=1µs CB2 board
Tp=1µs CB3 board

Figure 4

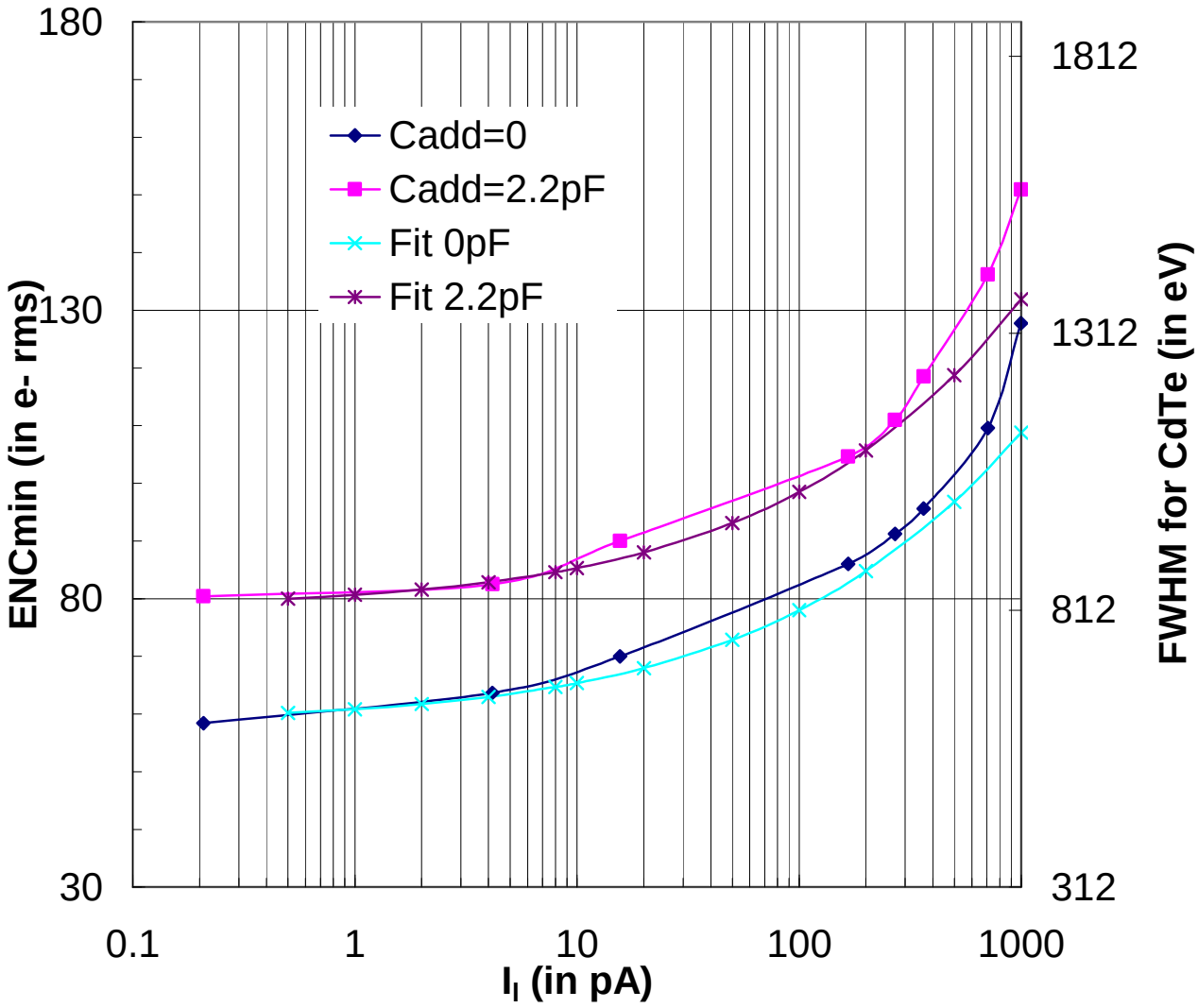
180
130
80
30
1812
1312
812
312
0.1
1
10
100
1000
Cadd=0
Cadd=2.2pF
Fit 0pF
Fit 2.2pF
ENCmin (in e- rms)
FWHM for CdTe (in eV)
I_I (in pA)

Figure 5

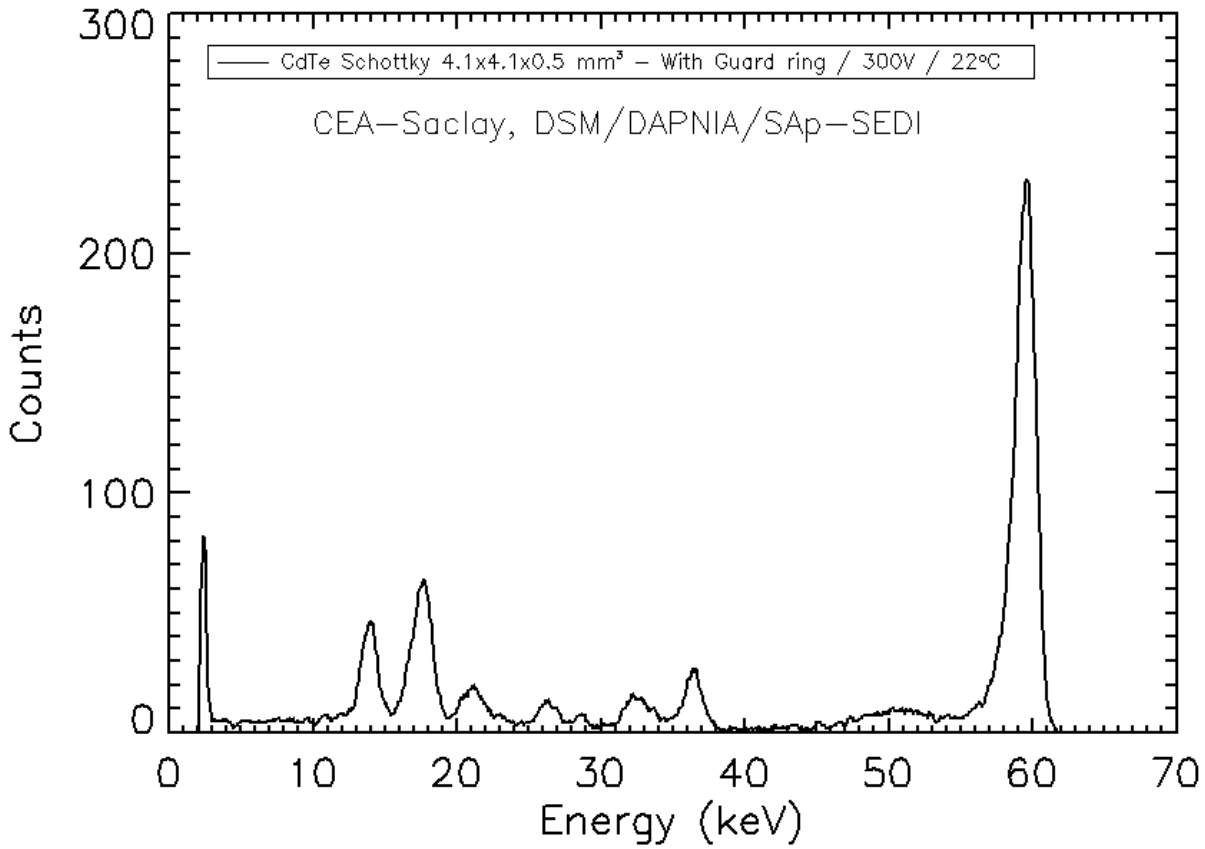
CdTe Schottky 4.1x4.1x0.5 mm³ – With Guard ring / 300V / 22°C
CEA–Saclay, DSM/DAPNIA/SAp–SEDI
Counts
Energy (keV)
0
100
200
300
0
10
20
30
40
50
60
70

Table captions

Table 1: IDeF-X V1.0 main characteristics.

Table 2: IDeF-X V1.0 Best reachable resolutions with the different chip boards.

Figure Captions

Figure 1: IDeF-X V1.0 layout. Sixteen analogue channels for high energy high resolution spectroscopy.

Figure 2: Setup for the evaluation of the input capacitance influence on the noise performances of IDeF-X V1.0 ; the circuit is directly wire bonded on the CB2 board and an additional input capacitance C_{add} is soldered at one of the inputs (channel 8) of the chip.

Figure 3: ENC as a function of additional input capacitance C_{add} at two different peaking times. The best performances are reached at 6µs. In that case, the slope is evaluated to 6 e^-/pF.

Figure 4: ENC_{min} as a function of input leakage current for two different additional input capacitances: measurement results and fits using (eq.2). For a leakage current lower than 10pA, the minimal ENC is almost constant. At higher leakage currents the parallel noise is no more negligible and the minimal ENC increase with the dark current.

Figure 5: Spectrum of an ^{241}Am source obtained with a $4.1 \times 4.1 \times 0.5$ mm^3 CdTe detector equipped with a Schottky contact at the anode. The cathode is 2×2 mm² pixel surrounded by a 1 mm guard ring. The detector is biased under 300 V at 22°C and is connected to the channel 1 of IDeF-X V1.0 at a 6µs peaking time.