DIGITAL LOW LEVEL RF SYSTEM FOR SOLEIL

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Abstract

In the SOLEIL storage ring, two cryomodules, each containing a pair of 352 MHz superconducting cavities, will provide the maximum power of 560 kW, required at the nominal energy of 2.75 GeV with the full beam current of 500 mA. Presently, an analogue Low Level RF system is successfully operating to control the amplitude and phase of the accelerating voltage.

A fast digital FPGA based I-Q feedback is currently under development. The digital I-Q loop is realised with a HERON IO2 FPGA module using a Virtex II with 1M gates. The performance of the digital LLRF system has been evaluated using a Matlab-Simulink based simulation tool taking into account different features (loop delays, bandwidth limitation, extra power budget). The hardware design is described and the first experimental results are reported.

INTRODUCTION

The Low Level RF system (LLRF) presently used in the SOLEIL storage ring (SR) consists in fully analogue "slow" amplitude, phase and frequency loops, complemented with a direct RF feedback in order to insure the Robinson stability at high beam loading [1]. The bandwidth of the slow amplitude and phase loops was set below 1 kHz and the gain of the RF feedback to 8, its bandwidth being around 30 kHz. Under these conditions, one routinely stores up to 300 mA with a stability margin large enough to easily reach up 500 mA. At 300 mA, the residual beam phase oscillations were measured below 0.1° rms.

As an alternative to the existing analogue system, a fast digital FPGA (Field Programmable Gate Array) based I/Q feedback, was developed in collaboration with CEA [2]. A prototype of this digital LLRF was recently tested and experimentally validated. Computed performance and experimental results for the digital system are reported.

DIGITAL LLRF ARCHITECTURE

The architecture of the SOLEIL digital LLRF system is based on a FPGA, with 12 bits ADC's, 14 bits DAC's, analogue IQ modulator and IF frequency conversion (see Fig. 1). The HERON IO2 module has been selected for the digital signal processing because of its short latency between the input interface (ADC) and output interface (DAC) through the Xilinx Virtex II FPGA.

To synchronize this process, one used a sine generator instead of the implemented 160 MHz clock PLL, which output level is too low for insuring a minimum of jitter and clock errors in the FPGA. Moreover this PLL requires a reconfiguration each time its supply is switched off. An improved configuration is being investigated.

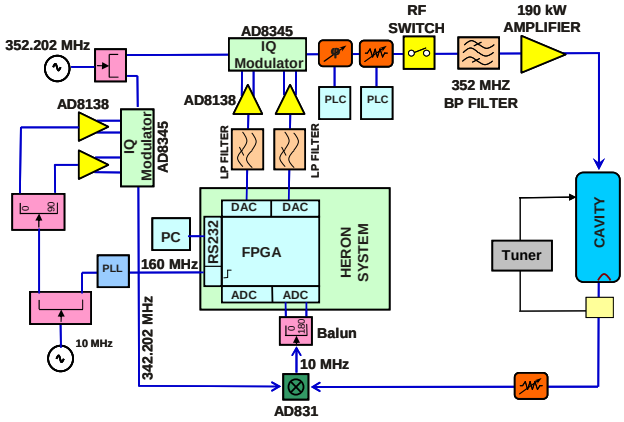

Figure 1: Block diagram of the digital LLRF

In order to have a better ratio signal/noise, the ADC's are operated in differential mode using a balun which frequency range is 10 kHz – 60 MHz.

The 352 MHz RF reference signal and 10 MHz machine master clock are mixed via a IQ modulator to generate the 342 MHz LO signal used to down-convert the 352 MHz cavity RF signal into a 10 MHz IF signal for the signal processing. This allows following the variation of the RF reference frequency which is driven by the Slow Orbit Feedback. The down-converted 10 MHz IF signal is sampled at 40 MHz via the ADC.

A 352 MHz bandpass filter with a bandwidth of 1.8 MHz is inserted upstream of the high power solid state amplifier, as a protection against fast transients induced by possible digital bug.

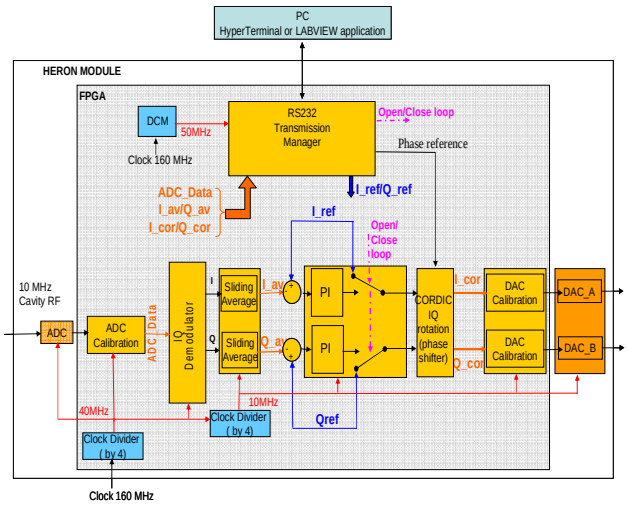

Figure 2: Digital LLRF building blocks

FPGA architecture

For the LLRF application, the building blocks in the FPGA are composed of a digital IQ demodulator, a few proportional/integral controller functions, clock and data managers, which are shown in Figure 2.

The digital IQ demodulator works with 4 samples over the 10 MHz period. As the FPGA HERON board is synchronized with the machine 10 MHz master oscillator, the demodulator does not need any reference signal.

The proportional gain of digital PI controller can be set to values which are powers of two (2^n) and its integral gain is fixed to $1/2^{18} = 1/262144$.

A CORDIC rotation block is implemented to adjust the loop phase at the operating value. It works correctly up to a proportional gain of 4; above this value the system becomes unstable, due to the too long latency of the CORDIC (22 clock cycles of 10 MHz). That will be improved using a rotation block based on multipliers and adders with cosine and sine table which will take only 2 clock cycles. The implementation of this faster rotation block upstream and downstream of the signal processing chain is needed to facilitate the phase adjustment and to allow for a doubling of the proportional gain.

The Heron board provides a basic RS232 interface with the FPGA. A RS232 manager control block was developed, in order to communicate with a PC, using a HyperTerminal or a Labview application (see Fig. 3). This block also manages the IQ calibration, the open/close loop commands and measurement data taken at different point of the chain. Phase adjustment can be done via the PC as well.

A correction table, stored in ROMs inside the FPGA, compensates for the DAC's and ADC's coding errors.

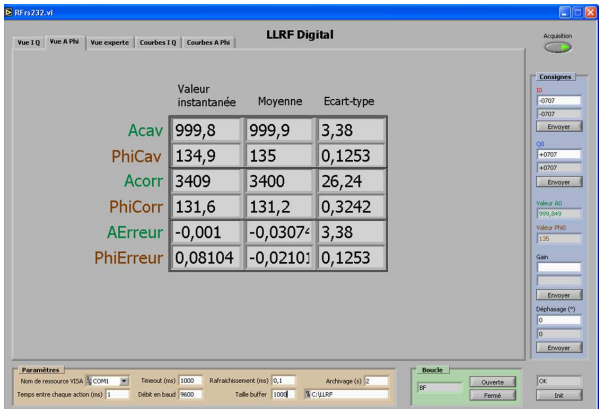

Figure 3: LABVIEW data display (I_{beam} = 300 mA)

EXPERIMENTAL RESULTS

First, the system was tested with a cavity simulator, implemented in the FPGA between PI controller and the demodulator. The SOLEIL cavity was simulated by a second order IIR low-pass filter with a 3 kHz bandwidth. The realisation of this filter required a reduction of the 10 MHz clock frequency down to 1 MHz, using a decimation function on the demodulator output data. This test confirmed the good functioning of all building blocks of the chain.

For the tests on the real cavity, one cavity of the cryomodule was controlled by the digital system, the other by the analogue system. The phase of the RF plant as compared to the injected beam and the relative phase of the two cavities were adjusted such to optimise the injection efficiency and balance the RF power of the two cavities.

The system was stable with a proportional gain up to 4, while with 8, it became instable due to the too large latency of the CORDIC rotation block (2.2 µs). Therefore the rotation block was removed and phase adjustments were realised in an analogue way. So far the 1 MV cavity voltage could be controlled by the digital system with a good accuracy. Figure 4 shows experimental measurements with electron beam current from 0 to 300 mA.

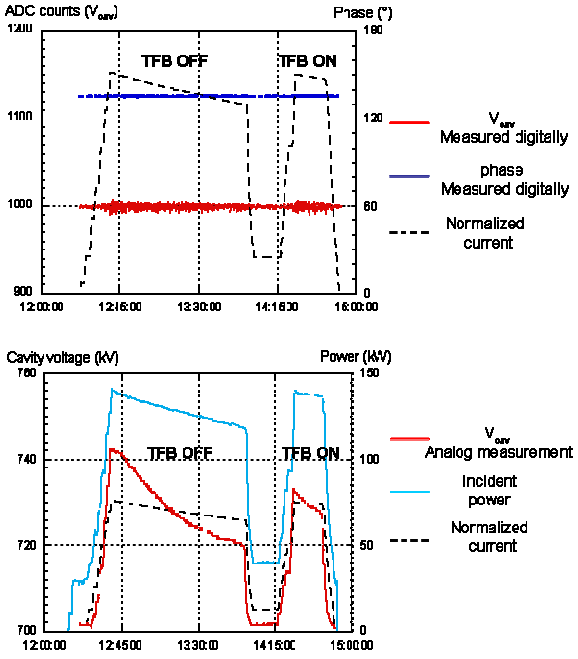

Figure 4: Experimental results with a maximum current of 300 mA

Without beam loading, the measured phase and amplitude stability were about 0.15° rms and 1 ‰ rms, respectively in closed loop. They slightly degraded to 0.2° rms and 0.3 % rms with a 300 mA beam. One observed a small discrepancy between the digital and analogue measurements of the cavity voltage: the latter, performed by means of a wave detector is slightly varying (about 5%) with the beam loading while the former remains constant. We also noticed that this effect was depending on whether the transverse multibunch feedback (TFB) was ON or OFF. That requires further investigations. Figure 5 shows the statistic error distribution for the amplitude and phase with beam loading.

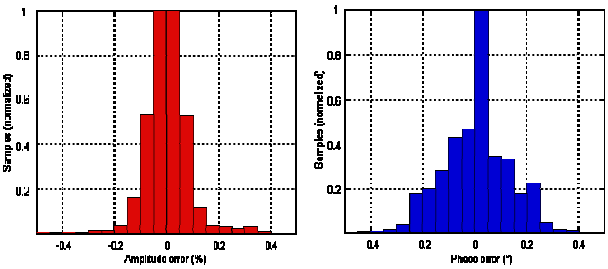

Figure 5: amplitude (left) and phase (right) error distributions.

A Matlab-simulink based simulation tool has been developped [3] for the optimization of the LLRF system parameters taking into account different features (microphonics disturbance, injection error, loop delays, bandwidth, limitation quantization, extra power budget, etc.). Micro-phonic disturbances have been measured on a SOLEIL cavity. Figure 6 shows the measured cavity resonant frequency variations versus time, which were used as data input for the simulation.

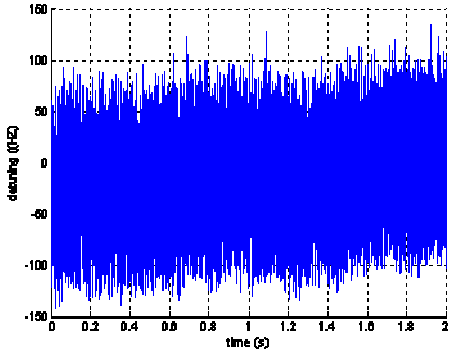

Figure 6: Cavity detuning due to microphonics

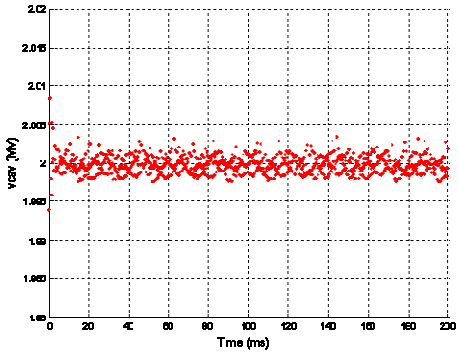

Figure 7: Simulated cavity voltage amplitude stability

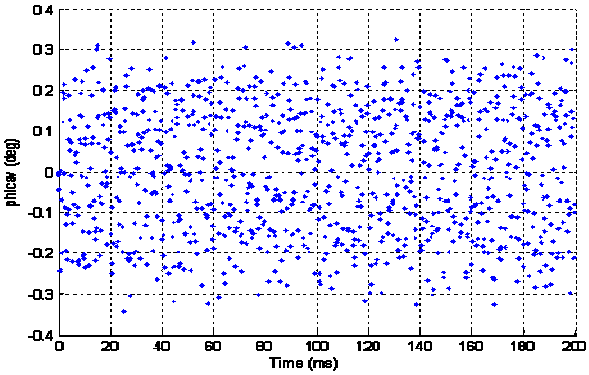

Figure 8: Simulated cavity voltage phase stability

The RF feedback was simulated with a delay of 3 µs, which is the estimated latency of our digital LLRF system, and a proportional gain of 8. The cavity voltage amplitude and phase are displayed in Figures 7 and 8. In steady state, the computed values of the residual errors are 0.1% rms in amplitude and 0.15°rms in phase, very close to the experimental results.

CONCLUSION

A fast digital phase and amplitude feedback, based on a FPGA, an analogue IQ modulator and IF frequency conversion, has been developed for SOLEIL, as an alternative to the analogue LLRF system which is presently in use.

A prototype of the new digital LLRF system was recently tested on one of the SOLEIL SR cavity. Its measured performance is similar to that achieved with the existing analogue system: residual amplitude and phase errors of about 0.1% rms and 0.1° rms, respectively, with a proportional gain of 8.

The main advantages of the digital version are the flexibility (possibility of adapting to any RF frequency with minor modification of the analogue part), modularity and simplicity (the 3 analogue loops are replaced by a single digital one).

ACKNOWLEDGEMENT

The authors would like to thank all the members of CEA/DSM/DAPNIA and SOLEIL who contributed to the success of this development.

REFERENCES

[1] P. Marchand et al, Commissioning of the SOLEIL RF System, this conference.
[2] P. Marchand et al, Proc. of EPAC06, TUPCH186.
[3] M. Diop et al, Modelling and Simulation of the RF system for SOLEIL Synchrotron, LLRF05 workshop.