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SIXTH FRAMEWORK PROGRAMME

IP-EUROTRANS
- INTEGRATED PROJECT ON EUROPEAN TRANSMUTATION -

FINAL REPORT: VHDL ARCHITECTURE AND SYNTHESIS

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1 INTRODUCTION

The European Transmutation Demonstration program requires a high power proton accelerator operating in CW mode up to 16 MW. A reference design is being developed since 2001 through the PDS-XADS and the EUROTRANS programmes[1]. It is mainly based on a superconducting linac.

The goal of the EUROTRANS task 1.3.4 "Conceptual design of an RF control system for fault tolerant operation of the linear accelerator" is to perform a full conceptual design of a specific Low Level RF system for the 704 MHz elliptical superconducting cavities. The main specifications for such RF control system were presented in a previous deliverable[2]: the stability for amplitude and phase of the accelerating cavities' voltage must be respectively ±0.5% and ±0.5°. Another strong constraint concerns the reliability of the accelerator, since the number of trips longer than one second must not exceed a few per year[3].

A superconducting RF cavity is sensitive to various perturbations like mechanical vibrations (microphonics) and Lorentz force detuning. These perturbations produce a significant detuning of the cavity, leading a strong instability for the amplitude and phase of the field because of the narrow bandwidth of the accelerating mode. Therefore, a fast RF feedback system is needed to realize the control of the field, and some power margin is required to fulfil the specifications. The modelling of the cavity interacting with proton beam and perturbations, presented in the previous Task 1.3.4 deliverable[4], provides a simulation approach in order to define the loop gain ensuring good system stability and to determine the additional RF power needed to ensure good cavity operation under perturbations.

Currently, accelerator projects are employing Digital Low Level RF (DLLRF) systems to achieve amplitude and phase stability of the accelerating field[5]. The recent progress in digital and telecommunication technology enables the use of new powerful real time digital systems in the accelerator framework. To provide low latency in the feedback loop and avoid loop instabilities, ADCs and DACs with few cycles conversion time, Field Programmable Gate Array (FPGA) and Digital Signal Processor (DSP) are implemented on a single chip to achieve the RF control within a few hundred nanoseconds of latency. Moreover, the digital implementation offers a high flexibility for the feedback system: complex algorithms and procedures, implemented within the digital signal processing, can be changed and remotely updated via software without hardware modifications. A unique hardware can therefore be developed for all the different cavities, and just some parameters have to be adapted[6]. This digital implementation also offers high reproducibility, which is difficult to obtain with analogue system. Finally, this kind of system provides extensive and built-in diagnostics and fast communication capabilities, which are essential for fast update of the cavities' set-points in the event of RF fault recovery. In summary, DLLRF systems require high-speed digital design for the hardware, and FPGA/DSP software skills to implement digital signal processing. The purpose of this document is to present the main characteristics of a system able to fulfill the EUROTRANS specifications.

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[1] J-L. Biarrotte et al., "A reference accelerator scheme for ADS applications", NIM A 562 (2006) 565-661.
[2] J-L. Biarrotte, "General specifications for all the tasks of DM1/WP1.3", Eurotrans Deliverable D 1.18.
[3] J-L. Biarrotte, C. Joly, M. Luong, "Preliminary RF Control Specifications", Eurotrans Deliverable D 1.17.
[4] M.Luong, O. Piquet, "RF control System Modeling", Eurotrans Deliverable D 1.40.
[5] M.E. Angoletta, "Digital Low Level RF", EPAC 2006, Edinburgh.
[6] P.Galdemard et al., "The architecture of the low level RF electronics for Spiral 2", LLRF 2007, Knoxville.

2 RF SYSTEM GENERAL ARCHITECTURE

A baseline generic scheme of the XT-ADS RF system is proposed in Figure 1. It consists of a 704 MHz β=0.5 superconducting cavity driven by an RF power source and a digital Low Level RF system to achieve the amplitude and phase stability of the accelerator field. The regulation loop principle is based on the processing of the transmitted RF signal coming directly from the cavity pick-up.

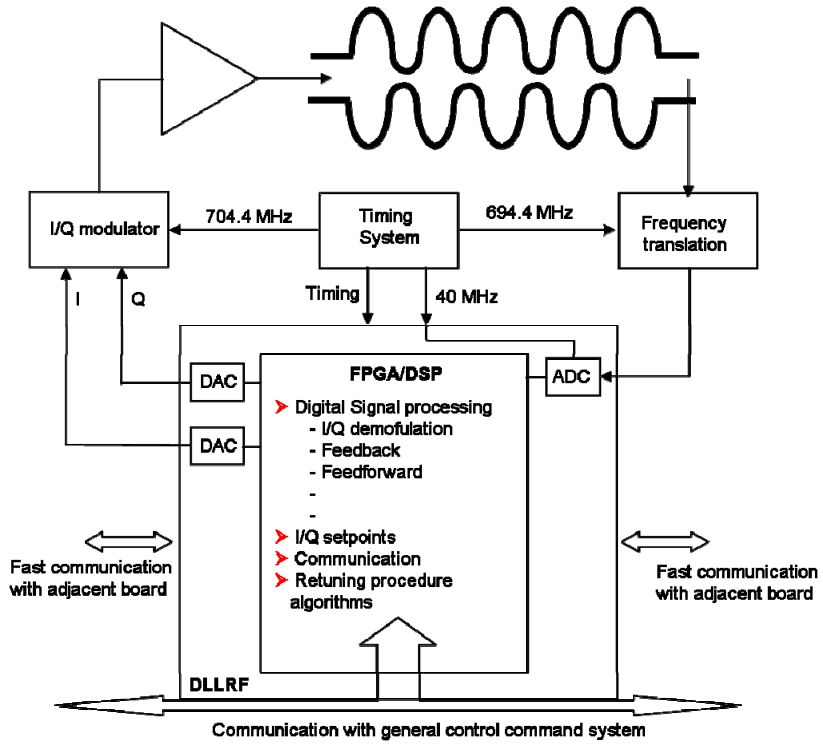


Figure 1: Scheme of an XT-ADS cavity's RF system.

The RF control system can also provide other functions, such as: control the cavity frequency acting on its cold tuning system; manage authorisations checking security interlocks; provide diagnostics for the calibration of the cavity field & of the beam phase; automatically control RF conditioning procedures according to vacuum readings; keep a number of key parameters in a circular buffer for post-mortem analysis, etc.. To ensure all these functions, extra measurements are needed, like forward/reflected RF signals or interlock/authorization signals from other systems. The LLRF RF system must be also capable to dialog with the upper level control/command system, and with adjacent LLRF boards with very fast communication links, because the fault recovery procedure requires a fast retuning of the neighbour cavities in the case of an RF fault event. In the next paragraphs, only the amplitude and phase regulation process will be fully detailed.

The 704 MHz RF cavity signal is first down-converted to an IF signal (typically between 250 kHz and 10 MHz) and then sampled by an ADC with a defined rate. In our scheme, we have chosen a 10 MHz IF signal sampled at 40MHz in order to process directly a digital IQ demodulation. The I/Q parameters describe the in-phase (I) and quadrature (Q) components of the cavity field vector. The timing distribution system must deliver a clock for the ADC in order to achieve the I/Q demodulation according to the reference phase, and must deliver the RF master signal to drive the RF power amplifier.

The digital board can be composed of some FPGA chips and DSP chips which will perform fast signal processing, and general logic and interfacing with the control system or the adjacent boards. On the digital board, the I/Q parameters, which can be filtered by a low pass filter to reduce high frequency noise, are compared to the nominal set-points. The differences for both components are corrected by a control algorithm. Different feedback control algorithms can be implemented. The most usual one is the PID controller[7,8,9] but more sophisticated algorithms such as Kalman filter, Smith predictor or time-optimal controller could be used[10]. Feedforward capability can also be implemented to enhance the field stability. The I/Q calculated control signals are finally converted by 2 DACs and used to modulate the reference signal via a vector modulator.

DLLRF systems can share digital signal processing operations between FPGA and DSP chips. FPGAs provide massive parallel processing but floating point operations are still rarely used. In this case, DSPs are more suitable for sophisticated algorithms, like a learning system for the feedforward control. For an efficient feedback system, a FPGA is preferentially used for processing the feedback control algorithms. This processing must be done as fast as possible in order to minimize the hardware latency, which corresponds to a direct limitation of the maximum gain allowed by the stability of the system.

One main key element of the digital feedback is the ADC for the conversion of the cavity voltage signal. For a high performance RF regulation, it is necessary to obtain high quality amplitude and phase measurement of the accelerator field. The sampling resolution and the time jitter of the ADCs sampling clock are the limiting factors of the digital I/Q demodulation performance[6]. A choice of a 14 bit ADC is widely adequate for regulation to better than ±0.5% for amplitude and better than ±0.5° for phase.

Another important point is the temperature stability of the LLRF system because some of the RF components are very temperature sensitive, leading to a phase drift of the accelerator field. Moreover, RF components can be shielded to minimize the electromagnetic compatibility (EMC) problems.

[7] T. Shilcher, Ph dissertation, “Vector Sum Control of Pulsed Accelerating Fields in Lorentz Force Detuned Superconducting cavities”, Universität Hamburg, 1998.
[8] H. Ma, “SNS Low Level RF Control system: design and performance”, PAC 2005, Knoxville.
[9] S. Michizono et al, “Digital RF control system for 400-MeV Proton LINAC of JAERI/KEK joint project”, LINAC 2002, Gyeongju.
[10] S.N. Simrock, “State of the art in RF Control”, EPAC 2004, Lubeck.

3 RF-FAULT RECOVERY PROCEDURES

3.1 The "RF-fault recovery" capability

The ADS accelerator is expected to have a very limited number of unexpected beam interruptions per year, which would cause the absence of the beam on the spallation target for times longer than one second. This reliability requirement is motivated by the fact that frequently repeated beam interruptions induce thermal stresses and fatigue on the reactor structures, the target and the fuel elements, with possible significant damages. Moreover, each of these beam interruptions would imply a reactor safety shut-down for a relatively long period (up to several tens of hours), dramatically decreasing the overall plant availability. Such an intimate relation between reliability and availability is very specific to these ADS systems. To reach a decent availability level, it has been estimated that beam trips in excess of one second duration should not occur more frequently than five times per 3-month operation period for the XT-ADS demonstrator (and three times per year for the future industrial transmuter). This corresponds to a reliability figure (MTBF, Mean Time Between Failure) of around 500 hours (2000 hours for the industrial transmuter).

The availability reached in present accelerators exhibits very honourable values, ranging from around 80% for large colliders, up to 95% for B-factories and even more (> 99%) for light sources[11]. But reliability performance is another story. After an unwanted beam interruption event, the beam can often be quickly recovered (within a few seconds/minutes). The beam availability is therefore not significantly degraded, even if the machine MTBF is poor, which is often the case (typically hours). Nevertheless, this is hopefully not fully true for all accelerators. In light sources especially, the beam has to be stored as long as possible, and therefore, reliability is somehow much more linked to availability than in other applications. Significant improvements, coming from careful design and maintenance, have been reached during the past years on light source facilities' MTBF. ESRF for example reached an overall MTBF of around 60 hours in 2006 and 2007[12], which strong potential for future improvement (up to more than 100 hours) by upgrading the High Quality Power System (HQPS) whose function is to protect voltage or phase drops during stormy events.

In the case of the ADS accelerator, a reliability analysis has been performed[13] within the PDS-XADS project, to be continued within Eurotrans. This study shows that the reliability of a superconducting linac composed with around 200 independently-powered cavities is clearly dominated by the reliability of the serial RF units, which have each an MTBF of 5000 to 6000 hours, thus determining a very low system MTBF of around 30 hours (that means about 70 failures per 3-month mission time). This situation, where the failure of each component in the RF unit causes a global system failure, is totally incompatible with the ADS goals and would imply to require much higher MTBF characteristic for all RF components, by at least one order of magnitude. From this, naturally comes the idea to be able to tolerate RF faults during operation, limiting the induced beam interruptions below one second. The same reliability exercise indeed shows that such a fault-tolerance capability drastically enhances the reliability

[11] N. Phinney, C. Adolphsen, M.C Ross, "Reliability Issues for linear colliders", PAC 2003, Portland.
[12] L. Hardy et al., "Operation and recent developments at the ESRF", EPAC 2008, Genoa.
[13] L. Burgazzi, P. Pierini, "Reliability studies of a high-power proton accelerator for accelerator-driven system applications for nuclear waste transmutation", Reliability engineering & systems safety, vol. 92, n°4, pp. 449-463, 2007.

performance of the system, leading to MTBF figures between 500 and 700 hours, depending on the RF system repair and maintenance policies.

To implement this fault-tolerance capability, the general philosophy is, in the event of a RF cavity / RF system failure, to re-adjust the accelerating fields and phases of the non-faulty accelerating cavities to recover the nominal beam characteristics at the end of the linac, and in particular its transmission and energy. A simple way to perform it is to react on the accelerating cavities neighbouring the failing one. This so-called local compensation method has the advantage of involving a small number of elements, and therefore of being able to compensate multiple RF faults in different sections of the machine at the same time. It is illustrated on Figure 2: if cavity #n is faulty, the (e.g.) 4 surrounding cavities (#n-2, #n-1, #n+1, #n+2) are retuned to recover the nominal beam energy & phase at the end of the following lattice (point M), and by consequence, at the linac end. It can of course be done with more (or less) cavities if necessary. Beam dynamics simulations show that the nominal beam parameters at the target can always be restored using such a retuning method, given the condition that a +30% rise in RF power and accelerating field can be sustained in the cavities[14]. The local compensation method is of course demanding in terms of RF power budget, but it is in-line with the ADS over-design criterion, so that it should not lead to dramatic over-costs.

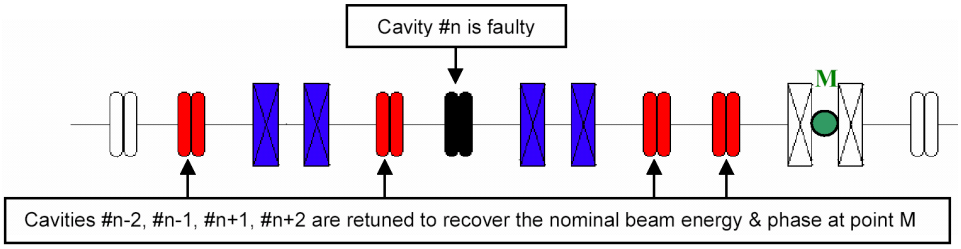


Figure 2 – Principle of the local compensation method.

Transient beam dynamics have been performed to better analyse what happens to the beam during such procedures. Two scenarios have been proposed[15], and at first approach, the simplest one consists in stopping the beam while achieving the retuning. This method will require performing in less than one second the following sequence:

- fault detection and beam shut-down;
- access to a predefined set-point general database (or to the result of an appropriated longitudinal beam dynamics simulation);
- update and tracking of the new LLRF field and phase set-points;
- adequate management of the tuner of the failed cavity to put it off frequency and avoid any deceleration effect due to beam loading;
- beam re-injection.

[14] J-L. Biarrotte, M. Novati, P. Pierini, H. Safa, D. Uriot, “Beam dynamics studies for the fault tolerance assessment of the PDS-XADS linac”, HPPA 2004, Daejeon.
[15] J-L. Biarrotte, D. Uriot, “Dynamic compensation of an rf cavity failure in a superconducting linac”, Phys. Rev. ST Accel. Beams 11, 072803 (2008).

3.2 Un-exhaustive catalogue of critical RF elements for reliability

As suggested before, RF systems indeed represent a significant part of the defaults generating the beam trips in accelerators, ranging from 5% to 30%[16,17,18,19]. For example, the trips distribution in the 805 MHz RF system of the LANSCE (44 klystrons and 7 HVPS (High Power Voltage Sources)) indicates that the three principal breakdown causes come from the high voltage sector, the control modules, and the klystrons[20]. We will hereafter present various typical RF failures, and gather them in two groups: RF power sources, and cavities/couplers/LLRF.

3.2.1 RF power sources

The XT-ADS demonstrator will operate at a frequency of 352 MHz for the low-energy section, and 704 MHz for the high-energy section. Such frequencies are compatible with klystrons, IOTs (Inductive Output tubes) and solid-state amplifiers (cf. Figure 3).

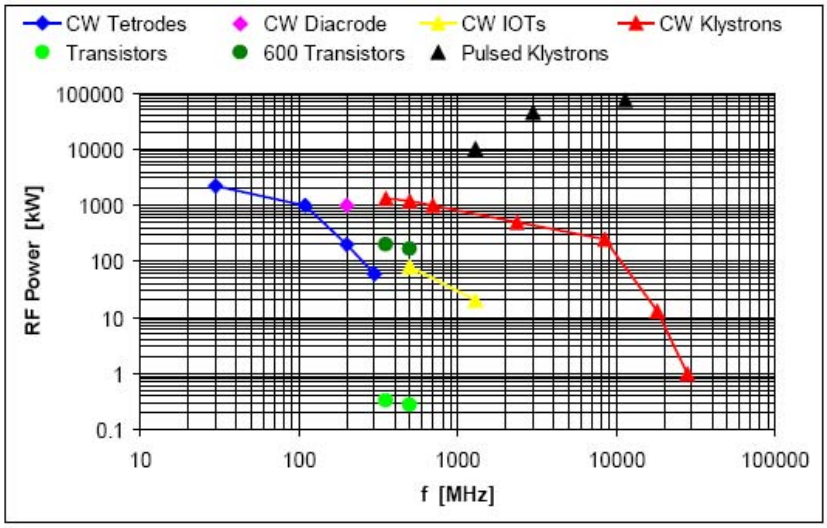


Figure 3 – Typical RF sources used in accelerators[19].

Klystrons

Available at both frequencies 350 MHz and 700 MHz, klystrons have the advantage of having a very high gain, which reduces the necessary input power below 100 W usually. Moreover, this technology is well mastered (commercial TV klystrons typically delivering 60 kW CW at 500 MHz have been widely used in accelerators) and can easily provide powers up to more than one MW CW (which is actually not needed for our independently-powered ADS linac), as shown in Figure 4.

[16] O. Brunner, "RF system reliability and Performances", CERN.
[17] Peter K. Sigg, J. Cherix, H.R Fitze, W. Tron, "Improving the reliability of the PSI proton accelerator RF system" Proc of ARW Workshop 2002
[18] C.W Allen, W. Colocho, R. Ericckson, M. Stanek, "PEP-II Hardware Reliability", IEEE Nuclear Science Symposium 2004
[19] J. Jacob, "New Development on RF power Sources", EPAC 2006, Edinburgh.
[20] M. Eriksson, "Reliability Assessment of LANSCE accelerator system" , Thesis, 1998.

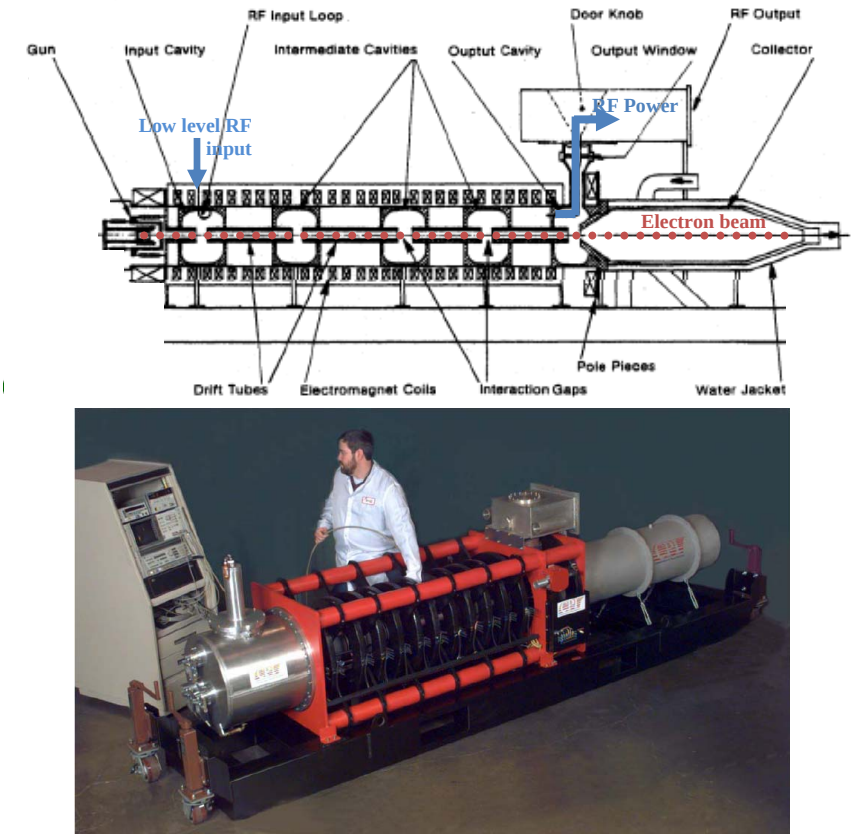


Figure 4 – The 1MW, 704 MHz CPI Klystron (VKP-7952).

The electron gun produces a flow of electrons and the bunching cavities regulate their speed so that they arrive in bunches at the output cavity, exciting microwaves. The microwaves then flow into the waveguide passing through the RF window. The electrons are absorbed in the collector.

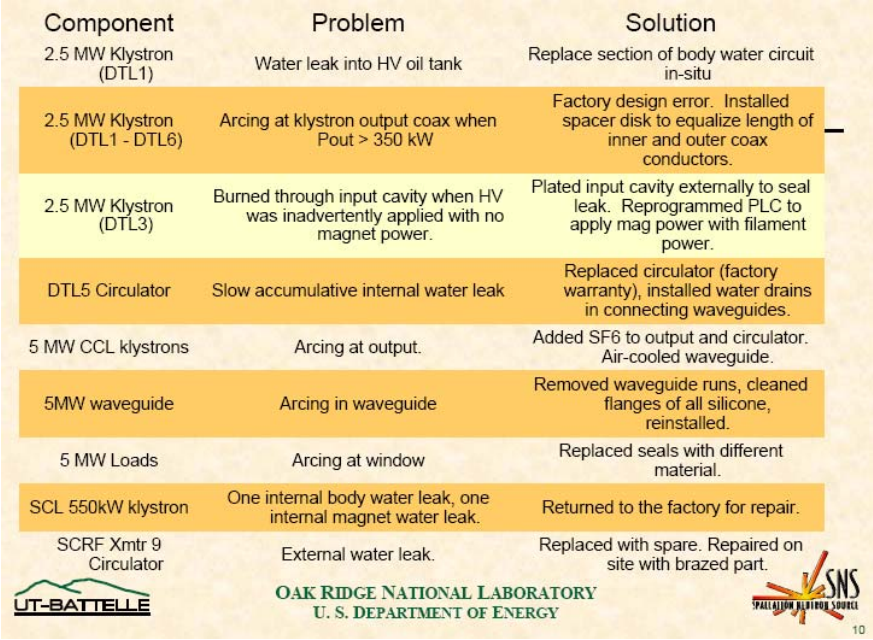
Typical problems or failures for klystrons are listed below[19,21,22].

- Coupling of the harmonic 2 of the RF;
- Instabilities due to multipacting in the input cavity or to the bandwidth wider than the circulator bandwidth;
- Breakdown in the gun between anode and body;
- Anode breakdowns by barium pollution from cathode;
- Ceramic breakdowns;
- Water leak in the cooling system;
- General breakdowns linked to HV, high RF fields, or vacuum leaks.

Despite these possible problems, the MTBF of a klystron reaches about 50 000 hours[23]. Actually, failures causing beam trips are often related to the equipment associated with the klystron itself. The high power voltage sources (HVPS) for example often show failures of

[21] S. Suhring, "Reliability at the JLab Nuclear Physics Accelerator", ARW 2002.
[22] P. McIntosh, "High power RF status", PEP-II Machine advisory Committee Review, 2003.
[23] 2EV Technologies, Data (TPD170, page 19).

amplitude and current regulations or overheating[19]. Figure 5 shows the experienced failures linked to the klystron and associated components during the commissioning of the SNS RF system.



Component	Problem	Solution
2.5 MW Klystron (DTL1)	Water leak into HV oil tank	Replace section of body water circuit in-situ
2.5 MW Klystron (DTL1 - DTL6)	Arcing at klystron output coax when Pout > 350 kW	Factory design error. Installed spacer disk to equalize length of inner and outer coax conductors.
2.5 MW Klystron (DTL3)	Burned through input cavity when HV was inadvertently applied with no magnet power.	Plated input cavity externally to seal leak. Reprogrammed PLC to apply mag power with filament power.
DTL5 Circulator	Slow accumulative internal water leak	Replaced circulator (factory warranty), installed water drains in connecting waveguides.
5 MW CCL klystrons	Arcing at output.	Added SF6 to output and circulator. Air-cooled waveguide.
5MW waveguide	Arcing in waveguide	Removed waveguide runs, cleaned flanges of all silicone, reinstalled.
5 MW Loads	Arcing at window	Replaced seals with different material.
SCL 550kW klystron	One internal body water leak, one internal magnet water leak.	Returned to the factory for repair.
SCRF Xmtr 9 Circulator	External water leak.	Replaced with spare. Repaired on site with brazed part.

Figure 5 – Problems encountered during the SNS RF system commissioning[24]

Inductive Output Tubes (IOTs)

Compared to klystrons, IOTs exhibits very interesting characteristics in terms of efficiency (>65% is usually reached), linearity and compactness. Moreover, existing IOTs are already operating at 700 MHz, with powers up to 80 kW CW (see Figure 6), compatible with our ADS application (high-energy section). Although having up to now a slightly lower MTBF than klystrons (about 30.000 hours[23]), IOTs have other advantages[25,26]:

- Maintenance is simpler: replacement of the tube only;
- IOT can be re-gunned twice, at about 60% cost of a new IOT;
- Output RF cavities are external to tube; they don't have to be replaced;
- Several suppliers are available: CPI, Thales, EEV, LITTON;
- Large market in TV domain => no problem of obsolescence.

As an example, TH793 IOTs from Thales have been chosen and successfully installed in recent machine upgrades or constructions like in Diamond or in Elettra[19]. For all these reasons, the IOT technology is, up to now, our reference solution for the 700 MHz RF system of the XT-ADS accelerator. The total cost of such a 700 MHz, 80 kW IOT amplifier including power supplies, circulator, cavity and pre amplifier is estimated to be about 350 k€.

[24] M. McCarthy, R. Fuja, P. Gurd, T. Hardek, Y. Kang, "Linac RF commissioning with the SNS HPRF system", 4th CWHAP workshop, 2006.
[25] P. K Sigg, "Summary of the 3rd workshop on high power RF-systems for accelerators", Cyclotron Conf, 2004.

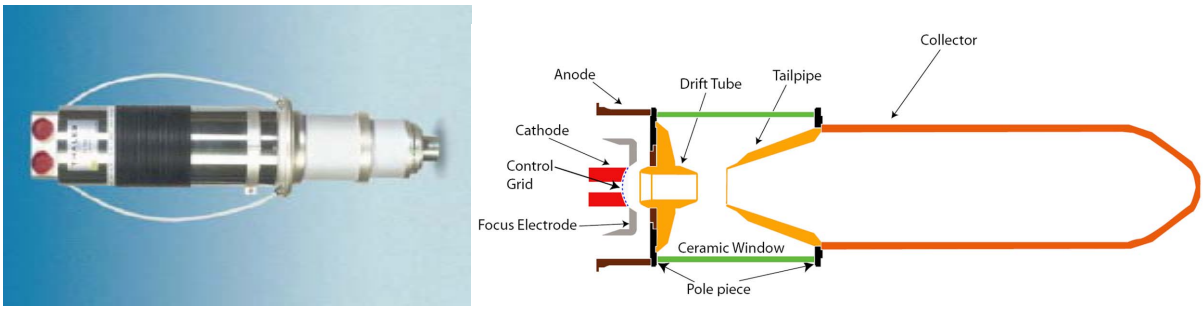


Figure 6 – The 80 kW, 704 MHz Thales IOT tube (TH-793).

An input UHF signal is used to modulate (control) the flow of electrons in an inductive output tube (IOT). The modulated flow of electrons is then accelerated by a DC field resulting in a high-energy modulated beam. Energy is removed from the beam and delivered to a load during its interaction with the electromagnetic fields in an output cavity. The energy not removed from the beam is dissipated in a collector.

The IOT whole system is comprised of four major subassemblies[26]:

- **Input Circuit Assembly**: The input circuit forms a resonator, which imparts a RF field between the cathode and grid of the IOT. The input cavity is designed to cover the desired frequency band.
- **Inductive Output Tube (IOT)**: The IOT itself is the heart of the amplifier system. It is comprised of four major subassemblies:
  - Gridded gun structure: Electron source and beam modulation grid
  - Anode: Accelerates the modulated beam to full potential.
  - Interaction Gap/Output Window: Couples the IOT beam to output cavity.
  - Collector: Residual beam energy is dissipated as heat in the collector.
- **Magnetic Focus Assembly**: As the beam travels down the drift tube and, more importantly, as it interacts with fields in the output gap, forces act on the electrons causing them to spread into the structure of the IOT. To prevent this, an axial magnetic focus field confines the beam to an appropriate diameter.
- **Output Cavity Assembly**: The output circuit has a primary and a secondary cavity. An iris opening with an adjustment paddle capacitively couples these cavities. Energy in the output cavity is extracted through a coaxial probe located at the output of the secondary cavity.

Typical problems or failures for IOTs are listed below[19,26].

- Weak cathode emission;
- Output cavity arcing;
- Cathode contaminated with material from an arc;
- Unstable power output;
- Excessive negative grid current and crowbar trips;
- Less amplitude & phase sensitivity to HV ripples.

[26] CPI, "Instruction Manual (K2) IOT Cavity Amplifier Water-Cooled Collector Series".

Moreover, the required high voltage power sources are as complex as for klystrons, although less powerful (generally 2 to 3 times less[27]), and can experience the same types of failure.

Solid-state amplifiers

Since its invention, the transistor has replaced vacuum tubes in many applications. Transistors have recently been used to build high-power RF amplifiers for 352 MHz (SOLEIL, ESRF) and 500 MHz cavities[19]. Hundreds of amplifier modules with typically 300 W unit power are combined to deliver up to 200 kW. The total cost of a 50 kW VDMOS amplifier, including power supplies, circulators, and spare parts is estimated to be about 200 k€.

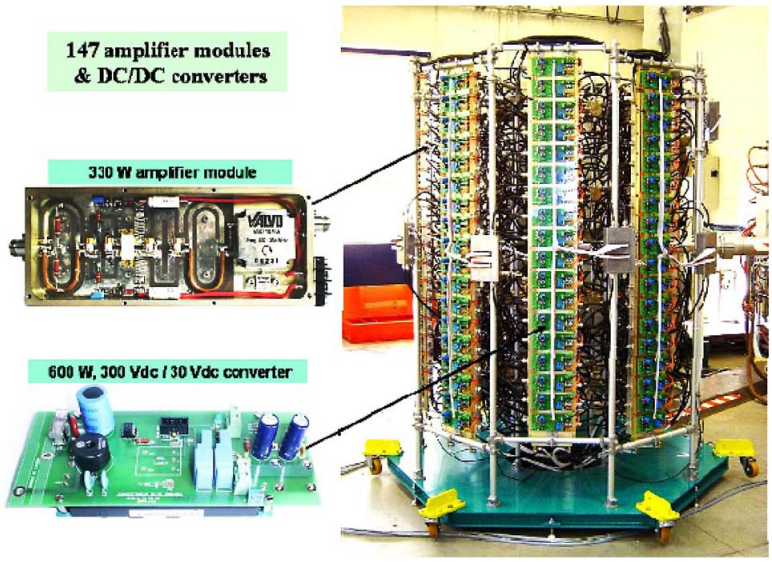


Figure 7 – SOLEIL 350 MHz, 50 kW solid-state amplifier.

This solid state amplifier has the advantages following[28,29]:

- To be extremely modular: 300W elementary modules combined (see Figure 7);
- A simplicity of maintenance associated to redundancy;
- The transistor of each module is protected by a low power circulator;
- No need for HV, no high power circulator;
- The start-up procedures and control are simplified;
- Distributed switching power supplies (DC/DC converters);
- Monitoring and fail functions included (PLC).

[27] A. Zolfghari, P. MacGibbon, B. North, "Comparison of klystron and inductive output tubes (iot) vacuum-electron devices for rf amplifier service in free-electron laser", EPAC 2004, Lucerne.
[28] P. Marchand, T. Ruan, F. Ribeiro and R. Lopes," High power 352MHz solid state amplifier developed at the Synchrotron SOLEIL", Physical review special topics- Accelerators and Beams-2007.
[29] P. K Sigg, "Summary of the 3rd workshop on high power RF-systems for accelerators", Cyclotron Conf, 2004.

Moreover, the expected reliability is clearly higher than for IOTs and klystrons, with a MTBF of the whole source of about 50 000 hours[23]. The principal failures come from the possible break-in of one transistor or of the load of an integrated circulator. But due to the extremely high redundancy of the concept, the interruption of the source is not required if such a trip happens: the operation can be still sustained with fewer modules, given that the available remaining power is sufficient to continue to operate (on can also use dedicated "stand by" modules for this).

This solid-state solution is especially suited to the ADS reliability requirements, and has therefore been chosen as the reference solution for the 350 MHz RF sources. This choice could also be extended to the 700 MHz area, since commercial solid state amplifier begins to be available in this TV frequency band, as shown in Figure 8.

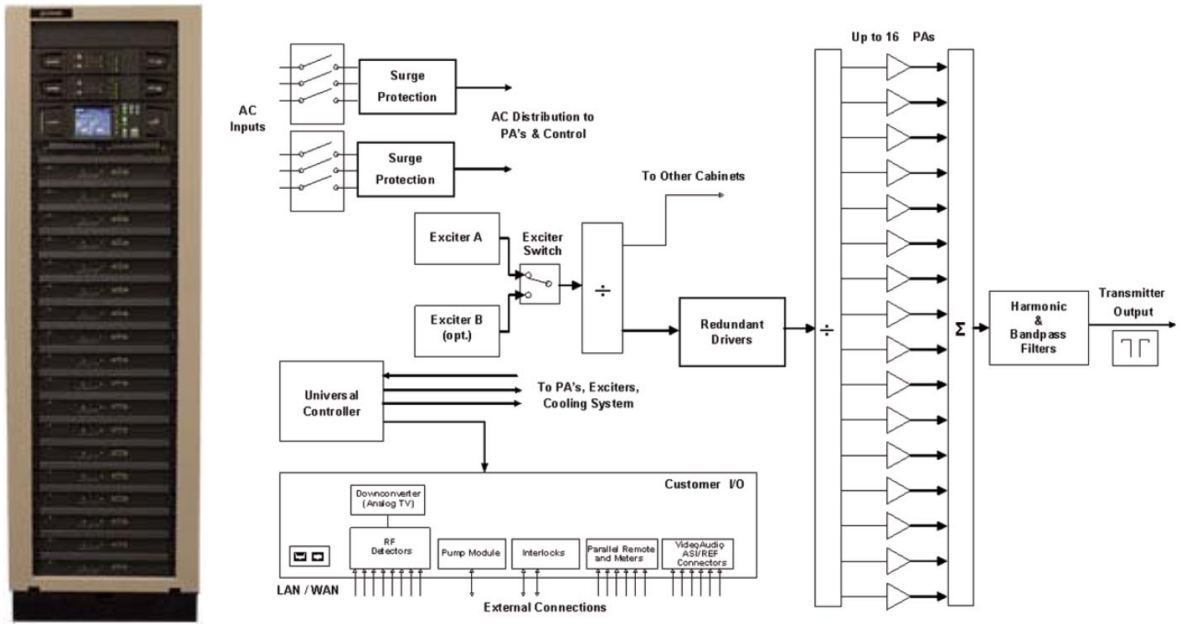


Figure 8 – HARRIS liquid cooled UHF transmitter[30].

Analog power levels up to 62.8 kW – Fully broadband PA modules (470 to 862 MHz with no adjustment) – 1:1 PA module to power supply redundancy – Hot-pluggable linear RF amplifier modules with integral soft-fail distributed power supplies – Automatic restart after AC mains interruption; returns to previous operational mode – Straightforward control, monitoring and in-depth diagnostics with easy-to-use, color touch screen – Harris® eCDi, Web-enabled remote GUI interface – Rugged, reliable construction – Liquid-cooled RF amplifiers, DC power supplies, RF combiners and reject loads to minimize air-conditioning costs

[30] HARRIS Corporation, "Maxiva™ ULX — Applying New Technology to a Liquid-Cooled Transmitter architecture".

3.2.2 Cavities, couplers and LLRF

A first lesson can be drawn from the operating experience of superconducting cavities worldwide[31,32]: the superconducting cavity performances are very stable over a long operating time. This property is almost intrinsic: due to the extremely low power dissipation on the cavity walls, and the wide beam port aperture (resulting in negligible beam loss), the cavity does not suffer any important aging effect. The usual cavity performance degradations reported on operating accelerators appeared after cavity warm up or vacuum break. Other possible failures are related to:

- Cavity quench, that occurs when the material can't transport anymore any increased thermal load to helium (material defect, beam loss);
- Field emission, due to the presence of electron emitters (cavity pollution);
- Excitation of low-coupled high-order modes by the beam;
- Cold tuning system errors or failure.

Like superconducting cavities, the coupler functioning is very stable under normal operation. The most fragile part of the coupler is the ceramic RF window which has to sustain the pressure difference and the local heatings, generating mechanical constraints. It may happen that the window breaks during operation, or at least starts to crack resulting in a vacuum leak. Possible problems linked with arcs/sparks or reappearance of multipacting barriers can also happen.

Following the technology used in military or space domains, where the reliability is crucial, the LLRF feedback systems of present accelerators widely use digital programmable components. Such a solution makes possible to integrate functions such as IQ demodulation, filters or other sophisticated algorithms, as explained in chapter 4. RF analog parts of course remain, like the down converter system, the instrumentation or the interlock systems.

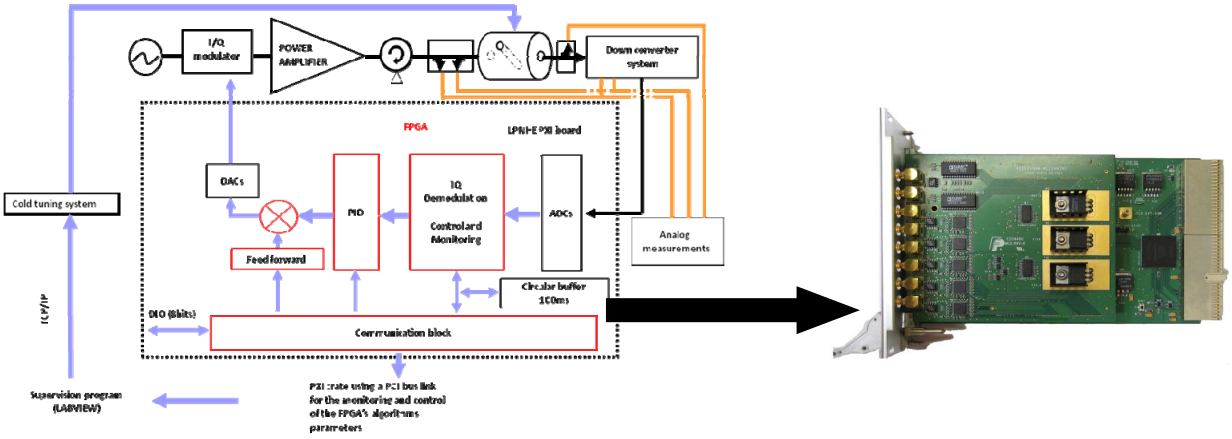


Figure 9 – View of a DLLRF system based on a FPGA + PXI board (IPNO/LPNHE).

[31] D. Boussard, E. Chiaveri, "The LEP Superconducting RF system: characteristics and operationalexperience", HPPA 1998, Mito.
[32] C. Reece, "Overview of CEBAF operations and SRF related activities at Jefferson Lab", SRF 1999, Santa Fe.

Such an integrated solution allows to reduce the components count, and by consequence enhances the reliability of the system, with a MTBF generally estimated to about 100 000 hours[13]. But the complexity of the digital feedback system makes it quite susceptible to hardware deficiencies or programming errors in software. These components are also sensitive to radiations, which can generate defaults or even destructions (Single Event Latchup[33]). Other failures are mainly of electric type, related to environment (T°, humidity, CEM): noise can trigger false defaults on interlocks; oxidation of connectors can generate breakdowns[21]…

3.3 Detecting an RF-fault

In the XT-ADS case, it's necessary to have a speed response to a default. To detect an unexpected condition, the RF system must have several diagnostics which run under the control of the LLRF system. These diagnostics must detect a default in a very short time in order to provide more time to LLRF system for analyzing the default and react.

An unexhaustive list of possible diagnostics is given here under[34,35,36]. All signals are carried back either to the LLRF system or to the interlock system (or both) for processing.

- RF directional couplers are integrated in the waveguide transmission system near the cavity couplers, RF output of the power amplifier, and near the RF splitter loads. These couplers detect incident and reflected RF power levels. The on-line analysis of these data can allow to detect several failure events (cavity quench, loaded Q errors, tuning errors, RF load breakdown…).

- Current and voltage monitoring of the high-voltage power supply to detect instabilities, arcing or slow shut down.

- Vacuum monitoring (vacuum gauges) of the cavity, coupler and IOT. It can especially allow to detect leaks at the power coupler RF window.

- Flow and temperature monitoring of the different cooling circuits. Temperature is for example an excellent predictor of impending RF window failure.

- Electric pick-ups or/and fibber-optic lines can be placed near the power coupler RF windows, near the RF power amplifier output to detect arcs or multipacting.

- Other dedicated diagnostics can be foreseen: X-ray detectors near the cavity to monitor the field emission level, helium flow-meters to monitor the cryomodule cryogenic losses, etc..

[33] N. Merabtine, D. Sadaoui, M Benslama, " Contribution à l'étude du phénomène de latchup induit dans les circuits intégrés embarqués dans un environnement radiatif spatial", 2006.
[34] M. McCarthy, "Response of the rf power system to off-normal conditions on APT", PAC 1999, Santa Fe.
[35] S. Simrock et al., "Exception detection and handling for digital RF control systems", LINAC 2006, Knoxville.
[36] J-L. Biarrotte et al., "XADS accelerator: radiation safety and maintenance", XADS Deliverable 48, 2004.

3.4 Example of an arc event inside an IOT

Let's finally analyse the example of an arc event inside the IOT.

In the hypothesis of such an event, the current and voltage monitoring system of the HVPS will detect over limits and trigger a shut down of the HVPS via interlocks, in less than 20 µs. The HVPS can not then be restarted very quickly.

The LLRF system is then informed of the power shut-down (via the HVPS status signal, but also via RF directional couplers monitoring). The LLRF system has to:

- send a signal to the Machine Protection System to shut down the beam temporarily (pulsing the source, or using a chopper); this can be achieved typically in much less than 100 µs;
- open the RF control loop, cutting off the pre amplifier via an RF switch (< 1 µs);
- detune the cavity sufficiently out of resonance using piezo actuators (100 ms should be largely sufficient[37])
- send a signal to the (e.g. 4) adjacent LLRF systems to update the set points (< 10 µs), stored into a database or a ROM memory.

Once the RF fields of the 4 correcting cavities are stabilized (10 ms should be enough), a global check of the status of the 5 RF systems has to performed, and a new signal has to be sent to the Machine Protection Signal to restore the beam. The duration of the whole procedure should be in the range of 200 ms, and anyway lower than 1 second; this duration is clearly dominated by the time needed to perform the cavity detuning.

Once the beam is restored, the LLRF system of the failed IOT can reset the HVPS and restart it within a few seconds.

- If arcs have disappeared, the RF system can be recovered and put on-line; the procedure is very similar to the previous one: beam is stopped, the failed cavity is retuned, the RF control loop is closed to power the cavity, adjacent LLRF systems return to their previous set-points, and beam is re-injected once the systems are stabilized.
- If the IOT still arcs, the RF system is definitely shut down. The IOT tube can then be changed in less than 1 hour, given that the source is outside the beam tunnel, and conditioning procedures can be performed on the new tube. The RF system can then be recovered like here above. An alternative solution is to wait for the next maintenance period.

[37] N. Gandolfo, private communication (measurements have shown that a 1.5 kHz detuning can be cleanly performed on a spoke cavity in less than 10ms, using piezo actuators ; this result will be detailed in the final deliverable of Task 1.3.2).

4 DIGITAL LLRF HARDWARE CONSIDERATIONS

4.1 General considerations

DLLRF architectures often depend on the existing laboratory knowledge and past developments. Thanks to the flexibility of this kind of system, complex algorithms developed for one application can be re-used for a new system. Bridge between FPGA and control/command interface is a long work and the choice of the interface standard is strongly dictated by previous developments in the laboratory. Basic arithmetic blocks for digital signal processing created for other applications can be used as a library. This approach also favours exchange within collaborations through free IP cores. In the case of the XT-ADS project, the same DLLRF algorithm will be used for the different kinds of cavities working at 352 MHz and 704 MHz. Only the down converter block must be changed to always work at the same intermediate frequency of 10 MHz.

Designers of RF systems have to choose between a commercial board and a home-made system. Commercial products with FPGA and DSP chips, ADCs and DACs can be used but they are often limited by the number of ADCs (often two) and their performances. Tree coders should be necessary if the cavity voltage, the forward and reflected signals have to be digital converted. The capabilities are also limited by the board architecture, which mainly includes the size of the FPGA or the DSP, and by the defined interface. On the contrary, a home made board allows to optimize the board design and cost. For example, the RF components and the FPGA/DSP do not put the same constraint on the Printed Circuit Board (PCB) fabrication. Their location can be well defined in order to optimize the PCB. Designers can also choose which family of FPGA will be the most efficient to fulfil the specific requirements of the DLLRF. Many functional blocks are now embedded into FPGA chip and simplify the architecture:

- RAM memory,
- dedicated DSP slices for arithmetic operations,
- digital clock manager (DCM) and PLL blocks for clock management,
- embedded processor,
- Gigabit links (ex: Rocket IO) for fast communications.

New FPGA also supports partial reconfiguration, which can greatly improve the versatility of the FPGA. It is possible to reconfigure only a portion of the FPGA while the rest of the logic remains active. The DLLRF board must then host the electronic components needed to reconfigure the programmable device.

Figure 10 presents a generic Digital Low Level RF board. Several ADCs and DACs may be connected to the same FPGA thanks to the high number of I/O pins. Fast links from board to board (ex: ROCKET IO) and communication with control/command system are completely embedded into the FPGA chip. Memory (RAM) is used to store set points for different operation modes of the accelerator, or to save some parameters needed for post-mortem analysis. A DSP can also be used for sophisticated algorithms that would require floating operations when latency is not as stringent. At the present state of the study, it seems that a simple solution based on a FPGA without DSP would be sufficient to develop a first version of an efficient RF feedback system fulfilling the needs of EUROTRANS task 1.3.4.

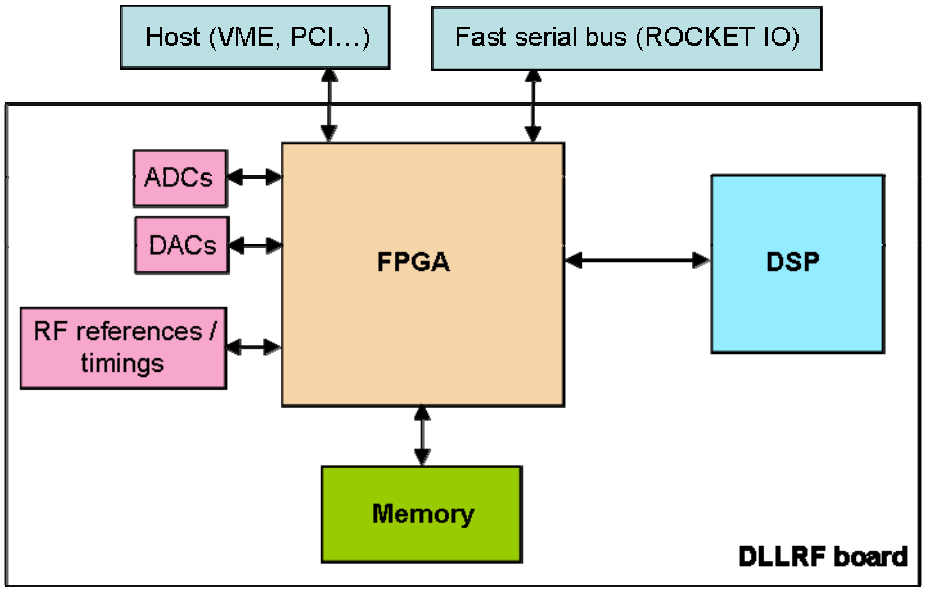


Figure 10: Generic DLLRF board.

Xilinx and Altera are the main companies in the field of FPGA components. They present a lot of different products with similar performances and helpful tools for the development of sophisticated algorithms. This choice depends also of the home-knowledge of the laboratory and the designers involved in the code development. Each company provides interface with MATLAB environment via toolboxes (see chapter 5) to facilitate the work of the DSP designer ("System Generator for DSP" for Xilinx and "DSPbuilder" for Altera).

The hardware standard is a major choice in the design of a RF system and will define the mechanical specifications such as board dimensions, connector specifications, and enclosure characteristics, as well as the electronic specifications for sub-bus structures, signal functions, timing, signal voltage levels, and master/slave configurations. One criterion is the modularity for the different components of the accelerator (diagnostics, vacuum system….), that need several boards with different functionalities. Working with the same standard for all the components of the accelerator will simplify the maintainability and reduce the maintenance cost. Moreover, since the hardware is a strong investment, it must support future hardware and software upgrade. Classical standards as VME[38,39], PCI[40] or VXI[41] can be used, but new systems as ATCA (Advanced Telecommunications Computing Architecture) can also be an efficient solution[42] because this standard is specially build for fast communication, that is an important requirement for the fault recovery procedure.

[38] A. Rohlev et al., "All digital IQ servo-system for CERN LINACS", PAC 2003, Portland.
[39] S. Peng et al., "The SNS ring LLRF control system", PAC 2005, Knoxville.
[40] S. Michizono et al, "RF feedback control Systems of the J-PARC LINAC", PAC 2007, Albuquerque.
[41] P. Corredoura, "Architecture and Performance of the PEP-II Low Level RF system", PAC 1999, New-York.
[42] S.N. Simrock et al, "Conceptual LLRF design for the European XFEL", LINAC 2006, Knoxville.

4.2 Cavities, DLLRF boards and communication links layout

In the event of a RF system or cavity failure, the nominal beam characteristics at the end of the linac must be recovered in less than 1 second. A simple way to achieve this requirement is to perform a local compensation using the cavities surrounding the failing one through very fast communication links. Figure 11 presents a communication strategy that is compatible with the local fault compensation scenario.

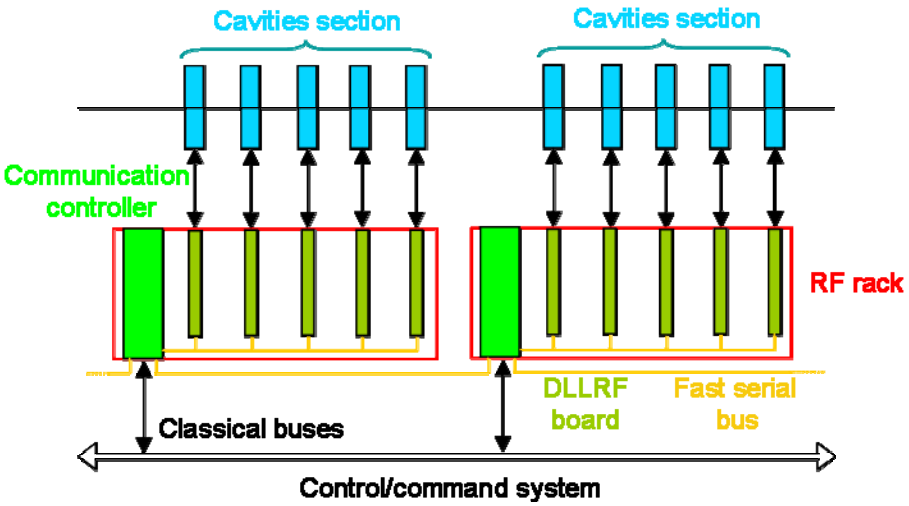


Figure 11: Possible communication strategy for DLLRF system

The layout of the LLRF racks along the accelerator defines which cavities (and how many) will be retuned in case of cavity or RF subsystem failure. Every RF rack allows to control a certain number of cavities through DLLRF boards. Fast communications links as Rocket IO can be easily implemented between the boards, each dedicated to one cavity. If one is faulty, all the cavities controlled inside the rack must be retuned with new set-points in order to obtain the same beam characteristic at the end of the section. If the faulty cavity is located at the end of the RF rack, retuning the cavities in the neighbouring rack might be necessary. This is the purpose of fast serial links between adjacent racks The number of cavities driven by one RF rack is a significant parameter: the higher this number, the lower the extra-power required to compensate the faulty cavity.

A communication controller board implemented with a FPGA or a DSP chip manages fast communication between the DLLRF boards on one hand and between adjacent RF racks on the other hand. It also manages slow communication at an upper level to the control/command system with classical buses as Ethernet.

5 DIGITAL LLRF SOFTWARE ARCHITECTURE & VHDL SYNTHESIS

5.1 Software architecture

The code implemented in the digital board has to run high level tasks as the control of the accelerator field, the cavity frequency control, communications between the upper level Control/Command and the FPGA, etc. The FPGA can be organized in a modular way to facilitate code integration step by step or to support the exchange of algorithms to different programmers working on the implementation (Figure 12). For example, there is one module for the LLRF application (divided itself in sub-modules) and one module for the VME interface. Most of the operations inside the FPGA are described in VHDL, but some of them can be developed in C language[43] mainly for the embedded processor. The FPGA can be divided into 2 parts, reprogrammable or not. The device configuration can be changed in one area without affecting another area. Communication, security tasks or clock management must not be reconfigurable by users after the prototyping step. LLRF functionalities like digital filtering for cavity field regulation or algorithms for cavity conditionning can be placed in a locally reprogrammable area allowing distant updates through the host bus. This functionality allows to upgrade LLRF system by RF engineer after first operations without risks for the whole digital system.

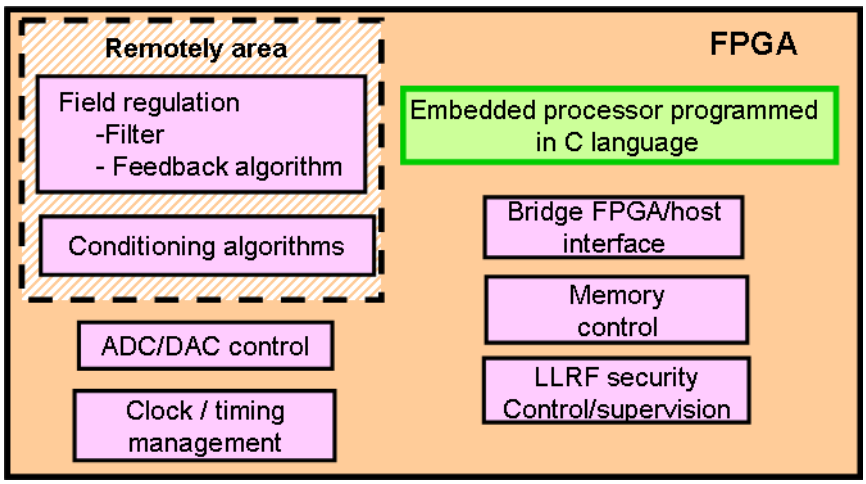


Figure 12: Internal architecture of FPGA

Figure 13 shows a basic scheme for the control of the accelerator field. The RF signal is converted to an intermediate frequency of 10MHz and sampled at 40 MS/s. Two consecutive measurements describe the I (In-phase) and Q (quadrature) components of the cavity field. I/Q parameters are retrieved by a demultiplexer and a sign flip scheme to change the sequence I/Q/-I/-Q in I/Q/I/Q. This sign inversion permits to remove analog DC offsets. A digital low pass filter is used to reduce the sensor noise. This data are scaled to correct the phase offset and to calibrate the voltage measured by the cavity probe. They are then compares to the set-

[43] Xilinx, Embedded Processing, http://www.xilinx.com/products/design_resources/proc_central

point and the error is corrected by feedback algorithm. Additionally, an adaptive feedforward function is added to the control values in order to minimize the control effort.

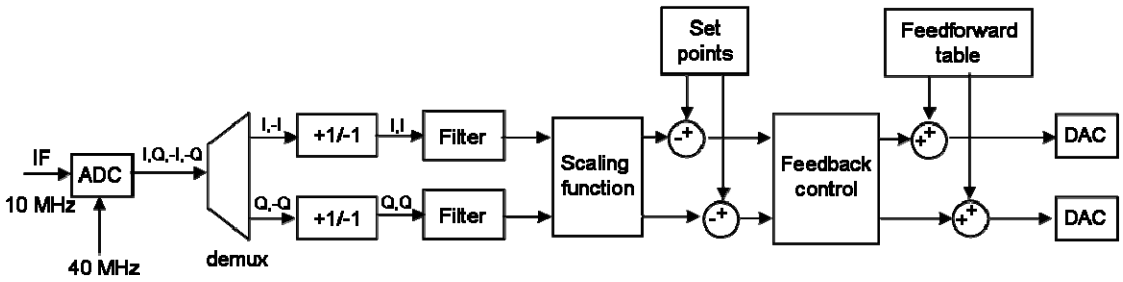


Figure 13: Schematic of the digital control of the accelerator field

Software implementation requires a special care for the resolutions of parameters and variables involved in the digital signal processing. Feedback algorithms as PID control require very low latency and could be often implemented in fixed point arithmetic with sufficient accuracy; but an adaptive feedforward algorithm may necessitate floating point logic to operate properly. Fortunately, in this case, the latency requirement is not as stringent. One limiting factor is the size and the mathematical resources (as DSP slices) on the FPGA. Practically, it is important to estimate the needed fixed point resolution for a required calculation precision before to start the implementation.

5.2 Design flows

Two software design flows can be used to implement the digital signal processing on the FPGA. Working with the hardware description language as VHDL (Very-high-Speed Integrated Circuit Hardware Description language) in the ISE development environment is the traditional way but the use of tool as the Xilinx DSP System generator (or the Altera DSP builder) can facilitate the design flow.

5.2.1 Traditional development environment

ISE Design Suite from Xilinx is a powerful Integrated Development Environment using VHDL description language. Programmers decide which calculations are going to perform in parallel or in sequence but he requires a lot of knowledge about binary operations, FPGA structures and digital systems. Figure 14 presents the ISE development environment for the PFGA coding. ISE Design Suite is full-featured HDL simulator, which permits to realize VHDL design and implementation, mapping and routing FPGA architecture. The association with Modelsim software provides a complete HDL simulation environment that enables to verify the functional and timing models of the design. This process permits to find error in the code at every step of the development and also to predict the FPGA behaviour. ChipScope software inserts logic analyzer, bus analyzer, and virtual I/O low-profile software cores directly into the design, providing the possibility to view any internal signal, which can then be analyzed. All this process permits to build robust signal processing blocks.

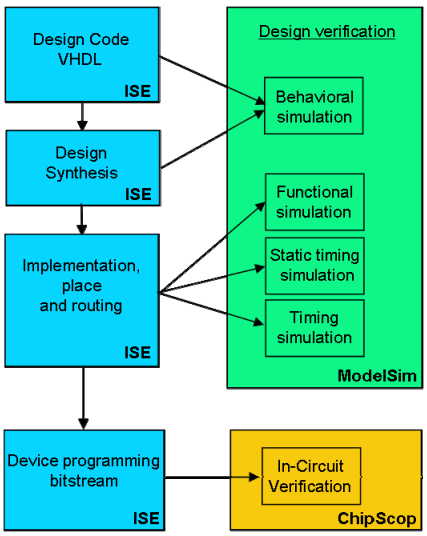


Figure 14: ISE development environment

There is a trade-off between clock frequency and precision of output signals to achieve the highest possible computation speed, so the lowest latency for the digital signals processing. ISE Design Suite permits also to use powerful tools as the Xilinx CORE Generator™ System which provides user-customizable functions.

For example, 2 ways could be use for the scaling of I/Q parameters. The CORDIC (Coordinate Rotational Digital Computer) IP core[44] can be used to rotate data in order to correct the phase offset due to the delay in the cable length. But this solution requires a high number of clock cycles. Instead, a basic algorithm[7,41] can be implemented to rotate the cavity field vector in few clock cycles but with lower accuracy. Modelsim simulations permits to define which solution presents the best trade-off between precision and speed and to choose which one should be implemented.

Moreover, Xilinx CORE Generator™ System generates optimized and customizable VHDL codes for FIR low pass filters used to reduce noise on the I/Q parameters. More sophisticated filters as IIR filters must be implemented directly in VHDL language.

5.2.2 Xilinx DSP System generator

DSP system generator is integrated with the MATLAB/Simulink environment[45,46] and is a powerful tool to develop FPGA applications without knowledge of VHDL language. It allows a high level arithmetic design to quickly model and implement a complex digital signal processing. Thanks to basic IP functions and special DSP blocks (FIR filter, FFT…), this tool permits to build the system in Simulink, to generate automatically a VHDL description for synthesis, which produces after “route and place” a binary file that is directly downloaded into the FPGA. Then, it also allows to achieve hardware-in-the-loop simulation, which permits to incorporate a design running in the FPGA directly into a Simulink Simulation. Figure 15 presents the design flow with the Xilinx DSP system generator.

[44] Xilinx, CORDIC, http://www.xilinx.com/products/ipcenter/CORDIC.htm
[45] A. Burghardt, S.N. Simrock, "FPGA Based RF Control, TESLA Report 2003-16
[46] Xilinx, System generator for DSP, http://www.xilinx.com/ise/optional_prod/system generator.htm

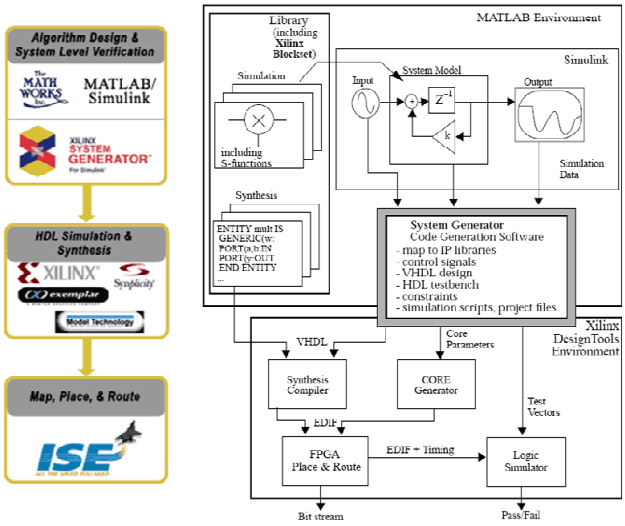


Figure 15: Xilinx DSP system generator design flow

All the blocks can be simulated in Simulink environment where many parameters can be optimized. Thus, the length of every variable can be checked in order to evaluate the fixed point resolution (rounding error) needed for each calculation of the signal processing. For example, this tool also permits to realize easily a FIR filter. The filter coefficients are evaluated with the filter toolbox of MATLAB and then simulate in the Simulink environment. The Xilinx DSP System allows to simulate which is the limited resolution of the parameters of the filters. The Xilinx DSP System generates then all necessary files as the VHDL file and the VHDL test bench used for the simulation with ModelSim software to verify the functional and timing models of the design.

Unfortunately, this tool does not allow to design completely a digital Low Level RF system: some IP-cores or differential I/O buffers must be only instantiated in VHDL code and request the traditional development environment as ISE.

A judicious choice would be a mix of the two design flows. An experienced VHDL programmer can perform the code around specific FPGA problems as the clock distribution, the communication with a highest level of Control/command system or the security tasks while an RF engineer can develop the digital signal applications through the MATLAB/Simulink environment.

6 EXAMPLE OF A LLRF SYSTEM IMPLEMENTATION

This section presents an example of a LLRF system implementation realized for the SOLEIL Synchrotron[47]. In its storage ring, two cryomodules, each containing a pair of 352 MHz superconducting cavities, provide the maximum power of 560 kW, required at the nominal energy of 2.75 GeV with the full beam current of 500 mA. Presently, an analogue Low Level RF system is successfully operating to control the amplitude and phase of the accelerating voltage. A fast digital FPGA based I-Q feedback is currently under development in order to substitute the analogue system.

[47] P. Marchand et Al, "Commissioning of th SOLEIL RF systems", EPAC 2006, Edinburgh.

6.1 Hardware

The architecture of the SOLEIL digital LLRF system is based on a FPGA, with 12 bits ADC's, 14 bits DAC's, analogue IQ modulator and IF frequency conversion (Figure 16). The 352 MHz RF reference signal and 10 MHz machine master clock are mixed via a IQ modulator to generate the 342 MHz LO signal used to down-convert the 352 MHz cavity RF signal into a 10 MHz IF signal for the signal processing. This allows to follow the variation of the RF reference frequency which is driven by the Slow Orbit Feedback. The down-converted 10 MHz IF signal is sampled at 40 MHz via the ADC. In order to have a better ratio signal/noise and then to improve the I/Q detection, the ADC's are operated in differential mode using a balun.

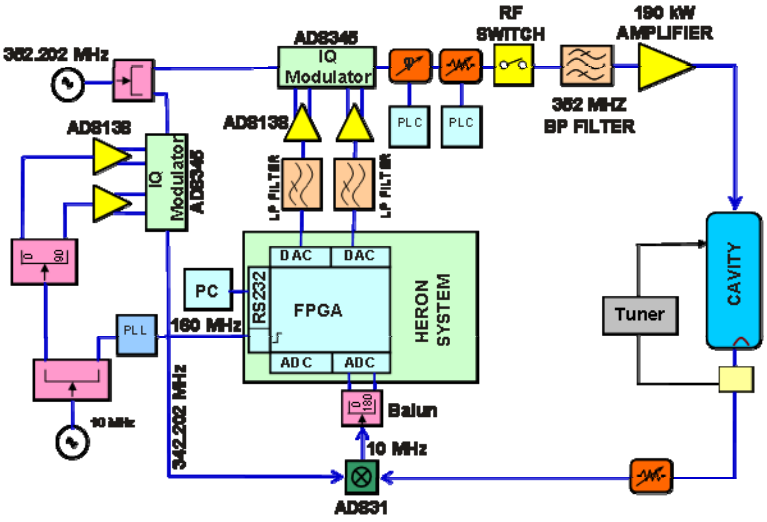


Figure 16: Architecture of the digital LLRF system

The Hunt Engineering[48] HERON IO2 module (Figure 17) has been selected for the digital signal processing because of its short latency between the input interface (ADC) and output interface (DAC) through the Xilinx Virtex II FPGA. The main features of the HERON module are given below:

- Xilinx Virtex II FPGA with 1M gates HERON-IO2S
- FPGA configuration downloaded using the HERON Serial Bus.
- Choice of clocking options
- Two 125MSPS 12 bit A/Ds connected to the FPGA
- Two 125MSPS 14 bit D/As connected to the FPGA
- High analog signal bandwidth of 500Mhz in and 145Mhz out.
- 8 uncommitted digital I/Os
- Several serial I/O options possible -- configured by the FPGA.
- Connects to all of the HERON FIFOs, UMI and module ID signals

[48] Hunt Engineering, http://www.hunteng.co.uk

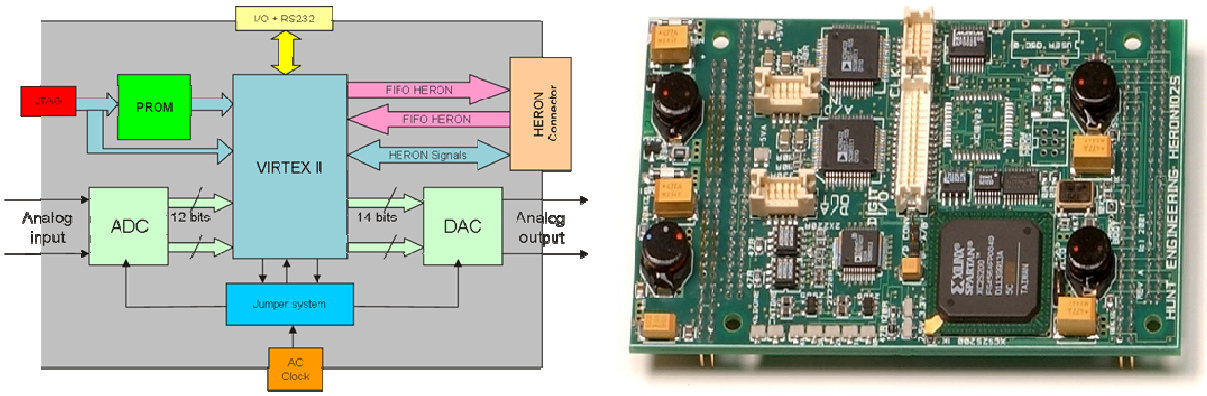


Figure 17: HERON –IO2 module

6.2 Implementation

Hunt Engineering provides a comprehensive VHDL support package with a Hardware Interface Layer[49] which defines all inputs and outputs from the FPGA on the module and correctly interfaces them with the module hardware. This package removes the need to understand how to use the hardware that is external to the FPGA. It also provides user constraints file, VHDL sources and simulation files to design the digital signal applications without high knowledge in VHDL code.

For the LLRF application, the building blocks in the FPGA are composed of a digital IQ demodulator, a few proportional/integral controller functions, clock and data managers, which are shown in Figure 18.

The digital IQ demodulator works with 4 samples over the 10 MHz period. As the FPGA HERON board is synchronized with the machine 10 MHz master oscillator, the demodulator does not need any reference signal. A sliding average (or low pass filter) is used to reduce the sensor noise.

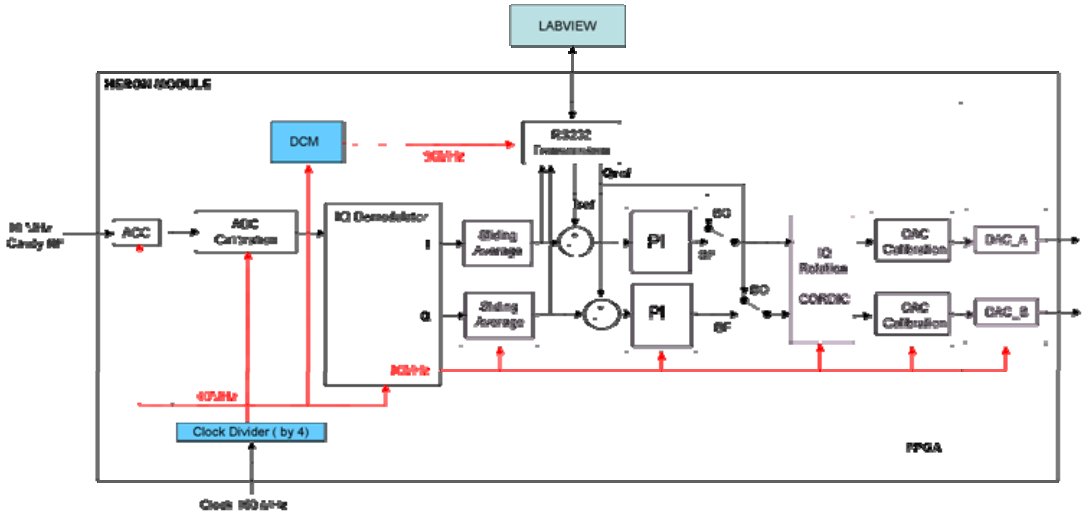


Figure 18: Digital LLRF building blocks

[49] Using the Hardware Interface Layer V2.0 in your FPGA Design, http:// www.hunteng.co.uk/pdfs/manuals/hilv20.pdf

The I/Q measured values are then compared to the set-point and the error is corrected by PI feedback algorithm. A CORDIC rotation block is implemented to adjust the loop phase at the operating value.

The Heron board provides a basic RS232 interface with the FPGA. A RS232 manager control block was developed, in order to communicate with a PC, using a HyperTerminal or a Labview application. This block also manages the IQ calibration, the open/close loop commands, phase rotation and measurement data taken at different point of the digital signal process.

A correction table, stored in ROMs inside the FPGA, compensates for the DAC's and ADC's coding errors.

6.3 Experimental results

First, the system was tested with a cavity simulator, implemented in the FPGA between PI controller and the demodulator[50]. The SOLEIL cavity was simulated by a second order IIR low-pass filter with a 3 kHz bandwidth. The realization of this filter required a reduction of the 10 MHz clock frequency down to 1 MHz, using a decimation function on the demodulator output data. This test confirmed the good functioning of all building blocks of the chain.

For the tests on the real cavity, one cavity of the cryomodule was controlled by the digital system, the other by the analogue system. The phase of the RF plant as compared to the injected beam and the relative phase of the two cavities were adjusted such to optimise the injection efficiency and balance the RF power of the two cavities.

The system was stable with a proportional gain up to 4, while with 8, it became instable due to the too large latency of the CORDIC rotation block (22 clock cycles of 10 MHz). That will be improved using a rotation block based on multipliers and adders with cosine and sine table[7] which will take only 2 clock cycles. The implementation of this faster rotation block is needed to allow an increasing of the proportional gain.

So far the 1 MV cavity voltage could be controlled by the digital system with a good accuracy. Figure 19 shows experimental measurements with electron beam current from 0 to 300 mA and with or without the transverse multibunch feedback (TFB).

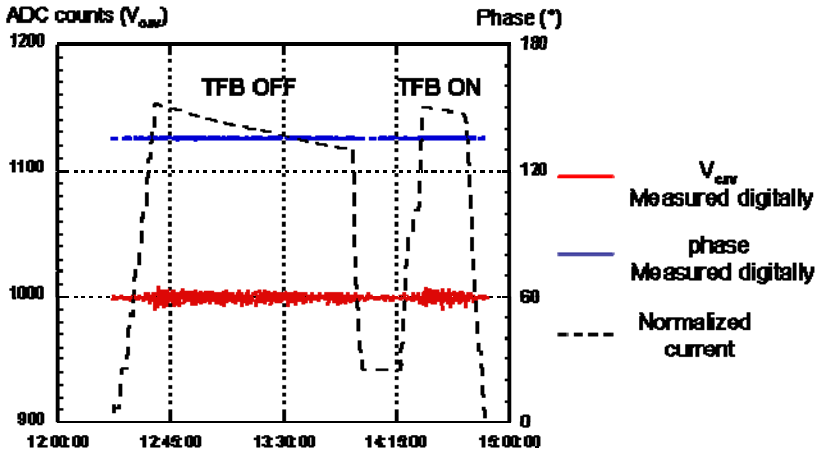


Figure 19: Experimental results with a maximum current of 300 mA

[50] O. Piquet et al., "Digital Low level RF system of the SOLEIL Synchrotron", LLRF 2007 Workshop, Knoxville.

Without beam loading, the measured phase and amplitude stability were about 0.15° rms and 1 ‰ rms, respectively in closed loop. They are slightly degraded to 0.2° rms and 0.3 % rms with a 300 mA beam.

7 CONCLUSION

A conceptual design of a Low Level RF system for the EUROTRANS superconducting cavities has been performed. It is mainly based on the use of an integrated Digital Low Level RF (DLLRF) board, containing:

- a FPGA chip, able to process the feedback control algorithms,
- several ADCs and DACs, to convert the received and produced signals,
- a RAM memory, used to store set-points or save operating parameters,
- a serial bus, to communicate with the general control/command system,
- a fast serial bus, to communicate with adjacent boards.

Such a solution, if carefully designed, should easily fulfill the needs of a LLRF control system with fault-tolerance capability. The next step is therefore to build a prototype of such a system, and to test its capability both to regulate the field and phase of the regulated cavity, and to manage the required procedures linked with a fault- recovery scenario. Very good regulation results have been already achieved on existing prototypes[50,51]. But further demonstration is required to test the capability of the DLLRF board to manage the whole fault-recovery sequence (to be performed in less than 1 second):

- detect the RF fault (via dedicated diagnostics) and trigger beam shut-down;
- update the new LLRF field and phase set-points (that are stored in the memory);
- detune the failed cavity and cut off the failed RF loop;
- trigger beam re-injection once steady state is reached.

It is therefore recommended to benefit from the on-going work in Task 1.3.2 (high-power test of a 352 MHz spoke cavity) and Task 1.3.3 (high-power test of a 700 MHz cryomodule) to try to validate these aspects as deeply as possible. Each of the above sequences should be able to be tested using at least virtual signals.

[51] C. Joly *et al.*, LLRF07 Workshop, Knoxville, 2007.