IDeF-X ECLAIRs: An ultra low noise CMOS ASIC for the readout of Cd(Zn)Te Detectors

O. Gevin, P. Baron, X. Coppolani, E. Delagnes, F. Daly, O. Limousin, F. Lugiez, A. Meuris, F. Pinsard

***Abstract*— The very last member of the IDeF-X ASIC family is presented: IDeF-X ECLAIRs is a 32-channel front end ASIC designed for the readout of low capacitive (2 to 5pF) and low leakage current (1pA to 2nA) Cadmium Telluride (CdTe) and Cadmium Zinc Telluride Detectors (CdZnTe). Thanks to its ultra low noise performances (Equivalent Noise Charge floor of 33 e^- rms) and to its radiation hardened design (Single Event Latchup Linear Energy Transfer threshold of 56 MeV.cm².mg^{-1}), the chip is well suited for very low energy discrimination, very high energy resolution, "space proof," hard X-ray spectroscopy. We measured a very low energy threshold of less than 2 keV with a 14 pF input capacitor and a minimal sensitivity of the Equivalent Noise Charge (ENC) to input capacitance of less than 7 e^-/pF obtained with a 6 µs peaking time. IDeF-X ECLAIRs will be used for the readout of 6400 CdTe Schottky monopixel detectors of the 2D coded mask imaging telescope ECLAIRs aboard the SVOM satellite [1]. IDeF-X ECLAIRs has also been designed for the readout of a pixelated CdTe detector in the future miniature spectro-imager prototype CALISTE 256 that is currently foreseen for the high energy detector module of the SIMBOL-X mission [2], [3].**

***Index Terms*— CMOS, Low noise ASIC, CdTe, Hard X-ray spectroscopy, Latch up, SIMBOL-X, SVOM**

I. Introduction

THE IDeF-X family includes a set of very low noise Application Specific Integrated Circuits (ASIC) dedicated to the readout of very low input capacitance and very low dark current detectors, especially Cd(Zn)Te detectors.

The characterizations of the previous members of the family [4]-[6] have demonstrated their good noise performances and their suitability for space environment:

- The Equivalent Noise Charge (ENC) and low threshold measurement results make them well fitted to low energy (4 to 200 keV) and very high resolution spectroscopy applications (~1 keV FWHM at 60 keV).
- The demonstrated radiation hardness of their process technology (AMS CMOS 0.35 µm) up to more than 200 krad makes them suitable for space applications.

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IDeF-X ECLAIRs is the very last member of the family, it has been planned to read a module built of 32 CdTe Schottky monopixel detectors (4x4 mm^2, 1 mm thick). This device (32-pixel detector + ASIC) will be the elementary detection unit of the DPIX camera that is currently developed for the high energy instrument of the SVOM/ECLAIRs X and gamma-ray 2D coded mask imaging telescope. IDeF-X ECLAIRs has also been optimized for the readout of pixelated (256 pixels) Cd(Zn)Te crystals to build a demonstrator (CALISTE 256) for the high energy detector module of the SIMBOL-X mission.

The paper is structured as follows: In Section II the ASIC architecture and some design choices are discussed. Section III presents some preliminary experimental results including noise, discrimination threshold, and latchup sensitivity measurements.

II. IDeF-X ECLAIRs ASIC Design

This new IDeF-X chip is a 32-channel analog front end with self-triggering capability. It is derived from the IDeF-X V1.1 chip [4] to which additional functionalities have been added.

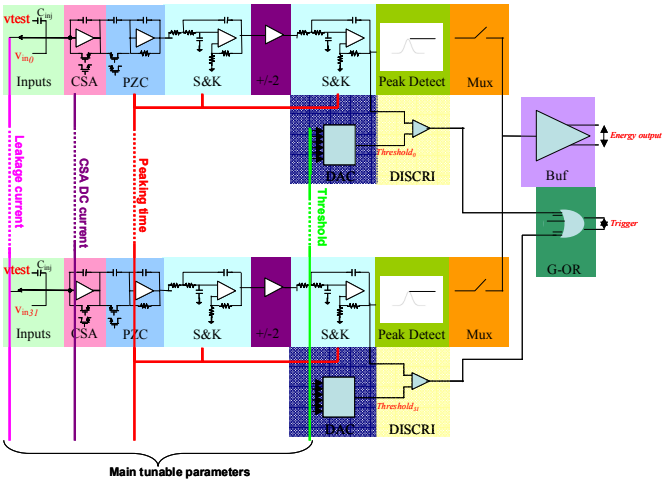

Fig. 1. Schematic of the chip: each channel includes a DC coupled continuous reset CSA, PZ cancellation stage, 4th order shaper (S&K) with an input signal polarity selector (+/-2), peak detector and discriminator with individual 6 bits threshold. A test input allows calibrated charge injection. A current input makes it possible to inject a "dark like" current in the channel. Many parameters are tunable via serial link: peaking time, "dark like" input current, discrimination threshold and test mask. Three modes of readout are achievable: hit channel only, "on demand" and all channels.

The analog part of the channel is almost the same as in IDeF-X V1.1. Conversely, the number of channel, the digital part of

the discriminators, and the readout procedure are fully different.

A. Architecture

The architecture of the analog channel includes a charge sensitive preamplifier (CSA) optimized for detector capacitance from 2 pF to 5 pF with a continuous reset system. The CSA is based on a classical "folded cascode amplifier" with a PMOS type input transistor. The continuous reset system is achieved by a feedback PMOS transistor operating in the subthreshold region. A pole zero cancellation stage (PZC) is used to avoid long duration undershoots at the output. Moreover it amplifies the signal at the output of the CSA and allows optimized DC coupling by minimizing the influence of the dark current on the gain [7]. A variable peaking time fourth order Sallen & Key type shaper with its input signal polarity selector optimizes the signal to noise ratio. A peak detector memorizes the maximum of the shaped signal for energy measurement purpose and a discriminator compares the shaped signal to a programmable threshold for energy discrimination. Each peak detector is connected to the differential output buffer through an analog multiplexer. The channel has been designed to be DC coupled to detectors with low dark currents. However it operates properly with currents up to 2 nA. Depending on the detector (type and geometry) and the measurement conditions (voltage and temperature), the leakage current may vary from few pico amps to roughly 2 nA max. An input injection capacitor is placed in front of every channel to inject a calibrated charge. At last, in order to simulate a detector current or to compensate a reverse detector current, each channel includes a programmable input current source.

TABLE I
IDEF-X ECLAIRS MAIN CHARACTERISTICS

PARAMETER	VALUE
CHIP SIZE	2800 µm × 6400 µm
NUMBER OF CHANNELS	32
POWER SUPPLY	3.3 V
POWER CONSUMPTION	96 mW (3 mW/channel)
GAIN	170-200 mV/fC (peaking time dependent)
DYNAMIC RANGE	50 ke$^-$ (220 keV for CdTe)
DISCRIMINATION THRESHOLD	210 e$^-$ to 4 ke$^-$ (LSB = 65 e$^-$)
SHAPING TYPE	unipolar
PEAKING TIMES (5%-100% OF SHAPED SIGNAL)	0.9 µs to 6 µs

In the IDeF-X V1.1 ASIC, the discrimination threshold is common to all channels. Consequently the low threshold of the chip is imposed by the worst pixel. To prevent this problem in IDeF-X ECLAIRs, each channel has now its own adjustable discrimination threshold thanks to an in-channel 6 bit DAC. A global trigger is built from the logical OR of the 32 discriminator outputs. The signal is sent out the chip differentially to the acquisition to initiate the readout but also for timing purpose.

All the chip configurations (peaking time, thresholds, test modes, CSA current, test injection mask) are programmable via a serial link. The readout operation is started by the chip controller after it received a trigger. First, the IDeF-X ECLAIRs chip send a serial digital pattern corresponding to the hit channel(s). Then, three modes of energy readout are possible: automatic readout of only the hit channel(s), readout of all channels, or programmed readout of the desired channels (on demand readout mode). The main characteristics of IDeF-X ECLAIRs are summarized in table 1.

B. Design for radiation hardness

The ASIC will be used in space: consequently the radiation dose effects on the design and particularly on the CSA have been measured on the previous versions of the chip using the same technology: we irradiated the circuit with a ^{60}Co source up to 224 krad at 1 krad/h dose rate and demonstrated the good tolerance of the design submitted to the total ionizing dose test [6]. These measurement results ensure a high stability of the performances of the circuits during the SVOM (2 years, low earth orbit, inclination 30°) and SIMBOL-X (3 years, highly elliptical orbit) space missions. In order to avoid damages or even destruction of the ASIC due to radiation induced Single Event Latchup (SEL), we optimized the layout of the analog and digital cells to improve the immunity of the chip to SEL. Thus we have designed a radiation hardened digital library: the hardening operation increases the digital surface by a factor of 1.3 but it doesn't increase too much the total surface of the circuit since the digital part of the chip is about only 10 % of the whole surface (without pads and dead areas). The chip has been designed in the standard AMS CMOS 0.35 µm technology, its total power consumption is 96 mW and its area is about 18 mm^2 (Fig 2).

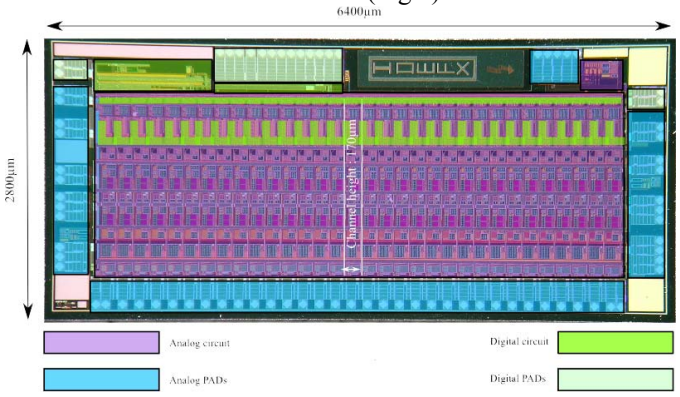

Fig. 2. IDeF-X ECLAIRs layout: SEL hardened design in the standard AMS CMOS 0.35 µm technology. The surface (6400 µm x 2800 µm) is dominated by analog circuit: 10 % only of the active circuit is digital.

III. MEASUREMENTS RESULTS

A. Equivalent Noise Charge

1) Noise floor

Since the IDeF-X ECLAIRs chip has been designed to be connected to very high spectral resolution detectors, the first characterization of the circuit consists in measuring the ENC of the channel at the different peaking times.

When no detector is connected to the chip and no leakage current is programmed, the lowest ENC is achieved at a 6 µs peaking time: the noise is 33 e$^-$ rms. This result is in excellent agreement with the previous IDeF-X chip characterization: 33

and 40 e⁻ rms for IDeF-X V1.0 and V1.1 respectively. When a leakage current is programmed, the parallel noise increases and consequently the optimal peaking time decreases.

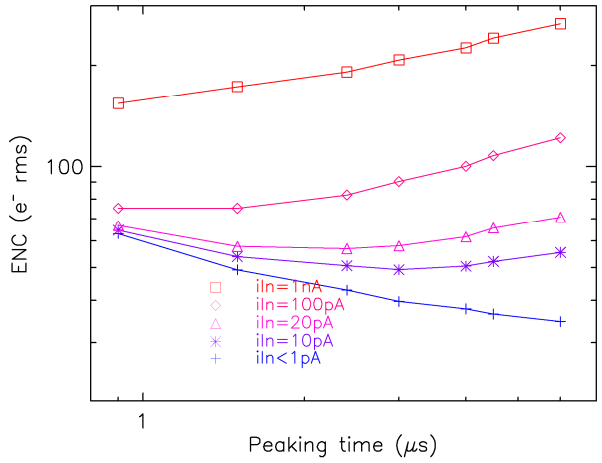

Fig. 3. ENC measurement results for channel 32 at different leakage currents (iln): the measurement is done without detector with a 200 µA current in the CSA, the leakage current is programmed via the serial link (except for 1nA: a 1GΩ resistor is soldered at the input of the channel). The lowest ENC of 33 e⁻ rms is reached for the lowest leakage current for a peaking time of 6 µs.

Fig. 3 allows us to predict the best reachable spectral resolution when connecting our chip to Cd(Zn)Te detectors. For instance, in the case of SIMBOL-X mission, the spectral response is of first importance. Therefore, extremely low dark current and low parasitic capacitance is mandatory. From previous Cd(Zn)Te detector characterizations and particularly of pixelated detectors we know that the typical leakage current will not exceed 30 pA at room temperature and will fall down to 1 pA or even less at a typical temperature of -17°C [3],[8]. Moreover the typical capacitances of the pixelated detectors are very small and can be neglected (100 fF per pixel for a 64 pixel 1 cm² × 1 mm pixelated CdTe detector). Assuming a Fano factor of 0.2, this leads to a floor spectral resolution at 60 keV ranging from 640 eV FWHM (ENC = 33 e⁻ rms) up to 825 eV FWHM (ENC = 60 e⁻ rms). Actually, with the constant decrease of the leakage current (thanks to Schottky contacts and cooling of the crystals) and of the input capacitance (thanks to miniaturization of the surface) of this type of detectors, the dominant source of noise becomes more and more often the parasitic capacitance brought by the interconnections between the detector and the electronics. It does not mean that the leakage current is a solved problem, it is only a postponed problem. When the parasitic input capacitance is reduced enough, one will be able to reduce the dimensions of the input transistor of the CSA and the influence of the leakage current will be unconcealed.

2) Effect of input capacitance

In order to predict the performances of the chip connected to a detector through a capacitive interconnection, we measured the influence of the input capacitance on the noise behavior of the circuit. We soldered discrete ceramic capacitors at the input of one channel of the chip (channel 32). For each peaking time, we plot the ENC=f(C_{in}) curve (for 7 different measured values of C_{in} from 1.5 to 33 pF) to extract the slope ENC/C_{in} with a linear fit for each peaking time.

As expected, the minimal slope is obtained at the highest peaking time (6 µs) where the series noise contribution is the lowest. For iln=10 pA, the ENC is:

$$ENC(at\ t_{peak} = 6\ \mu s) = 55\ e^- + 7\ e^-/pF \qquad (1)$$

Plotting the square slope $(ENC/C_{in})^2$ as a function of $1/t_{peak}$ (Fig. 4), intrinsic noise parameters for series (α_d) and *1/f* ($\alpha_{1/f}$) contribution may be derived.

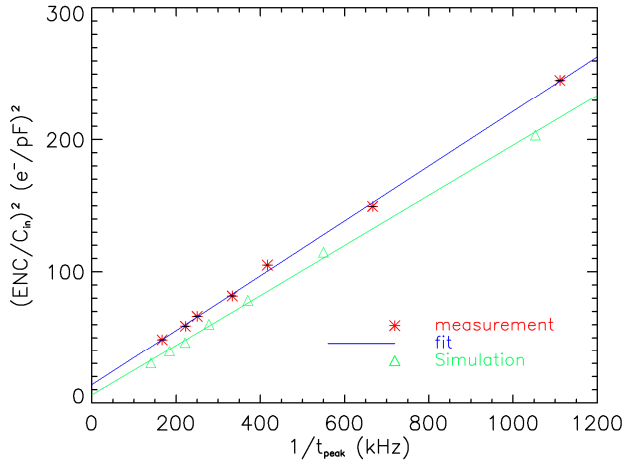

Fig. 4. The curves ENC=f(C_{in}) are fitted to extract the slopes ENC/C_{in} at different peaking times. The measurements are obtained with a 10 pA leakage current. The square slope is plotted as a function of $1/t_{peak}$. The slope of the straight line gives the series noise coefficient (α_d) and the ordinate at $(1/t_{peak})=0$ gives the $\alpha_{1/f}$ coefficient.

The theoretical expression of the ENC at the output of the shapers is [9]:

$$ENC^2 = C_{tot}^2\left(\frac{\alpha_d}{t_{peak}} + \alpha_{1/f}\right) + \alpha_{//} \cdot i_{leak} \cdot t_{peak} \qquad (2)$$

Where:

- $C_{tot} = C_0 + C_{in}$,
- C_0 is the total capacitance into the chip at the input of the CSA plus the capacitance on the ASIC board,
- C_{in} is the additional soldered capacitance,
- α_d is a parameter that depends on the filter order as well as the transconductance of the input transistor of the CSA,
- $\alpha_{1/f}$ is a parameter that depends on the filter order as well as technological parameters and the area of the input transistor,
- $\alpha_{//}$ is a parameter that depends on the filter order,
- i_{leak} is the leakage current injected at the input of the CSA.

For high input capacitances, the contribution of parallel noise to total noise can be neglected and the curves ENC= f(C_{in}) can be fitted by a linear model. The slope factor ENC/C_{in} is then given by (3).

$$\left(\frac{ENC}{C_{in}}\right)^2 = \frac{\alpha_d}{t_{peak}} + \alpha_{1/f} \qquad (3)$$

Thus, the slope of the fitted straight line gives the series noise coefficient (α_d) and the ordinate at ($1/t_{peak}$)=0 gives the $\alpha_{1/f}$ coefficient. The extracted noise parameters are summarized in table II.

TABLE II
SERIES AND 1/F EXTRACTED NOISE PARAMETERS

PARAMETER	MEASURED VALUE	SIMULATED VALUE
$\sqrt{\alpha_d}$	447 $e^-.ns^{1/2}.pF^{-1}$	436 $e^-.ns^{1/2}.pF^{-1}$
$\sqrt{\alpha_{1/f}}$	3.74 e^-/pF	2.45 e^-/pF

The simulated and measured series noise parameters are in excellent agreement. However we found an excessive *1/f* noise. This can come from the fact that the simulator underestimates the *1/f* noise of the input transistor of the CSA. That can also come from an additional capacitive sensitive unexplained noise.

Eight of the IDeF-X ECLAIRs Asics, coupled to a 256 pixelated CdTe detector will constitute a hard X-ray micro camera that will be the elementary part of the high energy detector module of the SIMBOL-X mission. This mission requires a spectral resolution better than 1.3 keV at 60 keV. To fulfill this requirement, the additional input capacitance of each channel has then to be smaller than 8 pF. The measurements that we have already performed with a 64-pixel detector [3] have demonstrated that the input capacitance was less than 2 pF. Thus we believe that the objective of 1.3 keV at 60 keV will be easily reached. Moreover, the results (697 eV FWHM at 13.9 keV and 808 eV FWHM at 59.54 keV) obtained with the 64-pixel prototype equipped with the previous chip that exhibits similar noise performances fortify this assumption.

B. Energy Discrimination Threshold

The challenging low threshold requirement for this chip is mainly driven by the CdTe based CXG (X and Gamma camera) of SVOM/ECLAIRs instrument. As a matter of fact, the main assignment of this camera is to detect gamma ray bursts down to 4 keV (905 e^- rms) and to alert in real time the other instruments on board.

The low threshold will mainly depend on the ASIC intrinsic noise, on the detector parallel noise (due to leakage current) and on the connection between the detectors and the ASIC inputs, especially on the parasitic capacitances brought by those interconnections. The leakage current should not be the dominant noise source thanks to the cooling of the detectors (~-20°C). This is the reason why we focused on the sensitivity of the discrimination threshold to the input capacitance (see §2).

1) Discriminator Transfer function

First of all, we characterized the discriminators in order to measure the value of the LSB of the DAC and to locate the 0 thresholds (the baselines of the comparators). For each channel of the ASIC, we measured the S-curves for different input charges. The inflection points of these curves correspond to the values of the threshold for which half of the event passes over the threshold. They are plotted as a function of the incident charge in Fig. 5.

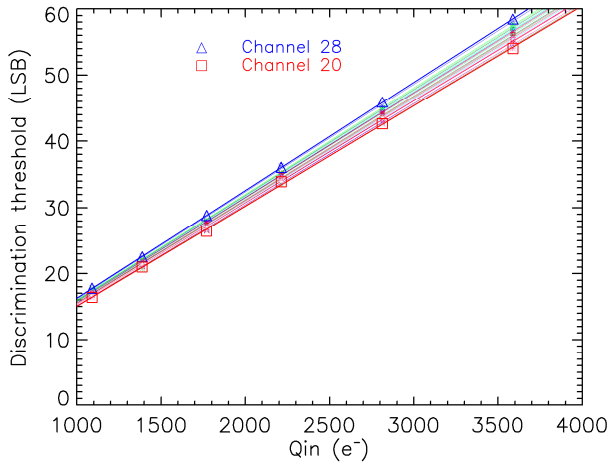

Fig. 5. Transfer function of the 32 discrimination channels: the measurements are performed with a peaking time value of 6 µs. The linearity is verified over 3.5 ke^-. The interpolated 0 threshold (Discrimination threshold for Qin=0) is found to be 4.3 LSB +/- 0.8 LSB (peak to peak).

This gives the transfer function of each discrimination channel including the 0 threshold (in LSB) and the slope (in LSB/e^-). The dispersion between the slopes of the curves are induced by dispersions of the transfer functions of the CSA+PZC+Shapers part of the channel and by the dispersions between the transfer functions of the DAC of the comparators. The LSB_i value of channel i can then be calculated using (4)

$$LSB_i(eV) = \frac{1}{a_i} w \qquad (4)$$

Where:

- a_i is the measured slope (in LSB/e^-) of channel i,
- w=4.42 eV/pair is the pair energy creation for CdTe at 300K.

The LSB value of each channel is given in Fig. 6.

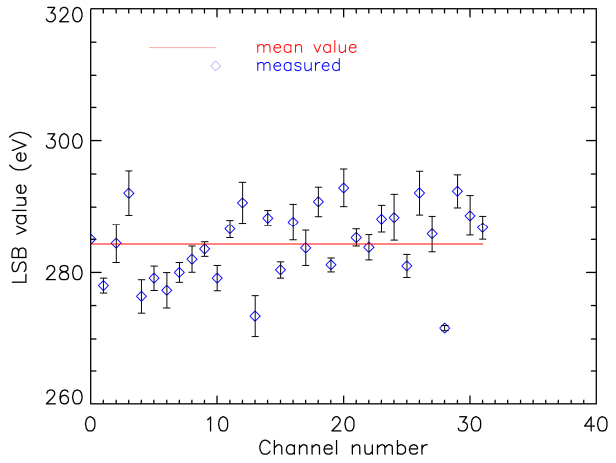

Fig. 6. Fitted LSB values as a function of the channel number. The mean value is 284 eV. The standard deviation between channels is 2% of the mean value.

The measured mean value is 284 eV, very similar to the simulated value of 285 eV.

2) Influence of Input capacitance

In order to evaluate the effect of the input capacitance on the low discrimination threshold of the chip, we soldered discrete ceramic capacitors at the input of two channels of the chip (channel 32 and 1). To make the plots clearer, only the results obtained with channel 32 are reported. For all measurements, we programmed a 20 pA input current. 20 pA is the order of magnitude of the leakage currents that have been measured with the cooled detectors of the CXG camera at -20°C. For each input capacitor, we measured the mean time of auto-triggering on noise as a function of the threshold of the discriminator (Fig. 7).

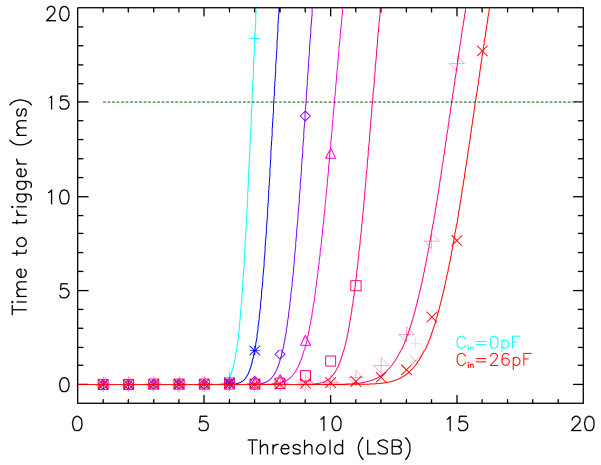

Fig. 7. Mean time to trigger as a function of discrimination threshold for different input capacitors: the measurements are performed with a peaking time of 6 µs, a leakage current of 20 pA and a bias current in the CSA of 200 µA. Each point of the curves is the average of 50 measurements.

A first threshold is programmed and a reset of the chip is done, then we wait for the comparator triggering. The time to trigger is then recorded (50 times), another threshold is programmed and the chip is reset again. This procedure is repeated until the time to trigger exceeds a time limit (timeout). In that case, we consider that the time to trigger equals the timeout and the measurement is stopped. Thus we are able to plot the intersection points between these curves and a time threshold. In Fig. 8 the results are plotted using a time threshold (15 ms) of half the timeout (30 ms). All the measurements have been performed using the highest peaking time value of 6 µs to minimize the serial noise contribution to total noise.

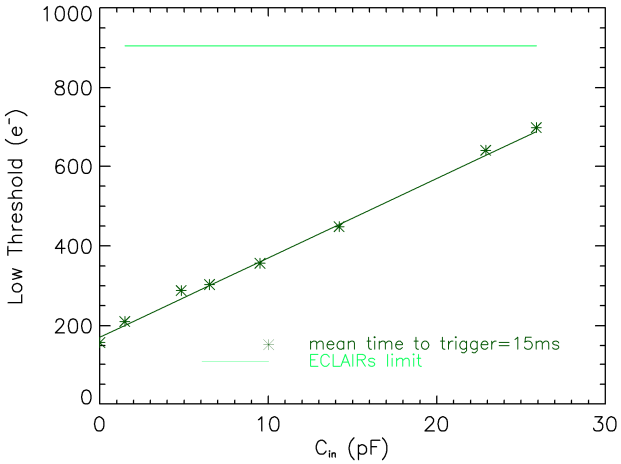

Fig. 8. Low threshold as a function of input capacitance C_{in} for a current in the CSA of 200 µA. The low threshold guarantees that the false triggers caused by noise induce a dead time smaller than 0.5 %. The measurements are realized without detector at a 6 µs peaking time with a 10 pA leakage current. The slope is evaluated to 20 e^-/pF (88 eV/pF).

The mean time to trigger value has to be compared to the time to read the ASIC in total: the ratio between these two values gives the percentage of dead time due to parasitic trigger caused by noise. The low threshold is the threshold that guarantees a certain maximal value of percentage of dead time caused by noise induced "false events". In our case, the time to read the entire chip is about 75 µs. A mean time to trigger of 15 ms implies a dead time of 0.5 % induced by noise events. The measured values in Fig. 8 can be fitted by a linear model and the low threshold is then given by (5).

$$LowThreshold = 171\,e^- + 20\,e^-/pF \qquad (5)$$

By comparing (1) and (5), we find that the threshold that guarantees a percentage of dead time induced by noise events smaller than 0.5% corresponds to about three times the rms noise for a peaking time value of 6 µs.

In the case of ECLAIRs mission, we find by using (5) that the input capacitance (detector + parasitic) has to be smaller than 36 pF for the maximal peaking time (6 µs). Actually, the measurements have been obtained with capacitors that exhibit very good dielectric properties. In reality the material of interconnection is not often so good and dielectric losses can induce an additional noise plateau (almost independent of the peaking time). In the specific case of CXG, the input capacitance (detector + parasitic) in the CXG camera has been evaluated to 7 pF and the optimization of the interconnection material is still in progress. According to these conditions, the

critical objective of a low threshold of less than 4 keV seems then to be easily reachable.

C. Heavy ion irradiation

1) Measurement setup

The space radiative environment can induce many degradations (dose effects) dysfunction (SEL, Single Event Upset) or even destruction (SEL) of the CMOS integrated circuits [10].

We have demonstrated that the dose effect was not an issue for the SVOM mission (few krad) nor for the SIMBOL-X mission (few tens of krad).

To detect SEU, all the programming registers have been duplicated in the chip. For each register, a XOR gate enables to detect a difference between the register and its duplicated neighbor. A global error output is then built from the logical OR of all the XOR outputs. The sensitivity of the chip to SEU has not been measured yet. Nevertheless, such events are less critical as far as a simple software reset will efficiently restore the proper ASIC configuration. For instance, in ECLAIRs, this procedure occurs at least daily or more often if necessary, possibly inducing dead time. SEU will mainly occur while the satellite goes through the South Atlantic Anomaly (SAA), where the science data are not usable due to induced background in the instrument.

SEL are much more dangerous: a SEL can destruct a chip. To deal with this issue, we first measured SEL sensitivity on IDeF-X V1.1 prototype which has been found insufficiently tolerant. Our current design for IDeF-X ECLAIRs has been improved and a second latchup campaign has been done. The cross section results are injected into the space missions ECLAIRs and SIMBOL-X radiation environment models to compute the in flight SEL rate, supposing the pessimistic assumption that the ASIC are shielded by only 3.7 mm of aluminum (OMERE 3.2 from TRAD Company).

Heavy ions induced SEL tests were performed at the Cyclotron of the University Catholique de Louvain (UCL) which is able to accelerate protons, alpha particles and heavy ions. By using the same ion cocktail, it is possible to cover a wide Linear Energy Transfer (LET) spectrum from a few MeV.cm^2.mg^{-1} to higher than 100 MeV.cm^2.mg^{-1}, with a good beam homogeneity. We developed a dedicated board to properly operate the circuits and to monitor the different power supplies in order to localize any SEL in the chip. Five different power supplies were under test: 4 analog supplies corresponding to different analog part of the channel and one digital supply (v_{ddd}) corresponding to the digital blocks of the ASIC. Two identical boards were mounted on a structure that enables translation (for alignment purpose) and rotations (for effective LET increase purpose) of the devices (Fig. 9). The chip under test was irradiated until an effective fluency between 35.10^4 and 10^7 particles/cm^2 is reached (depending on the type of particles) with a flux of several thousands of particle/cm^2/s.

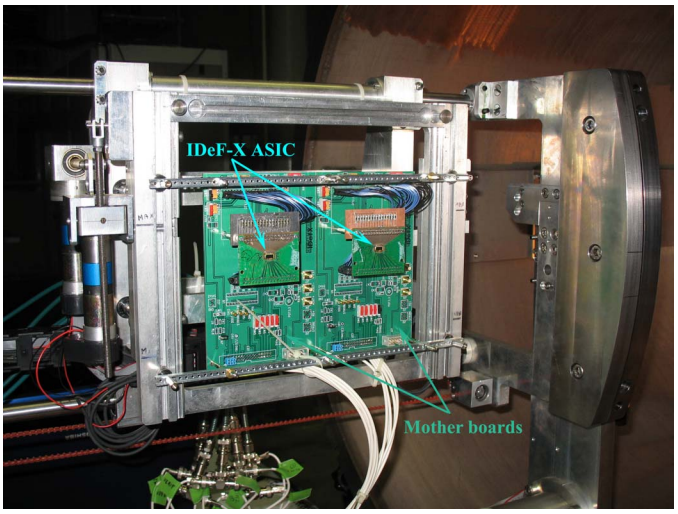

Fig. 9. Photograph of the setup: The two mother boards are connected to a mobile structure. Each ASIC under test is mounted on its own daughter board and each daughter board is connected to its mother board that delivers power supplies and programming signals.

We irradiated two IDeF-X ECLAIRs ASICs with different substrates:

- ID1: standard bulk substrate.
- ID6: substrate with an epitaxial layer of 14 µm.

During the experiment, the latchup counter was incremented when one of the current of the power supply rose above a pre-specified threshold. In our case, the current thresholds were settled to 1.5 to 2 times the nominal currents in order to be able to observe micro latchups.

2) Results

Fig. 10 gives the SEL cross section as a function of the effective LET for the two chips ID1 and ID6 and for the previous IDeF-X chip IDeF-X V1.1. The results have been obtained with Xenon, Krypton and Argon ions at different incidence angles. Thanks to our hardened digital library, we did not notice any latch up in the digital blocks. The LET threshold of the digital library exceeds 110 MeV.cm^2.mg^{-1} (with and without epitaxial layer). Previous SEL measurements performed with the IDeF-X V1.1 chip had lead to a LET threshold of about 12 MeV.cm^2.mg^{-1} of the digital blocks designed with the standard digital library. Thanks to the new hardened library, the SEL LET threshold of the chip is no more imposed by the digital cells even if the total digital area of IDeF-X ECLAIRs is 25 times larger the IDeF-X V1.1 digital surface. The extracted LET threshold of the ID1 chip is 49 MeV.cm^2.mg^{-1} and the latch up are induced in the analog parts only. The epitaxial layer provides a low substrate resistance that requires higher current to forward bias the substrate [11]. Thus we measured a higher LET threshold with the ID6 chip close to 56 MeV.cm^2.mg^{-1}.

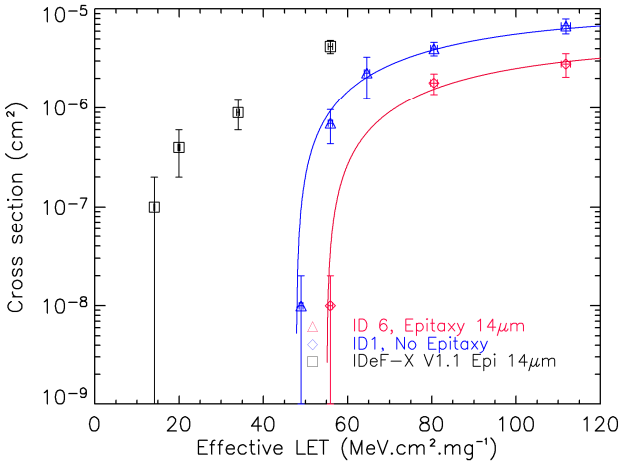

Fig. 10. Effective LET: influence of the epitaxial layer. Heavy ion SEL characterisation at UCL (Belgium) with Ar, Xe and Kr. Test results for two types of substrate: the epitaxial layer increases the effective LET. No EPI: 49 MeV.cm².mg^{-1}. EPI 14 µm: 56 MeV.cm².mg^{-1}.

Moreover, all the measurements have been realized at room temperature and it is widely admitted that the LET threshold decreases with temperature [12]. In the case of both missions, the detector and, to a lesser extent, the electronics will be cooled. We can then expect a higher LET threshold and thus an even better immunity to SEL. Anyway, injecting the SEL cross section vs. LET curves into the radiation environment models of ECLAIRs and SIMBOL-X, no latchup are expected at all, during both missions over five years of operation. Note that in the ECLAIRs case, the Low Earth Orbit inclined at 30° is particularly safe, even passing through the SAA several times a day. The SIMBOL-X orbit, far from the radiation belts, is more aggressive with respect to the heavy ions but the chips are SEL tolerant enough.

IV. Conclusion

The ASIC IDeF-X ECLAIRs is a very low noise multi channel integrated circuit. It is optimized for the readout of low capacitive (2-5pF) and low dark current (~ 1 pA to few nA) Cd(Zn)Te monopixel detectors or pixel arrays for future X and gamma-ray astronomy space missions. The noise performances of this chip are very promising since the floor ENC was found to be 33 e$^-$ rms and the low threshold is 2 keV with a 14 pF input capacitance. Thanks to our new SEL hardened digital library, the measured LET threshold of 56 MeV.cm^2.mg^{-1} demonstrated a very high SEL immunity that makes the ASIC well suited for spaceborne applications. Today, these very satisfactory results make possible the production of about 1500 chips on an epi-substrate for the SVOM mission. The next step will consist in connecting the chip to different types of Cd(Zn)Te detectors to confirm the predicted spectral resolutions and low thresholds. Finally, SEU test results will allow us to evaluate the frequency of reset during the mission and the induced dead time.

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VI. References

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