Picosecond time measurement using ultra fast analog memories.

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Abstract

The currently existing electronics dedicated to precise time measurement is mainly based on the use of constant fraction discriminators (CFD) associated with Time to Digital Converters (TDC). The time resolution measured on the most advanced ASICs based on CFDs is of the order of 30 ps rms. TDC architectures are usually based either on a voltage ramp started or stopped by the digital pulse, which offers an excellent precision (5 ps rms) but is limited by the large dead time, or on a coarse measurement performed by a digital counter associated with a fine measurement (interpolation) using Delay Line Loop, which exhibits a timing resolution of 25 ps, but only after a careful calibration. The overall precision of these systems includes the contribution of both elements (CFD + TDC).

In the meantime, alternative methods based on digital treatment of the analogue sampled then digitized detector signal have been developed. Such methods permit achieving a timing resolution far better than the sampling frequency. Digitization systems have followed the progress of commercial ADCs, but the latter have prohibitory drawbacks as their huge output data rate and power consumption. Conversely, high speed analog memories now offer sampling rates far above 1GHz at low cost and with very low power consumption.

The new USB-WaveCatcher board has been designed to provide high performances over a short acquisition time window. It houses on a small surface two 12-bit 500-MHz-bandwidth digitizers sampling between 400 MS/s and 3.2 GS/s. It is based on the SAM chip, an analog circular memory of 256 cells per channel designed in a cheap pure CMOS 0.35µm technology and consuming only 300 mW. The board also offers a lot of functionalities. It houses a USB 12 Mbits/s interface permitting a dual-channel readout speed of 500 events/s. Power consumption is only 2.5 W which permits powering the board with the sole USB.

When used for high precision time measurements, a reproducible precision better than 10 ps rms has been demonstrated.

The USB-WaveCatcher can thus replace oscilloscopes for a much lower cost in most high-precision short-window applications. Moreover, it opens new doors into the domain of methods used for very high precision time measurements.

I. State of the art

The currently existing electronics dedicated to precise time measurement is mainly based on the use of constant fraction discriminators (CFD) associated with Time to Digital Converters (TDC). The constant fraction technique minimizes the time walk effect (dependency of timing on the pulse amplitude). Several attempts have been made to integrate CFD in multi-channel ASICs. But the time resolution measured on the most advanced one is of the order of 30 ps rms. Moreover, the quality of the result with this technique is strongly dependent on the input pulse shape, because pure delay lines require inductances which are not designable in an ASIC, and delays are thus replaced by signal shaping.

Two main techniques are used for the TDC architectures. The first one makes use of a voltage ramp started or stopped by the digital pulse. The obtained voltage is converted into digital data using an Analog to Digital Converter (ADC). The timing resolution of such a system is excellent (5 ps rms). But this technique is limited by its large dead time which can be unacceptable for the future high rate experiments. Another popular technique associates a coarse measurement performed by a digital counter with a fine measurement (interpolation) using Delay Line Loop. Such a system can integrate several (8-16) channels on an FPGA or an ASIC. The most advanced DLL-based TDC ASIC exhibits a timing resolution of 25 ps, but only after a careful calibration.

It has to be noticed that with all these techniques, the overall timing resolution is given by the quadratic sum of those of the discriminator and of the TDC, thus leading to a degraded performance.

In the meantime, alternative methods based on digital treatment of the analogue sampled then digitized detector signal have been developed. Such methods permit achieving a timing resolution far better than the sampling frequency. For example, a 100-ps rms resolution has been reported for a signal sampled at only 100 MHz.

Digitization systems have mostly followed the progress of commercial ADCs, which currently offer a rate of 500 MHz over 12 bits. Their main drawbacks are the huge output data rate and power consumption. Their packaging, cooling, and tricky clock requirements also make them very hard to implement. Conversely, high speed analog memories now offer sampling rates far above 1GHz at low cost and with very low power consumption. They are a very interesting alternative to the use of ADCs wherever the sampling depth remains short. This will be shown again in this paper.

II. The SAM analog memory

The SAM chip [1], whose block diagram is shown in Fig. 1, makes use of the 3.3V CMOS AMS 0.35µm technology. Its area is only 11 mm^2 and it integrates 60000 transistors. It houses two channels, each including 256 analog storage cells.

The high sampling frequency (Fs) of SAM is obtained by a virtual multiplication of the lower frequency clock (Fp) using internally servo-controlled Delay Line Loops (DLL). But, rather using a linear structure, each analog memory channel is configured as a matrix of 16 lines with 16 capacitors each, as shown in Fig. 2. This structure was already used in the MATACQ chip described in [2]. In this structure, successive capacitors in the same column contain consecutive analog samples taken at 1/Fs whereas successive capacitors in the same line contain samples taken at 1/Fp = 16/Fs intervals. The sampling timing is ensured by a 16-step DLL associated with each column and of which the delay is servo controlled to 1/Fp. The input signal is split, using for each line a voltage buffer feeding the analog signal. In each line also, a readout amplifier permits reading back the analog information stored in the capacitors. During readout, the read amplifier outputs are time-multiplexed towards an external ADC. Both the write and read operations are performed in voltage mode in the capacitors in order to ensure total voltage gain robustness against parasitic elements or components mismatch.

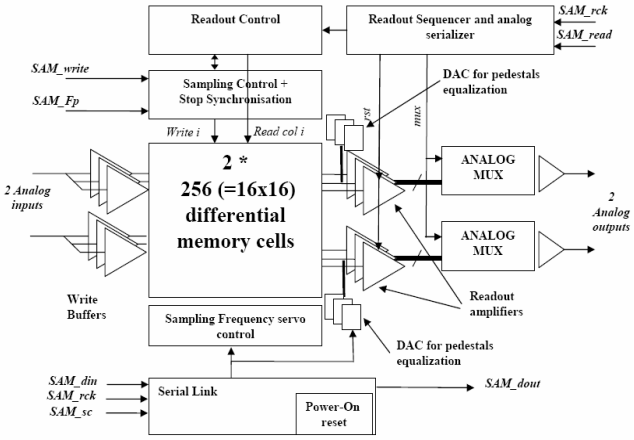

Figure 1: Block diagram of the SAM chip.

The matrix architecture offers the following advantages compared to the standard linear sampling DLL structure:

- Better analog bandwidth for the same power consumption dissipated in the input buffers.
- Lowest switching noise during the write phase as the switching time interval between two consecutive memory cells on the same line is long (1/Fp).
- Lower readout noise. This noise contribution is, at the first order, proportional to 1+Cr/Cs where Cs is the capacitance of the storage element and Cr is the total capacitor of the readout bus connected to the negative input of the readout amplifier. Actually, Cr is smaller in a matrix structure, because the read busses are shorter than in the linear structure
- Faster readout time, as 16 consecutive capacitors are read simultaneously by the readout amplifiers.

Several useful peripheral functions have been implemented in the chip:

- A functional block memorizing the position of the last cell written before the stop signal arrival and calculating the index of the first cell to be read back using an offset register called Nd.
- A functional block selecting the 16 capacitors to be read in parallel. Actually, these capacitors are eventually spread on two consecutive columns, depending on the index of the first cell to be read,
- One 7-bit DAC for each line of the matrix to compensate the static offsets due to the use of amplifiers on each line in the matrix structure. These DACs must be set during a dedicated calibration phase with no signal on inputs.
- The DLLs have been designed to avoid unlocking during readout which would introduce extra dead-time between acquisition.
- A slow-control serial link to program various parameters of the chip (Nd, DACs settings, test mode, biasing of the amplifiers…).

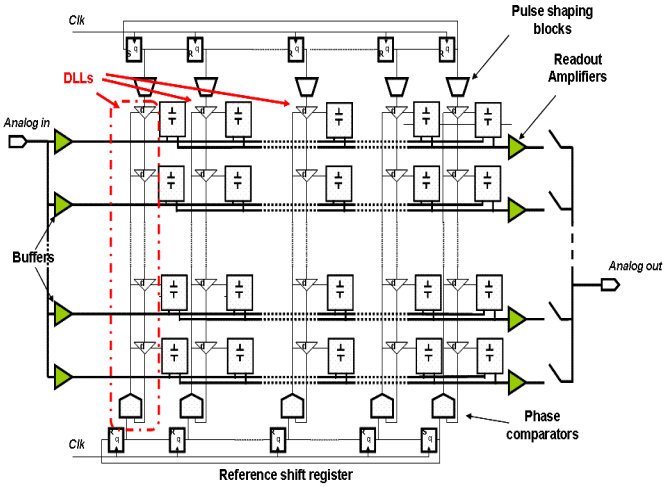

Figure 2: Principle of the sampling DLL matrix.

To decrease the effect of digital switching, each analog memory channel is actually fully differential and all the potentially noisy digital input or output external signals are using LVDS standard.

III. The USB Wave Catcher Board

The new USB-WaveCatcher board (see Fig. 3) has been designed to provide high performances over a short time window. It houses on a small surface two 12-bit 500-MHz-bandwidth digitizers sampling between 400 MS/s and 3.2 GS/s. It is based on the SAM chip described above.

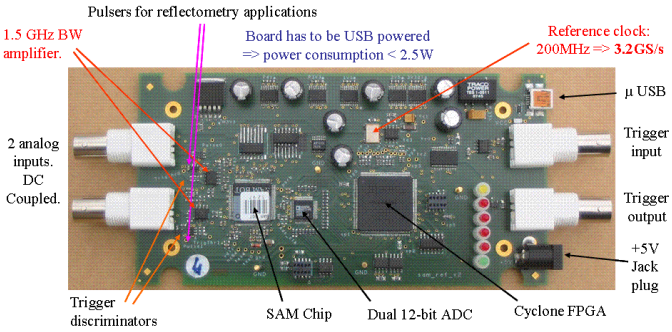

Figure 3: the USB Wave Catcher board

As the SAM chip memory depth is 256 samples, the acquisition time window duration depends on the sampling frequency (80 ns for 3.2GS/s up to 320 ns for 400MS/s).

The inputs are DC-coupled and a programmable DC offset covering the whole dynamic range (±1.25V) can be applied independently on the two channels in order to optimize the signal measurement. Trigger discriminators with programmable thresholds are located on each input. The board also houses individual programmable channel pulsers for reflectometry applications. The precision obtained for cable length measurements is then as good as 2mm. It can be triggered either internally or externally and several boards can easily be synchronized. Trigger rates counters and dead time estimator are implemented. Charge measurement mode is also provided, through integrating on the fly over a programmable time window the signal coming for instance from photo-multipliers. Photo-electron spectra can thus be realized very quickly.

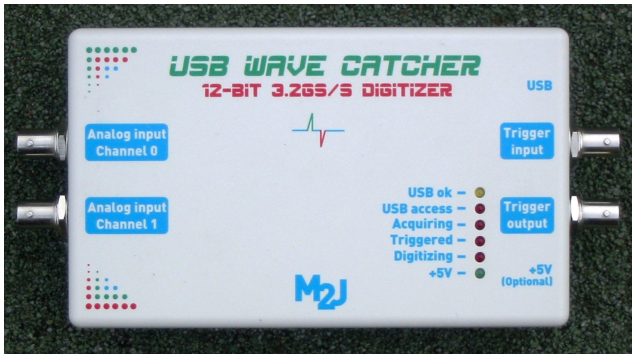

Figure 4: the USB Wave Catcher box

By default, the connectors implemented are BNC, but they can be replaced by LEMO or SMA on demand.

The board is packaged in a convenient plastic box (see Fig. 4). Its reduced power consumption (below 2.5W) allows it to be powered by the sole USB. It houses a USB 12 Mbits/s interface permitting a dual-channel readout speed of 500 events/s. Faster readout modes are also available. In charge measurement mode, the sustained trigger rate can reach a few tens kHz. A 480Mbits/s version will soon be available.

IV. Acquisition Software

A dedicated acquisition software has been developed with CVI/LabWindows.

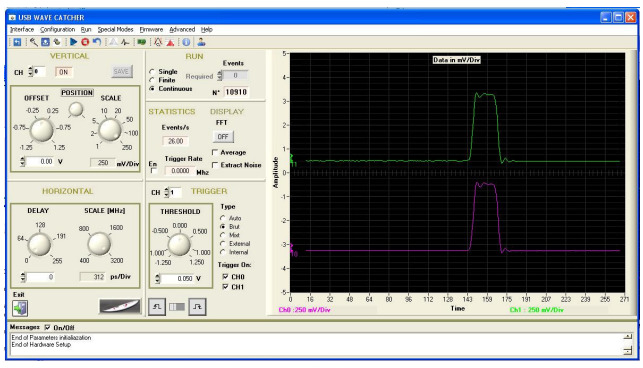

Figure 5: the main graphical user interface of the Wave Catcher acquisition software.

It offers an oscilloscope-like front panel and the same kind of possibilities for data taking and displaying. It permits taking benefit of all the features available on the board. Data can be stored in files on demand. Standard running can easily be handled directly on the front panel, and advanced modes are accessible via different menus. The main graphical user interface is displayed on Figure 5.

This acquisition software will soon be available as a Windows installation package on the LAL web site at the following URL:

http://electronique.lal.in2p3.fr/echanges/WaveCatcher/index.htm

V. Time Measurements

A. Raw measurements

In the usual configurations used for time measurement, the analog signals first have to be discriminated before being sent to TDCs as described in the first chapter. In this case, the discriminator is an additional source of error. Using analog memories permits getting rid of the discriminator. The measurement will be performed directly on the analog signal, thus permitting independence to the pulse shape. However, in order to reach the ultimate possible precision, a precise time calibration of the memory will have to be performed.

We will first present here the measurements performed without any time calibration.

An easy way to measure the jitter performance of a digitizing system consists in performing a measurement of its Effective Number Of Bits (ENOB). As shown on Fig. 6, it is expected from theory that ENOB diminishes with the increase of sine wave frequency for a given sampling jitter. The measurements performed on the Wave Catcher board, plotted as dots on the same figure, are compatible with a raw sampling precision of 16ps rms without any time correction.

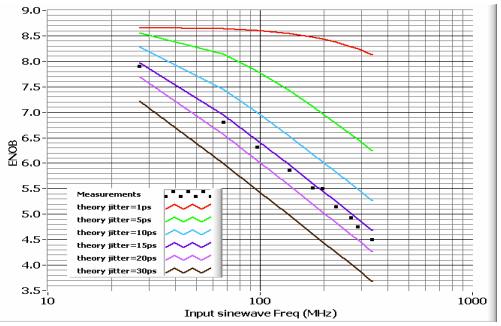

Figure 6: ENOB measurement with no time calibration with a 300mV pp sine wave compared to simulation.

The usual measurement one actually wants to perform is the time distance between two pulses. In order to characterize properly this type of signal, a simple setup has been used. It consists in sending a pulse from a generator both to the board and to an un-terminated cable. The signal is reflected at the open extremity of the cable and comes back to the board. This is a way to obtain very clean repetitive signals, but with slightly different amplitudes. Anyway, this is close to real life operation.

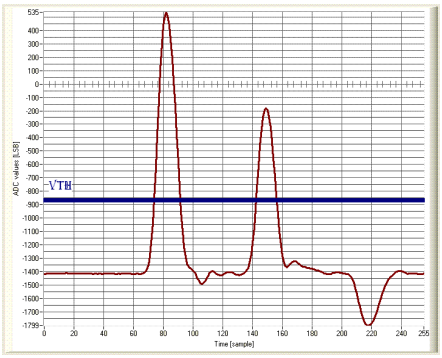

Figure 7: Two pulses generated by an open cable.

Different cable lengths have been used. The dual-pulse (see Fig. 7) is sent totally asynchronously with respect to the board clock, thus falling wherever in the sampling matrix of the SAM chip. That way, all the types of jitter are taken into account in the measurement. The timing is measured with a fixed threshold (drawn in green on the left plot), of which the crossing instant is extrapolated thanks to a fourth degree polynom. Whatever the distance between the pulses, the jitter is of 22 ps rms, which again gives a single pulse resolution of about 16 ps rms without any correction.

There are actually two main contributions in the time jitter: the random jitter and the Fixed Pattern jitter. Random jitter is dominated by two sources: the sampling jitter which is due to the random aperture jitter of the switches, and the noise on the signal itself. The smart design of the storage cells permits obtaining a very small aperture jitter, whereas the high SNR of the analog memory reduces the noise added to the signal. The Fixed Pattern jitter actually represents the main contribution as it will be shown below. But as its position is fixed in the matrix and very reproducible, it can be corrected.

B. Methodology for time calibration

The effect of the Fixed Pattern Time Distribution along the DLL which is the main element of the time INL on the measured signal can be viewed on Figure 8. Time spread is exaggerated here in order to make the understanding of the effect easier. The later actually appears as a fixed irregular distance between samples, due to the irregularities in the silicon and to fixed coupling effects.

Two methods can be envisaged to recover from this fixed time error after time INL calibration. The first one consists in using floating points for the time coordinates of the samples. This is not always easy to deal with, because it adds a dimension to the correlated arrays in the software. The second one consists in correcting the sampled points to extrapolate the position of the equidistant points located on the real signal. This has the supplementary advantage of making the FFT calculation of the signal possible. The algorithm used for the latter method is based on a simple third degree Lagrange polynomial interpolation. Three points are enough because the distance between the samples and the equidistant points always remains small (below 15% of the distance between samples) thanks to the matrix structure. Figure 8 shows how the signal is corrected that way.

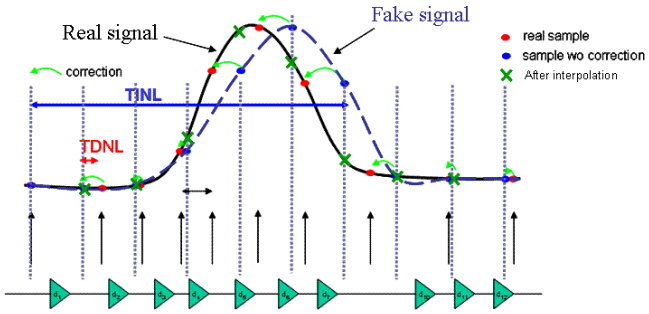

Figure 8: effect of Fixed Pattern Time Distribution on signal sampling.

In order to perform easily this type of high precision calibration, a new technique has been developed. It consists in sending to the board channels a sine wave signal at a frequency between 100 and 200MHz (the optimum is around 135MHz for 3.2 GS/s) and of rather high amplitude (500 mV rms i.e 1.4V pp). The part of the sine used for the measurements is all the segments crossing the zero (mid-height) of the curve (see Fig. 9). With the well chosen frequency and amplitude described above, these segments can be assimilated to straight lines with a systematic error remaining below 1ps rms. The mean length of said segments will give the time DNL, whereas the rms of their values will give the random sampling noise. If one integrates the time DNL and fits the result, the time INL can be calculated and then corrected online.

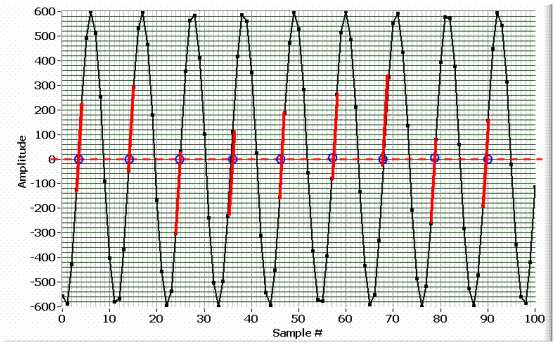

Figure 9: segments used for the DNL measurement.

C. Measurements after calibration

1) Calibration and characterization of the board

Thanks to the method described above (zero-crossing segments of a sine wave), fine measurements of the time characteristics of the board have been performed.

An example of raw time DNL is shown on Figure 10. Horizontal axis displays the cell number and vertical axis the segment lengths in ADC counts (with 0.61mV per ADC count). The rms on the segment length is of 9 ps. Once integrated and fit, it appears as shown on Figure 12 (vertical axis is now in ps), with an rms of 16ps, perfectly coherent with the ENOB measurement. Note that this shape is mainly chip-dependent, but very stable with time and temperature, thanks to the DLL servo-control.

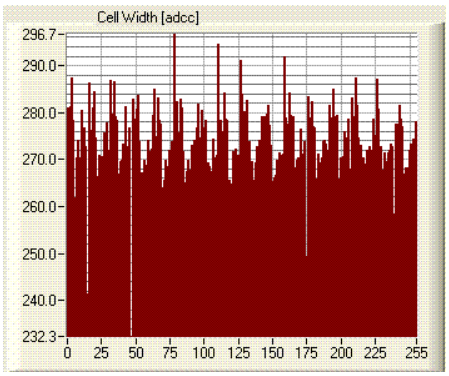

Figure 10: example of raw time DNL.

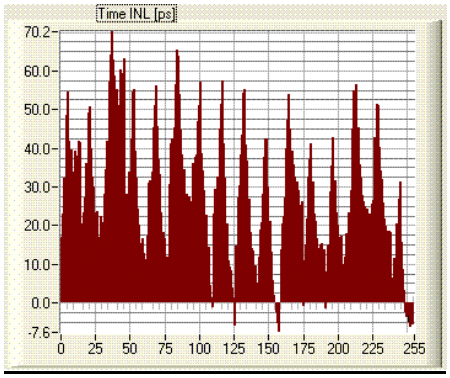

Figure 11: corresponding raw time INL.

Once this time calibration is performed, the time INL can be corrected online by software with the Lagrange polynomial interpolation. When sending the same sine wave to the board, time DNL and INL can be measured again. Figures 12 and 13 exhibit the improvement in the time precision, with an rms of 0.33 ps for the time DNL and of 1.15 ps for the time INL.

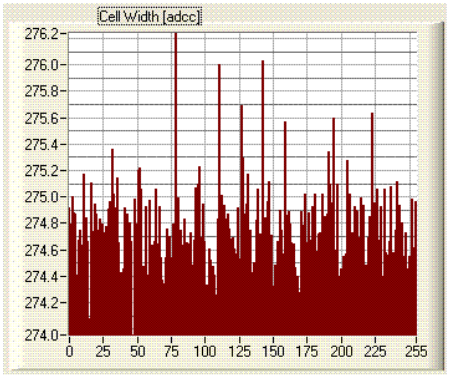

Figure 12: time DNL after correction.

Of course, in order to be useful, this calibration has to be valid for every kind of input signal. Therefore, keeping the same calibration files, the jitter measurement has been performed with different frequencies of the input sine wave covering the range where the method is effective (~ 100 to 200 MHz). The rms of the INL always remains below 2.5 ps, thus validating the method.

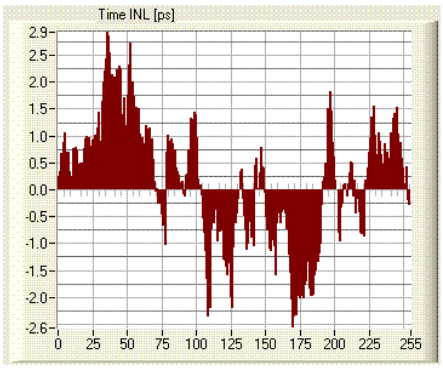

Figure 13: time INL after correction.

Now, we can come back to the measurement of the time difference between two pulses.

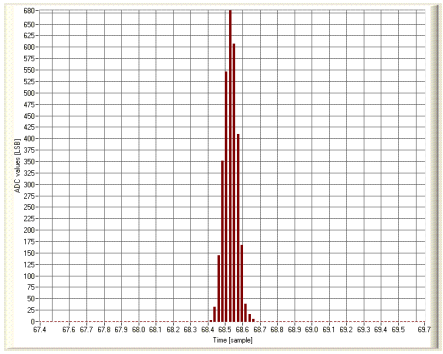

Figure 14: dual-pulse time difference distribution after correction.

Once the calibration performed, the time difference between the same pulses as in Figure 6 is measured with the same method (threshold crossing time extrapolated thanks to a fourth degree polynom). On figure 14, 5000 events are displayed (horizontal axis grid step is 3.125 ps). Whatever the distance between the pulses, the jitter is of 11ps rms, which now gives a single pulse resolution as good as 8 ps rms, improved by a factor of two compared to the raw one.

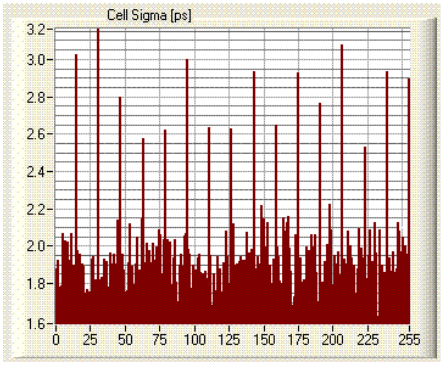

Figure 15: random jitter [ps rms].

Random jitter is a second order element in the raw jitter but as it cannot be corrected, its contribution may become more important after correction of Fixed Pattern jitter. Figure 15 shows the rms of random jitter along the different cells of the sampling matrix. It is higher at the junctions between the columns (every 16 samples), because that is where the jitter of

the clock can be seen. The mean jitter value here is however lower than 2 ps rms.

2) Time measurements with MCPPMTs

A preliminary test of the board on a Micro Channel Plate Photo Multiplier Tube (MCPPMT) characterization bench has been realized.

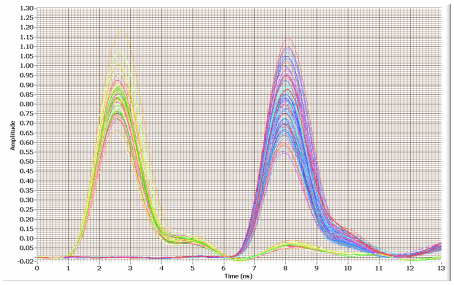

Figure 16: correlated pulses from MCPPMTs.

The bench comprises a laser feeding two quartz bars read by MCPPMTs with light pulses. The Time Transit Spread (TTS) of the MCPPMT had previously been characterized by high-end (CFD + TDC) commercial modules (~ 20 ps rms for 40 photo-electrons).

Figure 16 shows 5000 superimposed events. The FWHM of the signals is of only 1.5 ns but the pulses are cleanly sampled by the board. The high SNR and the quality of the signal stored permits an easy normalization of the pulse heights before applying by software a CFD-equivalent algorithm in order to perform an alignment of their first edge (see Fig. 17) and a measurement of their distance.

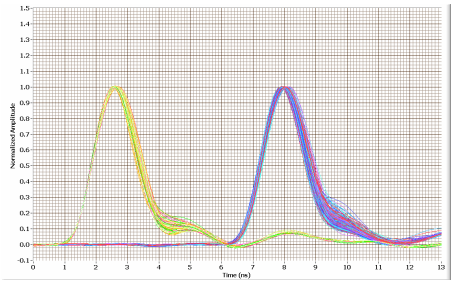

Figure 17: same pulses normalized and realigned.

The distribution of the distances is plotted on Fig. 18 (main horizontal grid step is 10ps).

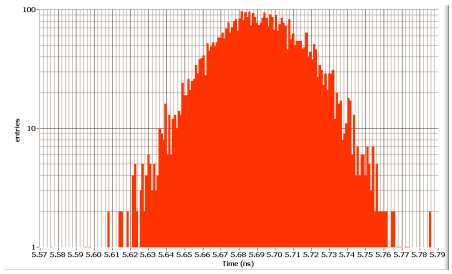

Figure 18: distribution of inter-pulse distance.

The sigma of the distribution of Figure 18 is of 23ps, which is in very good ad-equation with the measurements previously performed. This proves that the board can be used for the characterization of this kind of ultra fast photo-multipliers. Very promising preliminary tests with SiPMs (Silicon Photo Multipliers) have also been performed.

VI. Summary of Board Performances

The main characteristics and performances of the USB-WaveCatcher board are summarized below:

- 2 DC-coupled 256-deep channels with 50-Ohm active input impedance
- ±1.25V dynamic Range, with full range 16-bit individual tunable offsets
- Bandwidth > 500MHz
- Signal/noise ratio: 11.9 bits rms (noise = 650 µV rms)
- Sampling Frequency: 400MS/s to 3.2GS/s
- Max consumption on +5V: 0.5A
- Absolute time precision in a channel (typical)
  - without INL calibration: 20ps rms (400MS/s to 1.6GS/s)
    16ps rms (3.2GS/s)
  - after INL calibration: 12ps rms (400MS/s to 1.6GS/s)
    8ps rms (3.2GS/s)
- Trigger source: software, external, internal, threshold on signals
- 2 individual pulse generators for reflectometry applications
- On-board charge integration calculation
- Acquisition rate (full events): up to ~1.5 kHz over 2 channels
- Acquisition rate (charge mode): up to ~40 kHz over 2 channels

VII. Conclusion

This study proves the ability of fast analog memories to be used for high precision time measurement. Their main advantages are the very low power and cost and the ability to work directly with analog signals. Moreover, the shape of the signal is available if necessary.

Various evolutions of the SAM chip are under study, targeting either higher precision time measurements or longer time window. As a beginning, a R&D version of the chip has been recently submitted in order to study the optimization of the power and of the signal bandwidth in view of these more dedicated versions.

In a general way, the USB-WaveCatcher can replace oscilloscopes for a much lower cost in most high-precision short-window applications. Moreover, it can be used for very high precision time measurements, especially since said measurements can be performed directly on the analog signals.

VIII. References

[1] SAM: a new GHz sampling ASIC for the H.E.S.S.-II Front-End Electronics, E. Delagnes et al, Nuclear Instruments and Methods in Physics Research Section A, Volume 567, Issue 1, p. 21-26

[2] D. Breton, E. Delagnes and M. Houry, "Very High Dynamic Range and High Sampling Rate VME Digitizing Boards for Physics Experiments", IEEE Transactions on Nuclear Science, VOL. 52, No. 6, Dec 2005, pp 2853-2860.