A Novel CMOS Detector Based on a Deep Trapping Gate

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***Abstract*– A novel detecting device compatible with modified CMOS processes was studied using standard simulation codes. The physical principle of the device derives from the properties of a buried gate containing deep trapping centers. This gate, which modulates the drain-source current of the n or p MOS transistor selectively traps carriers generated by an impinging particle. This principle evaluated with realistic simulations parameters shows that a good signal to noise ratio might be obtained for an energy deposition equivalent to a minimum ionizing particle within a limited silicon thickness. Problems related to the physical implementation process for such a device are also discussed.**

I. Introduction

FUTURE high energy experiments at TeV linear colliders will require high precision vertex detectors in order to measure among other physical quantities the Higgs branching ratios [1]. Other physics that necessitate a high precision vertex detector is the exploration of extra dimensions. Up to now CMOS sensors [2] as well as the DEPFET [3] development, were proposed as realistic solutions for the Vertex detector as well as the classic HPD (Hybrid Pixel Detectors). These two former solutions are efficient to obtain a reasonably good spatial resolution with a high enough readout speed. However, DEPFETs require a spatial process with high bias voltages and CMOS sensors are sensitive to bulk damage, which may exclude them from some applications requiring high tolerance to neutron damage. To make further progress a novel device is proposed with the goal of decreasing pixel size, and using a technological process closely derived from a standard CMOS process. An inversion mode MOS transistor is the starting point of this device, contrary to the DEPFET, which require depletion mode FET. The major difference with a CMOS pixel is the absence of a separate collecting diode. The proposed device can be made in a very thin silicon layer.

II. Proposed Sensing Device

Whereas in the DEPFET principle an internal gate is used as a collecting electrode for the charges generated underneath in a thick bulk silicon, (a few hundreds of microns), in this Trapping Mode CMOS Sensor (TRAMOS) the buried gate is localized very close to the channel. It is made of a zone where very high densities of deep centers, which selectively trap holes or electrons, depending on the type of MOS transistor, are introduced. A deep n or p well is added below the deep gate to establish the adequate potential barrier that favors the trapping of holes for an nMOS, or electrons for a pMOS. By doing so, the active thickness of the device can remain small and therefore this avoids the need of a high voltage bias. Compared with a CMOS cell the collection diode and the biasing transistor are no more needed. Fig. 1 shows a band diagram summarizing the physical principle of the device.

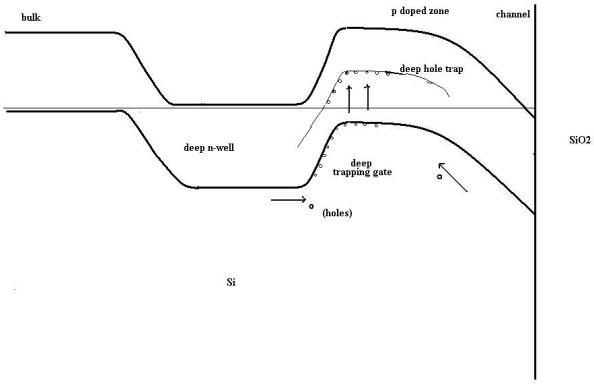

Fig. 1. Band diagram of the MOS structure at mid point between the source and drain. This diagram corresponds to an n-channel transistor. An n-well is introduced at the left side, corresponding to the backside or the bulk of the device. The active trapping gate is in the transition zone. Holes generated in the bulk or near the channel by ionizing particles should migrate towards this gate due to band bending, whereas electrons migrate towards the bulk or the channel.

The device is designed in such a way that holes in the case of an n-MOS induce a positive charge at the trapping gate while the generated electrons have a more limited influence. An ionizing particle incident to the device should then induce a charge on the deep trapping gate. This charge should modulate the channel and lead to an increased source to drain current. The absence of collecting diode pn diode and the use of inversion mode MOS transistors should enable dimension scaling and high tolerance to bulk damage. Fig. 2 introduces a schematic view of the proposed device with realistic dimensions.

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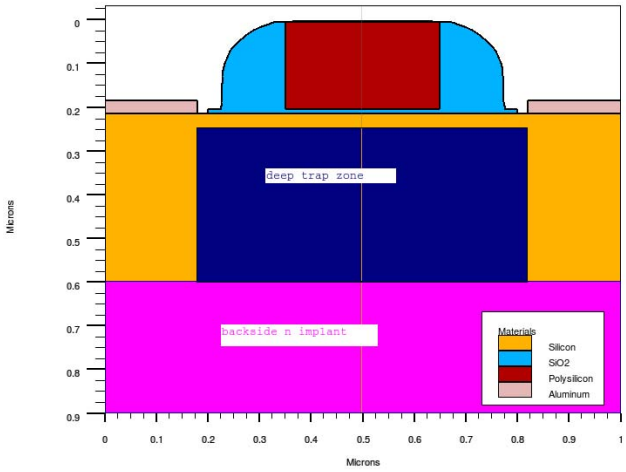

Fig. 2. Simplified schematic view of the MOS structure introduced here for particle detection. The deep trapping gate is shown together with the deep n-well. A TCAD software was used for generation of the view.

A. Processing Aspects of the Device

Starting from a simple silicon nMOS transistor, a process procedure can be introduced here. One possibility discussed here as an alternative to many epitaxial steps is the use of deep implants to create the n-well out of a p-substrate and to obtain a deep trapping gate by transition metal implantation. Reduction of the diffusion temperature is required in order to maintain a sharp enough impurity profile, within the deep trapping gate. Process simulations using a standard TCAD tool show, that the static electrical characteristics of the device satisfy MOS device functional requirements. A technological difficulty, which does not appear straightforwardly, is related to the use of a metal implant, which may act as a contaminant in the overall process. More work is required to circumvent the possible problems due to transition metal impurities. However early studies [4] and more recent ones [5] indicates, for instance that Zn induces two deep levels in the bandgap of silicon , one at E_v+0.6 eV , the other at E_v+0.27 eV. These two levels act as hole traps. Subsequently they can be used as a deep acceptor within the trapping gate. Implantation energies after oxidization in the 200-300 keV range is required to obtain the desired impurity profile. This is true for the n-well as well for the deep trapping gate. The implantation profile of the doping and trapping impurities is represented in Fig. 3. Note that high post-anneal deep impurity concentrations are required for the deep trapping gate. The backside n-well may be obtained by a phosphorous front implant at high energies. If the substrate is not thinned the n-well is then connected to an upper contact by an appropriate via. A bulk p contact is also needed near the source contact for appropriate biasing.

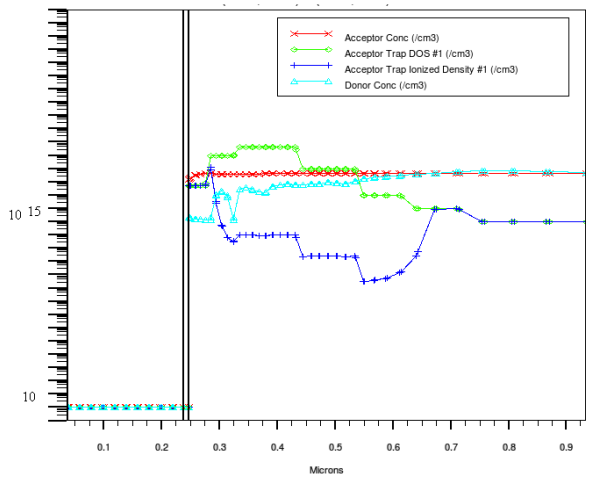

Fig. 3. Simulated impurity profile of the .MOS structure below the channel at mid-point between source and drain. The doping profile (donor and acceptor) is shown for comparison with the deep impurity profile.

The electron and hole profile below the SiO_2/Si interface is plotted in Fig. 4. This plot is a result of a TCAD simulation.

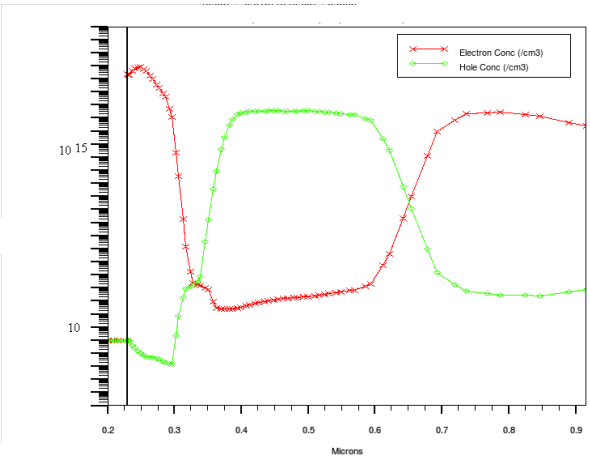

Fig. 4. Simulated carrier concentration of the .MOS structure below the channel at mid-point between source and drain. With a positive bias applied on the gate of the structure, the n-channel below the oxide is clearly present. The n-well is grounded. .

The electron concentration drops sharply below the channel to nil in the deep trapping gate and rises again to the net doping value in the n-well.

B. Static Simulation of the Device

Good electrical characteristics of the device can be obtained with the device described in the previous paragraph. Fig. 5 displays the output characteristics of the device.

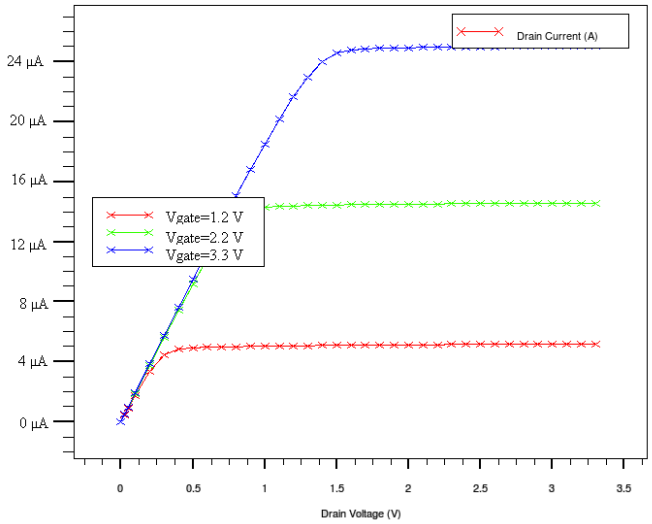

Fig. 5. Source-drain current versus drain-source voltage of the n-MOS structure for increasing gate voltages.

The device behaves like a normal n-MOS transistor in the static mode. The threshold voltage in the ohmic mode is approximately 0.5 V.

III. Operation of the Device

The device can be used in a single pixel, which in turn can be used in arrays. A simple biasing scheme is then needed. The gate is biased constantly at a positive voltage, together with the drain. A current mode biasing of the source is then needed, the bulk contact being grounded. The deep n-well can be biased either at a small negative voltages for reset or grounded for charged particle detection operation. Fig. 6 describes a proposed pixel configuration.

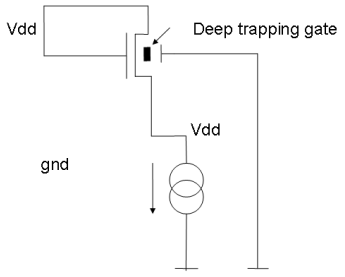

Fig. 6. Pixel schematic using the n-MOS device described above. The current biasing is set here to a few µA, for simulation purposes. The bulk contact is grounded and the Trapping gate contact can be negatively biased for adequate reset.

A. Simulated Effect of a single incident Minimum Ionizing Particle

As well as process and static device Simulation Technological Computer Aided Design, software can be used for time dependent simulation. The presence of deep levels can be modeled in the simulation scheme by introducing the appropriate deep impurity profile, energy levels and carrier capture cross sections. In the simulation studies the parameters were taken from [5] using the acceptor trap profile simulated in Fig. 3.

A minimum ionizing particle can be here modeled by a vertical incident track along the device. An electron-hole pair generation rate is set to 80e-h/µm. The simulation tool assumes a device depth of 1µm. This leads to a low charge value for the device used (Fig. 2). For a current bias of a few µA, using a high value resistor (50000 ohms), the response of the device to an e-h generation pulse along a vertical track midway between source and drain is represented in Fig. 7. The source voltage rise time is very short and the pulse follows a long decay time. The duration of the generation pulse is set to a value well below 100 ns.

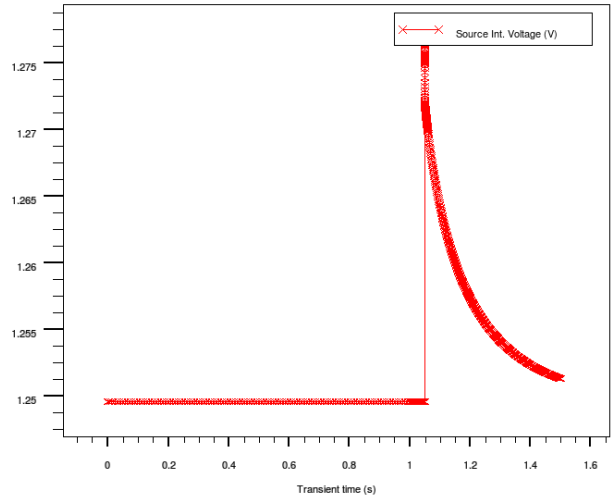

Fig. 7. Response of the pixel at the source contact of the n-MOS device to a generation pulse along the track. A voltage step of 25 mV is observed for a generation rate equivalent to a MIP. The temperature is 300 K and the deep level is E_v+0.6 eV.

The output noise related to the pixel is estimated to be approximately 0.5 mV rms in a 100 MHz bandwidth, which leads to a Signal to Noise ratio of 50. This value is very good compared with what was obtained for currently tested CMOS sensors.

The decay time is governed by the characteristics of the deepest trap, in this case the E_v+0.6 eV.The presence of the E_v+0.27 eV level does not change significantly the response shape. The rise is due to the trapping of generated holes within the deep trapping gate. An excess positive charge induces a change in the potential, which in turn increases the electron density in the channel. The source to drain current is then increased. The decay is due to the emission of the holes in the valence band and is therefore thermally activated. Fig. 8 shows the decay time of the signal when the temperature is increased to 350 K.

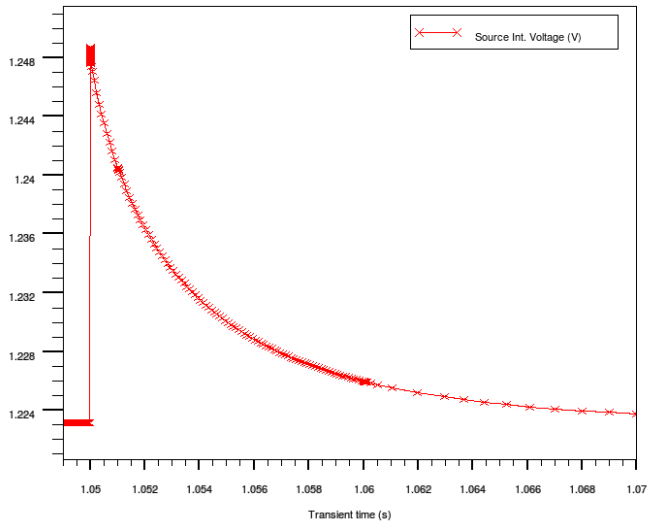

Fig. 8. Response of the pixel at the source contact of the n-MOS device to a generation pulse along the track. The temperature is 350 K for a single deep level and E_v+0.6 eV.

The decay time is then shortened to a few tens of ms. The simulations also indicate that for a E_v+0.27 eV level the decay time constant at 300 K is much lower (Fig. 9).

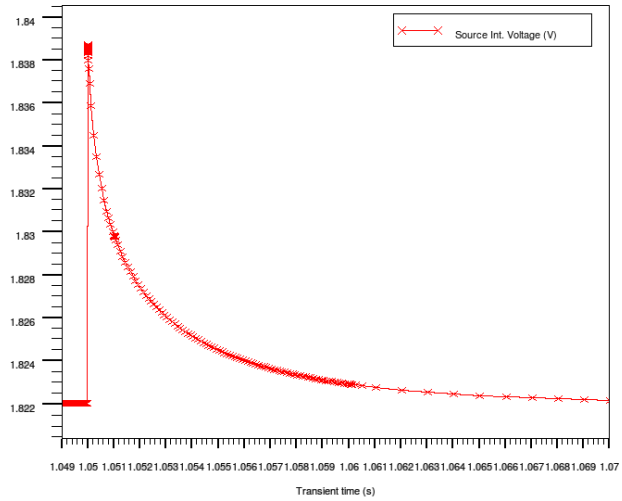

Fig. 9. Response of the pixel at the source contact of the n-MOS device to a generation pulse along the track. The temperature is 300 K for a single deep level at E_v+0.27 eV

Further simulations show that the response is not significantly altered by a concentration of deep traps corresponding to a 10^{16} $n_{eq}.cm^{-2}$ neutron irradiation.fluence.

IV. Proposed Reset Mode

In order to shorten the time between successive readouts a reset is necessary, the natural reset being to long for the deep levels introduced in the device simulated here. A way to obtain a reset is to bias the n-well to a negative potential. This induces a weak bulk/n-well current through the structure Electrons are injected from the n-well towards the deep trapping gate. Moreover, they may recombine with the trapped holes in the deep trap dense zone. With realistic capture cross sections for holes and electrons for the deep traps, one obtains a behavior of the signal represented in Fig. 10.

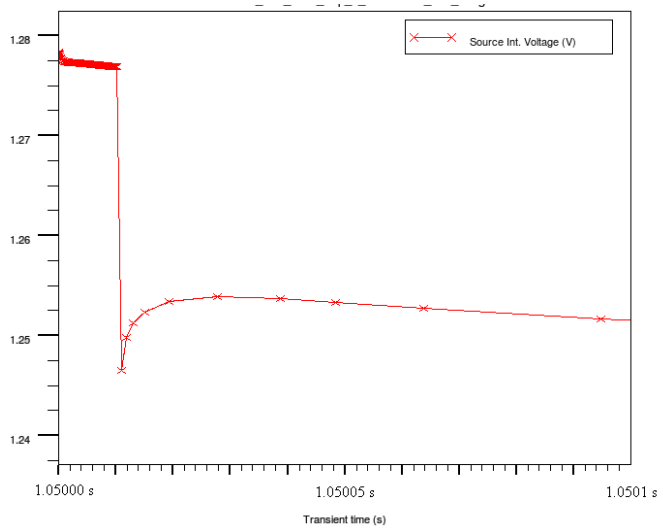

Fig. 10. Response of the pixel at the source contact of the n-MOS device to a generation pulse along the track. The temperature is 300 K. A reset signal is applied at the n-well, with a bias of - 0.275 V after 10 µs.

How fast and effective the reset can be depends on the values of the capture cross sections for minority carriers (electrons) that are not very accurately known. The trapping properties determine the recombination current within the trapping gate and therefore they should be fully understood. Further DLTS measurements under minority carrier injection [6] would be welcome for the Zn levels in silicon.

V. Conclusions and Further Developments

Simulations presented here show that an n-MOS device designed with a deep trapping gate would be functional as a detector for Minimum Ionizing Particles. The technological feasibility of the device was studied through process simulation. Further developments will involve better physical understanding of the implanted deep trapping gate and the elaboration of a test vehicle.

Acknowledgement

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