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Etude et développement d'ASIC de lecture de détecteurs matriciels en CdTe pour application spatiale en technologie sub-micrométrique

Studies and development of a readout ASIC for pixelated CdTe detectors for space applications

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« Experimental physics cannot be
properly done without instruments. »
Jean-Antoine NOLLET

Studies and development of a readout ASIC for pixelated CdTe detectors for space-applications

« Je n'ai fait celle-ci plus longue que parce que
je n'ai pas eu le loisir de la faire plus courte. »
Blaise PASCAL

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ABSTRACT

The work presented in this thesis is part of a project where a new instrument is developed: a camera for hard X-rays imaging spectroscopy. It is dedicated to fundamental research for observations in astrophysics, at wavelengths which can only be observed using space-borne instruments. In this domain the spectroscopic accuracy as well as the imaging details are of high importance. This work has been realized at CEA/IRFU (Institut de Recherche sur les lois Fondamentales de l'Univers), which has a long-standing and successful experience in instruments for high energy physics and space physics instrumentation.

The objective of this thesis is the design of the readout electronics for a pixelated CdTe detector, suitable for a stacked assembly. The principal parameters of this integrated circuit are a very low noise for reaching a good accuracy in X-ray energy measurement, very low power consumption, a critical parameter in space-borne applications, and a small dead area for the full system combining the detector and the readout electronics. In this work I have studied the limits of these three parameters in order to optimize the circuit.

In terms of the spectral resolution, two categories of noise had to be distinguished to determine the final performance. The first is the Fano noise limit. It is the one related to detector interaction statistics and it cannot be reduced or eliminated. The second is the electronic noise, also unavoidable; however it can be minimized through optimization of the detection chain. I focused on this aspect. Within the detector, establishing a small pixel pitch of $300\ \mu m$ reduces the input capacitance and the dark current. This limits the effects of the electronic noise. Also in order to limit the input capacitance the future camera is designed as a stacked assembly of the detector with the readout ASIC. This allows to reach extremely good input parameters seen by the readout electronics, namely and input capacitance in range of $0.3\ pF$ - $1\ pF$ and a dark current below $5\ pA$.

In the frame of this thesis I have designed two ASICs. The first one, Caterpylar, is a testchip, which enables the characterization of differently dimensioned CSA circuits to choose the most suitable one for the final application. It is optimized for readout of the target CdTe detector with $300\ \mu m$ pixel pitch and the corresponding input parameters. With this circuit I have also analyzed possible filtering methods, in particular the semi-Gaussian shaping and the Multi-Correlated Double Sampling (MCDS). Their comparison is preceded by the theoretical analysis of these shapers. The second ASIC D^2R_1 is a complete readout circuit, containing 256 channels to readout CdTe detector with the same number of pixels, arranged in 16×16 array. Each channel fits into a layout area of $300\ \mu m\ \times\ 300\ \mu m$. It is based on the MCDS processing with self-triggering capabilities. The mean electronic noise measured over all channels is $29\ electrons\ rms$ when characterized without the detector. The corresponding power consumption is $315\ \mu W/channel$. With these results the future measurements with the detector give prospects for reaching an FWHM spectral resolution in the order of $600\ eV$ at $60\ keV$.

CHAPTER I

New Instrument for Hard X-ray Imaging Spectroscopy

The observations in the hard X-ray domain are essential in modern astrophysics. One example is their relation to the physics of the black holes and their role in the Universe. Despite the highly penetrating properties of these high-energy photons, the thick atmosphere around the Earth absorbs the celestial flux and prevents its observation from the ground. The experiments must be carried out with instruments on satellites, in the space environment free from the atmospheric absorption. This explains why this branch of astrophysics is very young.

Another difficulty lies in the collection of the high-energy photons in hard X-ray telescopes. Because of the penetrating properties of this radiation and the very small number of photons arriving from the sources at the telescope level, this is a double challenge: for the telescope's optical system and for the detector. The optical system must provide an image of incoming photons that is then exploited further to localize the hard X-ray sources in the sky. At these wavelengths the image acquisition is realized with coded mask or focusing optics, with an image quality far from what is easily reached in the optical wavelengths detection. The detector system has to efficiently convert each of these photons, one by one, into a digital signal giving accurate position localization, the time of arrival and the energy of the incident photon. It must be realized with an extremely low intrinsic background because of the low source fluxes.

There is a list of parameters to be considered to ensure a good image quality, resolved in energy. Among them there are the position accuracy and the resolution in the energy measurement itself. To achieve good photon collection efficiency up to the hard X-ray band, an adequate detector material must be chosen. This chapter discusses why one of the most attractive materials for hard X-Ray imaging spectrometers is certainly the Cadmium Telluride (CdTe). It is a high Z and high-density semiconductor with potentially high spectroscopic performances at near room temperature. Therefore this is one of the best-suited materials for hard X-Ray space-borne applications. Once the detection material and sensor geometry are optimized, the signal from the sensor must be read out with a dedicated low noise compact electronics. Because of the number of pixels to be read out and their small size, the use of low power Application Specific Integrated Circuit (ASIC) is nowadays mandatory. In the last part of this chapter, I describe the main challenges for the readout electronics including: geometry, noise, power consumption and radiation hardness.

1.1. X-ray imaging telescope for astrophysics

The electromagnetic spectrum emitted in the universe is a wide continuum ranging from radio and microwaves through infrared, visible and UV light up to the high energy X and gamma rays. The wavelengths that can be detected by astronomers range from several meters in radio band to sub-femto meters corresponding to gamma rays energy of tens of TeV (Figure 1.1). Each wavelength band carries information about astronomical objects, related to their physical characteristics or to the processes developing in these objects. For example, all the recent knowledge on the origins, contents and the age of the Universe has been obtained by observations in the microwave domain, particularly by the Planck ESA mission. On the high energy side, this is in X-rays that the hot gas filling the intergalactic space in cluster of galaxies has been revealed. Through its thermal emission at temperatures of several millions of degrees one can measure the amount of dark matter in the Universe. Also this is in hard X-rays and gamma rays that the densest objects in the Universe are unveiled: neutron stars and black holes. They are both at the origin of very energetic non-thermal emission due to particles accelerated in their environment. The supermassive black holes at the center of all galaxies are now known to play a key role in the evolution, and maybe the formation, of the galaxies throughout the history of the Universe. A complete view of the Universe can be obtained only by observations in all wavelengths. Moreover in several cases this is the only way to disentangle the different theories that are competing to explain what we are observing.

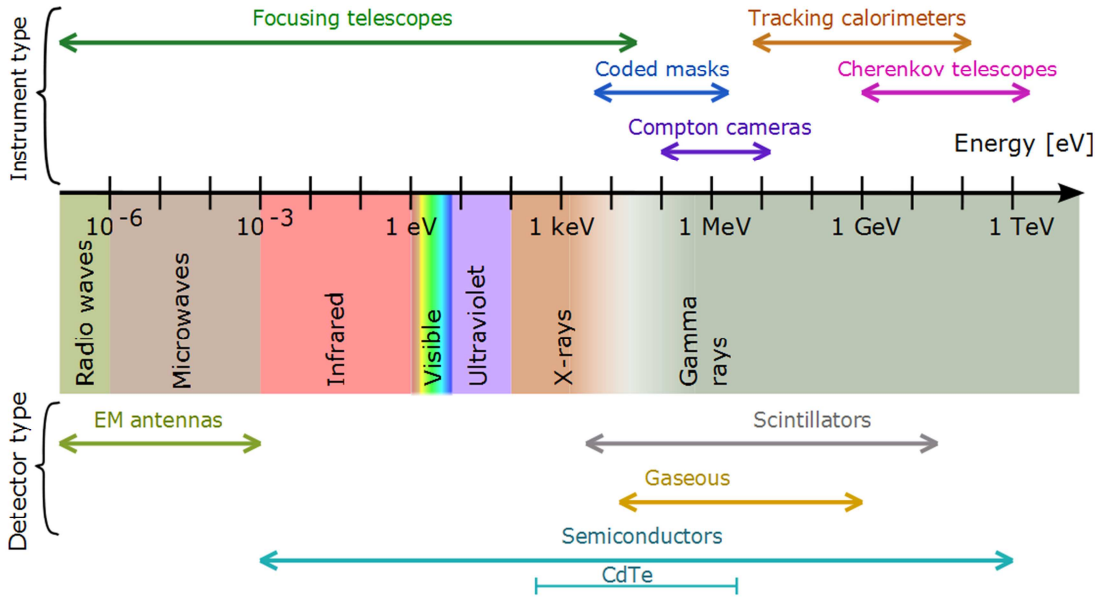


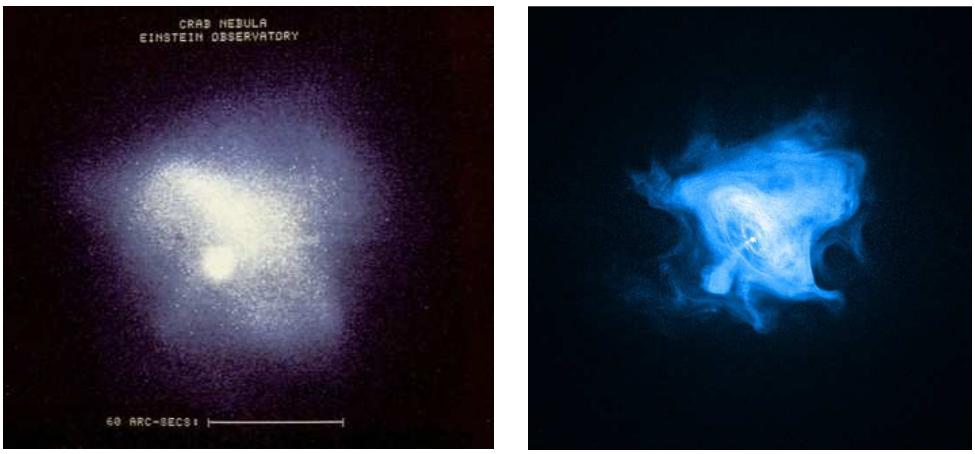
Figure 1.1 The electromagnetic spectrum with indicated characteristic bands. Instrument types used in detection for each band as well as corresponding detector types are indicated.

Investigation of each band requires a different detection method, since depending on the wavelength – the photon-matter interaction properties change. The radio and microwaves are received with antennas; light, even beyond visible, can be captured by a semiconductor-based camera. A similar principle is used for X-rays although the detector material and geometry varies with the energy range. In case of the gamma ray region – typical telescopes are based on tracking-calorimeters, Compton cameras or recently successful Cherenkov telescopes for the highest energy

range. Technological developments in the past few decades have contributed to new astronomical observations in all of these spectral domains. It is however worth noting that the Universe in far infrared as well as in X-rays has not been extensively explored, because of the limitation of the observation environment. Photons emitted within these wavelengths are completely blocked by the Earth's atmosphere. For a long time it was unknown that outside of the solar system there were astronomical sources emitting power in certain energy ranges. In the second half of the twenty-century the space environment, free from atmospheric absorption, became reachable for astrophysics experiments. The studies were then carried out with balloon-borne experiments in the upper atmosphere, rocket flights that were the initiators for X-ray sky surveys and eventually with space-borne telescopes. The latter provides the best observation conditions since in the absence of the atmosphere the detection efficiency is not restricted. Furthermore satellites can be equipped with fine pointing apparatus that prevent blurred image over long observation times. Finally duration of the mission can last up to 10 years typically, enabling an extended time for the experiment, in contrast to balloon and rocket flights – for which the observations last from few minutes up to few days at maximum.

1.1.1. High energy astrophysics in space, X and gamma rays

The history of X-ray astronomy starts a few decades back – in the sixties with the first discovery onboard the Aerobee rocket mission of X-rays originating from outside the solar system [1]. That event initiated this new branch in astronomy. Among the most remarkable discovery missions there were: the Einstein Observatory – the first fully imaging X-ray telescope, Chandra – with its exceptional angular resolution, XMM Newton – the largest area focusing telescope launched so far, and INTEGRAL and Fermi – covering with unprecedented performances the highest part of the spectrum, hard X-rays and MeV to tens of GeV gamma-rays. Numerous more examples could be listed all of which have contributed to the state of knowledge where we are now, in terms of astrophysics as well as detection instruments. The story continues with today's NuSTAR launched in 2012, the upcoming Astro-H, very likely SVOM, as well as well the international large projects as for example LOFT or ATHENA+ on the ESA side.



A) B)

Figure 1.2 X-ray image of the Crab nebula A) taken by the Einstein X-ray Observatory in 1979 [9], B) taken by the Chandra X-ray Observatory in 2001/2004 [8].

For the last few decades the imaging devices onboard these telescopes have demonstrated a successive improvement in sensitivity and angular resolution. Fainter sources can be detected while improved spatial resolution leads to finer separation of point sources. The achievements are on one side related to better optics, and on the other side to progress in detectors development. The comparison of two X-ray images of the Crab nebula in Figure 1.2 shows an example of the impressive progress in the imaging instruments' performance over a period of 20 years.

1.1.1.1. Optics – Imaging techniques

In terms of optics there are two principal imaging techniques that improve the sensitivity in a given energy bandwidth, and the angular resolution, when compared to a bare detector eye: direct imaging with focusing mirror and indirect imaging with coded aperture.

Grazing incidence mirror

In contrast to lower wavelengths, X-rays are not reflected at all angles, but only at shallow ones. If the incidence angle is too high then the X-ray photons penetrate the matter and pass through it or get absorbed. Therefore the spherical or parabolic mirrors used for example in telescopes for visible light are not suitable for these wavelengths. The optical X-rays focus is achieved with the grazing incidence technique instead, where a beam is reflected at low grazing angles. Such a mirror can be realized using cone-like shells with multiple layers to increase the effective collecting area (Figure 1.3). Its incident curvature (combination of paraboloid and hyperboloid shells) ensures concentration of the image onto a detector area, much smaller than the telescope opening. Limitation of this method lies in the dependency between absorption incidence angle and the X-ray energy, as well as necessity to have an almost perfect mirror shape at both macroscopic and X-ray wavelength scales. This involves an excellent surface quality in order to keep the angular resolution to the requirements of modern telescopes.

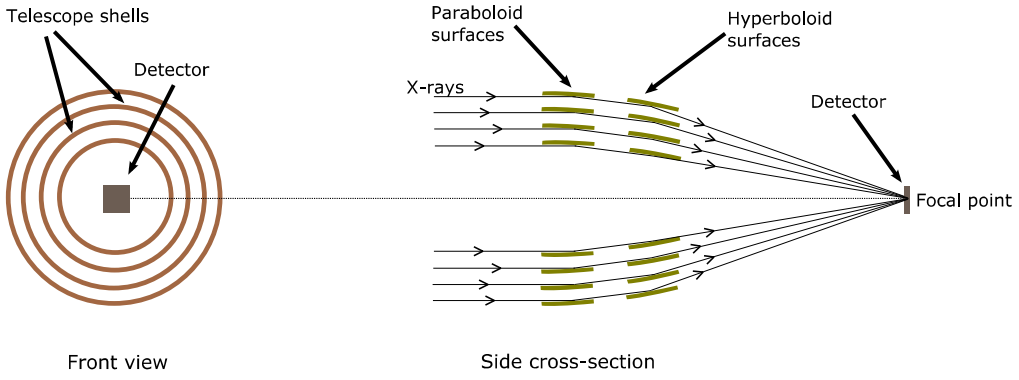


Figure 1.3 Grazing incidence mirror used for X-ray focusing telescopes. The illustration includes the front view of circular shells and X-rays reflection profile in the side cross-section. A construction with multiple shells increases the effective collecting area, e.g. in the NuSTAR telescope there are 133 shells [5] and 235 shells in the future Astro-H HXT telescope [11] .

In practice the spectral window is restricted to range between a few hundreds of eV and about 100 keV. XMM Newton [6], Chandra [8] and NuSTAR [5] missions use the X-ray focusing telescope technique. The NuSTAR example demonstrates performance near the achievable upper limits of the spectral window, with energy range up to 79 keV. Figure 1.4 shows the XMM Newton satellite, with openings for the three grazing incidence mirrors. In addition the photon path through the optics to the focal surface, 7.5 meters away, is illustrated.

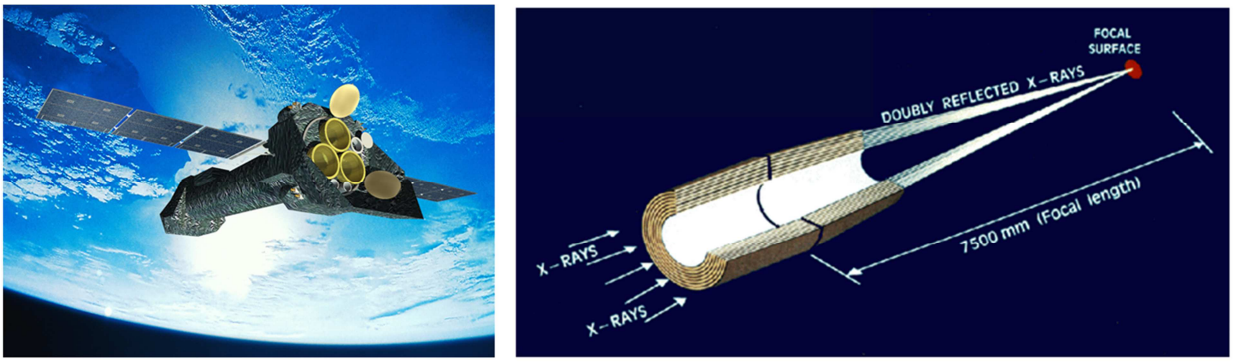


Figure 1.4 Image of the XMM Newton satellite [6] and illustration of its grazing incidence mirror. The energy range is from 0.1 to 10 keV and the angular resolution is 15 arcsec. This system characterizes a very good signal to noise ratio.

Coded mask

Coded mask is a different imaging technique that requires post processing to build the image. The mask is realized as a flat surface with a pseudo-random mosaic of elements that are either transparent or opaque to the photons. Typically the coded mask is larger than the detection area and placed some distance in front. Some rays pass through the mask, while others are blocked by the opaque elements casting a shadow onto the detection surface, as illustrated in Figure 1.5. The final image is obtained by unfolding the registered image from the known coded pattern of the mask. This technique is not competitive with focusing mirrors in terms of sensitivity and angular resolution. But the coded mask technique allows construction of instruments with a very large field of view, of several tens of degrees, whereas focusing telescopes are limited to a fraction of degree. This is a true advantage for all sky surveys and for the study of transient events, very important in neutron stars and black holes astrophysics. This is also the only method to cover a wide dynamic range up to the MeV region. The Integral and Swift are examples of missions using coded masks. Swift offers a very large field of view of 1.4 sr (or 4600 $square\ degrees$) [10] and can cover nearly one sixth of the sky at a time. Meanwhile the Integral IBIS instrument profits from the coded aperture technique with a very high dynamic range, which permits to observe gamma rays up to 10 MeV [2]. The Integral is shown in Figure 1.6 together with illustration of one of its coded masks used for the SPI instrument.

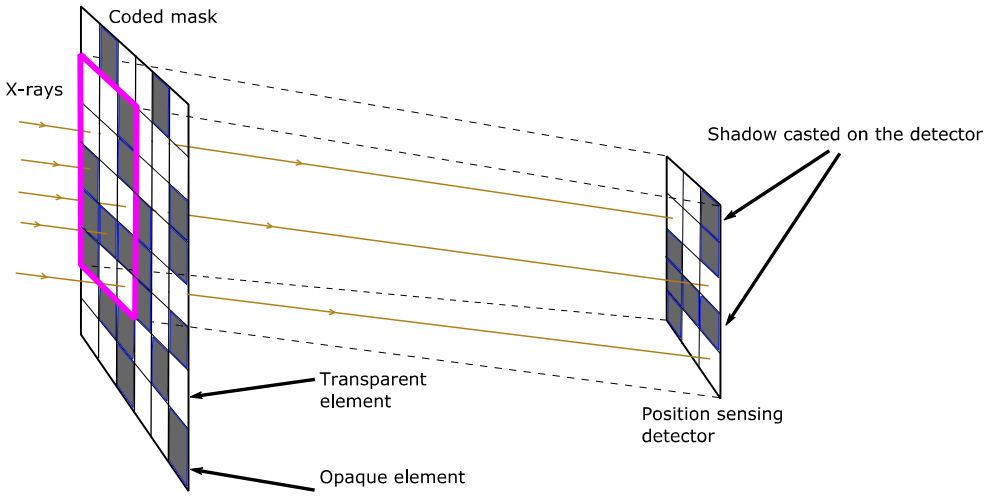


Figure 1.5 Illustration of the coded mask aperture imaging principle. The X-rays can pass through the transparent mask elements while they are stopped by opaque ones. In consequence a shadow is casted onto the position sensing detector. X-rays arriving from different directions result in different shadows, each of them unique. The final image is reconstructed by deconvolution of the actual detector image with the known mask pattern.

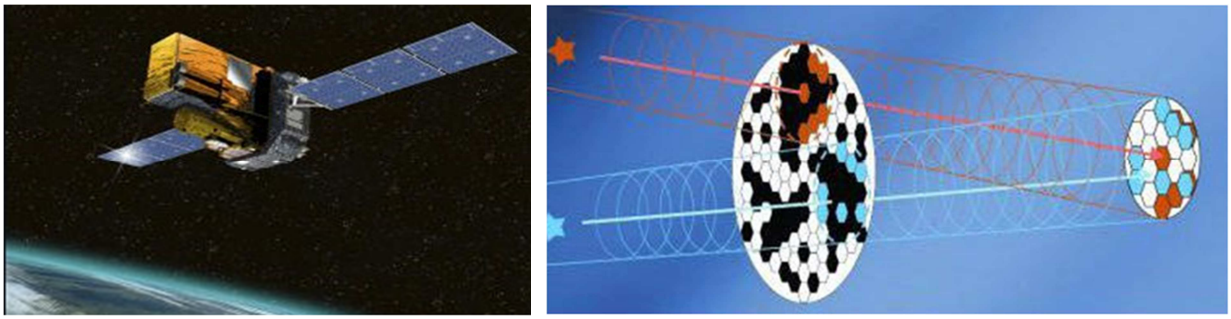


Figure 1.6 Image of the Integral satellite [3] and illustration of one of its coded masks (for the SPI instrument). The energy range is very large: from 15 keV to 10 MeV and the angular resolution is 12 arcmin. With coded mask it is difficult to achieve a signal to noise ratio as good as in the case of telescopes with focusing optics.

1.1.2. How the detector parameters contribute to telescope quality

The improvement in the fabrication process of grazing incidence mirrors allows their use for wider energy range and permits the construction of telescopes with extraordinarily large effective detection areas. Contemporary missions propose focusing mirrors of fine sensitivity up to energies of ~ 80 keV. Also coded masks can still be improved by geometry and image processing optimization. With both imaging techniques – scientific developments have led to an increase in sensitivity and angular resolution. However in addition to the optics – the observation capabilities are also associated with detector parameters. Those parameters that translate directly to sensitivity and angular resolution are the detector area, the detection efficiency, the spatial resolution in position sensing and the energy resolution as the imagers are actually spectrometers[1].

	Integral/IBIS [2][3]	SIMBOL-X [4]	NuSTAR [5]	Astro-H/HXI [11][12]
Optical system	Coded mask	Grazing incidence	Grazing incidence	Grazing incidence
Energy range	15 keV - 10 MeV	0.5 keV – 80 keV	3 - 79 keV	5 - 80 keV
Collecting area	2600 cm^2	100 cm^2 at 70 keV	60 cm^2 at 60 keV	300cm^2 at 30 keV
Spectral resolution	9 % at 100 keV	< 1.3 keV at 68 keV < 150 eV at 6 keV	0.9 keV at 60 keV	< 1 keV FWHM
Field of View at 30 keV	8.3˚ × 8˚ fully coded 29.1 × 29.4° total	12’	10’	9’
Angular resolution	12’ FWHM	20” HEW	18” FWHM 58’’ HEW	1.7’ HEW
Focal length	3.2 m	20 m	10 m	12 m

Table 1.1 Principal parameters of hard X-ray instruments onboard: the contemporary space missions – Integral (launched in 2002) and NuSTAR (launched in 2012), the future ASTRO-H (expected launch in mid-2015) as well as the SIMBOL-X (project). For IBIS, which is not a focusing instrument, the focal length is the distance from the mask to the detector. For focusing instruments, the value quoted for the Field of View is the diameter of the image at 50 % vignetting (i.e. the location off axis for which the effective area is half of the on axis effective area). For Integral IBIS, the fully coded Field of View is the one for which the collecting area (quasi-constant) is at its maximum value, the total corresponds to the angle at which the collecting area falls down to zero.

[1] I will call this type of detectors – imaging spectrometers in the rest of the text.

1.1.2.1. Sensitivity

One of the most important parameter of a telescope is its capacity to detect sources and to localize them over the background noise. The sensitivity of a telescope is measured in terms of a minimal flux that a source must have to be detected in a given observation time. The flux is measured in photons per unit area per second, in a given energy range. This "minimal" flux can be quantified through ratio of source signal to background noise. This Signal to Noise Ratio (SNR) is defined as:

$$SNR = S/\sqrt{S+N} \qquad 1\text{-}1$$

S being the number of counts from the source detected during the observation time, N the number of noise counts for the same observation conditions (duration, sky area, energy range). The noise considered here can have the following origins: either detection of photons and particles that are not originating from the source of interest, or detector intrinsic noise[2].

Collecting area

Clearly, the signal to noise ratio always increases when the collecting area increases, whatever imaging system is considered. The larger the collecting area, the more sensitive is the telescope. Consequently the collecting surface of the telescope must be as large as possible.

In a coded mask system, the detector area is strictly proportional to the collecting area, and thus the noise is also proportional to the collecting area. A two fold increase in sensitivity can be obtained only through an increase by a factor of four of the detector area. When the coded mask aperture imaging technique is applicable (mainly in the hard X-rays and gamma rays, or in compact missions requiring a large field of view), this translates directly to large detector surfaces, typically several thousands of square centimeters. Detectors using this imaging technique, flying on INTEGRAL or SWIFT, are now at the development limit for a space borne instrument (using coded mask aperture) in terms of mass, collecting power and SNR.

In a focusing X-ray instrument, similar from the sensitivity point of view to optical telescopes, the collecting area is decoupled from the detector area. The collecting power, that is number of source counts, can be assumed to be independent from the noise counts (apart from the astrophysical noise originating from the sky itself, as e.g. the X-ray emission, at low energies, of the local bubble in which is located the solar system). The size of the mirror can be as large as feasible without increasing noise, as the photons from a point source are concentrated in a small fraction of the sensor surface (few square millimeters). For given instrument parameters (focal length and angular resolution) – the noise is constant, independently of the size of the collecting area. In consequence the background generated in the small region of the sensor where the photons are projected, is very low. Therefore the focusing X-ray telescopes provide much better sensitivity, than instruments with coded mask aperture.

Detection efficiency

In parallel to maximization of the detection area the detection efficiency also has to be maximized to improve the sensitivity of a telescope. It is described by the probability that an arriving photon interacts with the detector. As far as the hard X-rays are concerned, at energies below the pair-

[2] In the following chapters the term "noise" will be reserved to the electronic noise.

creation threshold, there are two possible mechanisms of interaction: the photoelectric effect and the Compton Effect. The interaction probability of each process depends on the X-ray energy, detector material type and its thickness (for more details please refer to the paragraph 1.2.1). Material appropriate for detection of $6\ keV$ X-rays may not give the same efficiency at $60\ keV$. In many applications not only the interaction itself is important but also it is required that the photon's entire energy is deposited within the detector. This is relevant to detectors with spectral resolution capability.

Observation time

On the top of the detection area, intrinsic noise and efficiency, there is also the observation time that influences the telescope's sensitivity. With a longer exposure time a higher number of photons may be accumulated and separated from the background. For an effective observation the count rate of the instrument should match the expected luminosity of the celestial sources, typically described in number of photons per second per square centimeter. For many reasons there is only a limited exposure time given for a single observation and this is not only for the efficient use of a telescope. An object in the target image might have a transient property like gamma ray bursts or emissions from binary stars or pulsars. The observable change in these phenomena is slow enough that observation with milliseconds rate capabilities should be amply sufficient. However, a typical microsecond timing accuracy for each photon is desirable: for timing analysis of bright sources and to enable the synchronization of multiple detectors aboard.

Finally there is one more effect that may indirectly become critical for the time exposure – the emissions from beyond the desired energy band: cosmic background of high energy gamma rays or charged particles. These events also interact with the detector. The instrument responds to the resulting signal just as to any of the X-rays from the desired energy band. Such events can be rejected afterwards, however the instrument may need some time to recover until it is ready for reception of any new arriving X-rays. This dead time should be considered in the detector design, thus minimizing probability of losing any desired photon during the image acquisition time.

1.1.2.2. Spatial resolution

Resolving power of two celestial sources, that appear very close, depends on the spatial (angular) resolution. Having a good angular resolution is obviously also important for mapping in details extended sources, as e.g. supernova remnants which can have very thin structures. The use of imaging detectors is also needed for measuring the polarization of the radiation in hard X-rays (through the properties of the Compton interaction), a recent field under development because of the importance of this additional diagnostic for understanding the processes in the sources.

The ability to localize events is the most obvious property of imaging instruments. This can be achieved on the detector level in two ways. One possibility is a composition of multiple discrete detectors on a common detection surface. Alternatively a monolithic detector can be equipped with multiple electrodes: with one-sided pixelated or double-sided strip arrangement (for more details please refer to the paragraph 1.2.3). The total number of these segments gives the number of channels. In all cases the element in which the interaction occurs can be determined, thus providing position sensitivity with accuracy equal to separation between the elements. The parameter quality

is described by spatial $[\mu m]$ or angular resolution $[arcseconds]$. For a telescope with an ideal detector the angular resolution is the minimum angle that allows distinguishing two point sources.

In the X-ray imaging spectroscopy the spatial resolution is given in terms of the Point Spread Function (PSF). As illustrated in Figure 1.7 – PSF is the image of a point source object projected on the focal plane.

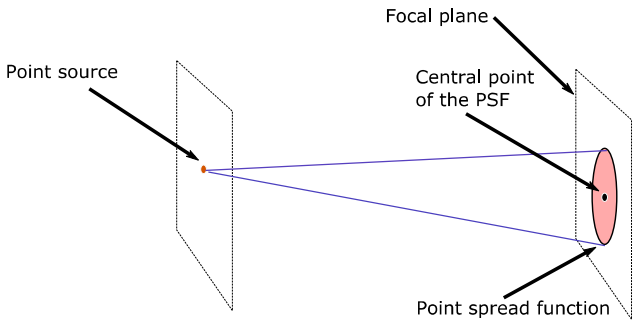


Figure 1.7 Illustration of the Point Spread Function – describing response of an optical system to a point source object. For simplicity no focusing optics was included on the photons path.

Because of the scattering effect the X-ray PSF has a particular distribution profile: narrow at the top and widened at the bottom [13]. For a first order evaluation of the angular performance of such a profile, the PSF shape is characterized either as FWHM (Full Width at Half Maximum) or as HEW (Half Energy Width):

- **FWHM**. If the maximum of the PSF corresponds to N counts, FWHM is found as the PSF width at $N/2$.
- **HEW** defines the PSF width where 50 % of the flux is included [14].

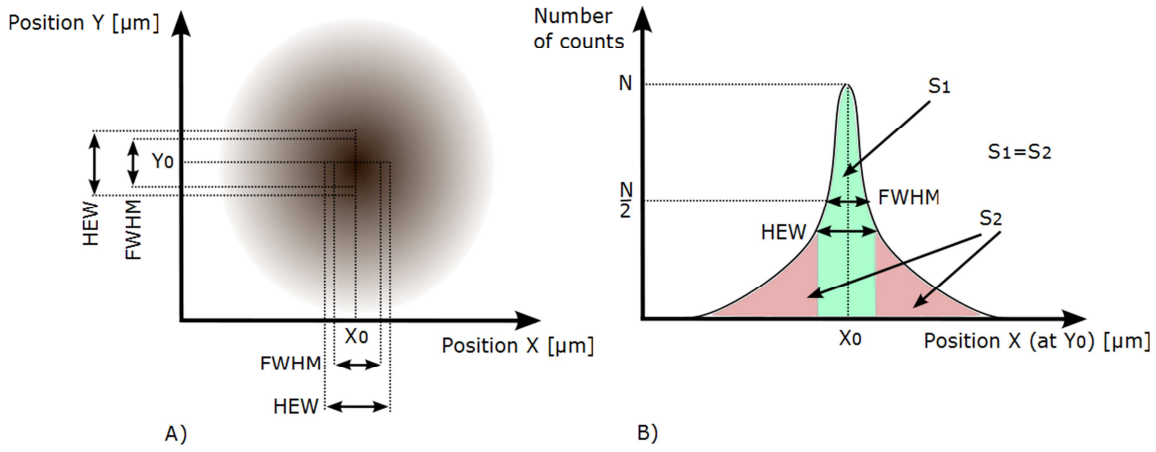


Figure 1.8 Illustration of the Point Spread Function parameters. A) The PSF is shown as a function of the X and Y position. The center of the PSF corresponds to coordinates [X_0,Y_0]. B) The number of counts in the PSF distribution is shown as a function of the X position at the central point Y_0, with the peak of N counts. The Full Width at Half Maximum is the PSF profile width that corresponds to $N/2$, whereas HEW indicates width where 50% of the total flux is included (indicated with the shaded area S_1 and S_2).

Both definitions are illustrated in Figure 1.8. In X-rays imaging the FWHM term is used to describe the minimum separation of two point sources that are possible to detect, whereas HEW informs about the capability to detect faint sources [7]. FWHM and HEW, defined in Figure 1.8, are given in the unit

of micrometers and they describe the spatial resolutions. In order to describe the PSF angular resolution in arcseconds a conversion has to be considered:

$$\Theta_{optFWHM} = \frac{FWHM}{focal\ length} \cdot \frac{180}{\pi} \cdot 3600\ [arcsec] \quad 1\text{-}2$$

$$\Theta_{optHEW} = \frac{HEW}{focal\ length} \cdot \frac{180}{\pi} \cdot 3600\ [arcsec] \quad 1\text{-}3$$

These equations are valid for small angles, where it can be assumed, that: $tg(\theta) = \theta$.

In Table 1.1 (shown at the beginning of this paragraph 1.1.2) there are listed a few space missions with their principal parameters, including the angular resolution. Observatories using coded masks, like the INTEGRAL, have the angular resolution of several of arcminutes. The NuSTAR mission [5] and the SIMBOL-X project [4], both with grazing incidence mirrors and their angular resolution (HEW) of 58 and 20 $arcsec$ respectively, are excellent examples of achievable capabilities.

Influence of detector on spatial resolution

According to the Shannon theorem in order to sample the PSF obtained for an optical system (with an ideal detector) the pixel size should be at least twice smaller than FWHM of the PSF. Thus the minimum condition between optics and detector spatial resolution is established. Ideally the detector resolution should be large enough so as not to degrade the angular resolution determined by the optical system. Therefore we must design detectors with good spatial resolution as well. In a detector of a given area, the increase in spatial resolution means an increased number of channels. For a detector with a specified pixel size, the corresponding angular resolution is defined as:

$$\Theta_{det} = \frac{pixel\ size}{focal\ length} \cdot \frac{180}{\pi} \cdot 3600\ [arcsec] \quad 1\text{-}4$$

However there are effects related to detector physics, which will cause us to revisit the relationship for the optimal pixel size (*1-4*). Namely this is the charge sharing effect that degrades detector's spatial resolution. On the other hand there are processing techniques that permit to oversample the position given by geometry.

1.1.2.3. Energy measurement

Spectral resolution

The ability to measure energy of the incoming photons is another fundamental function of an imaging instrument. The parameter known as spectral resolution is quantified in terms of Full Width at Half Maximum. Because its profile on the energy axis (Figure 1.9) is typically Gaussian (with standard deviation of σ) FWHM can be calculated as:

$$FWHM = 2 \cdot \sqrt{2 \cdot \ln(2)} \cdot \sigma \quad 1\text{-}5$$

In astrophysics the small FWHM value is important for determining the spectral emission lines, used for example in chemical composition or in red shift measurements. The energy resolution depends primarily on the type of the detector and its geometry. Furthermore the readout electronics connected to detector has significant influence on that parameter. The value of the FWHM spectral resolution usually depends on the absolute measured energy – therefore FWHM is calculated in

electronvolts at the given energy. Alternatively it is quantified in the relative unit of percent of the measured energy. Spectral resolutions of modern hard X-ray spectro-imaging instruments are shown in Table 1.1, i.e. FWHM in NuSTAR is $0.9\ keV$ at $60\ keV$, whereas for the Astro-H it is envisaged to be below $1\ keV$ over the entire energy band.

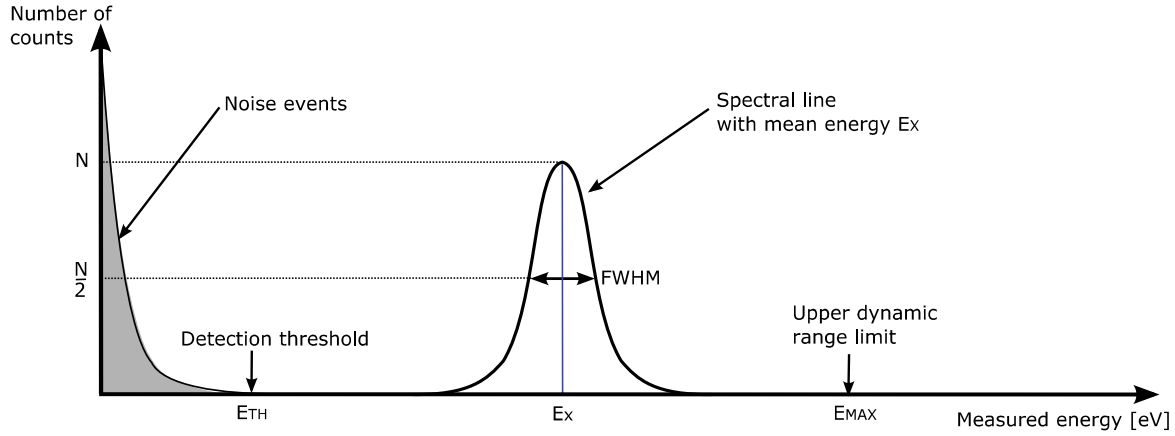


Figure 1.9 Characteristic points on a spectroscopy plot of an imaging spectrometer. The detection threshold E_{TH} has to be chosen above the intrinsic noise, no energy measurement can be achieved above the upper limit of the dynamic range E_{MAX}. A photon beam of discrete energy E_x appears in the measurement as a broader line, typically of a Gaussian shape and is described with the FWHM resolution.

Detection threshold and dynamic range

Within the subject of the energy measurement there are two more critical parameters: the detection threshold and the dynamic range. They both define the energy band for the observation. A large energy range is desired to observe astronomical objects over a wide band. While the low energy range reveals the thermal emission of the celestial sources, the high energies are characteristics of non-thermal emissions occurring for example during particle acceleration processes. The two components are of major importance to identify the observed object nature. Most of the high-energy sources are subject to these different emission processes simultaneously, thus astronomers claim the parallel observations over wide energy band, as much as possible. There are even more arguments for that. Observation of a given type of high-energy sources in nearby galaxies or at cosmological distance will generate similar light distribution but red-shifted to the low energies. Getting a low energy band as well as a high-energy cut-off is equivalent to extend the “depth of focus” of a telescope. Besides, most of the sources, independently of their nature (black hole, neutron star, supernovae) offer much more photons at low energy than at high energy – therefore lowering the range in a high energy detector is advantageous in terms of sensitivity regarding the detection capabilities (for those sources obviously that emit at both high and low energy, which is not always the case). Using a unique instrument in these observations facilitates the cross calibrations.

The thickness of a detector will drive its detection efficiency at high energy, through the absorption probability. A relatively “large” thickness is necessary for detecting high energies, but for most techniques generates a higher background than a thin detector. Choosing the detector thickness results thus from an optimization between the efficiency and the noise level, strongly depending on the energy range of interest.

Concerning the lower energy band, in addition to the astronomer requests to detect low energy photons, low detection threshold is also useful in measurement of high energy photons. As a matter

of fact, segmented detectors, especially the pixelated ones, are subject to charge sharing between the pixels. In this case, measuring the energy in each of the pixels in which the charge is distributed is necessary for reconstructing the initial energy, by a simple sum. The lower the detection threshold, the less information is lost about the photon. Its value is mainly limited by the electronic noise of the imaging spectrometer.

For detectors, which can efficiently extend to the hard X-ray domain (above ~ $10\ keV$) the minimum detection threshold is typically in order of few keV, as for example in case of the ASTRO-H and NuSTAR missions (Table 1.1). Concerning the upper limit, in the systems using coded masks, as the INTEGRAL – the dynamic range reaches $10\ MeV$. However X-ray telescopes using grazing incidence mirrors have a limited dynamic range to 70 - $80\ keV$, as demonstrate the examples from Table 1.1 with the SIMBOL-X, NuSTAR and Astro-H parameters.

1.1.2.4. Qualifications for space environment

Ability to fly in a space mission implies another group of parameters for the X-ray detector. It is related to the harsh environment for the X-rays astrophysics experiments. The shock and vibrations at the satellite launch raises requirement of solid mechanical structure. In addition, endurance as well as sensitivity to thermal environment, which may change instantaneously during the flight, must be considered in the instrument design. Once placed into orbit a satellite is exposed to all kinds of radiation from cosmic origin, both directly and indirectly through secondary particles generated into the spacecraft with intensity depending on the orbit position. This includes high-energy photons and charged particles, which not only may cause false triggers of the detector, but also far more severe consequences. The detector material is being damaged with the accumulated radiation dose, and the readout electronics can possibly experience slow degradation.

In order to guarantee a proper function of the instrument all along the space mission duration, the material and construction have to be carefully chosen. A potential detector that meets the functionality and performance requirements must undergo a series of qualification tests. The shock and vibration proofs constitute some pass conditions. There are also qualifications against damage due to radiation dose and cosmic rays effects. Finally there are life tests, which ensure a long-term operation in the harsh environment of the satellite.

1.1.2.5. Cost: power and material

What kind of detector type should be chosen in the X-ray astronomy experiments to meet all of the specified requirements – bulky scintillators, gaseous or semiconductor crystals? The physical dimensions are one of the cost aspects, since they often translate to the satellite payload structure mass. Compactness is one of the most important conditions that make the semiconductor detectors so popular on-board today's space-borne X-ray observatories.

The operating temperature is the second criteria in the material choice. A detector that operates in cryogenic conditions requires a complicated cooling system. This significantly increases the instrument cost: because of additional development time and – even more importantly – additional weight and complexity due to the temperature control device. This is a problem which is for example of utmost importance for detectors intended to operate in a near zero temperature. In this case the front-end electronics of the spectro-imager designed to readout the detector becomes the main

concern. For the purpose of good energy resolution this circuit should be physically placed directly next to the detector. Consequently the power dissipated by the readout electronics works against the temperature cooling (and regulating) system. This fact is important in the overall instrument design concept: the dissipated power has to be traded-off against the spatial resolution. A good spatial resolution requires a high number of detector units (pixels or strips). However the high number of channels translates to an increased power consumption in the readout electronics and more severe requirements for the temperature stabilization.

These main issues that influence the system cost, namely the material volume and the power consumption, are addressed by a careful selection of the detector type and use of integrated low power readout electronics. These two elements together constitute the core of an imaging-spectrometer instrument. In the consequent sections of this chapter I will justify the choice of the CdTe semiconductor detector, selected for the new X-ray imaging device. Secondly I will discuss requirements for the electronic circuit design: the necessary features to correctly read out information from the given detector, while meeting the criteria imposed by the astrophysicists' demands.

1.2. CdTe – a candidate for hard X-ray instrument

A hard X-ray imaging device can be realized in several ways. Common solutions include gaseous, semiconductor- or scintillator-based detectors. Those that are considered here are the semiconductor detectors. Typically they have significantly smaller dimensions than gas-filled instruments and a superior energy resolution when compared to indirect conversion of scintillators.

1.2.1. CdTe vis-à-vis other semiconductor detectors

An X-ray photon interacting in a semiconductor induces free electrical carriers. Resolution of the X-ray energy measurement increases with the number of carriers generated by the photon inside the detector. The accuracy of the energy measurement improves with a higher number of carriers. This is related to the interaction statistics. A common characteristic of semiconductor materials is a relatively low value of the ionization energy, in the order of few electronvolts per electron-hole pair. This results in a high number of carriers due to an X-ray interaction, significantly higher than e.g. in gases. In fact semiconductors offer the best intrinsic energy resolution among all types of detectors [15]. Materials belonging to this family differ from each other with certain properties. Each of the available semiconductor-based detectors has its own advantages and drawbacks, which have to be compromised to fit the application.

Material:	Si	Ge	CdTe
Atomic number	14	32	48/52
Density [g/cm^3]	2.33	5.33	5.85
Bandgap [eV]	1.12	0.72	1.44
Ionization energy [eV/e^-–h^+ pair]	3.61	2.98	4.42

Table 1.2 Comparison of semiconductor properties [15][17]

1.2.1.1. Bandgap voltage

The implied characteristic of all semiconductors is the presence of the bandgap between the conduction and the valence band. Its value is strongly related to the electron-hole pair creation energy. In a low bandgap material an interacting photon generates a higher number of free charge carriers, than when the bandgap is high. Consequently a better accuracy in the energy measurement can be achieved. With this respect germanium detectors are the most valuable (Table 1.2). However the low bandgap also results in higher probability of thermal excitation of an electron-hole pair, which is independent of any X-ray event arrival. The thermally generated carriers are the cause of the dark current in the detector. This effect degrades the energy resolution. The dark current has an exponential dependency on the temperature. With the compromise between the pair creation energy and the dark current a good energy resolution for germanium is achieved only in cryogenic conditions. Unfortunately a cryogenic cooling in an astrophysics instrument significantly increases the overall cost and reduces the potential lifetime of the space mission. In contrast to germanium, in silicon the operation near room temperature is sufficient to achieve a good spectral resolution below 1 % FWHM (in the energy range of up to few keV typically measured with silicon). An only slightly

higher bandgap value is observed in Cadmium Telluride, which is also suitable for operation at room temperature.

1.2.1.2. Photon-detector interaction

At the energies corresponding to hard X-rays the probability of an interaction between the photon and the detector also becomes an important issue, because of the important penetration capability of X-rays. In materials with higher atomic number and density, the photon absorption length is smaller. Therefore such semiconductors can provide good detection efficiency for a reasonable thickness. Cadmium telluride has the atomic number and the density significantly higher than Si, as shown in Table 1.2. Meanwhile their bandgap energy values are similar. This makes CdTe an interesting candidate for the X-ray detection.

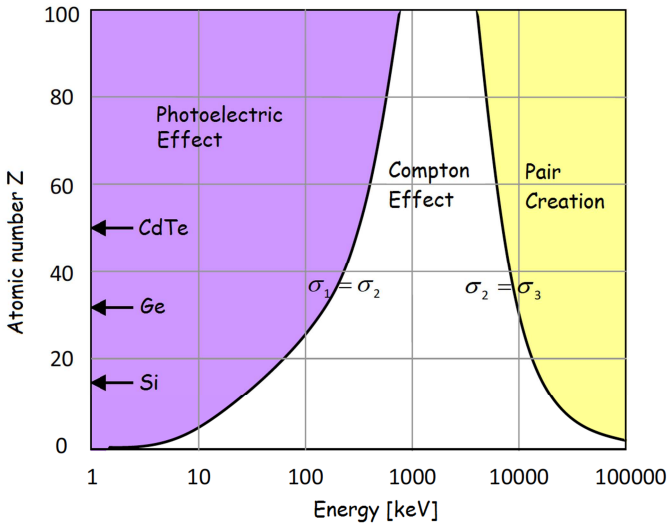


Figure 1.10 Dominating interaction effect (photoelectric, Compton and pair creation) as a function of the incident photon energy and the atomic number of the detector material [16].

There are three dominating interaction mechanisms: photo-electric effect, Compton scattering and pair production. Their respective predominance on the photon energy and on the detector atomic number is illustrated in Figure 1.10.

- **Photoelectric effect** is the dominant process of interaction for low energy X-rays. During the interaction between a photon with an atom the photon is completely absorbed and a photoelectron is freed from the atom. Its kinetic energy is equal to that of the photon reduced by the binding energy between the atom and the electron. The electron undergoes further interactions. In consequence the entire energy of the primary photon is absorbed locally in the detector [15].
- **Compton effect.** With higher energy of the incident photon, the probability of the Compton effect increases. An incident X-ray hitting the detector is scattered from an electron within an atom. As a consequence the initial trajectory of the photon is diverted by an angle ϕ. Meanwhile the electron is recoiled from its rest position. The energy of the secondary X-ray is given by the equation [15]:

$$E_{scatter} = \frac{E_{initial}}{1 + \frac{E_{initial} \cdot [1 - \cos(\phi)]}{m_e c^2}} \quad 1\text{-}6$$

Where $m_e c^2$ is the electron rest-mass equal to $511\ keV$. The scattered photon can escape the detector. Thus the energy of the initial incident X-ray often cannot be measured. Meanwhile the electron energy is typically absorbed resulting in a Compton background on the spectroscopic image.

- **Pair production.** Finally at high energies the result of interaction can be the production of an electron-positron pair [15]. This effect can occur if the energy of the photon is higher than $1.02\ MeV$, which is twice the electron rest-mass energy. In practice this effect occurs at energies significantly higher than that – at few MeV, corresponding to gamma-rays. Only special detectors with a very large volume can fully absorb the initial photon energy.

The most desirable interaction mechanism for a photon energy measurement is the photoelectric effect, where the energy is usually absorbed completely and locally. In case of the Compton and the pair-production effects – the secondary interaction product is likely to escape the detector, with only fraction of the initial energy being deposited. In Figure 1.10 the three interaction mechanisms are analyzed as a function of the photon energy and the atomic number of the detector material. From this plot it can be determined which detectors ensure that photoelectric effect dominates in the energy band of interest. In the hard X-ray domain, where the energies reach few hundreds keV, its occurrence probability is much higher with CdTe than with Si or Ge. This is a result of the high atomic number of CdTe. The photoelectric effect domination becomes the most important motivation to choose the CdTe semiconductor for photon energies measurement in the hard X-ray band.

1.2.2. Cadmium telluride operation characteristics

A typical size of commercially available CdTe crystals is up to $1\ cm^2$ of surface area with a thickness d in the range from 0.5 mm to a few millimeters. Each side of the detector is equipped with one or multiple metal electrodes. Like in other semiconductor detectors the X-ray interaction with CdTe results in a cloud of electrical carriers. The number of the electron-hole pairs is given by:

$$N = \frac{photon\ energy}{ionization\ energy} = \frac{E}{w} \quad 1\text{-}7$$

Parameter	Symbol	Unit	Value in CdTe
Electrons mobility	μ_e	cm^2/Vs	950
Holes mobility	μ_h	cm^2/Vs	80
Electrons life time	τ_e	μs	1.2
Holes life time	τ_h	μs	4.6
Fano factor	F	–	0.15

Table 1.3 Physical properties of CdTe [17][21]

The amount of free charge is linearly proportional to the energy of the incoming photon. In order to collect the charge on the detector electrodes a bias voltage V has to be applied. Finally the information carried by the electrical carriers is read out by an electronic circuit connected to the

detector electrodes. In CdTe the electric field Ɛ applied across its volume of length d is in the order of a few hundred volts per millimeter.

$$\mathcal{E} = V/d \qquad 1\text{-}8$$

In a large electric field the free charge can be transported between the interaction point and the detector electrodes in a shorter time. This is required to provide good charge collection capability.

1.2.2.1. Charge transport in CdTe

Free holes and electrons in a semiconductor are characterized by two parameters related to their transport: mobility μ and lifetime τ. The acceleration of charge carriers due to the electric field Ɛ is disturbed by successive collisions with the semiconductor lattice. Consequently the charges move with an average velocity limited by the rate of collisions. This average drift velocity is a product of carrier mobility μ and the applied electric field Ɛ [18].

$$v_{drift} = \mu \cdot \mathcal{E} \qquad 1\text{-}9$$

The second mentioned parameter, the lifetime τ, is the average time that an electric carrier remains in free motion. In reality it may meet an impurity trap or a crystal defect where it recombines before reaching the detector electrode. A long life time and high mobility are both favorable for a good charge transport. Therefore we often speak about the products of mobility and lifetime: $\mu_e\tau_e$ for electrons and $\mu_h\tau_h$ for holes [15]. Unfortunately the parameters: μ and τ in CdTe (Table 1.3) are significantly smaller than in Si or Ge. Due to high density of the material, both holes and electrons have very low mobility. Crystal defects, even in a high purity CdTe, are manifested with relatively short life times.

1.2.2.2. Charge loss: detector thickness vs. bias voltage

The holes and electrons resulting from the X-ray interaction travel in opposite directions, towards the negative and the positive electrodes respectively. Only once they reach the corresponding electrode the full signal is induced on both electrodes. If a carrier recombines within the detector bulk, it contributes only partially to the signal. This causes a degradation in the measurement accuracy and consequently in a worse energy resolution.

The distance that a free carrier has to travel to reach the relevant electrode, and to induce the full signal, depends on the interaction point. The maximum distance is equal to the crystal thickness d. However both electrons and holes have a finite lifetime, which is a limiting factor in the charge transport. In a polarized detector a carrier moving with drift velocity v_{drift} typically travels a distance s_{drift} until it recombines. This distance known as the mean drift path is different for electrons ($s_{drift/e}$) and holes ($s_{drift/h}$), as shown in Figure 1.11, and is described as:

$$s_{drift/e} = v_{drift/e} \cdot \tau_e = \mu_e \cdot \tau_e \cdot V/d \qquad 1\text{-}10$$

$$s_{drift/h} = v_{drift/h} \cdot \tau_h = \mu_h \cdot \tau_h \cdot V/d \qquad 1\text{-}11$$

Where μ and τ are the mobility and lifetime, d is the detector thickness and V is the voltage applied between the electrodes. For good charge collection capability the mean drift distance should be longer than the detector thickness to minimize the probability of recombination [17]. In CdTe holes

have a shorter mean drift path than electrons, because of their poor transport properties, as shown in Table 1.3. Consequently the holes properties establish the minimum relationship between the detector thickness and the applied electric field Ɛ:

$$\mu_h \cdot \tau_h \cdot \mathcal{E} > d \qquad 1\text{-}12$$

However to minimize charge loss the recommendations are the following [15]:

$$\frac{\mu_h \cdot \tau_h}{d} > 50 \qquad 1\text{-}13$$

This condition implies that in a 0.5 mm thick CdTe crystal a high bias voltage of 700 V is required for obtaining a good energy resolution, with a negligible effect of recombination.

1.2.2.3. Cathode side exposition to X-rays

As it has been already emphasized, the holes transport is the limiting factor in CdTe charge collection. If the interaction takes place near the cathode the holes have only a short travel distance to reach the electrode. The probability of recombination is thus very low. Therefore in this location the charge loss due to holes is not as significant as in case of an interaction in the anode proximity. The interaction point has an impact on the charge collection. This is illustrated in Figure 1.11. The charge loss due to electrons is usually not a concern in CdTe.

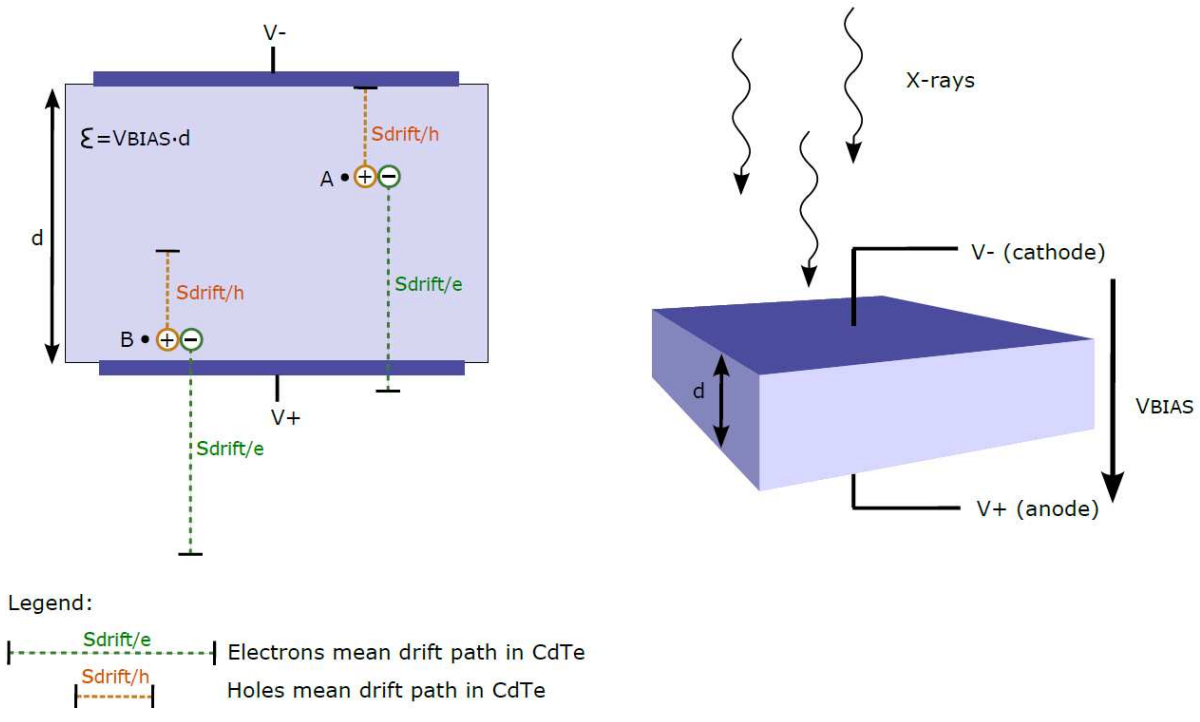


Figure 1.11 Illustration of the charge loss effect in CdTe. If the cathode side is exposed to X-rays, the interaction point A (closer to cathode biased with V^-) corresponds to a lower energy photon, which interacts near the surface. The distance that the resulting free carriers have to travel to reach the electrodes is smaller than the mean drift path, both in case of electrons and holes. Consequently the charge loss probability is very low. In the case of interaction at the point B, corresponding to a higher energy photon penetrating deeper into the detector volume, holes are likely to recombine before reaching the cathode.

A method commonly used to provide a good energy resolution at lower energies is to expose the cathode side of the detector to the ionizing radiation. This greatly increases the probability for the

low energy photons to interact near the irradiated surface. Of course the events corresponding to higher energies are likely to penetrate deeper inside the crystal, being more susceptible to charge loss in this arrangement. However in the upper region of the dynamic range there are also other effects that cause the measurement resolution to be worse, therefore the effects of charge loss are more acceptable at high energies.

The essential result of the cathode side irradiation is the reduced charge loss and the improved spectral performance. In a detector, with a given thickness d, this adds flexibility in the electrical field adjustment. It is very valuable and there is a good reason to decrease its value Ɛ: to limit the level of the undesired dark current, which is the next detector parameter discussed.

1.2.2.4. Dark current

Semiconductors at a temperature above the absolute zero have a certain amount of free carriers per volume unit. The electrons and holes are continuously liberated from atoms due to their thermal excitation, being the origin of a dark current in the detector. The number of carriers determines the current density, therefore it is interesting to gain more overview on this mechanism. The free electron density n and free holes density p are defined respectively as [19][20]:

$$n = N_C \cdot e^{-(E_C - E_F)/kT} \qquad 1\text{-}14$$

$$p = N_V \cdot e^{-(E_F - E_V)/kT} \qquad 1\text{-}15$$

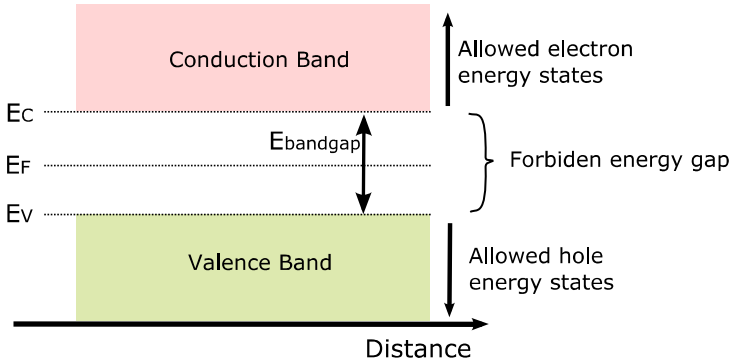


Figure 1.12 Simplified diagram of energy bands in a semiconductor.

The carriers concentrations are typically given in units of cm^{-3}. In the expressions N_C and N_V are respectively the conduction and valence states densities. They describe the number of quantum states per unit volume and are characteristic to the semiconductor material. E_C is the energy defining the bottom of the conduction band, while E_V is the higher limit of the valence band (Figure 1.12). The energy E_F is the Fermi level in the semiconductor. The equations describe the case of an intrinsic semiconductor. Calculations of the carrier concentrations in a p-type, n-type or a compensated semiconductor will result in similar expressions with exponential dependency on the temperature.

Once the electric field Ɛ is applied across the crystal, it forces the free carriers to move along the field lines, towards the lower potential. As a result a current flows between polarized electrodes, this is the dark current. The mean density of the total current contributed by holes and electrons motion can be calculated as [18]:

$$J = q \cdot \mathcal{E} \cdot (p \cdot \mu_h + n \cdot \mu_e) \qquad 1\text{-}16$$

Where q is the unit charge equal to $1.602 \cdot 10^{-19}\, C$. The current density is given in the unit of amperes per semiconductor cross-section area $[A/m^2]$. In a detector this continuous thermal motion of the electrical carriers has undesirable effects. It constitutes a background to the instantaneous charge signals due to X-ray events. The thermal nature of carrier's excitation implies transient fluctuations in their density, which is source of shot noise [19]. Therefore by all possible means the average dark current should be minimized in detectors.

1.2.2.5. Dark current reduction

There are few ways to reduce the dark current in a CdTe detector, they are listed below. Some of them, namely temperature and bias voltage, are the adjustable operating conditions. The others are related to the fabrication of the detector: layout of electrodes as well as type of metal deposited on anode and cathode side.

Temperature

Typically CdTe instruments operate between the room temperature and a few tens of degrees below 0 ℃. A decrease in temperature results in an exponential reduction of dark current, therefore it plays the most important role on the dark current level.

Bias voltage

The bias voltage directly defines the electric field across a detector with a thickness d. Its effect on the detector dark current is linear. Again it is desirable to have a voltage as low as possible. However, as it has been highlighted earlier, the bias voltage in CdTe is important for the charge collection properties. For this reason its value has to be carefully balanced to achieve the best possible energy resolution.

Electrode area

The absolute amount of dark current I_{DET} in a CdTe crystal is determined by its density J and the detector area A, with the linear relationship:

$$I_{DET} = J \cdot A \qquad 1\text{-}17$$

If the application allows, crystals with possibly small surface should be used. This would decrease the value of dark current and its parasitic effects. The dependency is exploited in multiple electrode detectors. In the segmented arrangement, the detector area is covered with several electrodes, each collecting only fraction of the total dark current flowing across the crystal. It turns to be an advantage since the signal due to an X-ray event is typically collected by only one of the electrodes. Consequently the unchanged signal value and lower background with only fraction of the total dark current result in improved accuracy of the signal measurement.

Schottky barrier

In Si detectors the p-n diode structure in reversed bias configuration is used to reduce the dark current. When depleting the detector area from majority carriers the conductivity drastically decreases, limiting the dark current. Similar blocking contact can be formed on a metal-

semiconductor junction by introducing a Schottky barrier [20]. The blocking contact has been successfully introduced also in CdTe detectors [24], by adding a doping in the semiconductor and choosing metal types and electrode deposition method. Detectors that can operate as Schottky diode are nowadays commercially available. The typical electrode structure for a p-type CdTe, is a high energy barrier for holes formed on the anode side (indium or aluminum) and a quasi-ohmic contact on the cathode side (platinum or gold). Consequently holes removed from CdTe on the cathode cannot be replaced by holes from the opposite electrode. This blocks the current flow through detector. CdTe with Schottky barrier is known for the great improvement in energy resolution due to dark current reduction [24][25]; good results have been demonstrated with detector bias voltage high enough to provide complete charge collection.

Guard ring

The studies of dark current as a function of the crystal area have shown that the current increases with the square root of the area [27], what indicated existence of significant surface current due to edge effects. While the Schottky barrier can reduce the semiconductor bulk dark current, between detector electrodes, it cannot suppress the surface current. A guard-ring electrode on the crystal border, around the active electrodes (Figure 1.13) is now a commonly used practice to deal with undesired effects of the surface current. Decrease of the dark current by an order of magnitude has been demonstrated with cathode surrounded by a guard-ring [26]. Also more recent studies of the anode guard-ring have confirmed effectiveness of the structure by comparing current densities in the anode and in the surrounding electrode [28].

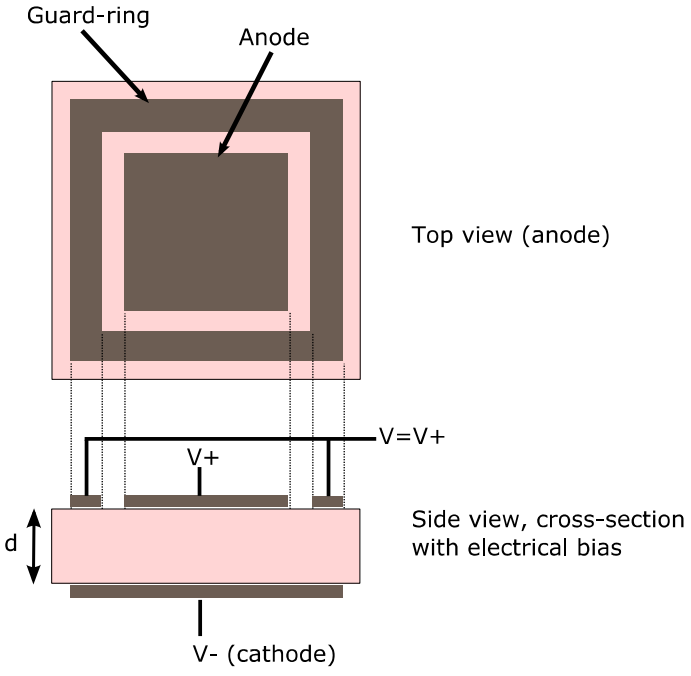


Figure 1.13 Illustration of the guard-ring structure application in a detector. The guard-ring here is on the anode side.

Nowadays with application of the above techniques – extremely low levels of dark current are achieved, in the range of pico-amperes at room temperature. The CdTe crystal intended for use in the X-ray imaging detector discussed in this work is expected to be equipped both with Schottky contact and the guard-ring. In the paragraph 2.1.2 I estimate the value of dark current in the dedicated detector.

1.2.2.6. Energy resolution

The most important parameter of a spectro-imaging instrument is the energy resolution. To define it let's consider for a moment the detection of a mono-energetic photon beam of energy E_x. Even with full photon absorption in the detector the measured energy would not be the same for each detected event. The result of multiple acquisitions is a Gaussian distribution, as shown in Figure 1.14. Its mean measured value E_x is equal to the energy of arriving photons. The energy resolution is usually described with the Full Width at Half Maximum of the peak (FWHM). Typically FWHM is given in electronvolts at the mean energy E_x or in the relative unit of percentage of the measured energy. For a Gaussian distribution with standard deviation σ it can be shown that:

$$FWHM = 2.35 \cdot \sigma \qquad 1\text{-}18$$

There are several phenomena originating in detector that result in this non-monoenergetic energy distribution. In Figure 1.14 it is illustrated how different phenomena influence the measured spectrum.

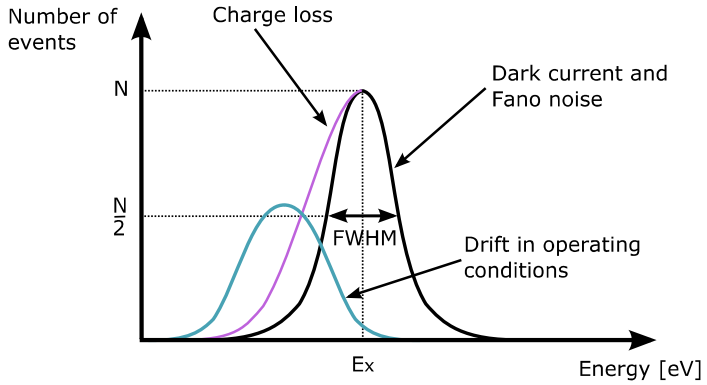


Figure 1.14 Illustration of energy spectrum in energy measurement of a mono-energetic photon beam E_x. The detector energy resolution is defined as Full Width at Half Maximum (FWHM). Dark current and Fano noise cause symmetrical fluctuations in measurement. Charge loss degrades energy resolution into a non-symmetric distribution with tail at low energies. Drift of parameters due to polarization effect shifts the peak to lower energies.

Dark current

The measured signal is accompanied by a continuous dark current background. Due to its nature of thermal generation, there are transient fluctuations from its mean value I_{DET}. The transient variations in the charge flow cause imprecision in the energy readout. These are directly proportional to the dark current mean value. As discussed above, there are several techniques that can greatly reduce the dark current. However even a small current might become a problem, unless carefully considered in the electronic readout circuit design. Therefore the dark current influence on the energy resolution is one of the subjects that I will study in depth throughout the presented work.

Fano factor

An X-ray interacting in a detector deposits its energy E by ionization. The expected number of electron-hole pairs N_{e-h} created in this process is determined by the mean ionization energy w (expressed in electronvolts per electron hole-pair):

$$N_{e-h} = \frac{E}{w} \qquad 1\text{-}19$$

However the exact number, when observed over many events shows a variance from the mean number defined by *1-19*. This is related to interaction statistics. The standard deviation in the number of pairs N_{e-h} is given by the equation [15]:

$$\sigma_N = \sqrt{\frac{F \cdot E}{w}} \qquad 1\text{-}20$$

The coefficient F is known as the Fano factor. The fluctuations in the number of carriers can be also expressed in terms of FWHM resolution:

$$FWHM_N = 2.35 \cdot \sqrt{F \cdot E \cdot w} \qquad 1\text{-}21$$

The last relationship shows that the achievable energy resolution becomes worse as the energy increases. The effect of Fano noise is only related to detector physics and there are no means to eliminate it. Consequently it sets the limit on the energy resolution in a CdTe-based imaging instrument.

Collection efficiency

It has been already pointed out that holes have poor transport properties in CdTe. In consequence the free carriers, generated upon a photon interaction, might recombine before reaching the detector electrode. Indeed only part of the deposited charge is induced on electrodes and the measured signal charge is smaller than that generated through the initial energy deposition. Thus in the measured energy spectrum, the so-called charge loss effect induces a tail at lower energies which degrades the energy resolution. This is illustrated in Figure 1.14. If the cathode-side of the detector is exposed to a photon beam the tail increases with the measured X-ray energy. By adjustment of the detector bias voltage to higher values the charge collection improves and the asymmetry of the peak is minimized.

Time drift of collection efficiency – polarization effect

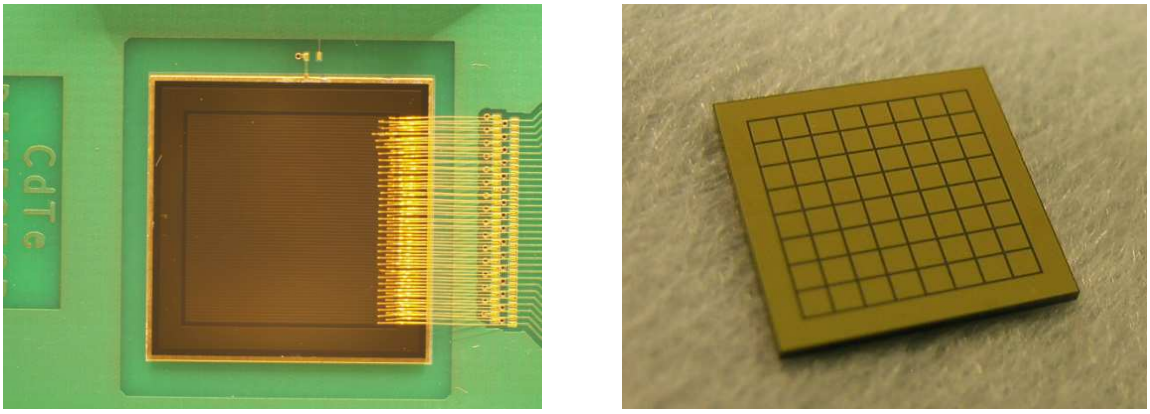
In CdTe with the Schottky barrier a degradation of the energy spectrum with time has been observed [25]. In this type of detectors progressive modifications in the electric field distribution occur, causing worsening of the charge collection efficiency with time. The consequence is a variation of the detector gain, shifting the energy peak towards lower energies, and worsening the energy resolution, as illustrated in Figure 1.14. The polarization effect develops over hours. A high bias voltage and a low operating temperature slow down the undesirable process. Also a smaller detector thickness is greatly favorable. Meanwhile a data correction scheme can be introduced to compensate for the changes in collection efficiency. Eventually by switching off the bias voltage the initial spectral performance can be recovered. It has been demonstrated in [28] that in a $1\ mm$ thick CdTe biased to $300\ V$ and at a temperature of -8℃ the $60\ keV$ peak drifts to lower energies with a rate of $1\ eV/h$.

From all dominating phenomena that influence the energy resolution of a detector the Fano limited noise is the one that cannot be avoided. With a careful choice of the detector type and operating conditions all the other effects may be diminished to a negligible scale. What has not been mentioned so far is the non-ideal process of the energy readout, which is external to detector. The

readout circuit is also burdened with imprecision due to electronic noise, which may severely degrade the energy resolution. The methods to decrease the electronic noise and the possibility of designing a complete detection instrument limited only by the Fano statistics are the subjects of the subsequent chapters and will be wider discussed.

1.2.3. Position sensing: strip or pixel?

One of the reasons why the CdTe is commonly considered in imaging applications is the possibility of producing segmented electrodes on a single crystal. Consequently position sensing can be achieved with fine spatial resolution. There are two arrangements that are typically used: the double-sided strip and the pixelated layout. Photographs of detectors for both position sensing techniques are shown in Figure 1.15.



A) B)

Figure 1.15 A) 20 µm pitch double-sided strip CdTe detector with guard-ring, bonded to an external readout circuit, fabricated by the Paul Scherrer Institut [51]. B) 500 µm pitch pixelated CdZnTe with guard-ring, fabricated by Acrorad [52][16].

1.2.3.1. Double-sided strip detector

This position sensing technique exploits properties of the orthogonal geometry. Each side of the crystal is equipped with multiple parallel strip electrodes. The pattern on the cathode side is the same as on the anode side, but rotated by $90°$. Electrodes placed on the same surface are biased to identical potential, however each electrode is connected to an individual electronic readout channel. The position resolution of n in each direction (x and y) can be achieved with n-cathode and n-anode strips. An interaction occurring in the crystal results in charge inductions on i-th cathode and j-th anode. The corresponding readout channels connected to these electrodes receive a charge signal. The intersection of the two orthogonal electrodes indicates the X-ray arrival position. However if two events occur simultaneously at point A and B, there may be four possible intersection points between the receiving electrodes, as shown in Figure 1.16. The two photons cannot be identified unambiguously.

The total number of electronic channels required to readout the double-sided strip detector is only $2n$. This is the major advantage of the discussed arrangement, as it translates to low power consumption and to system simplicity. The second benefit is related to the fact that the induced

charge is read out from both sides: a cathode strip and an anode strip. The signal obtained from both polarities (electrons and holes charge) can be used to correct for charge loss [29]. Furthermore in case of a complete charge collection, with no charge loss, the algebraic sum of energies measured at each electrode reduces contribution of the electronic noise by a factor $\sqrt{2}$.

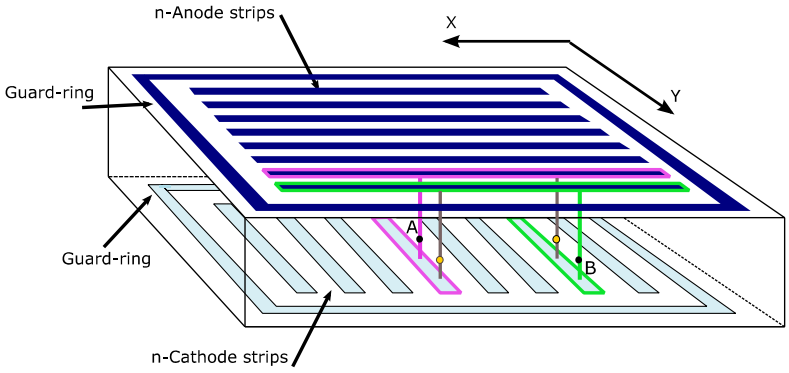


Figure 1.16 CdTe detector in the double-sided strip arrangement with guard rings. The position resolution is n in each direction: x and y. Interactions of two photons are indicated, at points A and B. The X-ray event is localized on the intersection of the cathode and the anode strips that receive charge signal. If two events arrive simultaneously their position is uncertain.

1.2.3.2. Pixelated detector

The second common position sensing technique used in CdTe is the pixelated arrangement. The detector has a planar electrode on one side and a pixelated pattern on the opposite side. The resolution of n in both x and y directions is achieved with n^2 pixels. In this type of detector, in order to determine the position of an incident photon, only the signal charge induced on the pixelated side needs to be read out. Therefore each pixel has an individual readout channel. The total number of electronic channels is significantly higher than in the case of a strip detector with the same position resolution. Because the total power consumption is proportional to the number of channels, their high number is a disadvantage in the pixelated arrangement. Also the realization of physical interconnections between multiple pixels and the electronic readout circuit becomes far more complicated when compared to the double-sided strip detector.

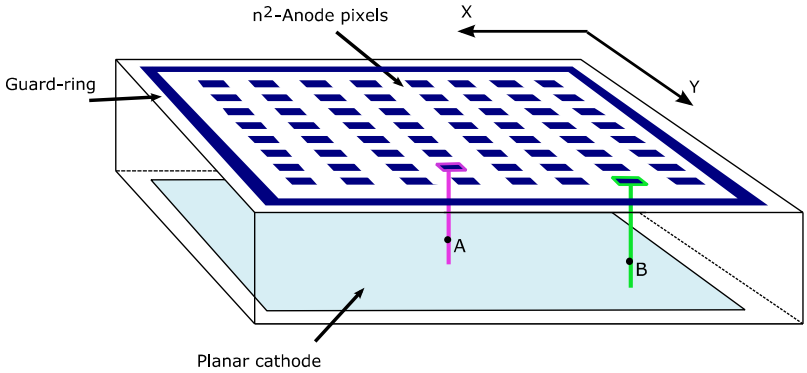


Figure 1.17 CdTe in the pixelated arrangement with a guard ring. The position resolution is n in each direction x and y. Interactions of two photons are indicated, at points A and B. Even if two photons hit the detector simultaneously they can be clearly distinguished, localized and measured.

The pixelated layout has also important benefits. With the single-polarity readout, in the case of two or even more simultaneous photon interactions, the coinciding events can be clearly localized and

measured (Figure 1.17). To continue the comparison with the previous technique, the pixel electrodes are significantly smaller than strips, when two detectors of identical spatial resolution are considered. Dense segmentation of detector surface into pixels finely divides the total dark current generated within the CdTe bulk, so each electronic channel receives only a small fraction of it. Also the capacitance of a single electrode segment is much smaller in the pixelated architecture than in the previously discussed double-sided strip approach. Minimization of these two parameters, the dark current and the input capacitance, significantly helps to reduce the electronic noise. Consequently the best energy resolution can be achieved with pixelated detectors.

The requirement of high number of electronic readout channels in the pixelated arrangement is a great challenge in terms of power consumption and system complexity. The benefit of an excellent energy resolution however is worth the efforts to overcome these issues. The two difficulties can be primarily addressed by using the integrated circuit technologies, which offers compact solutions, and by applying the low power design techniques. This work is dedicated to readout of a pixelated detector with the aim to approach the Fano-limit for the energy resolution. As a consequence the power consumption and the system hybridization issues will be the driving factors when determining the parameters of the electronic readout circuit.

1.2.4. Optimal pixel pitch

In imaging spectrometers the requirement for small pixel (or strip) pitch comes in the first place from the astrophysicists' demands. A certain upper limit size is always necessary to meet the specified angular resolution. For instance let's consider the NuSTAR mission launched in 2012. It is based on an X-ray focusing telescope with a $10\ m$ focal length. The FWHM angular resolution of the Point Spread Function is $18\ arcsec$. To achieve this level of detail in position sensing the imaging instrument placed in the focal plane must have a pixel pitch not larger than $870\ \mu m$. The actual detector implemented on the NuSTAR has a somewhat smaller pitch of $600\ \mu m$ [5]. Future missions might require even higher pixel density either for better angular resolution or in order to afford a shorter focal length. This trend is already present in the ASTRO-H mission [53], where a fine pitch $250\ \mu m$ double-sided strip CdTe is used.

There are two physical phenomena related to the detector geometry that influence its performance: the small pixel effect and the charge sharing. Both have to be taken into account while optimizing the pitch between electrodes.

1.2.4.1. Small pixel effect

The voltage applied across the detector drives the charge transport. In case of CdTe with planar electrodes on both sides, the charge induced at either of them is a result of an electron-hole pair motion. Let's consider a single electron-hole pair generated in the planar detector volume (with a large single electrode on each side of the detector). The electric field forces the carriers to move toward the lower potential electrode. The charge induced on each electrode is given by [15]:

$$Q = \frac{q}{d} \cdot (s_h + s_e) \qquad 1\text{-}22$$

where s_h and s_e are the total drift paths traveled by the hole and the electron respectively. If the detector thickness d is significantly smaller than the carriers' mean drift paths ($s_{drift/h}$ and $s_{drift/e}$) then the hole and the electron are likely to reach the corresponding electrode before recombining. In consequence $s_h + s_e$ would be equal to d and the charge Q induced on each electrode would be equal to the unity charge q. Because of the linear distribution of the electric field, each carrier contributes equally to the electrode signal, at each unity distance traveled across the detector. However in the case of a pixelated detector the situation is more complex, even though the general electric field lines can be considered uniform, as in the planar case. First of all, the position of a charge carrier in the crystal determines which pixel electrode is the most sensitive to its movement. Naturally the highest signal is induced on the nearest electrode (indicated by the straight electric field lines). But also as the carrier moves across the amount of induced charge is not the same for each unity distance traveled. A general method to calculate the induced charge Q is described by the Shockley-Ramo theorem [15][17]:

$$Q = q \cdot \Delta\varphi_0 \qquad 1\text{-}23$$

where φ_0 is the weighting potential.

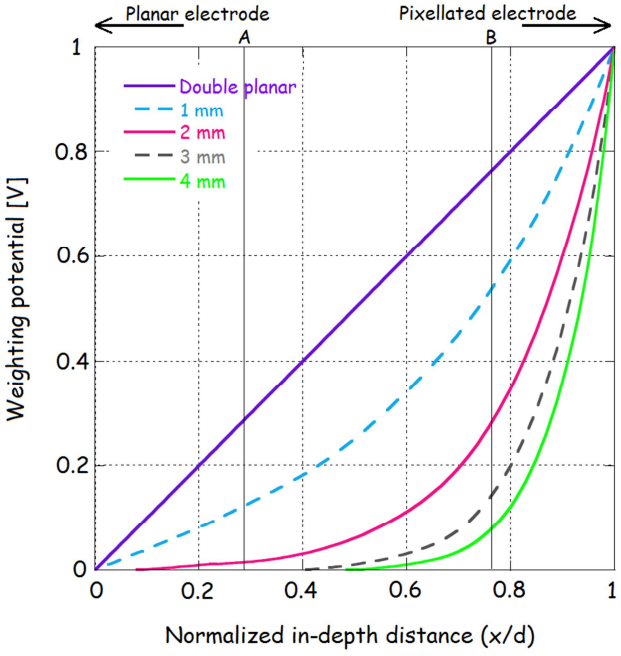


Figure 1.18 Illustration of the weighting potential for a fixed pixel size of 500 µm as a function of the detector thickness d, compared with a planar detector (with single electrode on each side and their size significantly larger than d) [33][16]. Two Interaction points: A and B, are indicated on the opposite sides of the detector. The charge transport properties change as a function of position for different detector geometries.

In case of a multiple-electrode arrangement (as in all position sensing detectors) the calculation of the signal charge is done for each electrode individually. The weighting potential φ_0 is obtained with the electrode of interest biased to unity voltage and all the others being grounded. Consequently the distribution of the weighting potential is highly influenced by the detector geometry, namely the pixel electrode shape and size as well as the detector thickness. This is illustrated in Figure 1.18. The

weighting potential obtained for the planar electrode is a slab. Meanwhile the plots obtained for pixelated detectors with fixed pixel size are flat at the planar electrode side and steeply rising as they approach the pixel electrode. The characteristic shape is further enhanced in detectors where the thickness d is high when compared to pixel dimensions. That is why in this case we speak about the small pixel effect.

1.2.4.2. Anode readout

The weighting potential φ_0 distribution has consequences on charge collection of the pixel electrode. A charge carrier (either electron or hole) contributes more to the signal when it moves in the proximity of the pixel electrode. Therefore in both cases of X-ray interactions, at point A and at point B (Figure 1.18), the charge carrier type moving towards the pixel electrode has the higher contribution to the induced signal. This is not necessarily the case in a detector with planar electrodes. Given the poor transport properties of holes it is especially beneficial to attract the electrons to the pixelated side, while exposing the planar side to the X-ray flux. In this configuration the contribution of holes motion to the induced signal becomes negligible (for most events) and the detector becomes less sensitive to charge trapping.

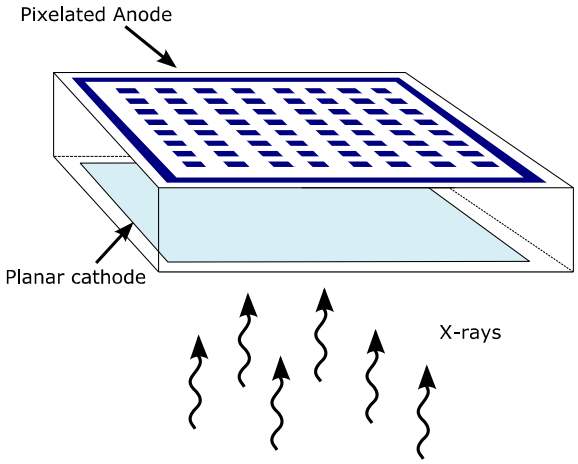


Figure 1.19 Illustration of how the small pixel effect is exploited in practice to improve the charge collection and consequently the energy resolution of a spectro-imaging instrument.

The small pixel effect improves the charge collection when the planar electrode is biased as cathode and the pixelated side as anode (shown in Figure 1.19), as confirmed by the experimental results from [34]. In consequence a detector with the pixelated arrangement can be biased with much lower voltage than a planar detector and still achieve better energy resolution. The discussed effect implies that the detector geometry should have a possibly small pixel size. There are however other boundaries that restrict the minimum dimensions.

1.2.4.3. Charge sharing

Minimizing the pixel size is worthwhile as long as it improves the detector performance. If the spatial resolution exceeds the requirement imposed by the X-ray focusing optics, no improvement in position sensing is achieved. However, a too small pixel geometry could also have a negative effect on the spectral resolution. If the pixel size becomes comparable to size of the charge cloud formed

due to X-ray interaction – the total induced signal is distributed over several neighboring electrodes. This effect is known as charge sharing.

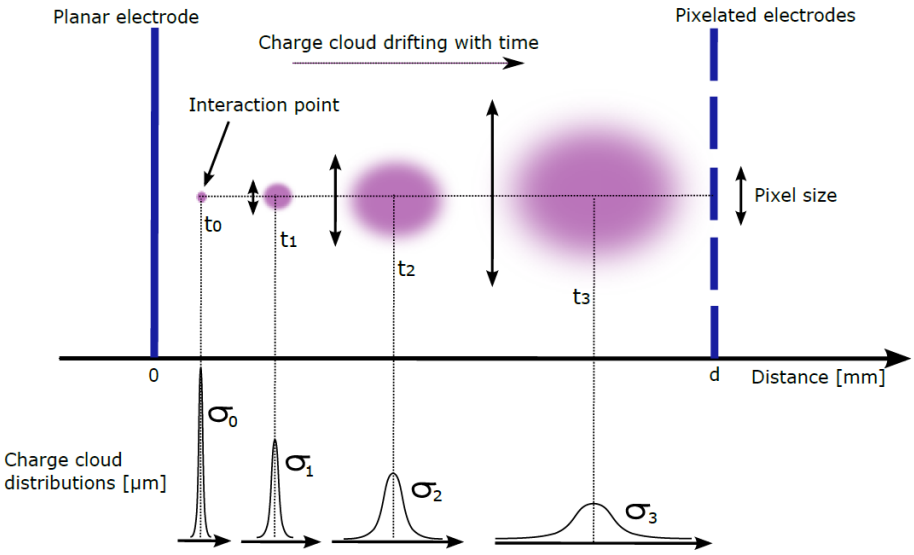


Figure 1.20 Illustration of charge cloud diffusion in a detector as it moves towards the pixelated electrodes (only the electrons charge is considered). The charge cloud drifts across the detector due to the electric field between the electrodes, but it also diffuses with time. A small pixel size in comparison to the diffused charge cloud results in sharing of the charge between several pixels.

Charge sharing may also cause serious degradation in the energy readout accuracy. In an ideal detector, an X-ray event subjected to charge sharing can still be measured. The signals read out from each pixel, once summed up together, provide the incident photon energy. In reality the readout circuit has a discriminator which recognizes event occurrence only if it exceeds a certain signal level. In today's hard X-ray imaging applications this minimum charge corresponds typically to a few keV. The charge sharing may become an issue in the energy measurement: when one of the pixel electrodes receives a portion of charge lower than the detection threshold level [31]. Then this part of deposited energy is lost and the sum of the remaining pixels does not contain the complete energy information. Therefore the probability of charge sharing should be minimized.

The charge sharing can be avoided when the pixel pitch is large enough that the signal from a charge cloud is induced onto a single pixel. For that the charge cloud must be significantly smaller than the pixel size. What is then the size of a charge cloud generated upon a photon energy deposition as it approaches the pixelated anode? Initially its cross-section is very small and can be thought of as a point. However the random thermal motion of carriers causes a successive expansion of the cloud, which is independent of the drift across the detector due to electrical field. This effect is illustrated in Figure 1.20. Considering that the anode side is the pixelated one, it is the electrons charge that is considered. The spatial broadening of the cloud is described by the Einstein's relation [20]:

$$D = \frac{k \cdot T}{q} \cdot \mu_e \qquad 1\text{-}24$$

The diffusion constant D has units of $[mm^2/s]$, k is the Boltzmann constant, T is the temperature expressed in Kelvin, q is the electron unity charge and is μ_e the electron mobility in CdTe. Once the

diffusion constant is known, the standard deviation σ of the charge cloud Gaussian distribution after time t can be obtained [15]:

$$\sigma = \sqrt{2 \cdot D \cdot t} \qquad 1\text{-}25$$

1.2.4.4. Pixel size

In a detector biased with voltage V the charge cloud expands in all directions as it moves with drift velocity v_{drift} along the electric field Ɛ towards the electrode. The worst case is obtained when the interaction occurs near the cathode surface and charge has to travel the full distance d corresponding to the detector thickness. This case is illustrated in Figure 1.20. By the time that the charge cloud reaches the anode, it reaches by diffusion a certain size, with the standard deviation given by [15]:

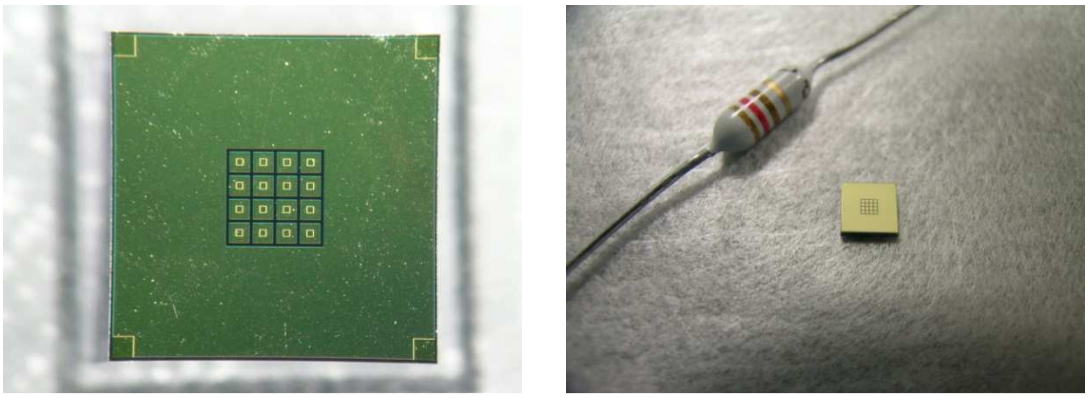
$$\sigma = \sqrt{2 \cdot D \cdot \frac{d}{v_{drift}}} = d \cdot \sqrt{2 \cdot \frac{k \cdot T}{q \cdot V}} \qquad 1\text{-}26$$

The equation has been transformed using the drift velocity v_{drift}. This transformation shows that the cloud size is only dependent on the detector thickness and the operating conditions: the temperature T and the voltage V applied between the cathode and the anode. For example in a $1\,mm$ thick detector, biased to $500\,V$ with the temperature set to 0°C the worst case Gaussian distribution of the charge cloud would be $9.7\,\mu m$. The size of the pixel electrode has to be significantly larger than that of the diffused cloud to minimize the probability of shared events. A powerful tool to optimize a Cd(Zn)Te detector geometry against the charge sharing probability is the analytical model proposed in [32]. Its simplified version [31] states that probability of a charge shared in a detector with the pixel pitch p and the gap between pixels g is described as:

$$P = 1 - \left(\frac{1.1p - 2.3\sigma}{p + g}\right)^2 \qquad 1\text{-}27$$

where σ is the standard deviation of the electron charge cloud distribution as it reaches the anode calculated for the worst case of interaction near the detector's cathode surface. In [31] the model has been compared with experimental results for a CdTe detector with pixel pitch of $625\,\mu m$. The rate of shared events estimated by the model is between 9 % and 11 %, whereas the measurements indicate slightly lower probabilities with rates from 8 % to 10 %. With a reduced pixel pitch the count rate of shared events increases from 10 % at $500\,\mu m$ to 30-40 % at $250\,\mu m$ [35].

For the future X-ray imaging instrument, whose electronic readout is discussed in this thesis, a pixel pitch of $300\,\mu m$ is proposed. A detailed examination should be carried out to confirm the optimal dimensions and operating conditions. The range of X-ray energies and required detector thickness must be considered. Finally the geometry aspects, like: spaces between electrodes, distance to guard-ring and its dimensions, also need optimization. These numerous issues become a subject for extensive studies, not covered in my work.



A) B)

Figure 1.21 The first prototype of the CdTe crystal fabricated (by Acrorad) for the project discussed in this thesis: on the images the detector's anode face is shown. It is a pixelated CdTe arranged in a 4×4 *array with pixel pitch of* $300\ \mu m$*. The structure is surrounded by a guardring.*

The CdTe detector in the future X-ray spectro-imager is expected to be a large matrix of 32×32 or 64×64 pixels. The first CdTe samples with the proposed pitch of $300\ \mu m$ are available for the experimental studies. The dedicated prototype ordered and fabricated (by Acrorad) is illustrated in Figure 1.21. It is a small array of 4×4 pixels with $300\ \mu m$ pitch surrounded by a wide guard-ring. This detector will be used for the performance tests as well as for the technological studies of assembly with the electronic readout ASIC.

1.2.5. State of the art CdTe based instruments for hard X-rays

From the recently developed imaging instruments using CdTe there are few qualified (or being qualified) for hard X-ray experiments in astrophysics. Five of them are summarized in Table 1.4; one is based on a double-sided strip detector, the others on pixelated detectors. The spatial resolution pitch ranges from $250\ \mu m$ to $625\ \mu m$. All these detectors operate at temperatures close to 0 °C. The main common feature is that each instrument uses an ASIC (Application Specific Integrated Circuit) to readout the signal from segmented electrodes.

The Caltech detector has a pixel size of $498\ \mu m$ with crystal thickness of $0.5\ mm$ [39]. Its characteristic feature is a very low power density within the readout ASIC of $0.16\ mW/mm^2$. However, in contrast to other instruments, it needs an external processor for calculation of the photon energy. The Hexitec pixelated detector with $250\ \mu m$ pitch is distinctive for its high number of pixels, 80×80 [36]. The detector uses a single Hexitec ASIC to readout the CdTe matrix. Its application in multiple module (2×2) has been demonstrated [37] with the total detection surface of $16\ mm^2$. A similar hybrid application with a single ASIC coupled to detector is demonstrated in [40]. The pixel size is $270\ \mu m$ in an array of 12×12. The power consumption per ASIC channel, which includes the processing chain, is $0.33\ mW$. The fourth example of the pixelated instruments is the Caliste HD, whose pixels are designed with $625\ \mu m$ pitch, in a 16×16 arrangement [41]. It is distinguished for the high dynamic range up to $1\ MeV$ and the capability to measure photons with energies below $2\ keV$ [45][48]. Consequently it currently offers the lowest detection threshold among the hard X-ray imaging-spectrometer instruments.

1.2. CdTe – a candidate for hard X-ray instrument

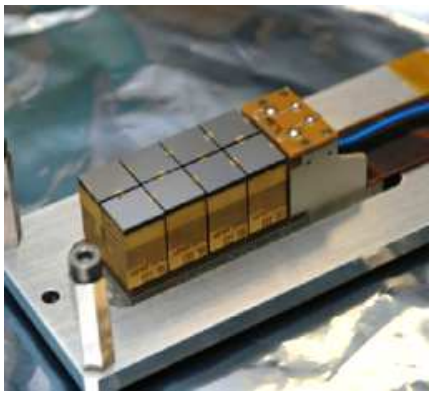


Figure 1.22 MACSI (Modular Assembly of Caliste Spectro-Imager) [44], one of the most recent instruments for X-ray astronomy with $8\ cm^2$ *detection surface and resolution of* 2048 *pixels.*

The Caliste HD has been demonstrated in assembly of multiple modules (2×4) MACSI [43] with the total detection surface of $8\,cm^2$. The MACSI camera is three-sides buttable, which permits construction of focal planes much larger than that. It is illustrated in Figure 1.22.

The four presented pixelated instruments have similar spectral capabilities in terms of FWHM resolution, which ranges between $0.9\ keV$ and $1\ keV$ at $60\ keV$.

	Hexitec [36][37]	**JAXA group [40]**	**Caltech [38][39]**	**Caliste HD [41][42]**	**HXI/ASTRO-H [53][54]**
Pixel/Strip pitch	**$250\ \mu m$** pixel	**$270\ \mu m$** pixel	**$498\ \mu m$** pixel	**$625\ \mu m$** pixel	**$250\ \mu m$** strip
Number of position segments	**80×80**	12×12	$24 \times 44^{*}$	16×16	**128×128**
Number of channels	80×80	12×12	$24 \times 44^{*}$	16×16	**128×2**
CdTe thickness	$1\ mm$	$0.5\ mm$	$0.5\ mm^{*}$	$1\ mm$	$0.75\ mm$
Energy range	$4 - 200\ keV$	$4 - 300\ keV$	$5 - 100\ keV$	**$2\ keV - 1\ MeV$**	$5\ keV - 80\ keV$
FWHM at $59.5\ keV$	$1\ keV$	$0.9\ keV$	$0.9\ keV$	$0.9\ keV$	$1.5\ keV$
Power cons. per channel**	-	$0.33\ mW$	$0.66\ mW$	$0.78\ mW$	$0.5\ mW$
ASIC power density***	-	$1.9\ mW/mm^2$	**$0.16\ mW/mm^2$**	$1.33\ mW/mm^2$	$0.42\ mW/mm^2$
Module elements	**CdTe, ASIC**	**CdTe, ASIC**	CdTe, ASIC, ADC, processor	CdTe, 8 ×ASIC	CdTe, 8 ×ASIC

* 24×44 is the resolution of the HEFT prototype detector, the final CdTe modules placed in the NuSTAR space mission focal plane have resolution of 32×32 each with the pixel size of $0.6\ mm$ [NuSTAR]
** Power cons. per channel is calculated for the whole modules. In case of Caltech - ADC and processor are included.
*** The power density is calculated per ASIC area. In case of Caltech, the ADC and processor are not included.

Table 1.4 Comparison of spectro- imaging instruments for hard X-rays astrophysics experiments, based on CdTe.

Finally there is the HXI strip detector being developed for the ASTRO-H mission [53], whose typical energy resolution is $1.5\ keV$ measured at $60\ keV$, worse than the values reported for the pixelated instruments. This is a consequence of larger electrode segments related to strip detectors. However in this specific application the energy resolution cost is worth the power supply advantage. To read out the detector with position resolution of 128×128 only 256 electronic readout channels are required. Therefore, even with moderate power consumption per electronic readout channel, the

total power needed to readout signals from the complete detector module is significantly lower in comparison to the four pixelated instruments.

Development of a detector system composed of a pixelated CdTe and a low power and low noise readout ASIC has been set as my target in this work. The low power is one of the principal requirements for a space-borne instrument. However the examples presented in Table 1.4 show quantitatively that the energy resolution and the ASIC power consumption are the conflicting parameters. Since by their nature the double-sided strip detectors have worse spectral resolution, the pixelated architecture is preferred and the challenge for the low power consumption is handed over to the electronic readout circuit.

1.3. Challenges for the readout electronics

The best achievable performances of an X-ray imaging instrument are given by the detector type, its geometry and the operating conditions. The actual characteristics however highly rely on the readout circuit. Especially the spectral resolution can be seriously degraded by the electronic noise. Before focusing on the readout precision the principal circuit functions will be first reviewed through retrospection to the detector characteristics (the paragraphs 1.2.2 to 1.2.4). Then, taking as the reference the IDeF-X HD readout ASIC (developed within our microelectronics group in IRFU), I will conclude the goals for the resolution limits in the new CdTe-based imaging instrument, under development.

1.3.1. Desired key features

The pixelated CdTe with $300\ \mu m$ pitch has been selected as the best suited detector for the hard X-ray spectro-imaging instrument. For good charge collection the anode side has the pixelated arrangement. After a photon interaction in the detector the resulting charge induced at the anode side must be detected, localized and measured by the readout electronics. The following features of the circuit are required to carry out this process:

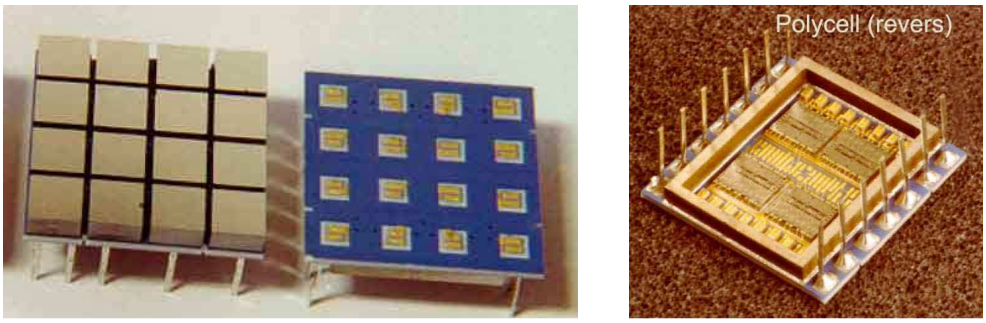
- **Self-trigger with low detection threshold.** The arrival time of an X-ray event is unknown. The electronics circuit has to be able to detect all signals that exceed a minimum value and to send a flag to the external acquisition system upon each event. This minimum detectable charge value, corresponding to certain X-ray energy, is called the low threshold of the readout channel. It sets the bottom of the dynamic range. In order to be able to detect low energy photons and to deal with charge sharing effects, this threshold has to be as low as possible.
- **Multi-channel electronics.** The readout electronics will be connected to anode pixels. Because of numerous electrode segments, the circuit must support readout of individual pixels through independent channels.
- **Position sensing.** The multi-channel readout electronics has to be able to determine which channel(s) has been triggered. A pointer is required (for example a digital register) that provides to the acquisition system the information of which channels experienced an event. The communication should have an accurate timing with delay in a sub-microsecond range. This is important for the acquisition system, for example in case of a double event, to be able to decide whether this is an interaction pattern resulting from a single photon or if this is a pile-up of few independent photons.
- **Charge measurement.** Measurement of the instantaneous charge induced at the electronic channel input is equivalent to the X-ray energy measurement capability. This is because of the linear dependency in CdTe between the photon energy and the amount of charge created within the detector. The dynamic range of arriving photons should be accounted. The required high accuracy of the charge measurement will be further discussed in the paragraph 1.3.4.

- **Anode readout.** The pixelated electrodes, each coupled to an individual electronic channel, are on the anode side of the CdTe crystal. This means that a current pulse of negative polarity (resulting from an instantaneous electron charge) has to be read out. The circuit must be able both to detect and to measure signals of this particular polarity.
- **Low power.** Because of the CdTe demands for operation in a stable temperature and of the limited temperature control capabilities on-board space-borne instruments, the power consumption of the readout electronic circuit must be very low.

From the functionality list above there are two aspects which have the highest impact on the readout electronics concept: the requests for a high number of readout channels combined with low power consumption. This enforces the circuit realization with the integrated technology. Only a custom electronic system implemented in an ASIC (Application Specific Integrated Circuit) can respond to all these requirements for the pixelated CdTe readout.

1.3.2. Trend toward a hybrid detector

There are different methods to realize the electrical connection between ASIC readout channels and the detector electrodes. One of them, that has been used in different projects like the ISGRI polycell [21] for instance and more recently in XRDPIX cell for SVOM ECLAIRs [46], is indirect bonding via a PCB board. Electrodes of the detector and inputs of the ASIC are bonded to a routing board that performs the pitch adaptation. Wire bonding or flip-chip bonding techniques can be used. This kind of hybridization has many advantages since with the pitch-adapter the geometry of the ASIC is virtually independent of the geometry of the detector. One can use an ASIC with the convenient layout of parallel channels without strict constraints on the length and width of each readout channel or on the pitch between them.



A) B)

Figure 1.23 The polycell developed for the ISGRI gamma-ray imager [21] on-board the INTEGRAL satellite. A) the front view with 16 cells of $4 \times 4\ mm^2$ mono-crystal CdTe, dead zone between crystals is $600\ \mu m$ [22], B) the bottom view showing assembly with four readout ASICs through the pitch-adapter [22].

This method is well suited for relatively large mono-pixel detectors, as in the ISGRI polycell shown in Figure 1.23. However it has a major drawback when used for fine-pitch pixelated detectors: the adapter board adds some parasitic capacitances between the ASIC inputs and the electrodes of the detectors. With small electrode size these stray capacitances become dominant, they increase the electronic noise and finally degrade the achievable energy resolution. In the worst case, the final energy resolution is mainly set by the board. The best way to get rid of these parasitic capacitances is

direct bonding between the detector electrodes and the ASIC. Direct bonding to pixelated detector means that the geometry of the ASIC has to be adapted to the detector. The most compact way to realize it would be the stacked technique. In this case the elementary detection unit is an ASIC with a matrix of readout channels directly bump bonded to the pixelated detector, as it is shown in the example in Figure 1.24. As a result the imaging instrument becomes a compact hybrid detector module. This assembly is favorable both for an improved energy resolution due to low input capacitance and for increased spatial resolution, which would be more limited with the wire bonding technique. This interconnection technique is used in pixelated radiation detectors [47], also with semiconductor sensors other than CdTe.

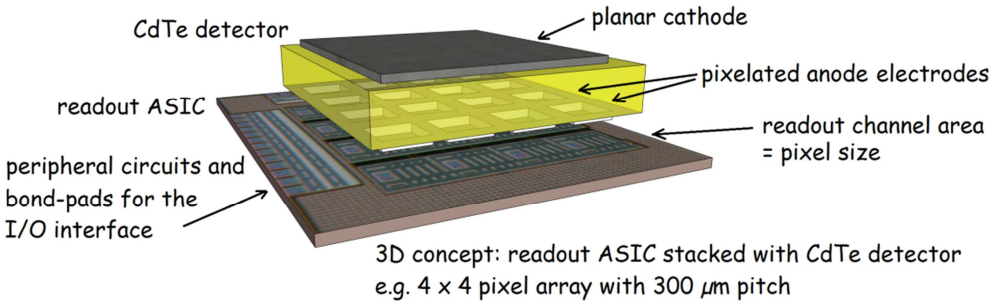


Figure 1.24 Illustration of a hybrid detector. The readout channel input pads (on the ASIC side) and the anode pixels (the CdTe electrodes) are connected through the bump bonding technique. The layout area of a single ASIC channel corresponds to the CdTe pixel size. The top planar electrode is the cathode: this side is exposed to the X-ray radiation.

The assembly through bump bonding method influences the readout electronics design, resulting in additional requests to those previously listed:

- **Channel area equal to pixel area.** The pixelated detector has a fixed pitch between the anode-side electrodes. In the stacked assembly the pitch between bond-pads on the ASIC side must be exactly the same. With a large number of pixels the optimal solution is when the readout channels are also organized in an array, with each channel area corresponding exactly to a single detector pixel.
- **Minimized area of the peripheral circuits.** Except for the active electronics with the readout channel, there are other circuit elements that must be included on the same ASIC. Among them are the I/O pads for the signal interface and for the power supply, general control logic and other peripheral circuits common to all channels. In the ASIC, being a part of a module like the one from Figure 1.24, there is a great interest for the silicon area occupied by all of these peripheral blocks to be as small as possible. The spectro-imaging instruments are often constructed from a set of few identical hybrid modules placed on a common focal plane. This permits to increase the detection surface to large dimensions. In a hybrid module with the ASIC and detector stacked together the peripheral area of the ASIC determines a dead zone region in the focal plane, and thus it should be minimized.

1.3.3. High performance ASIC requested for CdTe readout

The most recent CdTe-based spectro-imaging detector developed at IRFU is the Caliste HD camera [41]. The crystal is divided into 256 pixel electrodes with a $625\ \mu m$ pitch. The pixels are read out by 8 IDeF-X HD ASICs. A single ASIC is equipped with 32 parallel channels, therefore eight ASICs are needed to readout the detector. The Caliste HD assembly is shown in Figure 1.25. The crystal is on the top side of the module. The bottom side of the module is called the electrical body; it is made of 8 PCBs that are glued all together with a dedicated resin. Each PCB contains its own wire bonded ASIC and a few passive devices. The electrical connections between PCBs are done on the four vertical sides of the module, which constitute the external surface of the electrical body, providing the mechanical strength. Finally the bottom side of the electrical module constitutes 16 electrical pins for power supply, control signals and analog readout. The dimensions of Caliste HD module are $1 \times 1 \times 2\ cm^3$. Its four-side buttable design enables construction of a larger focal plane using several identical modules. The demonstration has been made recently with the MACSI camera that uses 8 Caliste modules with a total detection area of $2 \times 8\ cm^2$ [43].

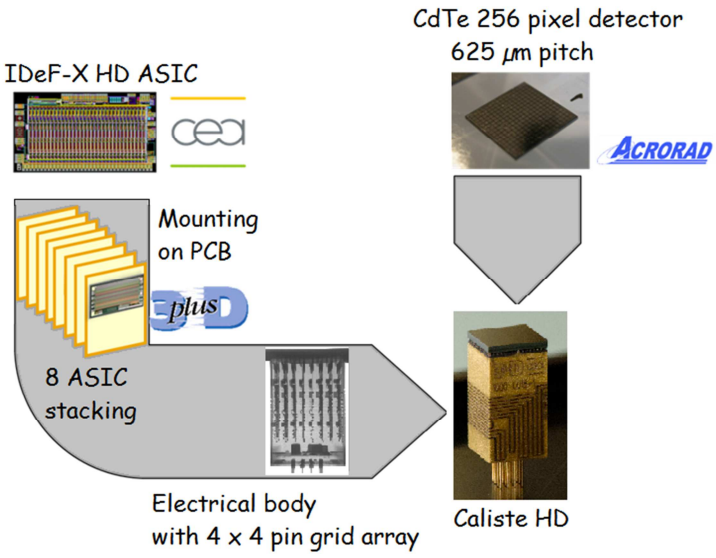


Figure 1.25 Assembly of the Caliste HD module.

The Caliste HD has shown a very good spectral performance with $0.82\ keV$ and $0.92\ keV$ FWHM resolution at 14 keV and $59.5\ keV$ respectively, and $0.73\ keV$ and $0.77\ keV$ FWHM when measured on a single pixel. The second remarkable parameter is the dynamic range with the higher limit adjustable between $250\ keV$ and $1\ MeV$ [41], and with the detection threshold capable to measure photons below $2\ keV$ [45].

The power consumption of a single Caliste HD module is $200\ mW$, i.e. $0.8\ mW/channel$ [41]. It is purposeful to represent it also in terms of power per detector area, since the electrical circuit dissipates heat in the near proximity of the crystal. The value, calculated with $1\ cm^2$ of the total detector area with the total power of $200\ mW$, yields $2\ mW/mm^2$ of CdTe area.

I set the presented performance of the Caliste HD module as the reference for the new ASIC developed for the future spectro-imager based on CdTe with pixel pitch of $300\ \mu m$. The intention for

the new detector module is to realize the assembly through a direct bump-bonding between the detector and the ASIC. The smaller pixel size and the different bonding method, with comparison to the Caliste HD module, should result in a lower total capacitance at the input of the ASIC channel. There is a direct relation between the input capacitance and the electronic noise and the power consumption, which is discussed in the paragraph 1.3.4 and more widely in the following chapters. Consequently the reduction of the total input capacitance can be seen as a noise "reserve" that may be used for energy resolution improvement and/or power consumption reduction. The power consumption should be regarded in terms of the dissipated power per unit area of the detector, since the main reason of designing a low power ASIC is to avoid excessive heating of the temperature-controlled CdTe. In this view, the density of $2\ mW/mm^2$ in the Caliste HD module can be translated to $0.18\ mW/channel$ in the new hybrid detector, whose channel area (equals to pixel area) is $300 \times 300\ \mu m^2$. This boundary becomes my objective for the upper limit power consumption in the new readout ASIC discussed in this work.

1.3.4. Reaching the resolution limits

The best energy resolution measured with CdTe that has been reported with the IDeF-X HD ASIC [41] is $0.77\ keV$ at $59.5\ keV$, for a single pixel. The three main noise contributions that degrade this energy resolution are the electronic noise, the noise due to dark current of the detector and the Fano noise. The last one is the only one that cannot be decreased with the operating conditions or reduced through electronic processing. Let's take a closer look on the Fano interaction statistics.

1.3.4.1. Fano limit

Fano noise, as has already been clarified in the paragraph 1.2.2, is related to the interaction statistics. Photons of identical energy absorbed in the detector result in a number N of free charge carriers. The number fluctuates from one occurrence to another. The fluctuations depend on the type of detector material and on the energy of the photon. They are described using the Fano Factor F and are reflected on the FWHM resolution as [15]:

$$FWHM_N = 2.35 \cdot \sqrt{F \cdot E \cdot w} \qquad 1\text{-}28$$

The resolution varies with the X-ray energy, and the accuracy of the photon energy measurement cannot be any lower than indicated by the expression. The FWHM value due to Fano noise is traced in Figure 1.26 as a function of the photon energy. This plot is the holy grail of the ASIC designer: it is the resolution achievable with an ideal un-noisy electronics connected to a CdTe detector with dark current equal to zero. According to these theoretical calculations, the minimum absolute resolution at $59.5\ keV$ is $0.47\ keV$ FWHM. This value is significantly smaller than measurement accuracies obtainable in today's applications (demonstrated in Table 1.4 in the paragraph 1.2.5).

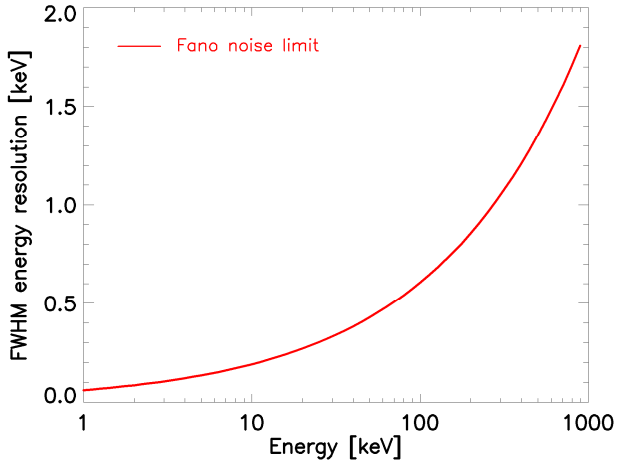


Figure 1.26 Limit of the energy resolution: $FWHM_N$ due to the Fano interaction statistics as a function of the X-ray energy.

1.3.4.2. Equivalent noise charge

The readout electronics is often characterized at first without the detector. Especially its gain A and the intrinsic noise $\overline{v_{n\,rms}}$ are measured under different operating conditions. From this characterization the circuit's intrinsic resolution of energy measurement $FWHM_E$ is obtained. This value, together with the theoretical Fano resolution $FWHM_N$, provide an estimate of the overall energy resolution, $FWHM_{total}$:

$$FWHM_{total} = \sqrt{FWHM_N + FWHM_E} \qquad 1\text{-}29$$

In the characterization process a charge of a known value Q_{in} is injected instantaneously at the readout channel input. Typically it is realized as an input voltage step from a waveform generator applied on an injection capacitance C_{inj}. The input instantaneous charge Q_{in} would result in the mean voltage V_{out} at the electronic channel output. Consequently the channel gain can be calculated:

$$A = \frac{V_{out}}{Q_{in}} \qquad 1\text{-}30$$

The electronic noise is measured at the channel output, as the root mean square voltage fluctuations at the output $\overline{v_{n\,rms}}$. A particular value of the input charge Q_{inx} can be found, such that the resulting output voltage V_{outx} would equal $\overline{v_{n\,rms}}$. We say that this input charge Q_{inx} is the Equivalent Noise Charge (ENC). Using the known gain value it can be expressed as:

$$ENC = Q_{inx} = \frac{\overline{v_{n\,rms}}}{A} \qquad 1\text{-}31$$

where $\overline{v_{n\,rms}}$ is the root mean square noise measured on the channel output and A is the measured channel gain. It should be noted that for good precision in the ENC determination the injected charge Q_{in} used for gain measurement is typically much higher than the calculated ENC (that is Q_{inx}).

The ENC is typically given in the units of $electrons\ rms$. In the language of detector electronics ENC is a more habitual manner of expressing the noise than FWHM. The relation between ENC and the resolution of the pure electronics channel $FWHM_E$ (without the detector) is:

$$FWHM_E = 2.35 \cdot ENC \cdot w \qquad 1\text{-}32$$

where w is the ionization energy of the envisioned detector, which is $4.42\ eV/e^{-}h^{+}\ pair$ in the CdTe. However using the analogy with the equation *1-32*, also an equivalent noise charge ENC_N corresponding to the Fano resolution $FWHM_N$ can be obtained:

$$ENC_N = \frac{FWHM_N}{2.35 \cdot w} \qquad 1\text{-}33$$

The total energy resolution of the detection chain including noise contributions of the detector and the electronic readout channel can be expressed either in ENC using the following formula:

$$ENC_{total} = \sqrt{ENC_N + ENC} \qquad 1\text{-}34$$

where ENC_N represents the effects of the Fano fluctuations in carriers number and ENC is the contribution of the purely electronic noise[3].

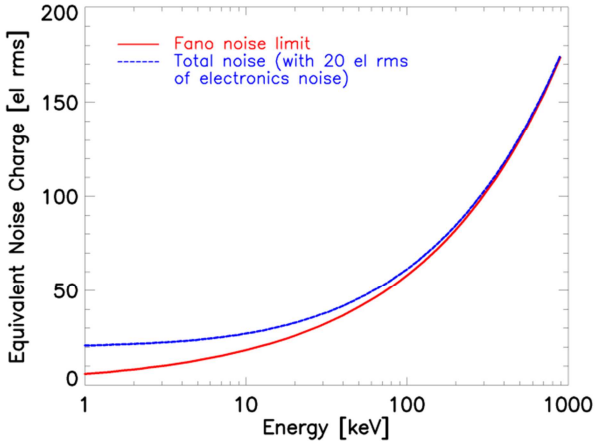


Figure 1.27 Energy resolution expressed in the Equivalent Noise Charge (ENC) plotted as a function of photon energy. The Fano resolution limit (the same as in Figure 1.26 but converted to ENC units) is compared to system contaminated with the electronic noise of $20\ el\ rms$*. The value is low enough to become negligible above energies of few tens of keV.*

We can assume that the electronic noise (not alike Fano noise) is independent on the photon energy, which is often the case in the real circuits. According to the given equations (*1-29* and *1-34*) describing the total noise, the electronics contribution should be much lower than the Fano limit to become negligible. This would be an ideal situation in a Fano-limited system. In Figure 1.27 the Fano resolution limit, now expressed in terms of ENC, is shown as a function of the X-ray energy. On the same chart the total noise of a system with CdTe detector and the electronic readout is plotted, where an electronic noise of $20\ el\ rms$ is assumed. This electronic noise level has been chosen to show that, next to the Fano noise, its contribution is significant only in the lower energy range. Already at $60\ keV$ the energy resolution equals $48\ el\ rms$ (the equivalent of $500\ eV$ FWHM at this energy) and the total system noise is dominated by the Fano effect. At higher energies this hypothetical system becomes Fano-limited.

The Caliste HD module, introduced in the paragraph 1.3.3, is limited by the electronic noise. This noise originating from its readout ASIC, the IDeF-X HD, is highly dependent on the input capacitance.

[3] Unless otherwise mentioned in the rest of the text the term ENC (with no index) will be reserved to describe the electronics noise only.

An experiment has recently been made, where a modification was introduced on a single IDeF-X HD ASIC to minimize the input capacitance (without modifying the readout circuit parameters and the noise sensitivity to the input capacitance). Then its electronic noise has been measured in the absence of the detector. The ENC results are shown in Figure 1.28, plotted as a function of the ASIC internal peaking time, related to the signal processing time. The lowest measured ENC is below $18\ electrons\ rms$. The measurements of the same ASIC connected to a detector would certainly result in a higher value because of the additional detector and stray capacitance and because of shot noise related to dark current. Nevertheless it is an interesting task, to perform a spectroscopic measurement of the modified IDeF-X HD with a CdTe detector.

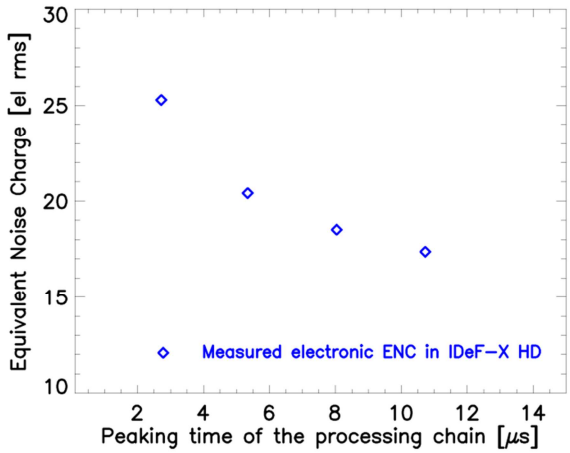


Figure 1.28 Equivalent noise charge measured with the IDeF-X HD ASIC (the same as in the Caliste HD module from Figure 1.25) as a function of the processing chain peaking time. The measurement was obtained at conditions of no detector connected, with no dark current and with the total internal input capacitance in the order of 1 to 2 pF. The minimum ENC for the long peaking time is $17\ electrons\ rms$.

The X-ray astronomy would be delighted having a complete imaging-spectrometer instrument available, which offers spectral performance limited by the Fano noise. However the readout circuit is highly challenged to meet this goal. The noise level in the order of $20\ el\ rms$ (with detector) is difficult to meet, which is evident when looking at the parameters of the existing instruments (shown in Table 1.4, paragraph 1.2.5). To achieve it a very low input capacitance and low dark current are must-have. These are the input parameters imposed mainly by the detector. In this work I will study a possibility of designing a Fano-limited instrument with the chosen CdTe pixelated detector with $300\ \mu m$ pitch and the stacked assembly. However apart from the input capacitance and the detector dark current, there are also other factors located within the ASIC which have a great influence on the energy resolution. One of them, and maybe the most important in this multi-channel imaging-spectrometer application, is the power consumption.

1.3.4.3. In the balance: noise and power consumption

There is a compromise between the energy resolution and the current supplying the active circuit. The electronic thermal noise $\overline{v_{n\,rms}}$ can be decreased with a higher current through the amplifying stages, which typically scales with the proportion [55]:

$$\overline{v_{n\,rms}} \sim \frac{1}{\sqrt{I}} \qquad 1\text{-}35$$

However the increase in current also influences the dissipated power P with the linear relation:

$$P = I \cdot U \qquad 1\text{-}36$$

The flexibility to decrease the supply voltage U, so as to balance for the higher current, exists through choice of the IC technology integration scale, new technologies of smaller feature size can operate with lower supply voltages. The intrinsic noise of MOS transistors may vary from one process to another, which makes the technology choice not a simple task.

The upper power limits of $0.18\ mW/channel$, set by the existing reference detector module Caliste HD, can be exploited to reach the lowest noise by choosing the IC process and studying the current budget against noise at the circuit block-level. The technology considerations, and why the XFAB $0.18\ \mu m$ has been finally chosen, will be discussed in Chapter III and Chapter IV, where the ASICs designed in the frame of this work are described.

1.3.5. Radiation hardness

The X-ray instrument has to be qualified for operation in the space environment. There are two major aspects that are a threat to its functionality: the mechanical stresses during the satellite launch and the continuous exposure to high-energy radiation in the space environment. Integrated circuits are especially sensitive to the ionizing radiation. Not all of the ionizing radiation is absorbed by the CdTe crystal which shields the electronics by one side only. Especially gamma-rays and cosmic ray protons with higher penetrating capabilities can reach the electronics, either passing through the detector or through the shield surrounding the instrument. This has consequences in additional requirements for the readout electronics, which have not been discussed yet. To achieve high robustness the potential dangers have to be considered possibly early in the development stage. The negative effects of the ionizing radiation on the electronics performance can either be suppressed or the unavoidable successive damages can be stretched in time. Consequently the circuit becomes radiation-hard. The major radiation effects and their prevention methods are detailed below.

Total ionizing dose (TID) effects

Continuous radiation cumulated into a significant dose leads to damage of the oxide layer of MOS transistors. As a result, a modification of the transistor parameters is observed with time. The possible consequences include the increase in the noise level and the disruption of the circuit functionality. The technology choice and radiation-hard layout techniques are the principal factors through which the TID effects can be reduced. Modern technologies with smaller feature size show reduced effects of the ionizing dose with time [49]. The enclosed transistor geometry further improves the radiation hardness [50].

Single event upset (SEU)

The readout electronics might experience single events due to charged particles. A large number of electron-hole pairs generated in the Si bulk results in a short current pulse. If the carriers gather at a sensitive node, it may lead to serious implications. One of them is SEU, where the value of a digital

register is changed, resulting in a soft error. By introducing in the design redundant registers the fault can be detected and possibly corrected.

Single event latch-up (SEL)

A more serious problem due to a high-energy ionizing particle is the latch-up. The generated charge pairs moving through the substrate provoke undesired effects. If a parasitic thyristor structure triggers and opens a path for a high current between the circuit supply rails. With the high current intensity the circuit can be damaged immediately, and in the worst case the ASIC can be fully destructed. For this reason SEL belongs to the category of hard errors. Dedicated modifications in the layout of the electronic circuits may increase the immunity to latch-up events. The necessary actions involve primarily a cautious revision of the parasitic resistances.

Circuits designed in the frame of this work are implemented in a $0.18\ \mu m$ technology, new in our IC development team at IRFU. Therefore the first TID and SEL verifications are performed on the standard process. However the functionality of the digital circuitry against SEU is anticipated from the first ASIC prototypes, a dedicated design approach will be detailed in Chapter IV.

The properties of Cadmium Telluride make the II-VI semiconductor the most interesting material for the hard X-ray imaging in space-borne applications. This choice has been made by most of the actors of the field in the world. Our group has a long history in this domain, after INTEGRAL/ISGRI through the recent Caliste development, till today's further work on the advanced CdTe-based sensors together with the associated microelectronics. The latter is the main subject of my research.

To ensure a balance between the energy resolution and the position resolution, the detector has to be organized in a pixelated arrangement. In this development the pixel pitch is set to $300\ \mu m$. I have shown that this size should be close to the optimum, being a compromise between a fine segmentation for the position accuracy and the significant dimensions of the charge cloud causing charge sharing between pixels.

With pixelated detector the readout electronics must support multi-channel readout. A low electronic noise contribution is required for the individual channels. An important factor to improve noise in the fine pitch detector with respect to previous generations is the decreased channel input capacitance and detector dark current. It can be achieved partly through the detector geometry and partly with the stacked assembly. With a small pixel pitch of 300 µm and with a very low electronic noise the energy resolution of the overall instrument could be limited only by the Fano factor of CdTe, resulting in $500\ eV$ FWHM at $60\ keV$. The most serious challenges in the development of the Fano-limited device are the constraints of the ultra-low power consumption (below $0.18\ mW/channel$), the ultra-low noise ($20\ el.rms$ when the detector is connected) and the restricted layout area ($300 \times 300\ \mu m^2/channel$). Understanding the detector properties and careful studies of the processing chain are essential to further proceed in the right directions.

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CHAPTER II

Readout Electronics for CdTe

The very first stage in the radiation detection chain is the sensor, where the charge is induced upon photon interaction. The required electronics processing circuit highly depends on the electrical characteristics of the sensor. In the previous chapter, I have established that the elementary sensing unit is a CdTe pixel of $300 \times 300\ \mu m^2$ size. The sensor can be represented by a very simple electrical model. With knowledge of its characteristics and the experimental data accessible in our experience and scientific resources – its equivalent capacitance and the dark current can be estimated rather precisely. In the first part of this chapter I will propose the relevant detector model that is later used in all circuit simulations.

The output signal of the CdTe pixel resulting from a photon interaction is charge varying with time. However the final readout at the detection chain output is done in the more convenient: voltage domain. In case of CdTe, as for many other capacitive sensors, the conversion from charge domain to voltage domain is realized with the charge sensitive amplifier (CSA). Unfortunately and inevitably the operation is accompanied by addition of electrical noise. I will show that the noise power highly depends on the detector and the stray capacitances as well as on the detector dark current. The total noise has to be minimized to provide the best readout accuracy. For this reason the noise filter stage is required in the detection chain.

In this chapter the CSA characteristics are discussed in details. After reviewing the principal noise sources, the noise transfer functions at the CSA output are obtained. At that point, the required properties of the filter stage will become clear: it must be a band-pass filter. In the last part of the chapter I will present the filter types relevant to the radiation signal processing. The filters will be compared through their noise reduction capabilities: their three parameters describing the achievable resolution in the energy measurement.

2.1. CdTe detector characteristics viewed by electronics designer

The target CdTe detector used for the X-rays detection has been identified in Chapter I. To understand its functionality – some physical phenomena occurring inside the crystal had to be considered. I have shown through simple analysis that a pixelated detector with $300\ \mu m$ pitch should offer a sufficient position resolution required by the future X-ray telescopes. The previously discussed physical properties of CdTe together with the established geometry will now serve me again – to model the electrical behaviour of the detector. The accurate model of CdTe applicable in electrical simulations is essential to form the readout circuit concept and to optimize its performance.

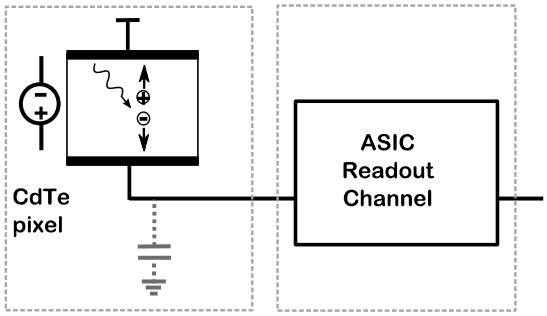


Figure 2.1 Illustration of detector connected to the electronic readout ASIC.

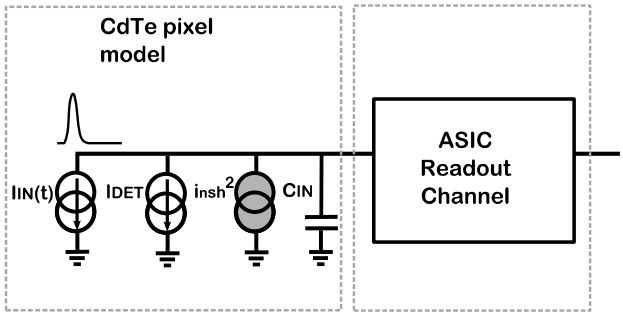


Figure 2.2 Electrical model representing the detector, connected to the readout ASIC. The signal with defined polarity, the dark current and the parasitic capacitance – are all included.

2.1.1. Electrical model of the CdTe

The CdTe crystal, as the radiation detection element in a readout chain, is connected to an input of the ASIC. Figure 2.1 illustrates a single pixel linked with an individual electronic channel. The electrical charge constituting the measured signal is generated within the crystal, induced on the pixel electrode and then processed by the readout ASIC. This entire process can be covered by a purely electrical simulation, if only the detector model, truthfully reflecting the relevant features, is available. The following aspects important in such model need to be considered:

Signal polarity

Through X-ray energy deposition there is free charge generated: electrons and holes in equal number. This signal is induced on the detector electrodes as the carriers' move towards the lower potential inside the crystal. In CdTe the best collection efficiency is achieved when the electrons signal is dominant. As explained in the paragraph 1.2.4: this can be achieved by exploiting the small pixel effect – when the position sensitive segmented electrode is on the anode side. The readout ASIC only has to measure signals induced on these individual pixels. Consequently each single channel connected to positively biased pixel electrode has to deal with signal of the negative polarity. This imposes the current sources orientation "out of the input node" in the detector model from Figure 2.2.

Current signal

The electron-hole pairs, generated at time t_0 by the incident X-ray, are source of the signal of interest. The amount of charge carriers is proportional to the photon energy. As the charge moves across the detector along the electric field Ɛ – a current pulse is being induced on both electrodes. With a detector $0.5\ mm$ thick and biased at $500\ V$, the maximum signal formation time t_{sig} is $50\ ns$ (for electrons) and $625\ ns$ (for holes). These theoretical values are the extremes related to full distance d transit time of electrons and holes respectively:

$$t_{sig\ MAXe} = \frac{d}{\mu_e \cdot Ɛ} \qquad 2\text{-}1$$

$$t_{sig\ MAXh} = \frac{d}{\mu_h \cdot Ɛ} \qquad 2\text{-}2$$

Where d is the detector thickness, μ_e and μ_h are mobility of electrons and holes, and Ɛ is the electrical field across the detector. However the given numbers do not truly reflect the reality, in fact most of the photons interact near the cathode because the detector is illuminated on the cathode side. Thus especially the upper limit is a rarity – in practice with the hard X-ray spectroscopy the signal duration is much shorter: between $10\ ns$ (electron current) and $100\ ns$ (holes current) [33]. Meanwhile a typical signal processing time of the CdTe readout ASIC is in the microseconds range, over one order of magnitude higher than the signal duration. Consequently from the electronics point of view, in most of the cases the signal current pulse can be thought of as a Dirac delta function. In the simulation model a short square current pulse is applied, as illustrated in Figure 2.3. Its duration time t_{sim} is set to a value well below the electron signal to model the case of an ideal detector. The pseudo-ideal charge pulse once integrated over time, gives the total number of the electron-hole pairs equal to Q_{IN}. This value in the model must be the same as the amount of charge induced with a real detector upon an incident X-ray event of an identical energy:

$$Q_{IN} = \int_{0\ ns}^{t_{sig}} I_{IN}(t)\ dt = \int_{0\ ns}^{t_{sim}} I_m\ dt \qquad 2\text{-}3$$

If the readout ASIC has signal processing time comparable to the real signal duration t_{sig}, a ballistic effect occurs. In that case the presented model with signal duration time t_{sim} (shorter than t_{sig}) is no more valid.

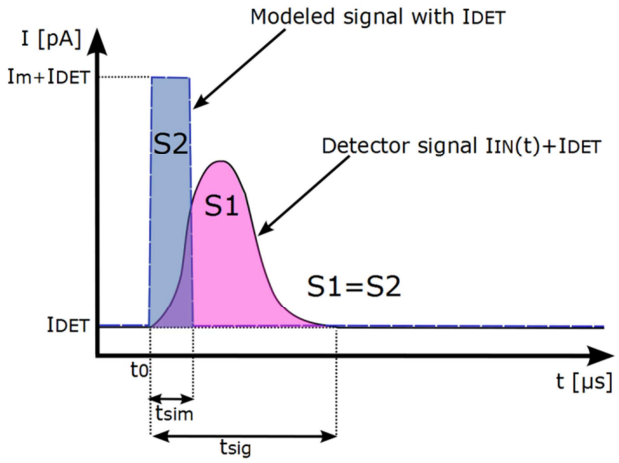


Figure 2.3 Detector charge signal and simulation model; both include the dark current contribution I_{DET}.

Dark current

The thermally generated charge is the second current component in the detector. In contrast to the current due to X-ray induced charge, this signal is present continuously. It has a constant value which depends on the crystal structure, size and operating conditions (bias voltage and temperature). When dark current is taken into account the total detector current signal can be modeled as illustrated in Figure 2.3 – with DC shift equal to I_{DET}. The dark current mean value in a single pixel of $300 \times 300\ \mu m^2$ is estimated in the next section 2.1.2.

Shot noise

The dark current described in terms of its mean value I_{DET} is in fact fluctuating. The variations have form of a white noise, in this particular case known as the shot noise. The spectral power density ${i_{n\,sh}}^2$ of the current noise is proportional to the dark current mean value:

$${i_{n\,sh}}^2 = 2 \cdot q \cdot I_{DET} \qquad 2\text{-}4$$

In the CdTe detector model these fluctuations are modeled as a separate current component with the additional current source ${i_{n\,sh}}^2$, shown in Figure 2.2.

Capacitance

The detector present at the readout channel input represents a capacitance C_{IN}. This input capacitance has an influence on the signal propagating through the readout chain. The effects of additional electronic noise inside the ASIC are magnified through its value C_{IN}. This process will be discussed later in this chapter (in the paragraph 2.2.5). Knowledge of the capacitance value is required in the ASIC development stage to optimize the energy readout accuracy and therefore its presence must be included in the detector model. There are two contributors to the input capacitance reflected in *2-5*: the capacitance of the detector C_{det}, related mainly to the CdTe properties and to the pixel size, and the stray capacitance C_{stray}. The last one includes all the parasitics between the CdTe and the ASIC: bonding as well as the capacitances associated with the metal paths and the silicon bulk (but not directly related to blocks constituting the readout chain, i.e. CSA).

$$C_{IN} = C_{det} + C_{stray} \qquad 2\text{-}5$$

In the section 2.1.3 I will present the estimation of the total value C_{IN} for the specific case: of the $300\ \mu m$ pitch pixelated CdTe.

The complete electrical model of the CdTe detector used in the readout circuit simulations is illustrated in Figure 2.2. It consists of three current sources: the signal of interest $I_{IN}(t)$, the constant dark current I_{DET} and the shot current noise ${i_{n\,sh}}^2$. The orientation of the current sources – "out of the CSA input node" is the result of polarity with the anode readout. In parallel with the current sources there is the input capacitance, which represents the parasitic capacitances of the detector and interconnections. The next step to complete the model is the estimation of the dark current I_{DET} and the input capacitance C_{IN} values.

2.1.2. Expected dark current limits in the small pixel CdTe

In CdTe there are two paths for the dark current between the electrodes: through the crystal bulk and through the side surface of the crystal. The Schottky barrier originating from the semiconductor-electrode junction greatly reduces the bulk current. Meanwhile, with a guard-ring electrode around the pixels collecting the signal, the surface current has a negligible effect on the pixel. Figure 2.4 illustrates an example of a mono-pixel Schottky CdTe [33]: showing how significantly the dark current seen by the pixel electrode can be reduced with the guard-ring structure. The simultaneous measurement of the pixel and the guard-ring electrode currents show that the second one is at least an order of magnitude higher.

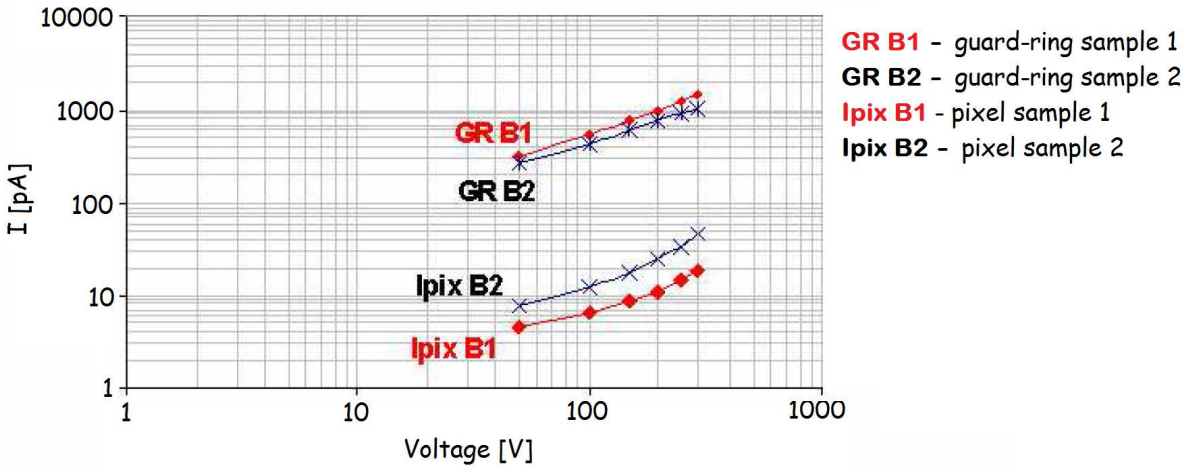


Figure 2.4 Dark current shown as a function of the detector bias voltage obtained at $20℃$*. Two geometrically identical samples are presented: dimensions* $4.1 \times 4.1 \times 0.5\ mm^3$ *with indium electrode on the anode side and platinum electrode on the cathode side: single pixel (*$2 \times 2\ mm^2$*) surrounded by the guard-ring (*$1\ mm$ *wide). Source of the measurements and the figure: [33].*

The CdTe dedicated to the instrument discussed in this work is intended to include both the Schottky blocking contact and the guard-ring structure. Consequently with domination of the bulk current and with the assumption of a uniform current density – the dark current should scale proportionally with the pixel area. To extrapolate the I_{DET} value in the modeled detector with the $300\ \mu m$ pixel, I use the reported dark current levels measured in CdTe with a larger readout electrode size.

Three dark current measurement reports [1][2] and [16] of four different structures have been analyzed. They all include Schottky detectors with or without the guard-ring, with pixel sizes of $1 \times 1\ mm^2$ and $2 \times 2\ mm^2$. The examples cover both the mono-pixel and the pixelated arrangements. The detectors' thicknesses range between $0.5\ mm$ and $1\ mm$. The obtained dark current values are summarized in Table 2.1 with indicated operating conditions. The last column contains my calculations of what would be the dark current in a $300 \times 300\ \mu m^2$ pixel at the operating conditions corresponding to the given measurements. The calculations are obtained assuming a uniform current density. Because of the negligible influence of the surface current in the crystals with the guard-ring structure this calculation should be especially valid in case of the second and the fourth of the presented examples. Consequently the dark current I_{DET} in the small pixel CdTe model from Figure 2.2 would be certainly below $0.5\ pA$ at 0 ℃ with the applied electric field of $200\ V/mm$.

2.1. CdTe detector characteristics viewed by electronics designer

CdTe Description from reference measurements: [1][2] and [16]	Guard-ring	Temp. [°C]	Electric field $[V/mm]$	Dark current $[pA]$	Current estimation in a $300\ \mu m$ pixel $[pA]$
In-CdTe-Pt, $2 \times 2\ mm^2$, mono-pixel, cathode readout [1]	No	-25	300	4	0.1
		25		1000	22.5
		20	200	400	9
In-CdTe-Pt, $2 \times 2\ mm^2$, mono-pixel, anode readout [2]	**Yes**	20	200	**7**	**0.16**
			1000	**20**	**0.45**
In-CdTe-Pt, $1 \times 1\ mm^2$, mean of 8×8 matrix, anode readout [16]	No	-35	200	3	0.27
		0		24	2.16
Al-CdTe-Au, $1 \times 1\ mm^2$, mean of 8×8 matrix, anode readout [16]	**Yes**	-35	200	**0.3**	**0.03**
		0		**4.7**	**0.42**

Table 2.1 Review of dark current performance obtained in CdTe with Schottky blocking contact [1][2][16], with and without guard-ring. Results are shown for different conditions of the operating temperature and electric field. From the current densities in a pixel of known size, the estimated dark current in case of a small pixel $300 \times 300\ \mu m^2$ *is calculated for the corresponding operating conditions.*

However the CdTe simulation model (Figure 2.2) should reflect the worst case value, meaning that the following aspects should be also included:

- Spread in the operating conditions (higher electric field and temperature)
- Dark current increase due to the radiation damage
- Non-uniformity of the crystal
- Surface current between pixels and the guard-ring

Already the example from Figure 2.4 shows, that the dark current could double with a two-fold increase in the bias voltage. Furthermore because of the thermal origins – the bulk current is expected to increase exponentially with the temperature. However the influence of the other factors is more difficult to quantify. Because of that, I have decided to take into account a significant safety margin in the dark current estimation. The value of $5\ pA$ is concluded for the electrical model of the target CdTe. This DC current directly sets also the shot noise power in the model. Therefore it has a direct consequence on the minimum energy resolution calculated for the detector from Figure 2.2.

The last of the listed dark current increase factors requires some more attention. The surface current between pixels and the guard-ring may occur if there is a tiny potential difference between these electrodes. In case of large pixels, where the absolute dark current is much higher – this effect was negligible. The assumption might be no more valid in a small pixel CdTe matrix with very low dark current values. An issue arises whether the surface current between pixels would become dominating. In this case the dark current polarity seen by the pixel cannot be predicted. In the worst case the polarity would be inversed with respect to the model from Figure 2.2. Effectively the current I_{DET} would become negative. The implication for the readout circuit design is that it must support both positive and negative polarities with respect to the DC current originating in the detector (with the unchanged signal polarity).

2.1.3. Expected capacitance of the small pixel CdTe

In Chapter I, the concept of the new X-ray instrument has been proposed: the pixelated CdTe of $300\ \mu m$ pitch stacked with the readout ASIC. Knowing the properties of CdTe detector as well as those of Si that constitutes the ASIC die – the pixel capacitance C_{IN} can be calculated. Let's suppose the following geometry of this hybrid detector module:

- CdTe detector with the pixel pitch of $300\ \mu m$, with $50\ \mu m$ gap between the electrodes and $1\ mm$ crystal thickness.
- An ASIC substrate on $0.5\ mm$ thick Silicon and the metal pad on the Silicon side of $60\ \mu m \times 60\ \mu m$.
- Interconnection between the CdTe pixel and the ASIC pad realized with gold stud bump bonding, where the contact cross-section is $30\ \mu m$ and the height is $200\ \mu m$. The gap between ASIC and CdTe is filled with air.

Because of symmetry of the pixelated detector array, decomposition into two dimensions is possible to simplify the problem. The proposed geometry is illustrated in Figure 2.5. The structure with three pixels has been used to calculate the capacitance of the pixel of interest: the middle one. The other two pixels are necessary to include the neighboring pixels effect. For calculations – the electrostatics equations from the electrical field theory have been used [5]. The CdTe bulk is assumed free of the electric charge, turning the crystal into an ideal dielectric. Therefore the Laplace equation could be applied to calculate the potential distribution Φ:

$$\nabla^2 \Phi = 0 \qquad 2\text{-}6$$

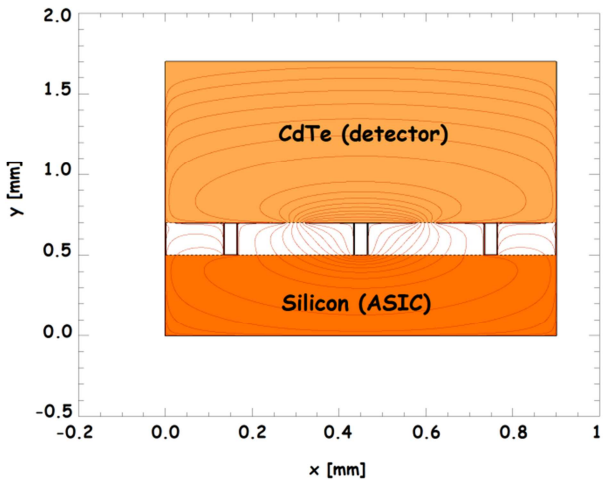


Figure 2.5 Two dimensional hybrid detector structure used for estimation of a single pixel capacitance in a pixelated detector. From the bottom: Si bulk of the ASIC, three parallel gold stud bump connections, the CdTe detector on the top. The detector has three pixels spaced with 300 μm pitch. The model described in [33] has been adapted to this structure to solve the potential distribution, the contours show resulting equipotential lines. The middle pixel electrode is the one of interest in the consequent capacitance calculation, with the estimated value of $145\ fF$.

The calculated potential distribution is the result of the imposed boundary conditions: non-zero potential on the conducting electrodes and $0V$ at the borders (around the whole structure in Figure 2.5). Once the potential distribution is known, the electric field can be calculated:

$$\vec{\mathcal{E}} = -\nabla \Phi \qquad 2\text{-}7$$

The surface electrostatic charge induced on the conducting electrodes is given through the Gauss law:

$$Q = \oint \varepsilon \vec{\mathcal{E}}\, d\vec{S} \qquad 2\text{-}8$$

where ε is the relative permittivity of the dielectric. The last two equations establish the relationship between the charge Q and the potential distribution Φ. The coefficient that links charge on the electrode of interest with the potential – is the capacitance related to this electrode C_{IN}, which has to be found.

Because of the complex geometry with the three different dielectrics involved (CdTe, Si and the air) it would be difficult to find the capacitance C_{IN} through an analytical solution. Instead it has been calculated numerically. For this purpose the tool originally developed within our group and described in [33] has been adapted to the desired geometry to perform the calculation. A regular fine square grid mesh was superimposed on the structure depicted in Figure 2.5. Consequently the finite difference method has been applied to calculate the potential distribution. The equipotential lines in the dielectric volume, resulting from this computation, are traced in Figure 2.5. In the following step the electrical field in this cross-section was determined. Finally the individual contributors to the total capacitance C_{IN} have been calculated. Each is related to the middle pixel through medium of different values of the relative permittivity: cadmium telluride, silicon and the air between them. Their sum is the final outcome of the described procedure: $145\ fF$. This is the total capacitance of the electrode of interest from Figure 2.5. The obtained value includes the principal geometrical properties and the neighboring pixel effects, which should make it a fair approximation of the capacitance C_{IN} – of a single CdTe pixel in an array with $300\ \mu m$ pitch.

Meanwhile a result of experimental capacitance estimation has been found in [6]. In a similar CdTe matrix with $270\ \mu m$ pitch – the capacitance of a single pixel is reported to be approximately $400\ fF$. The value is more than twice higher than the above theoretical calculation for the $300\ \mu m$ pitch. Part of the inconsistency could be due to the difference in the geometrical details: separation between pixels, the gold stud dimensions and size of the on-chip metal pad (on the Si side). More likely however my calculations would underestimate additional on-chip tracks and structures on the ASIC, those that are not related to the actual processing chain (i.e. CSA). Certainly at the capacitance level of a fraction of a picofarad the input node becomes very sensitive and the placement of the metal tracks should be carefully optimized. The large discrepancy between the two compared C_{IN} values (the described calculation and the reported experimental outcome) indicates that it is reasonable to allow for additional capacitance margin. For the described CdTe model of a $300\ \mu m$ pixel, I propose the capacitance range from: 0.3 to $1\ pF$. In the ASIC development process described in Chapter III the readout chain will be optimized for both C_{IN} extrema. Consequently two values for the energy resolutions will be obtained and compared, to understand the risk of the detector capacitance underestimation. This procedure is demonstrated through the Caterpylar test chip development.

2.1.4. Summary of detector parameters in the CdTe electrical model

The electrical model of a single CdTe pixel from a larger array with $300\,\mu m$ pitch has been established. Its purpose is to include the detector parameters in the circuit simulation of the entire readout chain. The most important detector parameters that decide about the spectroscopic performance of the imaging instrument are: the dark current I_{DET} and the capacitance of the readout electrode C_{IN}. Equally important is the fact that these parameters have a functional influence on the readout ASIC. I have determined both parameters' values. Additional margins have been included in the final model, so that the simulations can reflect the worst case resolution of the complete readout chain.

Parameter	Symbol	Value	Comments
Detector dark current	I_{DET}	$< 5pA$	Possibility of inverted polarity
Detector shot noise PSD	${i_n}_{sh}^2$	$< 1.602 \cdot 10^{-30}\ A^2/Hz$	
Detector capacitance	C_{IN}	$0.3\,pF \ldots 1\,pF$	Includes: CdTe pixel and stray capacitance

Table 2.2 Summary of the CdTe detector parameters. The parameters are obtained for the model from Figure 2.2 and provide the electrical representation of a single CdTe pixel from a $300\,\mu m$ matrix used for simulation of the entire radiation detection chain.

The detector model from Figure 2.2 is concluded with a maximum dark current of $5\,pA$ and a capacitance in the range from $0.3\,pF$ to $1\,pF$. In parallel with the known dark current value the worst case shot noise could be estimated. The complete model parameters are summarized in Table 2.2.

2.2. Concept of the readout circuit

2.2.1. Three-element detection chain

The radiation measurement is typically realized in three steps. In the first place the X-ray interaction takes place in the detector. A charge proportional to the photon's energy is generated and induced on the electrodes. Secondly the charge is converted into voltage that is more convenient to process and measure. The operation is realized by the Charge Sensitive Amplifier (CSA). CSA is an amplifier with capacitive feedback that integrates the input charge on the feedback capacitance. This is a common solution for measurement of instantaneous charge. In case of CdTe with a typical depth in the millimeter range and the bias voltage of few hundred volts – the detector signal is a short current pulse with duration of about $10\ ns$ for the electron current and $100\ ns$ for the holes [9]. In response – a voltage step proportional to the total deposited energy is produced at the CSA output.

The CSA voltage signal is accompanied by noise: the shot noise coming from the detector (due to dark current) and the electronic noise added by the CSA Q-V conversion. This degrades the Signal to Noise Ratio (SNR) obtained at the CSA output. To improve the energy measurement precision – the third stage is introduced. It constitutes a filter which reduces the noise bandwidth. In consequence the SNR is better after the filter than at the CSA output. The complete detection chain is shown in Figure 2.6.

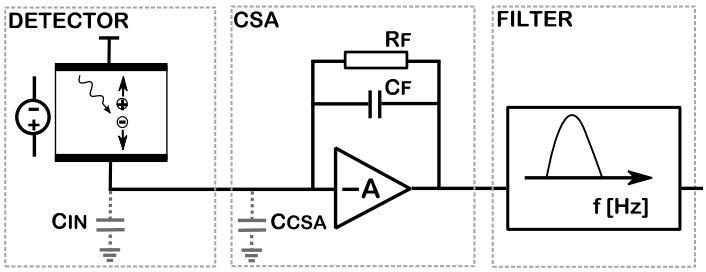


Figure 2.6 Basic radiation detection chain with: detector, CSA and filter. C_{IN} is the external input capacitance including the detector capacitance and all the stray capacitances between the detector and the CSA input. C_{CSA} is the CSA intrinsic input capacitance. C_F is the CSA feedback capacitance ranging from few fF to few pF depending on the dynamic range of the application and the value of C_{IN}. R_F is the CSA equivalent feedback resistance representing a reset circuit with value in $G\Omega$. A is the open loop gain of the inverting amplifier.

2.2.2. Linking physics and electronics: CSA

The charge sensitive amplifier (CSA), also referred to as a preamplifier, converts the charge from the detector to a voltage signal. It provides a bond between two worlds: from the physics of detector interactions to the more empirical engineering domain ruled by higher level electrical description. A low output impedance of the CSA makes it easy to perform energy measurement by monitoring the V_{CSAout} voltage.

2.2.2.1. CSA operation principles

Looking at the circuit in Figure 2.7 let's first consider that the CSA is ideal and has the following properties:

- the open loop gain A is infinite
- the parasitic input capacitances C_{IN} and C_{CSA} are equal to zero
- the bandwidth B_w is unlimited
- the feedback resistance R_F is infinitely high

Furthermore in the following discussion it is assumed that the current signal from the detector is very short and can be approximated by a Dirac delta function.

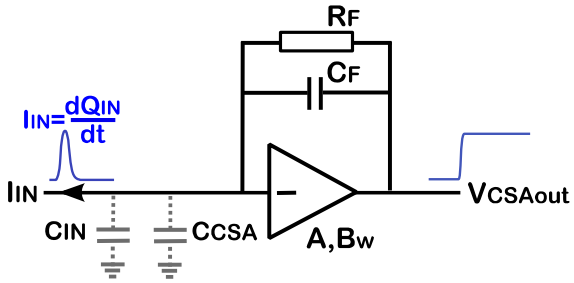
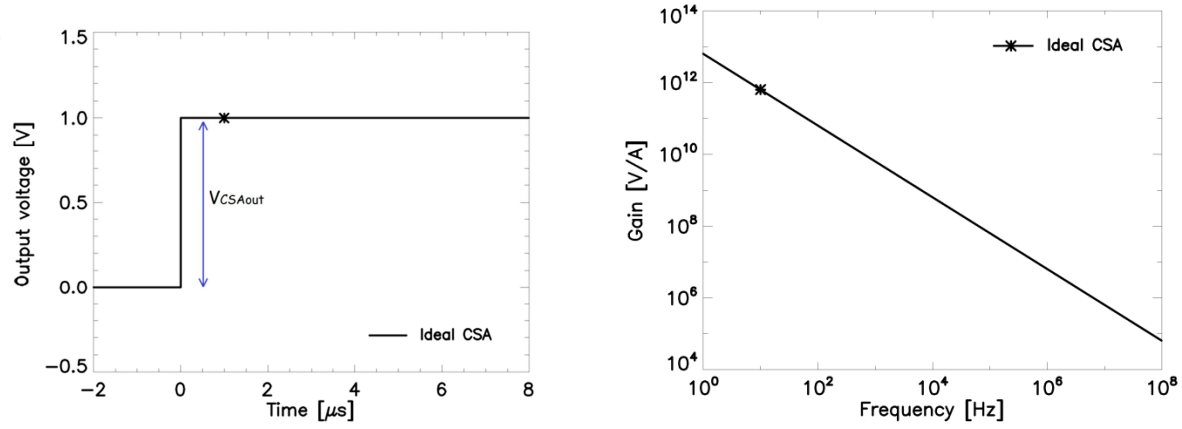


Figure 2.7 Schematic of the charge sensitive amplifier (CSA) with capacitance C_F and resistance R_F in the feedback loop. The inverting amplifier of the CSA is characterized by the open loop gain A and the bandwidth B_w. It converts the current pulse at the input I_{IN} to a voltage step at the output V_{CSAout}. C_{IN} and C_{CSA} are the parasitic input capacitances.

A charge packet Q_{IN} generated in the detector through an X-ray interaction is carried with the input current I_{IN} and has a form of a short current pulse. The current pulse is integrated on the CSA feedback capacitance. As a result, the circuit reacts to the detector current pulse with a voltage step proportional to the energy of the incoming photon. The transient response to the current pulse signal occurring at $t_0 = 0$ is illustrated in Figure 2.8 A). It can be shown that the amplitude of the output voltage step V_{CSAout} is equal to:

$$V_{CSAout} = Q_{IN} \cdot \frac{1}{C_F} \qquad 2\text{-}9$$

C_F is the CSA feedback capacitance and the term $1/C_F$ is known as the closed loop gain of the CSA.



A) B)

Figure 2.8 An ideal CSA with $C_F = 25fF$. A) CSA output transient response to detector current pulse carrying the charge $Q_{IN} = 25\ fC$ at $t = 0\ \mu s$. B) CSA gain (module of the transfer function) shown as a function of frequency.

The equation *2-9* is concluded directly from the frequency characteristics. In the given case, the CSA transfer function, defined as the output voltage to the input current ratio can be written as:

$$H_{CSA}(j\omega) = \frac{V_{CSAout}(j\omega)}{I_{IN}(j\omega)} = \frac{1}{j\omega \cdot C_F} \qquad 2\text{-}10$$

where ω is the angular frequency equal to $2\pi f$. The gain of the transfer function is illustrated in Figure 2.8 B) in the frequency domain.

2.2.3. CSA signal and transfer function: from ideal to real

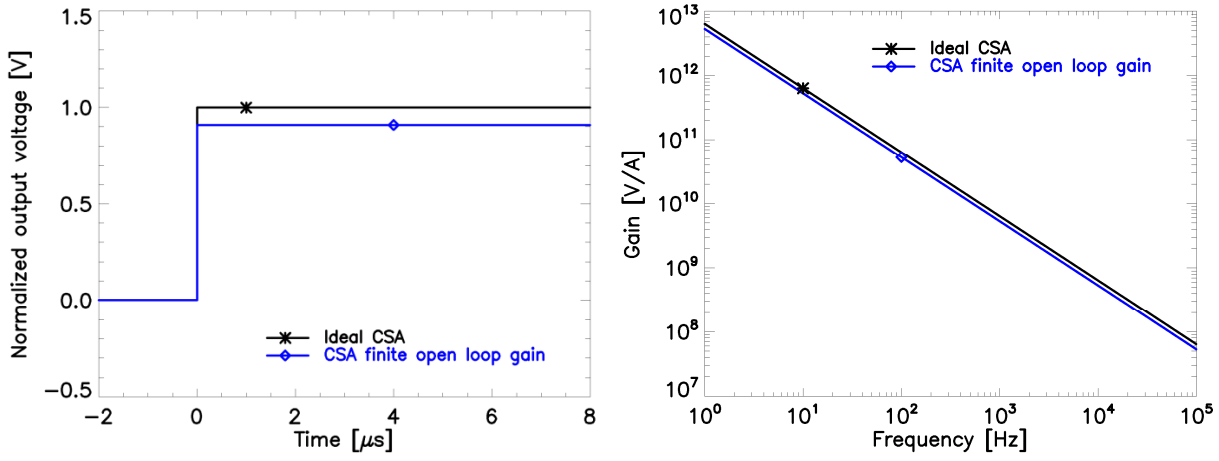
The simplified transfer function of an ideal CSA can be used in many cases. However *2-10* is an approximated expression, which may sometime give misleading results in real circuits. In reality the inverting amplifier in the CSA circuit has a finite open loop gain A and a limited bandwidth B_w. Also the presence of the feedback resistance has an influence on the characteristics. Finally – the non-zero value of the parasitic input capacitances C_{IN} and C_{CSA} also has negative consequences. All these aspects have to be considered individually in order to find an accurate mathematical description of the circuit. Their influence on the frequency and the transient characteristics will be now analyzed by comparison with the ideal CSA.

2.2.3.1. CSA with a finite open loop gain

If the effect of the amplifier's finite open loop gain A is taken into account an additional factor appears in the denominator of the CSA transfer function:

$$H_{CSA}(j\omega) = \frac{1}{j\omega \cdot C_F \cdot (1 + 1/A)} \qquad 2\text{-}11$$

Consequently the closed loop gain decreases by the factor of $(1 + 1/A)$, and the output voltage is expected lower than in the ideal CSA with identical input signal.



A) B)

Figure 2.9 CSA with the finite open loop gain $A = 20\ dB$ vs. ideal CSA, both with $C_F = 25fF$. A) CSA output transient response to detector current pulse carrying the charge Q_{IN} at $t = 0$ μs. B) CSA gain (module of the transfer function) as a function of frequency.

Figure 2.9 shows comparison of the ideal CSA with the CSA that has a finite open loop gain, limited to a poor value of $20\,dB$. The transient response in Figure 2.9 A) demonstrates effective loss of the output signal magnitude due to the low open loop gain. On the transfer function plot Figure 2.9 B) the effect is manifested by the attenuated gain.

The open loop gain in the order of 60 to $80\,dB$ is achievable in today's analog IC technologies of 0.18-$0.35\,\mu m$ with one- or two- stage amplifier. With $80\,dB$ the signal loss equals 0.01%. This value is typically sufficient to neglect the fact of a finite open loop gain in the transfer function.

2.2.3.2. Non-zero CSA input capacitance

In a real CSA – even with a relatively high value of the open loop gain the signal loss still may occur: the effect shown in Figure 2.9 is even further enhanced when the input capacitance is taken into account. Precisely, the parasitic capacitances shown in Figure 2.7: the capacitance of the detector and stray that form together C_{IN}, as well as the input capacitance of the CSA circuit itself C_{CSA}, may become an issue. The consequent loss of gain is explained as follows. The input signal Q_{IN} from the detector is divided between: these parasitic input capacitances C_{IN} and C_{CSA}, and the CSA feedback capacitance C_F:

$$Q_{IN} = \left(Q_{IN\,cap} + Q_{CSA\,cap}\right) + Q_{F\,cap} \qquad 2\text{-}12$$

However only the charge $Q_{F\,cap}$ integrated onto the feedback capacitance takes part in the actual energy measurement. To calculate the charge of interest $Q_{F\,cap}$, the Miller effect will be used. The Miller effect is known from the general theory of feedback amplifiers [55] and allows representation of the feedback impedance as an equivalent input impedance to ground. The effect is illustrated in Figure 2.10. The dynamic capacitance is located in parallel with the physical input capacitance and equals: $C_F \cdot (1 + A)$. Therefore the effective impedance seen by the input signal is:

$$Z_{INsignal} = \frac{1}{j\omega \cdot (C_{IN} + C_{CSA})} + \frac{1}{j\omega \cdot C_F \cdot (1 + A)} \qquad 2\text{-}13$$

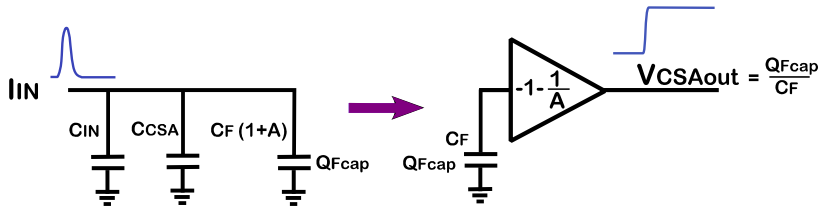


Figure 2.10 A circuit equivalent to the CSA with finite open loop gain and non-zero input capacitance; illustration of the Miller effect. The feedback capacitance is represented on the input as a dynamic capacitance. Only the charge accumulated on the dynamic capacitance participates in the output signal formation.

The expression *2-13* describing the input impedance illustrates the proportion of the capacitive division, experienced by the input signal from the detector. In consequence the effective charge $Q_{F\,cap}$ integrated by the CSA can be predicted from the following equation:

$$Q_{F\,cap} = Q_{IN} \cdot \frac{C_F}{\frac{C_{IN} + C_{CSA}}{1 + A} + C_F} \qquad 2\text{-}14$$

Finally the amplitude of the CSA output voltage can be calculated with the known CSA closed loop gain:

$$V_{CSAout} = \frac{Q_{F\,cap}}{C_F \cdot (1 + 1/A)} \qquad 2\text{-}15$$

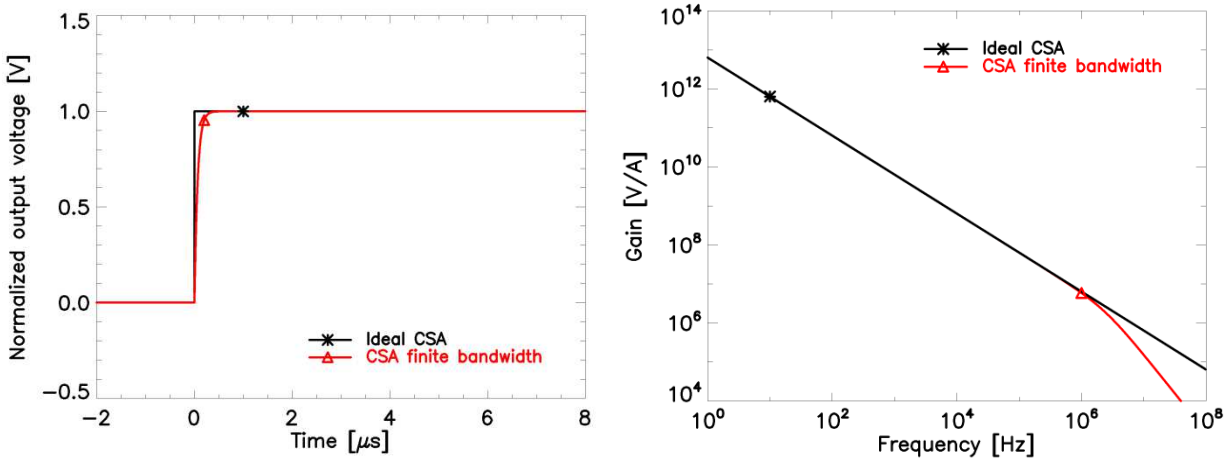
Using the calculated charge $Q_{F\,cap}$ integrated on the feedback capacitance, the CSA output amplitude resulting from the detector input charge Q_{IN} becomes:

$$V_{CSAout} = Q_{IN} \cdot \frac{1}{\frac{(C_{IN} + C_{CSA})}{A} + C_F \cdot (1 + 1/A)} \qquad 2\text{-}16$$

The equation in the given form demonstrates that the increase of the open loop gain A and the minimization of the parasitic capacitances C_{IN} and C_{CSA} are among the most essential criteria in the CSA design. With a sufficiently high open loop gain, the dynamic capacitance is dominant and the signal loss due to the capacitive division becomes negligible. In consequence the input to output signal gain is then controlled only by the feedback capacitance C_F and is insensitive to any variations in the detector capacitance. This is the principal advantage of the CSA circuit: using Miller effect to make the conversion factor independent of the input capacitance.

2.2.3.3. CSA with a finite bandwidth

The next property of the real circuit that influences the transfer function – is the limited bandwidth of the CSA. This is a consequence of the high frequency pole in the internal CSA amplifier, at a frequency B_w. When the effect is considered in the frequency characteristics – the CSA transfer function is described with the equation *2-17*.



A) B)

Figure 2.11 CSA with the finite bandwidth $B_w = 0.1\ MHz$ (and $A = 60\ dB$, $C_{IN} = 1\ pA$) vs. ideal CSA, both with $C_F = 25fF$. A) CSA output transient response to the detector current pulse carrying the charge Q_{IN} at $t = 0$ μs. B) CSA gain (module of the transfer function) as a function of frequency.

$$H_{CSA}(j\omega) = \frac{1}{j\omega \cdot C_F} \cdot \frac{1}{\left(1 + \frac{j\omega}{2\pi \cdot B_w \cdot A \cdot C_F/(C_{IN} + C_F)}\right)} \cdot \frac{1}{(1 + 1/A)} \qquad 2\text{-}17$$

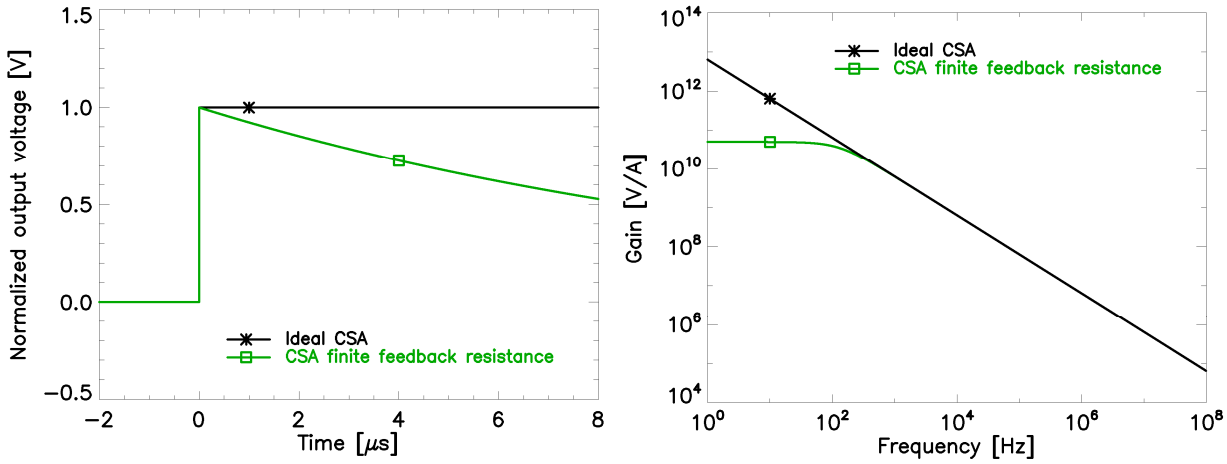
The module of the transfer function with limited bandwidth is shown in Figure 2.11 B). The characteristic roll-off appears at high frequencies above B_w. Its effect in the transient response is

witnessed immediately through comparison to the ideal CSA, demonstrated in Figure 2.11 A). The output signal resulting from the instantaneous input charge Q_{IN} is no more an ideal step, but a smoothed waveform, same as an RC low pass filter step response.

The conclusion from the transient response shape is that an accurate voltage measurement V_{CSAout} can only be taken once the output voltage settles. The definition of the settling time depends on the required precision – typically it takes at least the equivalent of four time constants RC. The shaping time of the successive stage in the signal processing chain should be longer than the CSA settling time.

2.2.3.4. Effect of the finite feedback resistance on the CSA transfer function

In all CSA applications, a CSA reset circuit must be implemented. There are different possible realizations of the reset network. However in most situations it can be symbolically represented with an equivalent resistance R_F in the CSA feedback, as shown in Figure 2.7. The reset circuit has a fundamental importance – after each event (resulting in V_{CSAout} step) it discharges the CSA output to the baseline level and prepares for a new incoming current pulse. As a result the reset circuit prevents the output voltage from saturation.



A) B)

Figure 2.12 CSA with finite reset feedback $R_F = 50\ G\Omega$ and vs. ideal CSA, both with $C_F = 25fF$. A) CSA output transient response to detector current pulse carrying the charge Q_{IN} at $t = 0\ \mu s$. B) CSA gain (module of the transfer function) as a function of frequency.

The finite feedback resistance influences the CSA transfer function and has to be considered. Until now the feedback network was purely capacitive, with the resistance R_F the total feedback impedance Z_F equals:

$$Z_F = R_F \| C_F = \frac{R_F}{1 + j\omega R_F C_F} \qquad 2\text{-}18$$

Therefore the transfer function of CSA with continuous reset is:

$$H_{CSA}(j\omega) = \frac{R_F}{1 + j\omega R_F C_F} \cdot \frac{1}{(1 + 1/A)} \qquad 2\text{-}19$$

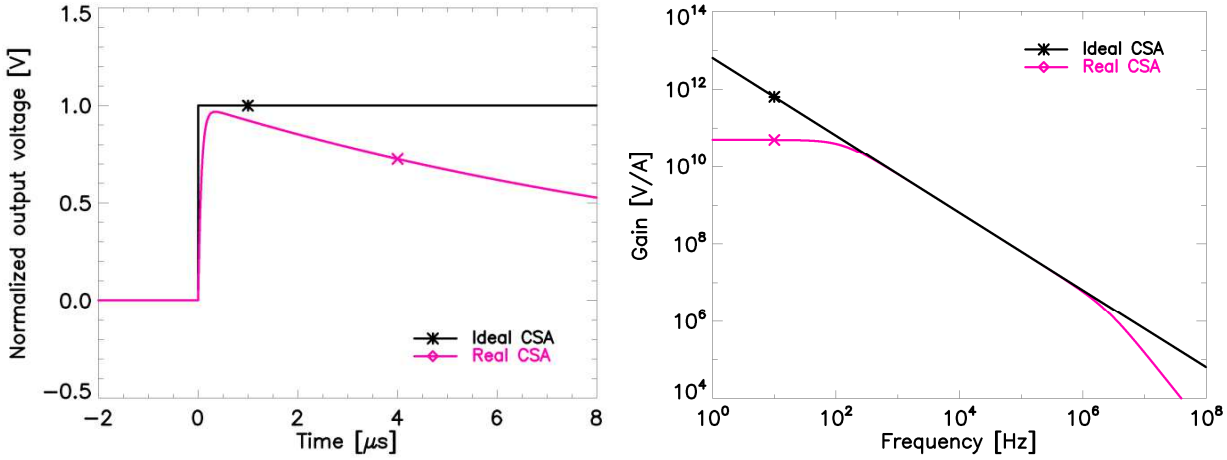
The characteristic feature of this expression is that its value is almost independent of frequency when ω is lower than $1/R_F C_F$. The corresponding frequency-domain gain plot is shown in Figure

2.12 B) illustrating that effect. The result could be compared to the ideal CSA equipped with a high-pass filter at the output, with the time constant $R_F C_F$. The behaviour is confirmed on the transient waveform showing the response to input current pulse in Figure 2.12 A). The plot which would be a step function for an ideal CSA – has now a decaying shape. The signal value is not maintained, but a slow return to baseline takes place. The reset circuit meets the required functionality – to discharge the CSA output voltage, thus avoiding its saturation.

There is however a drawback to it – the voltage amplitude has to be measured rapidly after the event occurrence to avoid loss of information due to decay. In conclusion: the finite feedback reset resistance sets conditions for the next stage – the filter shaping time should be short enough to assure a high precision measurement.

2.2.3.5. Real CSA

Following the above discussion of the real effects on the CSA characteristics – the side-effect of the finite open loop gain is the one that in most cases can be neglected. It is easy enough to ensure a sufficiently high value of the open loop gain in the CSA design. However the upper and the lower frequency limit (caused by: the amplifier bandwidth B_w and the feedback reset respectively) must be taken into account.



A) B)

Figure 2.13 Real CSA with $R_F = 50\ G\Omega$ and $B_w = 0.1\ MHz$ (and $A = 60\ dB$, $C_{IN} = 1\ pA$) vs. ideal CSA, both with $C_F = 25 fF$. A) CSA output transient response to the detector current pulse carrying the charge Q_{IN} at $t = 0\ \mu s$. B) CSA gain (module of the transfer function) as a function of frequency.

Including presence of these three essential effects, the following expression describes the real amplifier transfer function:

$$H_{CSA}(\omega) = \frac{R_F}{(1 + j\omega R_F C_F)} \cdot \frac{1}{\left(1 + \frac{j \cdot \omega}{2\pi \cdot B_w \cdot A \cdot C_F/(C_{IN} + C_F)}\right)} \cdot \frac{1}{(1 + 1/A)} \qquad 2\text{-}20$$

In Figure 2.13 the transfer function of a CSA with a limited bandwidth and a finite feedback resistance is compared with the ideal CSA. In the given example the open loop gain is sufficiently high, making the signal loss negligible. Meanwhile, the signal amplitude is lower than in the ideal CSA case. This is the consequence of two combined transient effects observed on the CSA impulse response:

- Rise time – increasing as the bandwidth limit shifts to lower frequencies
- Decay of the voltage step – faster with smaller feedback resistance

The given CSA limitations can be masked at the output of the complete processing channel (Figure 2.6). This is one of the purposes of the filter stage after the CSA, which gives the final shape to the channel output characteristics.

2.2.4. CSA reset circuit

The necessity for a reset network has already been highlighted with the introduction of the equivalent resistance R_F. The primary reason for this additional component is to avoid the CSA saturation. The output signal of an ideal CSA (with purely capacitive feedback) is a voltage step for each input delta current. Since the output dynamic range in the real world has a finite value, typically of several hundred millivolts, a number of consecutive input X-ray events would cause the signal pile-up on the output voltage – leading to its saturation. The effect is illustrated in Figure 2.14. The primary role of the reset circuit is to discharge the feedback capacitor after each event to keep the output voltage within the dynamic range.

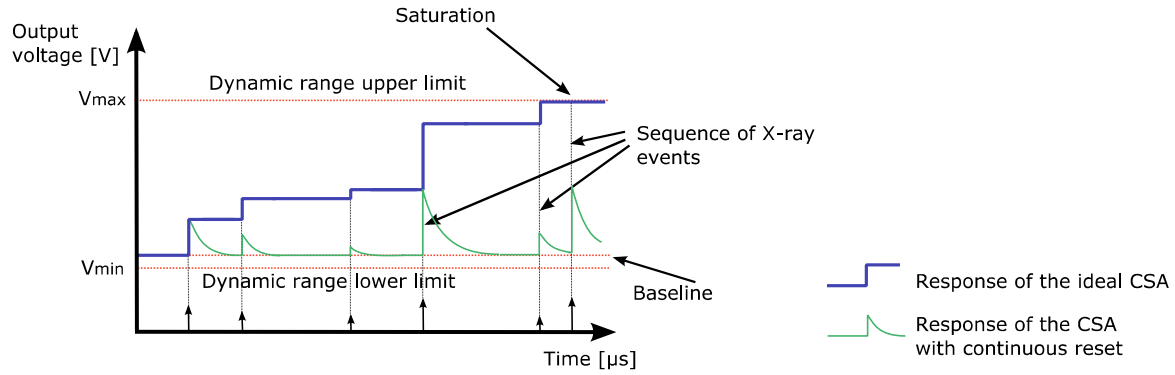


Figure 2.14 CSA output voltage saturation due to pile-up of multiple X-ray events of various energies in the absence of the reset circuit, compared with CSA equipped in continuous reset. In the example the effect of detector dark current I_{DET} is assumed negligible.

However there is another source of current which also leads to CSA saturation, even in the absence of the X-ray induced current pulses. Semiconductor detectors, including CdTe, suffer from dark current. In stable operating conditions this current can be assumed to be constant. In the detector model (Figure 2.2 in paragraph 2.1.1) it is represented by a DC current source I_{DET}.

In the detection chain it is located directly at the CSA input. If there is no DC path for the dark current, it is being successively integrated on the feedback capacitance following the CSA transfer function. In this situation a slope α in the output voltage appears:

$$\alpha = \frac{\delta V_{CSA\ out}}{\delta t} = \frac{I_{DET}}{C_F} \qquad 2\text{-}21$$

The effect is shown in Figure 2.15. The presence of the resistance in the CSA feedback (Figure 2.7) provides path for the continuous dark current. The circuit maintains the DC operating point and in a settled condition, the output voltage remains at a fixed baseline voltage level. With respect to the

illustration in Figure 2.15 the baseline can be set to any voltage value within the dynamic range: between V_{min} and V_{max}.

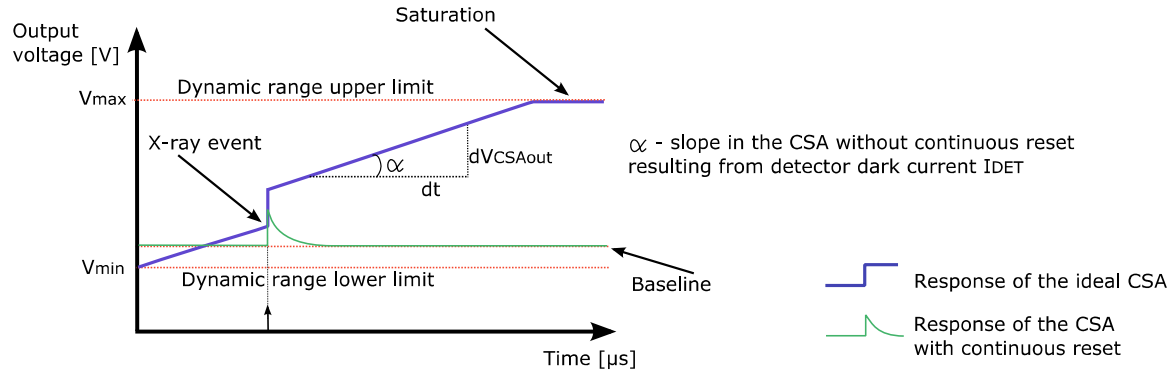


Figure 2.15 CSA output voltage saturation due to the detector dark current I_{DET} in the absence of the reset circuit, compared with CSA equipped with a continuous reset.

Until now the discussed reset circuit was based on the feedback resistance (Figure 2.7). This was meaningful since more complex reset topologies can be typically simplified to this form, very practical in the detection chain analysis. In this section I will review the typically used reset structures, mainly based on active devices.

Many reset approaches have been proposed. The most common networks used in contemporary radiation detection systems are described in [20]. The principal criteria in the reset choice are:

- Noise
- CSA equivalent feedback resistance
- Linearity
- Recovery time
- Layout area
- Power consumption

These parameters will be regarded in order to choose the reset structure for the final radiation detection chain, described in this work.

2.2.4.1. Feedback resistance

The basic reset circuit (already introduced in paragraph 2.2.1) is the passive resistance R_F in the CSA feedback, connected in parallel with the feedback capacitance. The concept is illustrated in Figure 2.16.

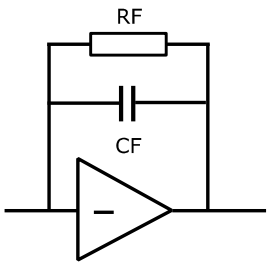


Figure 2.16 CSA with continuous reset – a resistive feedback.

This is a robust and simple solution used to fix the operating point around the feedback loop. The resistance provides a path for the detector dark current and discharges the signal charge integrated on the feedback capacitance. This prevents the CSA output from saturation. The effect of the R_F on the transient characteristics has been demonstrated in Figure 2.12 A) and Figure 2.13 A): after each event the CSA voltage signal decays exponentially back to the baseline. In the practical applications the resistance value R_F must be very large. This constraint comes mainly from the low noise requirement which is extremely tough in the first amplifying stage (CSA). The feedback resistance is a source of thermal current noise, which is equal to [7]:

$$i_{n\,R_F}{}^2 = \frac{4 \cdot k \cdot T}{R_F} \quad [A^2/Hz] \qquad 2\text{-}22$$

In our X-ray readout electronics this thermal noise should be negligible next to the shot noise contribution due the CdTe dark current. Since the dark current has been estimated to be below $5\ pA$ (in 2.1.2), the corresponding worst case shot noise is $1.6 \cdot 10^{-30}\ A^2/Hz$. This imposes, that the feedback resistance should be higher than $10\ G\Omega$. Such a high value of passive resistance is non-realistic to integrate in an ASIC. Consequently other solutions must be considered, which involve active circuits.

The second reason for the R_F resistance to be in the giga-Ohm range in our application is the functional requirement of the continuous reset. It should slowly discharge the feedback capacitance after each X-ray event. The discharge time should be long enough to not coincide with the processing time, which is in the order of ten microseconds. The signal from the radiation detector is usually very weak and must be amplified by the CSA. This is ensured by setting a very low value of the feedback capacitance C_F, in the order of tens of femto-Farads. Consequently a very large feedback reset resistance R_F is required to maintain high value (several tens μs) of the feedback network time constant $R_F C_F$.

2.2.4.2. Feedback MOS transistor

In the integrated circuits the equivalent resistance R_F in the giga-Ohm range can be realized with a MOS transistor [21]. The corresponding realization of MOS as a continuous reset is shown in Figure 2.17 A), with its gate voltage fixed at a constant value. The PMOS transistor is used when the dark current orientation is “out of the input node”, the same polarity is assumed for the signal current. In case of the inverse current polarity the NMOS transistor would be used.

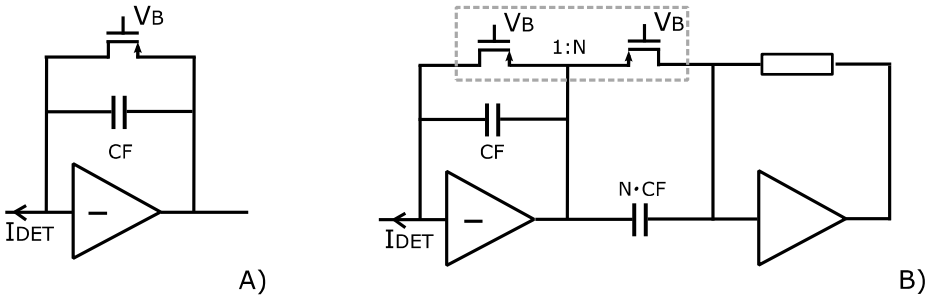


Figure 2.17 A) Reset realized with MOS transistor in the CSA feedback with equivalent resistance R_F. B) CSA with MOS reset followed by Pole-Zero cancellation stage to eliminate the $R_F C_F$ low frequency pole.

In this arrangement the feedback MOS can provide a DC path for the detector dark current by adapting its operating point (through regulation in the negative feedback loop) to achieve a drain

current equal to the dark current I_{DET}. Since the transistor generally operates in subthreshold region, its gate voltage characteristic $V_{GS}(I_D)$ is logarithmic with respect to drain current and the simple transistor reset can thus deal with a wide range of the detector input dark current.

The equivalent resistance R_F of a MOS transistor is dependent on its drain-source voltage V_{DS}. However, as the output signal arrives – the V_{DS} voltage changes dynamically. Thus a problem arises as the equivalent resistance varies with the output signal: nonlinearities appear in the detection chain transfer characteristics. The C_F discharge time depends nonlinearly on the signal level. The nonlinearities can be compensated with a pole zero cancellation stage. However, for it to be effective – the compensating element must be an exact (scaled) copy of the feedback MOS, as shown in Figure 2.17 B), only then the nonlinearities are eliminated [21][22].

2.2.4.3. Low frequency feedback loop

Also a low frequency feedback loop can act as a continuous reset. It can be realized with an OTA, its very low transconductance results in a high equivalent resistance of the circuit [25]. Figure 2.18 A) demonstrates the principle: the OTA sensing input is connected to the CSA output and the output current feeds the CSA input. In a stable condition its value is equal to the detector current. After each event carrying an instantaneous charge – the OTA current feedback discharges the capacitance C_F [26].

Another low frequency feedback implementation is shown in Figure 2.18 B). In this alternative – the output CSA baseline level value can be imposed through the reference voltage [24][27].

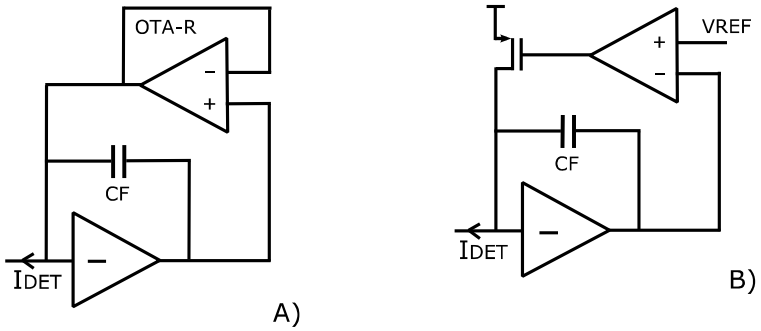


Figure 2.18 A) Low frequency feedback loop with low transconductance unity gain OTA-R. B) Low frequency feedback loop with low transconductance OTA where the CSA output is regulated to a reference level.

In the low frequency feedback reset circuits – the low transconductance value can be reached either by a current-mode division inside the OTA amplifier [26][27] or with an ultra-low bias current of the OTA amplifier [24]. Both of the circuits presented in Figure 2.18 can be represented with an equivalent feedback resistance, simplifying the schematic to the one from Figure 2.16. With this solution – an equivalent resistance highly depends on the bias current in the amplifier within the feedback network. Equivalent resistance of tens to few hundreds of megaohms can be achieved with rather good stability, but value this is not enough for our application. Any higher values can be achieved however R_F would be not stable with operating conditions and with a high dependency on the process spread.

One of the issues in the low frequency feedback loop circuits is the OTA transconductance variation with the process spread, especially when trying to reach higher values of the equivalent resistance. It

makes the PZ cancellation quite difficult to realize for this reset architecture. The second drawback is the additional noise of the OTA, which may become significant.

2.2.4.4. Current conveyor

Current conveyor is another method commonly used to stabilize the CSA operating point and to discharge the feedback capacitance. Its principle lies in scaling down the current that flows through a reference resistance R and feeding it back to the CSA input [30]. The current value changes dynamically upon the variations of the CSA output voltage. The example of a current conveyor circuit in Figure 2.19 is dedicated to system with the detector current oriented out of the CSA input node. An implementation is possible, where the input current is supplied in both directions [29], which allows for a bi-directional operation of the CSA. A pole-zero cancellation that cancels out nonlinearities of the circuit is demonstrated together with the additional stage of Figure 2.19.

In [28] it has been shown that with the current conveyor the equivalent feedback resistance R_F of tens of mega Ohms can be achieved. This makes the architecture more suitable for detectors with rather large charge signals, for example Multi-Wire Proportional Chambers (MWPC). Another constraint of the circuit is the significant noise contributed by the reference resistance R. Due to the associated input referred current noise the solution becomes more appropriate for applications requiring a fast signal processing [31][32]. The relationship between the processing time and the different types of noise is explained in more details in the next subchapter.

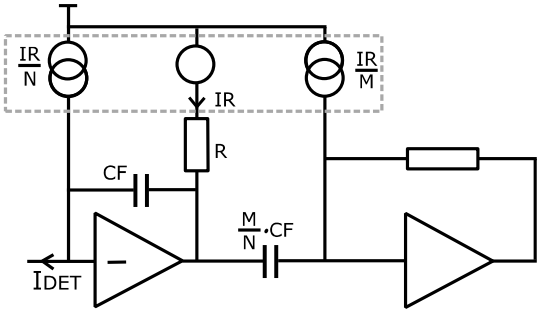


Figure 2.19 Current conveyor in the CSA reset. Additional PZ compensation stage implementation is included.

2.2.4.5. Switched reset

The reset switch from Figure 2.20 A) is a method that provides a fast discharge of the feedback capacitance. It simply shorts the CSA input and output during the reset pulse. With the rapid discharge of the CSA feedback capacitor the PZ compensation is not required. However this solution provides no DC current path for the detector dark current. Consequently the CSA output voltage is burdened with the slope, as shown in Figure 2.15. To avoid saturation the reset operation of closing the switch must be repeated regularly with a period that is directly connected to the detector dark current and the feedback capacitance values. In practice the reset pulse is either requested by a control logic monitoring the CSA level [35], by a logic associated with the event discrimination [33] or by a synchronization signal e.g. in accelerator applications preceding a bunch arrival [34]. With the switched reset there is an uncertainty of the reset level related to the switching noise kT/C. However as this structure is often used with discrete methods, where the DC offset is eliminated, the switching noise is not an issue.

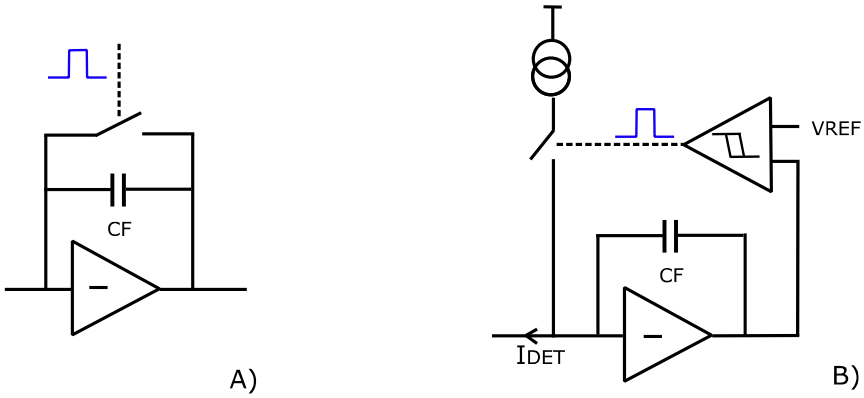


Figure 2.20 A) Switched reset. B) Switched reset – slew rate limited and controlled by a comparator in the feedback loop.

Another possibility for a fast CSA capacitance discharge can be realized in a more controlled manner with a slew rate limit imposed by the current source, as illustrated in Figure 2.20 B). This technique does not provide a DC path for the detector dark current either. When the CSA output voltage rises above the threshold level, set by V_{REF}, the current source is commuted to the CSA input for a certain amount of time to compensate for the charge integrated on C_F. Systems presented in [36][37][39] utilize this principle.

The switched current technique can be mixed with the continuous reset, like in [38] where it is used only for the overload condition due to large signals. Meanwhile upon an average signal charge – the CSA relies on the continuous restoration feedback.

The fact that the compensated charge is quantified with a known discharge current and time is exploited in [40] where a linear measurement of signals that rise above the CSA dynamic range is performed. However with detectors that produce input signals in the order of few femto-Coulombs, like CdTe, a very small reference current with negligible parasitic charge injection would be required. Therefore in CdTe readout circuit it is difficult to dose the compensating input charge to such small portions.

2.2.4.6. SCR – Switched Capacitor Resistance

A switched capacitor could offer a better precision for the controlled charge transfer. The control scheme can be realized with a capacitor commuting charge directly from the CSA output back to input at a fixed frequency, as illustrated in Figure 2.21. Relating to switched capacitor properties this is equivalent to a resistance of a value inversely proportional to the switching frequency [41]. With a switched capacitance C_c and switching frequency f_c the corresponding equivalent feedback resistance is:

$$R_F = \frac{1}{C_C \cdot f_c} \qquad 2\text{-}23$$

This discrete solution once combined with a simple logic, for fast discharge fulfills the requirements for the reset circuit with a path for the leakage current and rapid recovery without requiring a PZ cancellation.

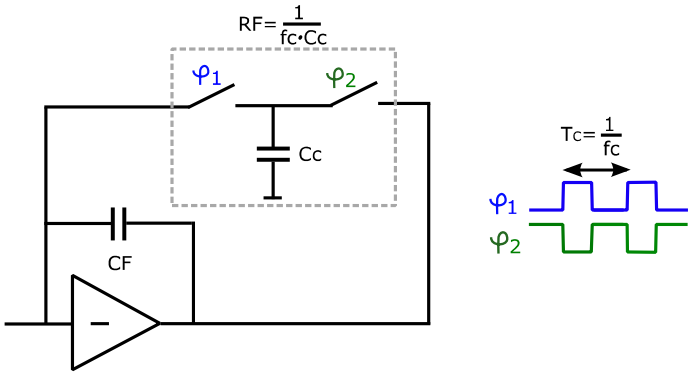


Figure 2.21 Equivalent of feedback resistance realized with Switched Capacitor Resistance (SCR).

It has been demonstrated [42] that with a ladder of switched capacitances an equivalent resistance of up to several tera-ohms can be reached with clock frequency in a reasonable MHz range. However the large value of the equivalent resistance comes at the cost of an increased layout area. The disadvantage of this solution is the switching noise added to the system.

2.2.4.7. Conclusion on reset networks

In Table 2.3 all of the discussed reset circuits are summarized with respect to the major criteria for the CSA block. From the perspective of the low power pixelated CdTe readout, low noise, small layout area and low power consumption are the most important parameters. Considering these requirements – a very good candidate with its simplicity is the continuous MOS feedback reset. It can be realized with a relatively small size single transistor and with almost transparent effect of additional noise and power consumption. In this case the PZ cancellation stage is necessary to provide a good linearity and a short processing time.

Reset circuit	DC path	Noise	Equiv. R_F	Linearity	Recovery time	IC Area	Low power
Feedback resistance	+	+	+	-	-	-	+
Feedback resistance with PZ	+	+	+	+	+	-	-
Continuous MOS feedback	+	+	+	-	-	+	+
Continuous MOS with PZ	+	+	+	+	+	-	-
Low freq. feedback loop	+	+	-	-	-	-	+
Current conveyor	+	-	-	+	+	-	+
Switched reset	-	+	+	+	++	+	+
SCR	+	-	+	+	++	-	-

Table 2.3 Comparison of different reset circuits with respect to main functional properties.

In comparison to analog feedback circuits, switched techniques can offer significantly faster recovery of the output voltage. Due to discrete nature they are preferred in applications with discrete filtering solutions. The switched reset can be realized with a small and power-efficient structure of a MOS switch. Involving only a single-MOS the solution can be viewed as a discrete counterpart of the MOS continuous feedback. Unfortunately in this case there is no DC path for the detector dark current thus a periodic reset signal is required to avoid saturation. The consequent lack of a fixed baseline introduces requirement for an AC coupling to the next stage, in order to read the signal amplitude.

Depending on the reset type, continuous or switched, the filter after CSA (Figure 2.6) is preferred to be either analog or discrete. For a practical choice of the reset circuit the filter techniques need to be analyzed as well. Because the purpose of introducing the filter is to deal with noise – the sources of noise in the readout circuit will be introduced in the following paragraph (2.2.5), next the focus will turn to the filtering techniques.

2.2.5. Presence of noise in the detection chain

The noise effects can be represented in a circuit as equivalent noise sources placed at the detection chain input. Knowing the CSA transfer function – the noise power density at the output of the CSA can be calculated. The resulting power spectrum will finally make it evident: why a filter is required after the CSA.

This paragraph is devoted to the identification of noise sources in the detection chain. In the first place however – an important property of noise is discussed: the noise amplification. This subject is tackled here to demonstrate that with a high enough value of the CSA closed loop gain – any noise present in the filter or a later stage has negligible influence on the measurement precision. Consequently in the later discussion the attention can be focused only on noise related to the detector and the CSA.

2.2.5.1. Noise amplification

The considered electronics readout chain consists of a CSA and a filter (Figure 2.22). The CSA is described by the noise Power Spectral Density (PSD) $i_{nCSA\,IN}(f)^2$ and the transfer function $H_{CSA}(j\omega)$. This noise takes into account the total effect of all CSA-related noise sources and is represented as an input referred current source. The second stage, a filter, is characterized by its input noise PSD $v_{nFILT}(f)^2$ and transfer function $H_{FILT}(j\omega)$. The readout circuit is illustrated in Figure 2.22 A). The output noise PSD of the full chain: the CSA with the filter, is calculated as follows:

$$v_{nOUT}{}^2 = i_{nCSA\,IN}{}^2 \cdot |H_{CSA}(j\omega)|^2 \cdot |H_{FILT}(j\omega)|^2 + v_{nFILT}{}^2 \cdot |H_{FILT}(j\omega)|^2 \qquad 2\text{-}24$$

However the noise of the filter can be also represented as a source related to the channel input, what is shown in Figure 2.22 B). At this location the filter noise effects are reflected by the equivalent input-referred current source $i_{nFILT\,IN}{}^2$. This is simply because of the current-to-voltage conversion realized by the CSA. The current source PSD is expressed as:

$$i_{nFILT\,IN}{}^2 = \frac{v_{nFILT}(f)^2}{|H_{CSA}(j\omega)|^2} \qquad 2\text{-}25$$

The total noise represented in this form based on Figure 2.22 B) permits the evaluation of the noise contribution by each stage in the readout chain. The above equations show that minimizing the input related noise due to filter stage can be achieved by: decreasing the filter noise or by increasing the CSA gain.

2.2. Concept of the readout circuit

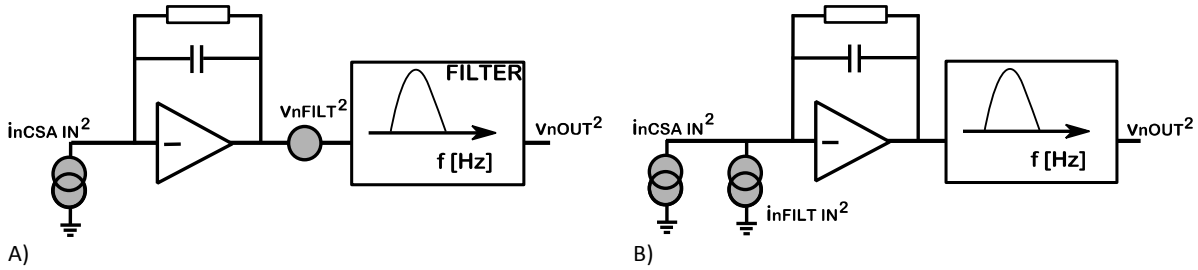


Figure 2.22 Readout chain with CSA and filter with their noise represented as discrete sources. The circuit is used to calculate the total noise on the channel output $v_{nOUT}{}^2$. A) Noise of the CSA $i_{nCSA\,IN}{}^2$ and filter $v_{nFILT}{}^2$ represented at the respective blocks' inputs. B) Noise of the CSA and the filter represented at the chain input: $i_{nCSA\,IN}{}^2$ and $i_{nFILT\,IN}{}^2$. Because of the CSA current to voltage conversion the noise sources located before the CSA are represented as current source. The two schematics are equivalent.

The considerations can be extended to multiple stages. Each following i-th stage noise contribution would be decreased by total gain of all the previous $(i-1)$ stages. Ensuring high gain in the primary stage is beneficial for the overall signal path. In consequence noise of the successive stages becomes less critical [7].

In the design of a detection chain – there is a high interest to increase the CSA closed loop gain. This reduces the proportional noise contribution of all secondary processing stages, resulting in an improved noise resolution. The CSA gain is maximized by decreasing value of the CSA feedback capacitance.

With a proper design of the CSA – the constraints on the filter noise are less severe. A scenario, where filter's contribution to the total noise of the readout chain would be negligible – is then reachable. With this assumption the following discussion will focus on noise sources physically localized before the filter stage: in the CSA and the detector.

2.2.5.2. Noise sources in radiation detection chain

The charge preamplifier and the detector contribute noise of different mechanisms. They include:

- Detector **shot noise** dependent on the detector dark current,
- **Thermal noise** of the electronic circuit, the theory originating in resistor extends also to MOS transistors,
- **Flicker noise** of the electronic circuits,
- **Fano noise** related to detector,
- **kT/C noise**, which is a consequence of the thermal noise theory,
- **Dielectric noise** associated with the physical properties of the substrate where the circuit is located.

All these mechanisms are described below in more detail. Among them, the three dominating sources are those mentioned in the first place: the shot, the thermal and the flicker noise. Throughout this work I will discuss possibilities of minimizing the power spectral density of these sources. There is also the Fano noise, the critical one in the detection system, since its fixed value sets the physical limit of the energy resolution. This mechanism has been introduced in the first chapter, however it is reminded now to provide, together with other noise phenomena, a complete summary of factors influencing the readout precision. The kT/C and the dielectric noise, whose presence is usually less apparent, might substantially degrade the energy measurement

performance. Therefore these two noise contributors also yield my attention. Finally there are few additional noise sources external to the detection chain, which need to be distinguished. These are listed at the end of this paragraph.

2.2.5.3. Detector shot noise

The dark current is a consequence of electrical carriers' thermal generation. It takes place in a semiconductor detector exposed to electrical field. The mean dark current I_{DET} is described as average motion of holes and electrons. However it undergoes random fluctuations known as shot noise related to the discrete nature of electric carriers. Its standard deviation is related to individual flow of each independent carrier. Spectral density of these fluctuations is derived using Campbell's theorem [10]:

$$i_{n\,sh}{}^2 = 2 \cdot q \cdot I_{DET} \qquad 2\text{-}26$$

It is expressed in units of $[A^2/Hz]$. The power spectrum is flat, independent of frequency, meaning that shot current noise is white. Its power can be minimized only through reduction of dark current. This can be achieved by: using a high quality crystal, decreasing the detector area, minimizing the bias voltage or reducing the operating temperature.

2.2.5.4. Detector Fano noise

Random fluctuations in the detector signal charge, resulting from X-ray events of a fixed energy E_i, are known as Fano noise. The variance depends on the energy E_i deposited in the detector and on the pair creation energy w, which in CdTe equals $4.42\ eV$. The standard deviation $q_{n\,in}$ in the charge Q_{IN} deposited at the CSA input is described as [11]:

$$q_{n\,in} = \sqrt{\frac{F \cdot E_i}{w}} \qquad 2\text{-}27$$

The Fano factor F is specific to detector material. In case of CdTe its value is 0.15. The effect of Fano noise on the energy measurement cannot be reduced by any means of electronic filtering. Therefore it sets the accuracy limits in a detection chain.

2.2.5.5. Thermal noise

Thermal noise, also known as Johnson or Nyquist noise, originates from random thermal motion of charge carriers. These random excitations occur in any conductor at temperature T above zero Kelvin and the standard deviation increases linearly with the temperature. It is a white type of noise with flat power spectrum constant with frequency.

Thermal noise in resistor

Power density of thermal noise voltage $v_{n\,th}{}^2$ across a resistance R is described as [12]:

$$v_{n\,th}{}^2 = 4 \cdot k \cdot T \cdot R \qquad 2\text{-}28$$

It is expressed in the units of $[V^2/Hz]$. In the equation, k is the Boltzmann's constant. The noise power can be also referred to the resistor noise current:

$$i_{n\,th}{}^2 = v_{n\,th}{}^2/R^2 \ [A^2/Hz] \qquad 2\text{-}29$$

Thermal noise in MOS transistor

The thermal noise phenomenon occurs also in MOS transistors. For a given operating condition a corresponding equivalent channel resistance can be determined from a known MOS transconductance g_m. Typically the channel thermal noise is described in terms of noise current through the channel. One of the popular models describing the thermal noise mechanism in MOS is given by the expression [13]:

$$i_{n\,th}{}^2 = 4 \cdot k \cdot T \cdot \gamma \cdot g_m \qquad 2\text{-}30$$

The noise effect can be also represented as thermal voltage referred to the transistor gate by following the following relation: $v_{n\,th}{}^2 = i_{n\,th}{}^2/g_m{}^2$. For a transistor in the saturation region the factor γ equals $2/3$. Under varying transistor bias conditions (e.g. decreasing the V_{DS} voltage) the operating region changes from saturation to linear. Consequently the coefficient γ gradually increases to 1. However in the condition of low drain current the transistor enters weak inversion and the factor γ decreases down to $1/2$ [14]. It has to be accounted that the transconductance g_m depends on the operating region, on the drain current and on the transistor geometry. Short transistor channel effects and velocity saturation may strongly influence the thermal noise model [19]. In consequence of the thermal noise complexity, there are several mathematical models which attempt to reflect the phenomena in various conditions.

2.2.5.6. Integrated thermal noise - kT/C noise

A band limited thermal noise integrated over the frequency bandwidth is often referred to as kT/C noise. Even though the source of noise lies in the resistance, it can be shown that the total integrated noise is independent of the resistance. It can be illustrated with the following example: let's consider a resistance R and a capacitance C connected in parallel, as shown in Figure 2.23.

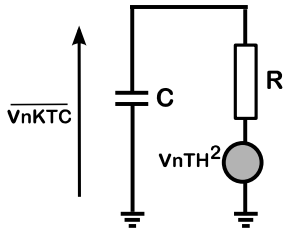


Figure 2.23 Illustration of the integrated kT/C voltage noise measurement, $\overline{v_{nkT/C}}$. It results from the thermal voltage noise $v_{n\,th}(f)^2$. The $\overline{v_{nkT/C}}$ value does not depend on the resistance R.

If the capacitance has a fixed value – the noise power density increases when the resistance increases. However the noise bandwidth proportionally decreases with $1/RC$. In result the resistance has no effect on the integrated noise. The total noise power known as the kT/C noise $\overline{v_{nkT/C}}$ and resulting from the thermal noise $v_{n\,th}{}^2$ of the resistance (Figure 2.23), equals [7]:

$$\overline{v_{nkT/C}}{}^2 = \int_0^\infty v_{n\,f}(f)^2\,df = \frac{kT}{C} \qquad 2\text{-}31$$

This result is valid for any value of the resistance: between zero and infinity. This property is important in switched capacitance circuits, i.e. capacitive sampling cells despite their negligible switch resistance suffer from thermal noise, the noise decreases with higher value of the commuted capacitance.

2.2.5.7. Flicker noise

Flicker noise is a low frequency noise whose power spectrum is a function of $1/f$. It is observed in resistors as well as in active components. In case of integrated circuits it is the MOS transistor where the flicker noise is a real concern. There are two mechanisms which have been identified as its root causes: the density fluctuations and the mobility fluctuations in the MOS channel carriers. Both effects exist within a single device and one or the other may become more dominating depending on the transistor type (PMOS or NMOS) and on the operating region [16]. There are different models that aim to describe $1/f$ noise spectral density with one or the other fluctuation phenomena. There is also a unified model approach that relates origins of both phenomena to charge trapping and de-trapping [15]. The most accurate models used by circuit simulators are summarized in [17]. One that is often referenced describes the channel current noise as:

$$i_{nf}{}^2 = \frac{KF \cdot {I_D}^{AF}}{C_{OX} \cdot W_{eff} \cdot L_{eff} \cdot f} \qquad 2\text{-}32$$

Where KF and AF are parameters related to IC technology and usually extracted by the specific process foundry, C_{OX} is the gate oxide capacitance, I_D is the drain current, W_{eff} and L_{eff} are effective width and length of the transistor.

Making a comparison between the different flicker noise models the main difference is in the denominator where instead of $W_{eff} \cdot L_{eff}$ another geometrical term appears: $W_{eff} \cdot {L_{eff}}^2$ or ${L_{eff}}^2$ or a combination. What all models agree with is that a larger transistor area reduces the flicker noise.

2.2.5.8. Dielectric noise

The dielectric noise has been first measured and described by Radeka [18]. In the detection system it arises from the parasitic input capacitance C_{stray} related either to the package or the mounting substrate. The involved dielectric material is characterized by its impedance:

$$Z_D(j\omega) = \left(G_D(\omega) + j\omega \cdot C_{stray}\right)^{-1} \qquad 2\text{-}33$$

where G_D is the loss conductance and C_{stray} is the capacitance. The conductance is a subject to thermal noise. Its power density is:

$${i_n}^2 = 4 \cdot k \cdot T \cdot G_D(\omega) \qquad 2\text{-}34$$

The dielectric noise current is modeled in parallel with the parasitic stray capacitance. In material datasheets the quality of a dielectric is typically described with the tangent loss. It is known as a ratio of the real and the imaginary part of the impedance:

$$tg(\delta) = \frac{G_D(\omega)}{\omega \cdot C_{stray}} \qquad 2\text{-}35$$

Therefore the dielectric noise is more commonly described in terms of the tangent loss and the capacitance:

$$i_n{}^2 = 4 \cdot k \cdot T \cdot \left(tg(\delta) \cdot \omega \cdot C_{stray}\right) \qquad 2\text{-}36$$

The dielectric noise can be minimized by reducing the stray capacitance and choosing high quality materials with low tangent loss.

2.2.5.9. External noise sources

In low noise applications there are several other possible dangers of interference located outside of the actual detection chain. Parasitic **crosstalk** from one detector pixel to another is one of the common risks. Also within the integrated circuit capacitive **coupling between signal lines** may introduce noise into sensitive nets. Here digital blocks need a special attention. They could inject noise in the common substrate that should normally be an even reference. Finally noise can propagate through power supply connections. The reason might be a **noisy supply** itself or current peaks drawn along the resistive power nets causing **voltage spikes**. A common issue in high speed circuits is the unintended **ground loop**, where AC currents choose a different return path than the one initially assumed.

The possibility of degrading the circuit performance can be minimized by applying design guidelines that include: separation in layout (e.g. sensitive blocks away from digital), prediction of decoupling capacitances, use of isolated devices, use of differential signals for routing and careful shielding.

2.2.6. CSA noise transfer function

The main noise sources present in the detection chain have been identified in 2.2.5. It has been demonstrated that the filter noise contribution can be neglected when the gain of the CSA stage is sufficiently high. Consequently there are the detector and the CSA that are primarily considered as noise suppliers. In the following study, only the three principal noise sources will be considered: the shot, the thermal and the flicker noise.

2.2.6.1. Noise referred to CSA input

Any noise present in the CSA circuit can be referred to its input and represented as a voltage or a current source. The noise power density has such value, that it reflects the actual effects measured on the output. The entire noise, coming from individual transistors and other circuit components, can be contained in the simplified model shown in Figure 2.24. Here all noise sources are allocated within the two symbolic noise sources: voltage noise $v_{nIN}{}^2$ and current noise $i_{nIN}{}^2$. Meanwhile the CSA amplifier represents a noiseless circuit.

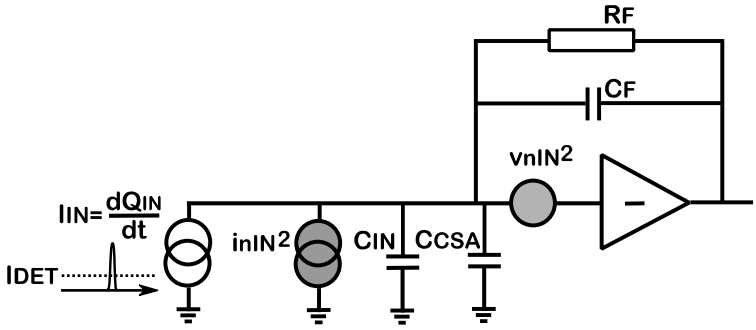


Figure 2.24 A noisy CSA and detector (from the Figure 2.6) represented with an equivalent circuit: noiseless CSA, input capacitances (C_{IN} related to detector and stray and C_{CSA} – the intrinsic input capacitance of the CSA), input current source including the detector signal Q_{IN} and dark current I_{DET}, current noise source ${i_{nIN}}^2$ (due to detector shot noise, noise of the reset resistance and the dielectric noise) and voltage noise source ${v_{nIN}}^2$ due to CSA electronic noise (thermal and flicker).

Input parallel noise

The input current noise source ${i_{nIN}}^2$ from Figure 2.24 is placed in parallel with the CSA input – therefore it is often referred to as the parallel noise. It represents the following contributors:

- detector shot noise
- CSA reset noise related to equivalent feedback resistance R_F (thermal and flicker contributors)
- dielectric noise related to CSA input stray capacitances of the substrate dielectric material

$$ {i_{nIN}}^2 = {i_{nIN\ sh}}^2 + {i_{nIN\ rst}}^2 + {i_{nIN\ dielec}}^2 \qquad 2\text{-}37 $$

In the following discussions only the detector shot noise and reset thermal noise will be considered. Assuming that the reset flicker contribution is insignificant – the noise current ${i_{nIN}}^2$ can be described with a white power spectrum. The dielectric noise will not be taken into account any further. Mainly because of its complex PSD, but also due to its expected negligible influence in the hybrid pixel application with very low stray capacitance.

Input series noise

The voltage source ${v_{nIN}}^2$ at the input of CSA in Figure 2.24 reflects the sum effect of all the internal noise sources in the amplifier. Because of the voltage source location, in series with the amplifier, it is also called – a series noise. Within this source there are two series components distinguished:

- white due to all CSA thermal noise contributors – ${v_{nIN\ th}}^2$
- $1/f$ due to flicker CSA noise contributors – ${v_{nIN\ f}}^2$

$$ {v_{nIN}}^2 = {v_{nIN\ th}}^2 + {v_{nIN\ f}}^2 \qquad 2\text{-}38 $$

They are both related to noise present in MOS transistors inside the CSA.

2.2.6.2. Noise referred to CSA output

Considering the noise source character – there are three dominant CSA noise components that have been identified: white series ${v_{nIN\ th}}^2$, flicker series ${v_{nIN\ f}}^2$ and white parallel ${i_{nIN}}^2$. Each produces a

power spectrum at the CSA output, designated respectively as: ${v_{n\,CSAth}}^2$, ${v_{n\,CSAf}}^2$ and ${v_{n\,CSAp}}^2$. The resultant total output PSD is:

$$ {v_{n\,CSA}}^2 = {v_{n\,CSAp}}^2 + {v_{n\,CSAf}}^2 + {v_{n\,CSAth}}^2 \qquad 2\text{-}39 $$

Effect of parallel noise on CSA output

From Figure 2.24 it follows that the parallel input noise has the same transfer function to CSA output as the detector signal. Consequently it has the contribution to CSA output noise described as:

$$ {v_{nOUTp}}^2 = |H_{CSA}(j\omega)|^2 \cdot i_{nIN}^2 \qquad 2\text{-}40 $$

In case of an ideal CSA the output noise becomes:

$$ {v_{nOUTp}}^2 = \frac{i_{nIN}^2}{(\omega \cdot C_F)^2} \qquad 2\text{-}41 $$

Because the parallel input noise i_{nIN}^2 is white and since the angular frequency ω equals $2\pi f$ – the power spectrum of the output voltage noise ${v_{nOUTp}}^2$ is proportional to $1/f^2$.

Effect of series noise on CSA output

The CSA noise transfer function for the series noise is different from the parallel one. In order to conclude the transfer function of the series noise ${v_{nIN}}^2$ to the CSA output – the input impedance seen by this source will be first determined.

The input impedance seen by the voltage noise source is different than the one seen by the signal. It can be illustrated by first replacing the single-ended input amplifier from Figure 2.24 with an equivalent CSA circuit based on a differential amplifier, as shown in Figure 2.25 A). The same series noise can be represented either on the inverting input or the non-inverting input. The second case, shown in Figure 2.25 B) is more intuitive for the series noise analysis.

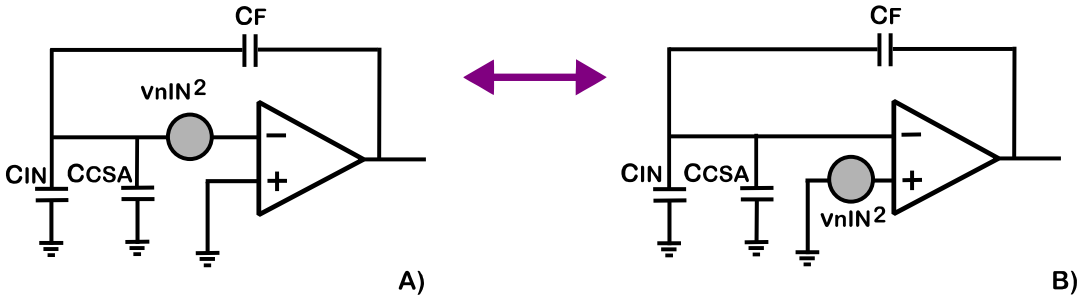


Figure 2.25 Two circuits representing a noiseless CSA with input referred voltage noise source. For the series noise analysis they are equivalent to the single-ended input CSA from Figure 2.24.

Analysis of the schematic from Figure 2.25 B) shows that the CSA input output noise is given by the equation:

$$ {v_{nCSA}}^2 = {v_{nIN}}^2 \cdot \left(\frac{\omega C_{IN} + \omega C_{CSA} + \omega C_F}{\omega C_F}\right)^2 \qquad 2\text{-}42 $$

Since the term $1/\omega C_F$ is the module of the ideal CSA transimpedance, the impedance $Z_{INnoise}$ – the one seen by the input voltage noise ${v_{nIN}}^2$ is:

$$Z_{INnoise} = \frac{1}{\omega \cdot (C_{IN} + C_{CSA} + C_F)} \qquad 2\text{-}43$$

The value has been obtained from the Figure 2.25 A).

Having defined the impedance $Z_{INnoise}$ it is possible now to rewrite the output noise equation in the more general form. The noise PSD at the CSA output resulting from the input referred series **white noise** equals:

$${v_{nCSAth}}^2 = |H_{CSA}(j\omega)|^2 \cdot \frac{{v_{nINth}}^2}{Z_{INnoise}(\omega)^2} \qquad 2\text{-}44$$

Assuming that the CSA is ideal with the transfer function equal to $1/\omega C_F$ the output power spectrum of the voltage noise ${v_{nCSAth}}^2$ is also white and independent of frequency.

Similarly the **flicker noise** contribution is obtained:

$${v_{nCSAf}}^2 = |H_{CSA}(j\omega)| \cdot \frac{{v_{nINf}}^2}{{Z_{INnoise}}^2} \qquad 2\text{-}45$$

With the same assumption of an ideal CSA – the output power spectrum of the voltage noise ${v_{nCSAf}}^2$ has the frequency dependence proportional to $1/f$, analogical to the input referred flicker voltage source ${v_{nINf}}^2$.

2.2.6.3. Noise power spectrum at CSA output

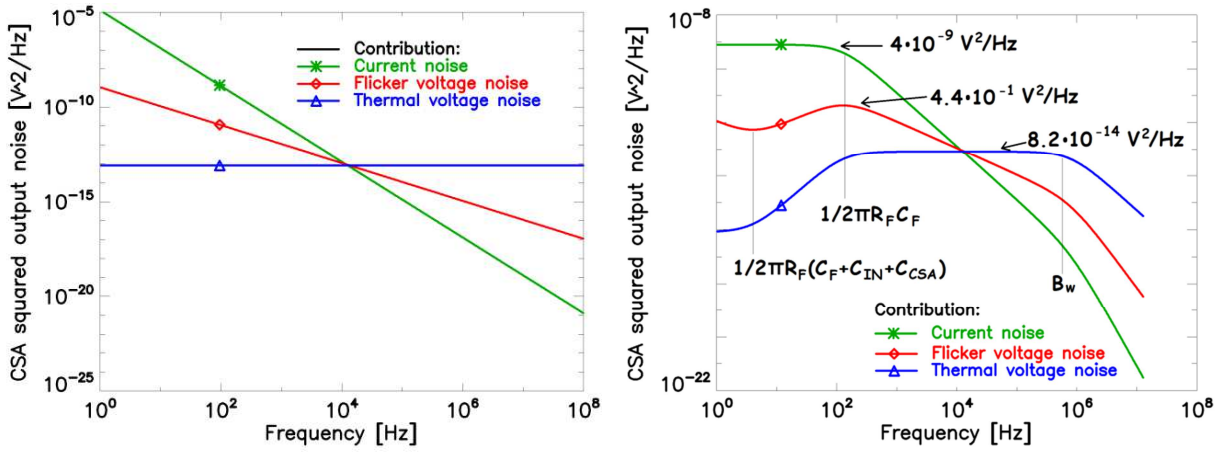
There are three principal noise contributors in the detection chain that have been discussed: the white current noise, the white voltage noise and the flicker voltage noise (Figure 2.24). Their PSD functions at the CSA output have been determined. They have the following properties in the frequency domain:

- Parallel noise ${v_{nCSAp}(f)}^2 \sim 1/f^2$
- Thermal noise ${v_{nCSAth}(f)}^2 = const.$
- Flicker noise ${v_{nCSAf}(f)}^2 \sim 1/f$

Each of the dominating noise sources shows different dependence upon frequency when referred to the CSA output, it is illustrated in Figure 2.26 A). These plots are all obtained assuming the transfer function $H_{CSA}(j\omega)$ of an ideal CSA. The PSD due to series thermal noise still appears as a white noise. The noise power is uniformly distributed along the frequency spectrum. Meanwhile the output referred parallel white noise and the series flicker noise show low frequency distributions, respectively proportional to $1/f^2$ and $1/f$. Most of their noise power is concentrated in low frequencies.

Figure 2.26 B) shows the output noise power spectrum of a real CSA, whose transfer function $H_{CSA}(j\omega)$ includes a finite reset resistance R_F in the feedback network and the limited bandwidth B_w of the amplifier. Both non-idealities find reflection in the CSA output noise power spectrum. The limited bandwidth cuts off the noise power at higher frequencies, like a first order low-pass filter. Meanwhile presence of the reset resistance causes attenuation of the noise power spectrum at low frequencies.

2.2. Concept of the readout circuit



A) B)

Figure 2.26 Output noise PSD due to input referred sources of: white current noise (green), flicker voltage noise (red) and thermal voltage noise (blue). A) The ideal CSA: $B_w = \infty$, $R_F = \infty$. B) The real CSA with limited bandwidth $B_w = 0.8\ MHz$ and with equivalent reset feedback resistance R_F of $50\ G\Omega$. Both results obtained with numerical calculations at the following conditions: $C_F = 25\ fF$, $C_{IN} = 0.3\ pF$, $I_{DET} = 1\ pA$, $C_{CSA} = 0.47\ pF$, ${v_{n\,INth}}^2 = 81\ nV^2/Hz$, ${v_{n\,INf}}^2 = 1.1\ \mu V^2/Hz$.

Knowledge of the total integrated output noise PSD $\overline{{v_{nCSA}}^2}$ is essential to determine the resolution of X-ray energy measurement. Its precision improves with decreasing ENC (Equivalent Noise Charge), introduced in the paragraph 1.3.4, which is defined as:

$$ENC = \frac{\sqrt{\overline{{v_{nCSA}}^2}}}{A_{CSA}} \qquad 2\text{-}46$$

In the ENC equation: $\overline{{v_{nCSA}}^2}$ is the total integrated noise, which is the sum of areas limited by each noise PSD curve ($\overline{{v_{nCSAp}}^2}$, $\overline{{v_{nCSAth}}^2}$ and $\overline{{v_{nCSAf}}^2}$) and A_{CSA} is the measured CSA closed loop gain, which in case of an ideal CSA is equal to $1/C_F$ (see equation *2-9*).

The two effects of the real-CSA demonstrated in Figure 2.26 B) might appear to be desirable: because the total integrated noise $\overline{{v_{nCSA}}^2}$ is lower than in the case of the ideal amplifier from Figure 2.26 A). Unfortunately, these two non-ideal effects can also affect the CSA gain, especially if their associated time constants ($R_F \cdot C_F$ and dominant pole of the amplifier, see Figure 2.13 in 2.2.3) are not split enough. In addition, the reset resistor is an additional source of noise.

The interest of implementing a proper filter stage after the CSA becomes now more evident: well precised frequency characteristics can be formed by the filter design to reduce the total integrated noise measured on the filter output. In case of the current white noise and the voltage flicker noise – the desired effect can be achieved only with a high-pass filter, since most of the noise power is accumulated at lower frequencies. For the thermal noise the attenuation from both high and low frequency side is desired. Consequently a narrow bandpass filter is a good solution to reduce the total noise power. However the filter affects also the second variable in the ENC equation *2-46* – the signal amplitude. To improve the ENC of the processing chain with the filter – it must be ensured that the gain would not reduce linearly with the noise reduction. Consequently the next part of my work will be devoted to the analysis of the filter and optimization of the ENC.

2.3. Noise filtering in the detection chain

The fundamental function of the radiation detection system discussed in this thesis is: discrimination of single photons and measurement of their energy. The minimization of noise with respect to signal, whose measure is the Equivalent Noise Charge (ENC), becomes the major purpose of the filter design. Small value of ENC ensures: potential for low detection threshold and good measurement precision. But there are also additional aspects essential to consider in the filter concept to provide the right functionality. These include: signal amplification, baseline stabilization, dealing with a given pulse rate and avoiding pile-up errors [48][49], not to mention the implementation concerns imposed by the system specification, namely the power consumption and the layout area. Typically the final architecture is a tradeoff between all these criteria guided by the future application.

2.3.1. Diversity of filters

Knowing how critical the resolution of energy measurement is in the system design – the first question that one might ask is: whether there is such a filter that provides an optimum ENC.

2.3.1.1. Optimal filter

From the ENC point of view – there is a known filter type which provides the best energy resolution: the optimal filter, also known as Cusp [51]. It can be derived using the Matched Filter theory. It reveals the best resolution achievable with input parameters imposed by the CSA and the detector: input referred noise and capacitance. In the presentation of the optimal filter (in paragraph 2.3.3), I will demonstrate that an infinite time between the X-ray event interaction and the measurement would be needed to achieve the theoretical lowest ENC limit [51]. This infinite processing time could be reduced to only several time constants without big penalty on the signal to noise ratio. Such variation of the matched filter is called a truncated Cusp.

The signal shape obtained with the Cusp or with the truncated Cusp has a sharp narrow peak. Its profile imposes that the measurement of the pulse peak should be infinitely short [47]. Otherwise one must count with loss of accuracy. The optimal filter weighting function shape of Cusp – self-explains the reason why it is not used in practical applications.

2.3.1.2. Triangular filter and other approximations of cusp

As a result existing detection systems employ alternative filter concepts. Typically they are approximations of the Cusp filter. One that best resembles the Cusp – is the triangular filter [47], whose weighting function has form of a triangle. Despite its good noise filtering properties the ballistic deficit and the measurement accuracy dictate modification to a trapezoidal form with a flattened top [71]. Some other solutions that also balance between the shape resembling Cusp and the flattened top are: semi-Gaussian, Gaussian, piecewise parabolic or sinusoidal lobe [47].

2.3.1.3. Semi-Gaussian filter

Amongst them the most common filter used in radiation signal processing is the semi-Gaussian. Its approximation of triangular filter with smoother peak makes it easier to measure the signal amplitude with a high precision. From the practical point of view – its implementation in analog electronic circuit is very straightforward. It can be constructed with a simple series network of the elementary filters: CR (high-pass) and RC (low-pass) [63]. Consequently it is also known as a $CR-RC^N$ filter, where N denotes the filter order.

2.3.1.4. MCDS filter

Multi Correlated Double Sampling (MCDS) is the third filter discussed in this chapter. In contrast to the previously described – continuous semi-Gaussian filter, MCDS is a discrete processing method. With a limited number of samples taken at the CSA output an approximation of the trapezoidal shape is produced [78]. The minimum number of samples needed to perform noise filtering is 2. In this simplest form the method is known as Correlated Double Sampling (CDS) [78]. Because of its simplicity, this is the most popular variant, especially known in light detection systems [66][80][82]. The MCDS is used not nearly as widely as the semi-Gaussian. However because of its flexibility to adjust the filter parameters, by changing the number of samples and the time interval between them [85][89], I expect it has a good potential for implementation in the radiation detection. Consequently the paragraph 2.3.5 is dedicated to MCDS, where I derive a detailed analysis of MCDS.

2.3.1.5. Time invariant or time varying filters

In search for the optimal "practical" solution a concern that often arises is: a long time constant for the baseline to recover after an event. In the application for astrophysics X-ray observations, discussed in this work, the count rate is very low and pile-up is not likely to be an issue. However there is always a certain probability that the offset of not-completed baseline recovery would cause inaccuracy of the consecutive event measurement, since baseline is the reference level. It is a general concern with most time invariant filters. Special circuit solutions are introduced to overcome this issue, simultaneously turning the processing chain to time varying system [51]. Time variant filters have been first introduced in radiation detection systems (in the form of gated integrators) for their advantage of limited dead time between two events [50]. The time it takes to make a measurement compared to recovery time is shorter than with time invariant filters [51]. This type of filter used in radiation detection incorporates a gating signal that indicates the events to be processed. The gating signal might be an external synchronous trigger or generated internally by means of a pulse discrimination path. Ideally only the X-ray events are selected to be processed, but there are also noise events present in the circuit [50]. These are equivalent to random input current pulses. To ignore them the discriminator threshold is set above the noise level. Consequently the X-ray and random noise events can be divided into two categories:

- events due to X-ray interaction recognized by the gating signal
- noise events ignored by the gating signal

An input current pulse that belongs to the first category with amplitude above the discriminator threshold – produces a known response at the filter output. The event is associated with dedicated

gating signal. The noise events occur very frequently and are always present: before and after the gating signal. The system response to this second category of input pulses: those that do not meet discrimination criteria, depends on their arrival time with respect to the gating signal.

In case of the filter types already mentioned above, it is often possible to realize a particular one in the time invariant or in the time variant version. The difference is mainly in the actual functionality scheme. From the ENC point of view both should give identical results [70]. In the circuit application, it is often one specific realization that is preferred. The semi-Gaussian filter, for example, can be easily realized with a simple analog processing, straightforward for the time invariant implementation. Meanwhile the MCDS filter, processing a limited number of discrete signal samples, strongly suggests implementation as time variant system. The category to which the system belongs: time invariant or time varying, will have influence on the noise analysis method.

2.3.2. Analysis in the frequency or in the time domain

The filter block is also called a pulse shaper. The two interchangeable terms suggest two ways of looking at it: either in the frequency domain or in the time domain. Depending on the analysis method a filter is characterized either by the transfer function $H(j\omega)$ – a function of frequency or by the weighting function $w(\tau)$ – a function of time. I am going to introduce suitable analysis tools for both approaches.

ENC – the parameter used for performance analysis

The signal to noise ratio, widely used in electronic systems of different domains, relates the output noise and the output signal amplitude. Equivalent noise charge (ENC) is a different manner of representing the noise performance, frequently used in radiation detection systems. The parameter has already been introduced in the paragraph 1.3.4, however, as it is the most important one in the filter analysis, it is useful to repeat the definition here. ENC refers the system noise to the channel input and is evaluated as follows:

$$ENC\ [el_{rms}] = \frac{total\ root\ mean\ square\ noise\ at\ the\ channel\ output\ [V_{rms}]}{channel\ gain\ [V/el]} \qquad 2\text{-}47$$

With ENC – noise is quantified in units of root mean square charge, typically in $electrons\ rms$. It translates to a number of electric careers generated in the detector by an incident photon, that would cause the channel output voltage equal to the rms noise value. Resolution of the energy measurement degraded by the electronic noise can be calculated as:

$$E_{FWHM} = 2.35 \cdot E_{\sigma} = 2.35 \cdot ENC \cdot w \qquad 2\text{-}48$$

Where $E_{FWHM}\ [eV]$ is the Full Width at Half Maximum energy resolution, $E_{\sigma}\ [eV]$ is the energy resolution in terms of standard deviation, $w\ [eV]$ is energy of an electron-hole pair creation, which in CdTe equals $4.42\ eV$. Once the electronic ENC contribution is determined (through measurement or calculation) it can be put under the same equation with complex phenomena related to the detector physics, namely the Fano noise. Thus the overall energy measurement resolution at a given energy E_i is obtained:

$$E_{FWHM} = 2.35 \cdot \sqrt{(ENC \cdot w)^2 + F \cdot E_i \cdot w} \qquad 2\text{-}49$$

I will use the ENC term to compare the electronic noise performance of different processing chains. Expressions of noise performance in terms of ENC can be obtained either in the frequency domain or in the time domain..

2.3.2.1. Frequency domain noise analysis

Noise can be analyzed in the frequency domain when a system is Linear and Time Invariant (LTI). Then the knowledge of the chain transfer function and of the input related noise PSD are sufficient to calculate the output noise, and more importantly – the ENC. In analysis of the detection chain from Figure 2.27, the pulse shaper together with the CSA are accounted in the channel transfer function $H(j\omega)$:

$$H(j\omega) = H_{CSA}(j\omega) \cdot H_{FILT}(j\omega) \qquad 2\text{-}50$$

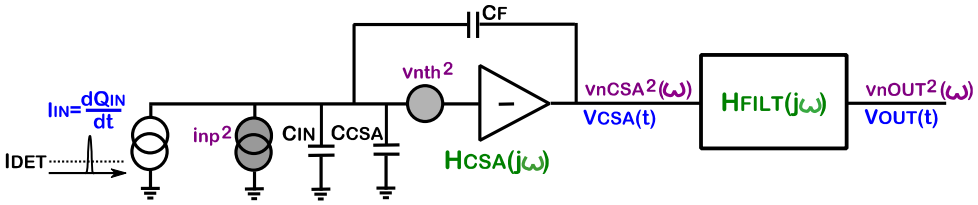


Figure 2.27 Detector readout chain with transfer function $H(j\omega)$ composed of: the CSA $H_{CSA}(j\omega)$ and the filter $H_{FILT}(j\omega)$.

Detection chain integrated output noise

The output noise of the whole detection chain is associated with the series and parallel input related noise sources. In the frequency domain the output noise PSD ${v_{nOUT}}^2$ is calculated by multiplication of the total squared input noise and the squared module of the transfer function:

$${v_{nOUT}}^2 = \left({i_{n\,p}}^2 + \frac{{v_{n\,th}}^2 + {v_{n\,f}}^2}{Z_{INnoise}(\omega)^2} \right) \cdot |H(j\omega)|^2 \qquad 2\text{-}51$$

Where $Z_{INnoise}(\omega)$ is the impedance seen by the input referred voltage noise sources, derived in the paragraph 2.2.6. The total mean square output noise appears in the numerator of the ENC equation (*2-46* and *2-47*) and it is essential to calculate it. It is defined as the integral of the PSD over the whole frequency range:

$$\overline{{v_{nOUT}}^2} = \frac{1}{2 \cdot \pi} \cdot \int_0^\infty \left({i_{n\,p}}^2 + \frac{{v_{n\,th}}^2 + {v_{n\,f}}^2}{Z_{INnoise}(\omega)^2} \right) \cdot |H(j\omega)|^2 \, d\omega \qquad 2\text{-}52$$

The integrated square noise has units of $[{V_{rms}}^2]$. In other practical notation the equation is described as a sum of three integrals, each related to a different input noise source, resulting in the final expression of: $\overline{{v_{nOUTp}}^2} + \overline{{v_{nOUTth}}^2} + \overline{{v_{nOUTf}}^2}$.

Detection chain output voltage

The output voltage $V_{out}(t_m)$ containing information about the detector signal is the second variable, after the integrated output noise, needed to determine the ENC. The output signal $V_{out}(t)$ results

from the input current impulse that carries charge Q_{IN} and arrives at $t_0 = 0$. Its amplitude that is of interest is taken at the measurement time $t_m > 0$. However if the processing channel transfer function $H(j\omega)$ is known – the output voltage at the time t_m can be calculated from the inverse Fourier transform:

$$V_{out}(t_m) = \int_0^{\infty} Q_{IN} \cdot H(j\omega) \cdot e^{j\omega t_m} d\omega \qquad 2\text{-}53$$

The measurement time is typically chosen when the output voltage pulse achieves its maximum value. Then it is referred to as the peaking time $t_m = t_{peak}$. In LTI system noise is assumed independent of the measurement time. Consequently it is desired to measure the peak amplitude, which results in: the highest signal to noise ratio and thus – the lowest ENC. For a system with a given transfer function the peaking time can be determined by calculating the derivative of its impulse response $h'(t)$, then the zero of the function is found at the time t_{peak}:

$$h'(t_{peak}) = 0 \qquad 2\text{-}54$$

Detection chain ENC

Finally the ENC can be calculated as the ratio of the total output noise and the channel gain, both obtained in the frequency domain:

$$\boldsymbol{ENC^2 = \frac{\overline{v_{nOUT}{}^2}}{[V_{out}(t_m)/Q_{IN}]^2 \cdot q^2}} \qquad 2\text{-}55$$

The squared equivalent noise charge: ENC^2 is expressed in $[el_{rms}{}^2]$. Therefore if Q_{IN} is given in $[C]$ it has to be converted to electrons, with division by the electron charge q of $1.602 \cdot 10^{-19}$ $[C]$. The total output noise $\overline{v_{nOUT}{}^2}$ is composed of three contributors: due to input white parallel noise, white series noise and flicker series noise. Consequently in the ENC equation three components can be distinguished: ENC_p, ENC_{th} and ENC_f:

$$ENC^2 = ENC_p + ENC_{th} + ENC_f \qquad 2\text{-}56$$

In the time domain analysis, presented next, each of these contributors will be analyzed separately.

2.3.2.2. Time domain noise analysis

In the time domain, the noise can be calculated from the weighting function $w(\tau)$, sometimes called the residual function [43]. The weighting function $w(\tau)$ of the system is the amplitude response of the system at the measurement time t_m produced by a current pulse (Dirac) occurring at a time τ. For linear time invariant filters, the weighting function is the mirror image of the impulse response of the channel shifted by the interval t_m corresponding to the measurement time: $h(t_m - t)$. This is because a time invariant filter provides the same response to each input event at any time. Nevertheless two filters: one time invariant and one time variant can be designed in a way that their weighting functions are the same [47].

2.3. Noise filtering in the detection chain

Weighting function

It will be shown on a simple example how the weighting function is produced. First of all two characteristic events are localized in the two analogical time domains, the real time t and the weighting function inversed time τ:

- On the real time t-axis the signal arrival and the energy measurement occur at times: $t_0 = 0$ and t_m respectively.
- On the weighting function τ-axis: the event of signal arrival corresponds to $\tau = t_m$ and the energy measurement time corresponds to $\tau = 0$.

Let's consider a filter whose output after an event arriving at t_0 settles back to zero in a finite time T_{settle}. The output pulse measurement time is performed at $t_m = t_{peak}$. Figure 2.28 illustrates an example of how the weighting function is created.

The measured output signal has to be examined in the presence of noise. Noise can be described as a series of discrete input charge events, occurring continuously – before and after t_0. Each of them might influence the measured output. If a single noise charge impulse appears on the CSA input at a time $t_x < -(T_{settle} - t_m)$, it will have a zero-contribution to the output voltage at the measurement time t_m. Therefore the weighting function for such time instant t_x equals zero:

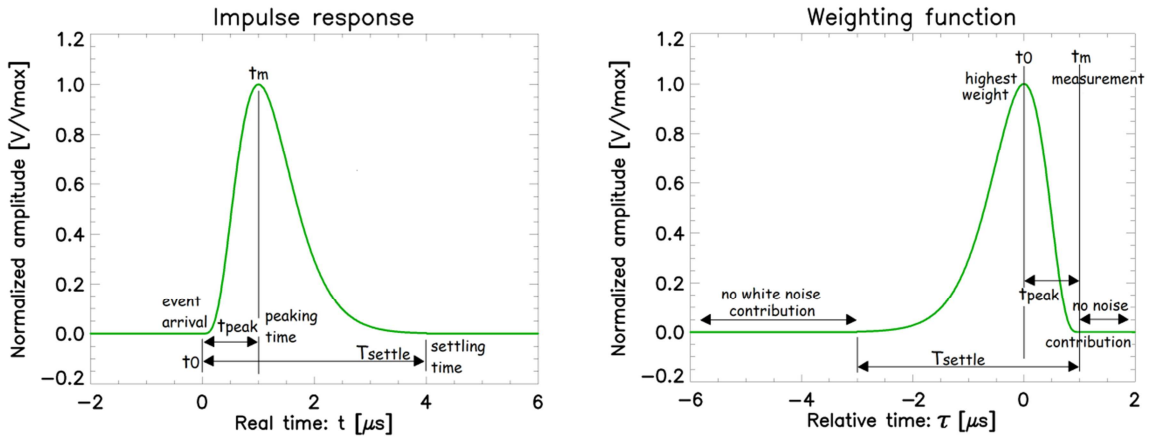
- $w\big(\tau > (T_{settle} - t_m)\big) = 0$

However if a single noise impulse occurs at the same time as the signal arrival: $t_x = t_0$, its contribution to the measured value is the worst possible. That is the noise impulse has the highest weight:

- $w(0) = w(\tau)_{MAX}$

Finally if a noise impulse occurs after the measurement time – again it does not contribute to the output noise measured at time t_m, therefore:

- $w(\tau < -t_m) = 0$



A) B)

Figure 2.28 Illustration of how a weighting function is produced. A) Impulse response. B) Corresponding weighting function. The example shows the second order semi-Gaussian shaper.

In practice the weighting function is often used in the normalized form, as in the example from Figure 2.28. Once the weighting function is divided by the channel gain, it turns to be the normalized weighting function $w_N(\tau)$, whose maximum value equals one:

$$w_N(\tau) = \frac{w(\tau)}{A_{filter} \cdot A_{CSA}} \qquad 2\text{-}57$$

Where the CSA gain A_{CSA} is the close loop gain, which in case of an ideal CSA, it is equal to $1/C_F$, whereas the gain of the filter A_{filter} depends on the filter type.

The complete noise and ENC calculation based on the weighting function approach should be decomposed into three cases of the input related noise: parallel white noise, series white noise and series flicker noise. It has been shown (in the paragraph 2.2.6) that each of the dominating noise sources produces a noise PSD at the CSA output – that is a different function of frequency. Also in the time domain each of them has to be analyzed separately. The analysis of the parallel white noise is the most straightforward and will be presented at first.

Effect of the white parallel noise passed through the weighting function

The input parallel noise is considered to be the white noise, typically dominated by the detector shot noise. Consequently it can be described as a random sequence of unit charge events q arriving with the average rate N. Each event $q_x = q \cdot \delta(t_x)$, when integrated on the CSA feedback capacitance – produces a voltage step at the CSA output. Therefore it is often called a step noise [43]. The effect of this train of events at the output of the detection chain (comprising the CSA and the filter) can be described with the weighting function. The output obtained at time τ due to a single input noise charge q_x arriving at a time t_x equals:

$$v_{nOUTpx}(t_m) = q_x \cdot w(t_x) \qquad 2\text{-}58$$

The influence of the input charge noise on the output voltage is illustrated in Figure 2.29.

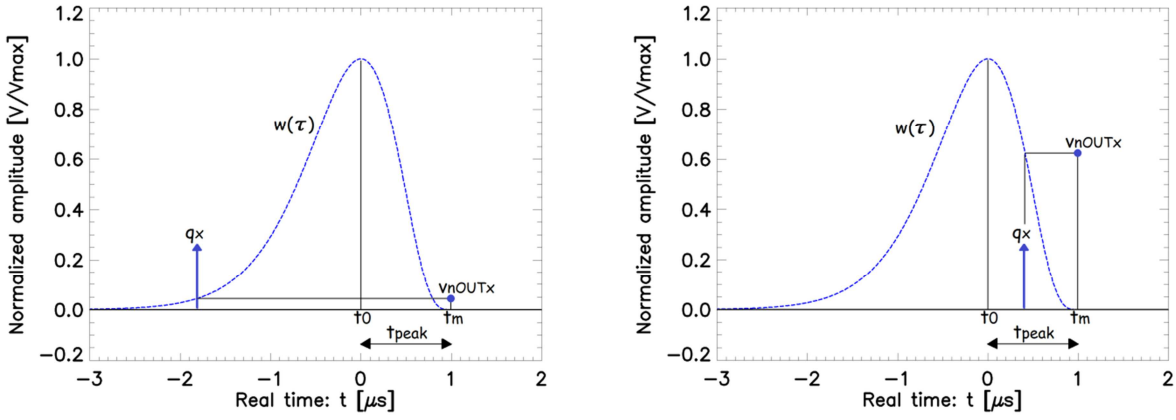


Figure 2.29 Influence of a single step noise event q_x, arriving at time t_x, on the output voltage at the measurement time t_m. In: A) and B) q_x arrives at different times with respect to the measurement time t_m. A second order semi-Gaussian shaper is used in the example.

When the weighting function $w(\tau)$ is known for the whole time range τ, the contribution of the step noise arriving at random time intervals can be calculated. The total output mean squared noise is:

2.3. Noise filtering in the detection chain

$$\overline{v_{nOUTp}{}^2} = N \cdot q^2 \cdot \int_{-\infty}^{\infty} w(t)^2 dt \qquad 2\text{-}59$$

The equation is a consequence of the Campbell's theorem [46] and is discussed in [43][10][45]. It states that the variance $\overline{v_{n\,OUT}{}^2}$ of random current pulses is proportional to the average pulse rate N.

By applying the Parseval's theorem to the noise variance $\overline{v_{nOUTp}{}^2}$ at the channel output obtained in the frequency domain *2-52* for the white parallel noise $i_{n\,p}{}^2$ the following relationship is established:

$$\overline{v_{nOUTp}{}^2} = i_{n\,p}{}^2 \int_0^{\infty} |H(j2\pi f)|^2 df = \frac{i_{n\,p}{}^2}{2} \int_{-\infty}^{\infty} w(\tau)^2 d\tau \qquad 2\text{-}60$$

The same result can be found when the parallel input noise is assumed to be a pure shot noise $i_{n\,sh}{}^2$ due to the detector dark current of mean value I_{DET}. It should be noticed that the term $N \cdot q^2$ can be written as: $I_0 \cdot q$, where I_0 is the average input current, resulting from the random current pulses. Therefore I_0 is equal to I_{DET}. With the known shot noise power density of $2 \cdot q \cdot I_{DET}$ the following relation occurs:

$$\overline{v_{nOUT\,sh}{}^2} = I_{DET} \cdot q \cdot \int_{-\infty}^{\infty} w(\tau)^2 d\tau = \frac{i_{n\,sh}{}^2}{2} \int_{-\infty}^{\infty} w(\tau)^2 d\tau \qquad 2\text{-}61$$

With the normalized weighting function, that is – divided by the channel gain, the ENC due to the input parallel white noise can be simply expressed as [10]:

$$\boldsymbol{ENC_p{}^2 = \frac{\frac{1}{2} \cdot i_{nIN}{}^2 \cdot \int_{-\infty}^{\infty} [w_N(\tau)]^2 d\tau}{q^2}} \qquad 2\text{-}62$$

Division by a unit charge q is applied to express ENC in the units of $[el_{rms}]$.

Effect of the white series noise passed through the weighting function

The second contributor to be considered for the time domain noise analysis is the white series noise, also referred to as a delta noise. An input unit voltage impulse $v_{nx} \cdot \delta(t_x)$ can be viewed in terms of the input charge as: a doublet $q'_x = q \cdot \delta'(t_x)$. When applied to the CSA input capacitance the doublet causes the same effect as the voltage impulse [44]. Thus the series input is transformed to the parallel input:

$$q \cdot \delta'(t_x) = C_{INnoise} \frac{d(v_{nx} \cdot \delta(t_x))}{dt} \qquad 2\text{-}63$$

where $C_{INnoise} = C_{IN} + C_F + C_{CSA}$ is the equivalent input capacitance seen by the series noise source, obtained from the noise impedance derived in paragraph 2.2.6.

The doublet $\delta'(t)$ is a derivative of Dirac delta $\delta(t)$. It can be represented as an input current positive delta followed by a negative delta. From its properties – a convolution of a doublet with a function equals the derivative of the function. Therefore, in the case of the weighting function $w(\tau)$ the following can be written:

$$\delta'(\tau) * w(\tau) = w'(\tau) \qquad 2\text{-}64$$

Consequently the effect on the channel output at time t_m due to a single input voltage pulse occurring at time τ can be written as:

$$v_{nOUTx}(\tau) = (v_{nx} \cdot \delta'(\tau) \cdot C_{INnoise}) * w(\tau) = v_{nx} \cdot C_{INnoise} \cdot w'(\tau) \qquad 2\text{-}65$$

Thus the effect of a single delta noise event on the CSA output voltage at the time t_m has been obtained mathematically. It is also illustrated graphically in Figure 2.30. The input charge q'_x, equivalent of the input voltage noise impulse v_{nx}, has a contribution to the output voltage measured at time t_m, depending on its arrival time τ.

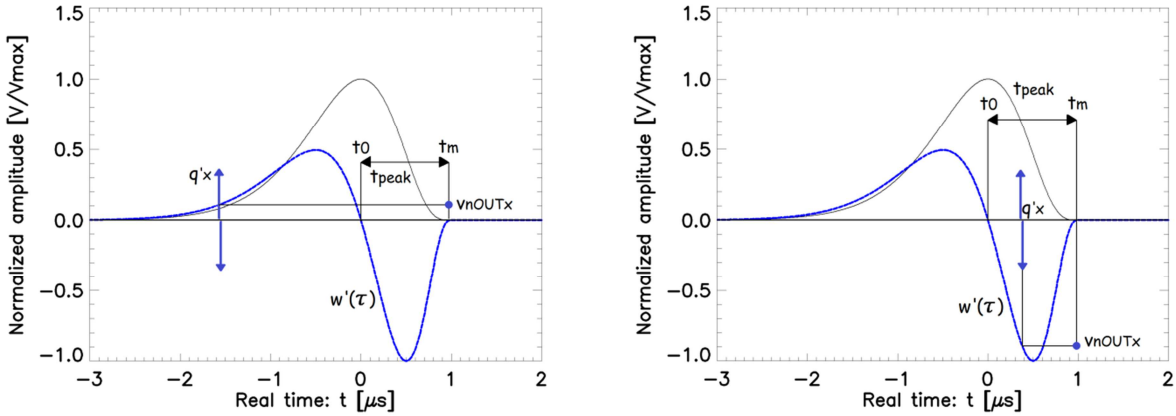


Figure 2.30 Illustrated influence of a single delta noise event q'_x, arriving at time t_x, on the output voltage at the measurement time t_m. In: A) and B) q'_x arrives at different times with respect to measurement time t_m. A second order semi-Gaussian shaper is used in the example.

The main question however is the value of the total integrated noise $\overline{v_{nOUT\,th}{}^2}$ resulting from the white series noise source at the CSA input $v_{n\,th}{}^2$. The Campbell's theorem can be applied to obtain the mean squared output noise:

$$\overline{v_{nOUT\,th}{}^2} = \frac{1}{2} \cdot v_{n\,th}{}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot \int_{-\infty}^{+\infty} [w'(\tau)]^2 d\tau \qquad 2\text{-}66$$

If in the calculations the normalized weighting function is used, also the derivative should also be normalized:

$$w_N{}'(\tau) = \frac{w'(\tau)}{A_{filter} \cdot A_{CSA}} \qquad 2\text{-}67$$

Finally the equivalent noise charge due to the input white series noise $v_{n\,th}{}^2$ can be written as follows:

$$\boldsymbol{ENC_{th}{}^2 = \frac{\frac{1}{2} \cdot v_{n\,th}{}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot \int_{-\infty}^{+\infty} [w_N{}'(\tau)]^2 d\tau}{q^2}} \qquad 2\text{-}68$$

Where $w_N{}'(\tau)$ is the normalized function obtained by division of $w'(\tau)$ by the channel gain: $A_{filter} \cdot A_{CSA}$. The division of the ENC expression by the unit charge q leads to ENC described in the units: $[el_{rms}]$.

Effect of the flicker series noise passed through the weighting function

The series flicker noise analysis in the time domain is less intuitive than the two discussed white noise contributors. It is performed with relation to the frequency domain, simply because of the flicker noise power with its characteristic low frequency spectral distribution. The input flicker noise power spectrum v_{nf}^2 is a function of: $1/\omega$. What has to be found is the resulting noise variance on the CSA output $\overline{v_{nOUT\,f}{}^2}$. This is the remaining contributor needed to calculate total ENC. The solution is derived in [53], where it is shown that the noise variance in the frequency domain has the following form:

$$\overline{v_{nOUT\,f}{}^2} = const \cdot \int_0^\infty \omega \cdot |H(j\omega)|^2 df \qquad 2\text{-}69$$

The time domain counterpart can be found by applying the Parseval's theorem. The noise variance is described in the time domain in terms of the impulse response, which is the time inversed and time shifted weighting function (as shown in Figure 2.28):

$$\overline{v_{nOUT\,f}{}^2} = v_{nf}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot \frac{1}{2} \cdot 2 \cdot \pi \cdot \int_{-\infty}^{\infty} \left[w^{(1/2)}(\tau)\right]^2 d\tau \qquad 2\text{-}70$$

Finally using the normalized weighting function the flicker noise contribution to ENC is obtained [72]:

$$\boldsymbol{ENC_f{}^2 = \frac{1}{q^2} \cdot v_{nf}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot \pi \cdot \int_{-\infty}^{\infty} \left[w_N{}^{(1/2)}(\tau)\right]^2 d\tau} \qquad 2\text{-}71$$

The time domain equivalent of $\overline{v_{nOUT\,f}{}^2}$ [53] and ENC_f both contain the weighting function fractional derivative of the order $n = 1/2$. According to the Riemann-Liouville definition – the fractional derivative $f^{(1/2)}(x)$ of a function $f(x)$ can be written as [57][58]:

$$f^{(1/2)}(x) = \frac{d}{dt}\left(\frac{1}{\Gamma(1/2)} \cdot \int_0^x \frac{f(\varphi)}{(x-\varphi)^{1/2}} d\varphi\right) \qquad 2\text{-}72$$

Where the function Gamma (Adrien-Marie Legendre) at $1/2$ equals:

$$\Gamma(1/2) = \int_0^\infty \frac{x^{1/2} \cdot e^{-x}}{x} dx = 1.7724 \qquad 2\text{-}73$$

The definition presented here will be especially important in the comparison of my models of the frequency domain and the time domain ENC with the MCDS filter, described in the paragraph 2.3.5.

Weighting function properties

ENC equations for the dominating noise sources have been derived in the time domain (equations *2-62*, *2-68* and *2-71*). In each ENC expression a relation with the normalized weighting function $w_N(\tau)$ or its derivatives has been found, under an integral. These integrals have characteristic properties:

- $\frac{1}{t_{peak}} \cdot \int_{-\infty}^{\infty} [w_N(\tau)]^2 d\tau = const$ – in parallel white noise ENC expression *2-62*
- $t_{peak} \cdot \int_{-\infty}^{\infty} [w_N{}'(\tau)]^2 d\tau = const$ – in series white noise ENC expression *2-68*
- $\int_{-\infty}^{\infty} \left[w_N{}^{(1/2)}(\tau)\right]^2 d\tau = const$ – in series flicker noise ENC expression *2-71*

Where t_{peak} is the measurement time performed at the specific time instance – when the output signal reaches the peak value. The given properties are concluded from [43][45][54] for many filters: CR-RC^N, triangular, trapezoidal, sinusoidal, parabolic or Gaussian. Consequently the features apply to weighting functions associated with filters commonly used in the radiation detection systems.

Noise coefficients

In consequence it is convenient to define the following noise coefficients to be replaced into the ENC expressions (*2-62*, *2-68* and *2-71*):

- $A_p = \frac{0.5}{t_{peak}} \cdot \int_{-\infty}^{\infty} [w_N(\tau)]^2 d\tau$ – the parallel white noise coefficient
- $A_{th} = 0.5 \cdot t_{peak} \cdot \int_{-\infty}^{\infty} [w'_N(\tau)]^2 d\tau$ – the series white noise coefficient
- $A_f = 0.5 \cdot 2 \cdot \pi \cdot \int_{-\infty}^{\infty} \left[w^{(1/2)}(\tau)\right]^2 d\tau$ – the series flicker noise coefficient

These noise coefficients are independent of the following channel parameters: the input referred noise, dark current and the input capacitance. However, in case of the optimal filter Cusp and the MCDS – the parameters' values vary with the measurement time.

The parameters A_p, A_{th} and A_f provide a more general way to express capabilities of a filter to reduce a specific type of noise. The lower is a noise parameter – the better filtering capabilities for the corresponding input noise. In the rest of the text, instead of using long expressions containing the integrals, I will use the noise coefficients to describe each shaper and later to compare them. In case of Cusp and MCDS I will determine parameters at different measurement times (Table 2.4 in 2.3.6).

2.3.2.3. Equivalence of noise coefficients in the time and in the frequency domain

The noise coefficients, presented above, have been obtained in the time domain. However they can be correspondingly defined for the frequency domain [44][54][72]. The respective expressions are obtained by applying the Parseval's theorem:

- $A_p = \frac{0.5}{t_{peak}} \cdot \frac{1}{2\pi} \cdot \int_0^{\infty} [H(j\omega)]^2 d\omega$
- $A_{th} = 0.5 \cdot t_{peak} \cdot \frac{1}{2\pi} \cdot \int_0^{\infty} ([H(j\omega)]^2 \cdot \omega^2) d\omega$
- $A_f = 0.5 \cdot 2 \cdot \pi \cdot \frac{1}{2\pi} \cdot \int_0^{\infty} ([H(j\omega)]^2 \cdot \omega) d\omega$

Having both equivalent notations available: in the time and in the frequency domain – is practical in the analysis of different filter types (paragraphs 2.3.3– 2.3.6). For the respective filters I will calculate the noise parameters either from the channel transfer function or from the weighting function, whatever is easier to obtain. It should be noted that sometimes in the literature the noise coefficients (described in the time or in the frequency domain) are defined without multiplication by the factor 0.5 (and 0.5π in case of A_f). Therefore the values, that I will calculate and present in this chapter, may appear twice larger with respect to certain references, but it is only the matter of the definition.

2.3.2.4. Equations describing ENC

The ENC expressions have been derived in both: the frequency and the time domain. This has led to definition of the noise coefficients: A_p, A_{th} and A_f. Using the noise coefficients the ENC equations (*2-62*, *2-68* and *2-71*) can be conveniently rewritten in the following form:

$$ENC_p{}^2 = \frac{1}{q^2} \cdot i_{n\,p}{}^2 \cdot t_{peak} \cdot A_p \qquad 2\text{-}74$$

$$ENC_{th}{}^2 = \frac{1}{q^2} \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot \frac{1}{t_{peak}} \cdot A_{th} \qquad 2\text{-}75$$

$$ENC_f{}^2 = \frac{1}{q^2} \cdot v_{n\,f}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_f \qquad 2\text{-}76$$

These equations taken together describe the total ENC of the complete radiation detection system. The total ENC is calculated as:

$$ENC = \sqrt{ENC_p{}^2 + ENC_{th}{}^2 + ENC_f{}^2} \qquad 2\text{-}77$$

The given notation is convenient in filter analysis and will accompany further discussions contained in this work. Defined in terms of noise coefficients, the ENC is revealed to be a function of:

- input referred parallel and series noise sources
- peaking time t_{peak}
- capacitance seen by series noise sources $C_{INnoise} = C_F + C_{IN} + C_{CSA}$
- filter type

The final conclusion, fundamental in optimization of the readout system, is the characteristic shape of the ENC function with respect to the peaking time. Each of the ENC components, related to the input noise of different characters, has a different behaviour with respect to the peaking time. The total ENC is a U-shaped function with the characteristic optimal peaking time $t_{peakOPT}$ where it achieves the lowest value ENC_{MIN}. This occurs when $ENC_p = ENC_{th}$. This specific point of interest is indicated in Figure 2.31.

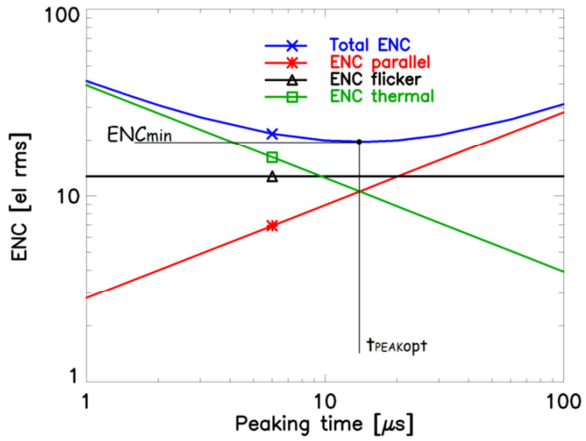


Figure 2.31 Total ENC of a radiation detection system as a function of peaking time. All three ENC contributors, due to: white parallel noise, white series noise and flicker series noise are distinguished. The optimal peaking time and the corresponding minimum ENC are indicated.

The optimal peaking time can be determined using the equations *2-74* and *2-75*, and it equals:

$$t_{peakOPT} = \sqrt{\frac{v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_{th}}{{i_{n\,p}}^2 \cdot A_p}} \qquad 2\text{-}78$$

The whole process of the readout chain ENC optimization is aimed to determine the CSA and the filter type, which result in the lowest possible value of ENC achieved at the optimal peaking time.

2.3.3. Presentation of the optimal filter and why this chapter will continue

The methods to obtain the ENC formula in the time and in the frequency domain have been already introduced. With the given calculation tools I can proceed to analysis of the filters of interest. The question that I would like to answer in the first place is: what is the optimal filter, which provides the lowest possible ENC? The matched filter theory proposes a method to obtain the transfer function of the optimal filter, for a given input signal [47][51]. This approach can be used in the detection chain. The general concept states that the matched filter is capable to detect an input signal of a specific template in the presence of white noise with the best signal to noise ratio (or the lowest ENC): this happens when the filter impulse response is a mirror image of the detected signal pattern. The matched filter theory finds applications in various engineering domains from X-rays imaging to data transmission, communications and radar systems [52].

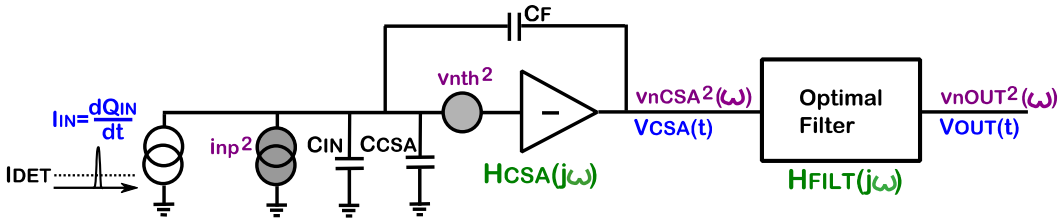


Figure 2.32 The schematic used for the optimal filter analysis.

The solution of the optimal processing in the radiation detection chain is described in the Annex I. It is based on the matched filter theory. The "unknown" optimal filter is split into two parts: the noise whitening filter and the matched filter. The whitening filter is a high-pass filter with the time constant τ_{white} equal to:

$$\tau_{white} = (C_{IN} + C_{CSA} + C_F)\sqrt{{v_{n\,th}}^2/{i_{n\,p}}^2} \qquad 2\text{-}79$$

The matched filter impulse response is chosen to match the output response of the whitening filter. Their convolution results in the maximum achievable power of the output signal and consequently – the best signal to noise ratio.

2.3.3.1. ENC of the readout chain with the optimal filter

The optimal filter for the system from Figure 2.32 is known as "Cusp". The impulse response of the detection chain with the Cusp filter is demonstrated in Figure 2.33. Two scenarios of t_m are

illustrated: the finite measurement time and with the measurement time approaching infinity. In the ideal case with $t_m = \infty$ the signal shape is called Cusp. This shape is expected to provide the lowest ENC. In the practical realization the measurement is performed within a finite interval after the event and the system response has form of a truncated Cusp, with loss of the measured signal power. The ENC for the optimal detection system with the matched filter is described with the following formula (derived in Annex I):

$$ENC^2 = (C_{IN} + C_{CSA} + C_F) \cdot \sqrt{{v_n}_{th}^2 \cdot {i_n}_p^2} \cdot \frac{1}{q^2} \qquad 2\text{-}80$$

This is the lowest possible ENC achievable in a system with a given CSA and the detector, where the noise parameters (${v_n}_{th}^2$ and ${i_n}_p^2$) as well as the capacitances (C_{IN}, C_{CSA} and C_F) are fixed. In this calculation the flicker noise contribution ${v_n}_f^2$ has not been taken into account.

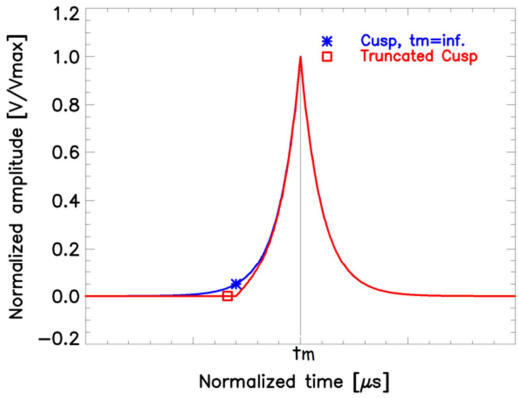


Figure 2.33 Impulse response of a radiation detection system with CSA and the optimal filter. Two cases of the measurement time are considered: with $t_m = \infty$ resulting in the Cusp-shaped output response (blue) and with a finite t_m resulting in the truncated Cusp output response (red).

2.3.3.2. Conclusions on the optimal filter

The best filter for the radiation detection in the presence of white noise sources has been presented, the flicker noise has not been included for simplicity. The impulse response of a detection system with the Cusp filter depends on the measurement time, what is demonstrated in Figure 2.33. The case where the lowest ENC is achieved, corresponds to t_m equal to infinity, for this reason the filter with the Cusp response is non-realizable. In the practical applications of detection systems, the suboptimal filter is implemented, with the measurement time set to a possibly high value of few time constants τ_{white}, resulting in the truncated Cusp response. The corresponding noise parameters of the Cusp filter: A_{th}, A_f and A_p, calculated from the filter's weighting function are given in the Annex I for different values of the t_m/τ_{white} ratio. This ratio, of the measurement time to the optimal filter time constant, defines the non-ideality of the truncated Cusp response. In the last paragraph of this chapter: 2.3.6 I will show, that the coefficients obtained with the optimal filter for white noise still show the best rejection of the flicker noise in comparison to other discussed shapers.

Even if the truncated version of the filter is considered there are some inconveniences in the practical realization. After each event, it takes a long time for the filter to recover the baseline output level. This results in a very long dead time between two input events that can be precisely measured. Furthermore, because of the sharp form of the output signal, its maximum value $V_{out}(t_m)$ is difficult

to measure – a precise measurement would need to be performed in an extremely short time. Finally the realization of Cusp is very difficult, if possible at all, to synthetize in an analog circuit. These issues are the main reasons why there are not many applications of the Cusp filter. Two references that I can mention, [55] and [56], implement digitally synthesized truncated Cusp, by processing digitized samples of the CSA output signal. In both cases a superior performance of the truncated Cusp is demonstrated – with ENC improved by over 10% when compared with other filters: the triangular filter (in [55]) and the semi-Gaussian filter (in [56], where the Cusp shape is optimized for flicker noise). Nevertheless in most of the detection systems other filters are used instead, where the listed inconveniences of the truncated-Cusp are eliminated. This is at the cost of an increased ENC. To maintain the ENC level as low as possible, the shape of typically implemented weighting functions is an approximation of the Cusp: with a flattened peak and limited recovery time. The most common substitute is the semi-Gaussian filter, very easy to realize in a fully analog manner. In the next paragraph, 2.3.4, I will describe this filter and demonstrate its advantages. The second filter that I will describe in this chapter is the discrete approximation of the trapezoidal filter: based on the Multi-Correlated Double Sampling (MCDS). The filter offers a good flexibility to control the noise parameters – by adjusting the sampling time and the number of samples. It is popular in its 2-samples version, which is the Correlated Double Sampling (CDS). In paragraph 2.3.5 I will extend the CDS analysis to MCDS with mathematical description considering any number of samples.

2.3.4. Charms of the Semi-Gaussian shaper

The semi-Gaussian shaper is often referred to as a CR-RC^N filter, since it is typically composed of a CR high pass filter followed by a N^{th} order RC low pass filter, as shown in Figure 2.34. The higher the order of the low pass filter the more the step response will resemble the Gaussian function. The construction of the shaper with only passive elements would cause attenuation of the signal level in the chain. In practice the CR-RC^N is realized as an opamp-based active filter, which symbolically can be illustrated with the additional gain stage, as in Figure 2.34. One of the numerous examples of this filter is the IDeF-X HD ASIC [23].

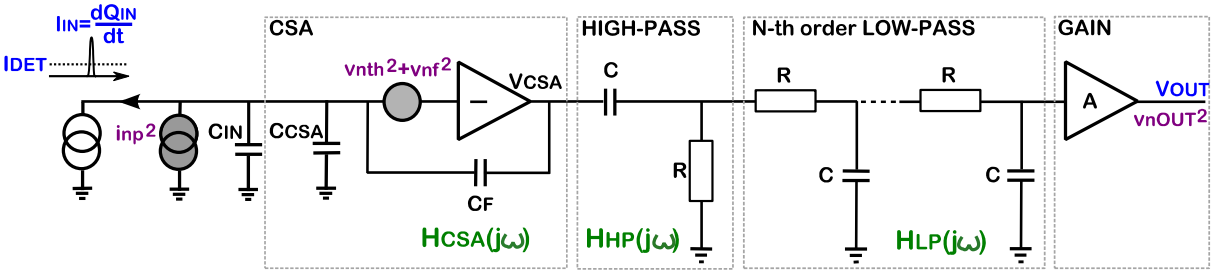


Figure 2.34 Detection chain with CSA and the N^{th} order semi-Gaussian shaper: CR-RC^N.

2.3.4.1. Filter characteristics

In the description of the filter it is assumed that the time constant τ of each elementary filter (high pass and low pass) is identical and equal to RC. The transfer function of a detection chain with the CSA and the N-th order CR-RC shaper is:

$$H(j\omega) = H_{CSA}(j\omega) \cdot H_{CR\,HP}(j\omega) \cdot H_{RC\,LP}(j\omega) = \frac{1}{C_F} \cdot \frac{1}{\tau^N \cdot (1/\tau + j\omega)^{N+1}} \qquad 2\text{-}81$$

From this frequency-domain description, the response of the system to an instantaneous charge at the CSA input can be obtained:

$$V_{out}(t) = Q_{in} \cdot \frac{1(t)}{C_F} \cdot \frac{t^N}{N! \cdot \tau^N} \cdot e^{-t/\tau} \qquad 2\text{-}82$$

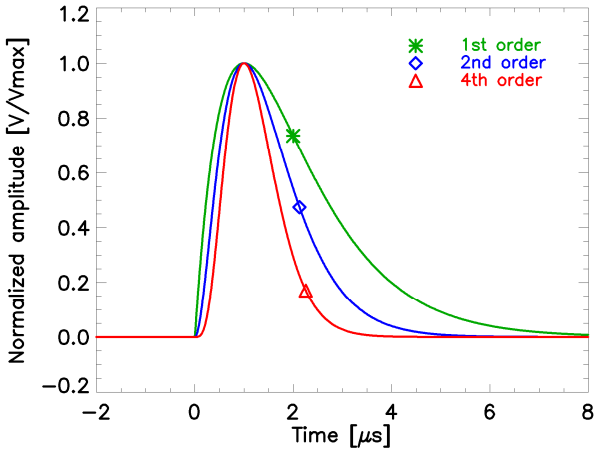


Figure 2.35 The output response of the detection chain with the CSA and the semi-Gaussian filter to an input instantaneous charge. Comparison of the filter order: 1^{st}, 2^{nd} and 4^{th} with a constant peaking time of 1 μs.

The shape of the output voltage pulse is illustrated in Figure 2.35. Three different values of the filter order N have been chosen. The plot shows the signal shape approaching the Gaussian pulse as the filter order increases. Simultaneously the settling time reaches the baseline level after the pulse becomes shorter, what is strongly desirable. For all the three waveforms in Figure 2.35, the maximum value is achieved simultaneously, at the target measurement time. This specific time instant is the peaking time, whose value t_{peak} is in the strict relation with the filter parameters. The peaking time is found from the derivative of the output voltage: $V_{out}{}'(t_{peak}) = 0$, which occurs when:

$$t_{peak} = N \cdot \tau \qquad 2\text{-}83$$

This result shows that the peaking time increases with the filter order and with the RC time constant.

2.3.4.2. Calculation of ENC

With the known transfer function of the channel *2-81*, the output integrated voltage can be calculated in the frequency domain, as the product of the input referred noise and the transfer function. The second quantity needed in the ENC calculation is the channel gain, which is simply the maximum output voltage $V_{out}(t_{peak})$ resulting from an input charge Q_{IN}, divided by this charge. Now the ENC equation can be written:

$$ENC^2 = \frac{\int_{-\infty}^{\infty} \left({i_n}_p{}^2 + \frac{{v_n}_{th}{}^2 + {v_n}_f{}^2}{{Z_{IN}}^2} \right) \cdot |H(j\omega)|^2 df}{\frac{1}{C_F} \cdot \frac{t^N}{N! \cdot \tau^N} \cdot e^{-t/\tau}} \qquad 2\text{-}84$$

2.3. Noise filtering in the detection chain

The ENC takes into account the three dominating noise sources already discussed: the parallel white noise, the series white noise and the series flicker noise. The squared ENC can be also represented as a sum of the three contributors:

$$ENC^2 = {ENC_p}^2 + {ENC_{th}}^2 + {ENC_f}^2 \qquad 2\text{-}85$$

For each case the integral over frequency in *2-84* can be solved analytically. The result is found with substitution of the integration over frequency, to variable x equal to $(\tau \cdot 2\pi f)^2$. The complete ENC calculation for the N-th order semi-Gaussian filter is presented in [62][63]. Consequently analytical expressions for each of the noise parameters can be extracted:

$$A_p = \left(\frac{N!}{N^N \cdot e^{-N}}\right)^2 \cdot \frac{B\left(\frac{1}{2}, N + \frac{1}{2}\right)}{N \cdot 4 \cdot \pi} \qquad 2\text{-}86$$

$$A_{th} = \left(\frac{N!}{N^N \cdot e^{-N}}\right)^2 \cdot \frac{N}{4 \cdot \pi} \cdot B\left(\frac{3}{2}, N - \frac{1}{2}\right) \qquad 2\text{-}87$$

$$A_f = \left(\frac{N!}{N^N \cdot e^{-N}}\right)^2 \cdot \frac{1}{2 \cdot N} \qquad 2\text{-}88$$

Where the function $B(a,b)$ is the Beta function. With these expressions inserted in the ENC equations of the general form (equations: 2-74 – 2-76 in the paragraph 2.3.2), the total ENC can be calculated. In the CR-RC^N filter, the values of the coefficients: A_p, A_{th} and A_f depend only on the filter order. E.g. if a second order semi-Gaussian would be considered, the parameters' values are respectively: 0.64, 0.854 and 3.411. Figure 2.36 illustrates how the noise parameters behave as a function of the shaper order N. Those related to the flicker voltage noise A_f and the white current noise A_p decrease with N. However with their highest gradient at low N values, only a little improvement is observed for N higher than 4. Meanwhile the white voltage noise coefficient A_{th} is the lowest for $N = 2$, then it increases almost linearly with N. The choice of the filter order highly depends on which of the input related noise contributors is dominating. In the typical applications the value of N ranges between 1 and 4. Any higher order adds too much complexity to the system.

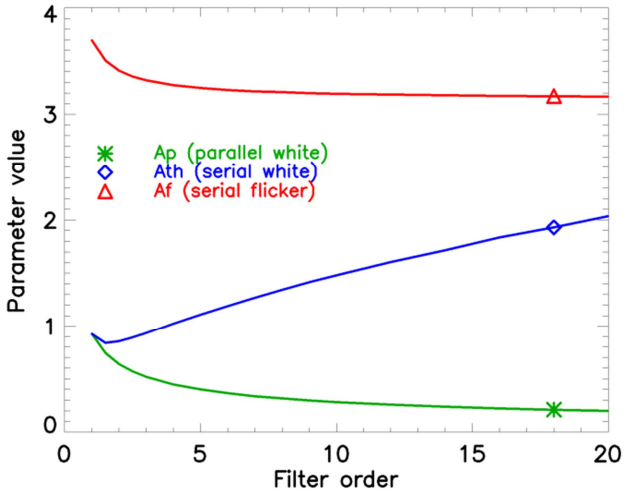


Figure 2.36 Plot of the CR-RC^N filter noise parameter: as a function of the shaper order N.

The mathematical description of the semi-Gaussian filter has been demonstrated. As in case of any other shaper – the ENC depends on the input related noise sources and the capacitances associated

with the CSA and the detector. Its value can be optimized, according to the relation between the ENC and the peaking time, what was illustrated in Figure 2.31 (paragraph 2.3.2). The noise parameters which also influence ENC can be modeled by choosing the filter order. However in practice – the lowest ENC obtainable with a given semi-Gaussian filter is found by adjusting the time constant τ equal to RC.

There are many radiation detectors designed for various sensors, where the semi-Gaussian filter is used. Typically the electronic chain is a combination of the CSA, pole-zero cancellation stage and a Sallen-Key 2^{nd} order low-pass filter, although there are also other architectures. In the IDeF-X HD ASIC [23] the 2^{nd} order filter is optimized for a CdTe detector with an input capacitance of few pF and its adjustable peaking time, ranging from 1 to $11\,\mu s$, allows for selecting the best ENC conditions. The ASIC AFTER [32], designed for a higher capacitance gaseous detector also integrates a 2^{nd} order shaper and is optimized with a peaking time adjustable between $100\,ns$ and $2\,\mu s$. Another ASIC also for readout of a similar detector type, SFE16 [31] uses a double Sallen-Key filter, resulting in a CR-RC^4 shaper. There are many more application examples that one could refer to. From the numerous publications, the techniques for the block-level design of the semi-Gaussian filter and improvements in its transient characteristics can be acquired. The maturity of the CR-RC^N implementations makes it a very attractive choice.

2.3.5. Deep explorations of MCDS

I would like to present one more filter, which is also an approximation of the optimal filter weighting function: the MCDS, which stands for Multi Correlated Double Sampling. The filter is also referred to as a pseudo-trapezoidal, because of its weighting function shape. Similarly as in the case of the semi-Gaussian filter, it is also possible to implement it in an analog circuit. Even though its implementation is not as obvious as it was in the case of the CR-RC^N. The practical aspects and a possible concept will be presented in Chapter IV. In this paragraph, I only focus on the mathematical description of this shaper and the advantages in terms of ENC. The processing channel from Figure 2.37, including the CSA stage and the MCDS filter will be discussed.

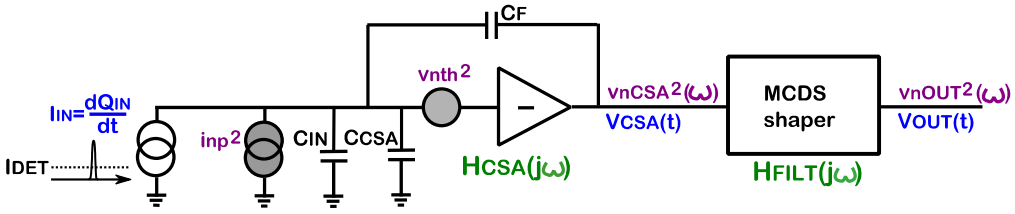


Figure 2.37 Signal processing channel for radiation detection with band-limited CSA and the MCDS filter.

2.3.5.1. Properties of the correlated noise – CDS

The MCDS method was first introduced in CCD imaging in a simpler form of the Correlated Double Sampling (CDS) [66]. The technique is used in amplifiers and comparators for offset reduction [61][67][68]. In the CDS processing a single measurement is accomplished with two samples: a baseline sample and a signal sample. The difference of the two samples gives the amplitude of the

measured signal. The principle is illustrated in Figure 2.38. The low frequency noise is highly reduced and the DC offset is totally removed in the final measurement. Noise has a decreasing correlation with increasing interval between the two samples, therefore a shorter interval between the two samples results in a higher accuracy of the measured amplitude, this is illustrated by comparison of the two plots in Figure 2.38: A) and B).

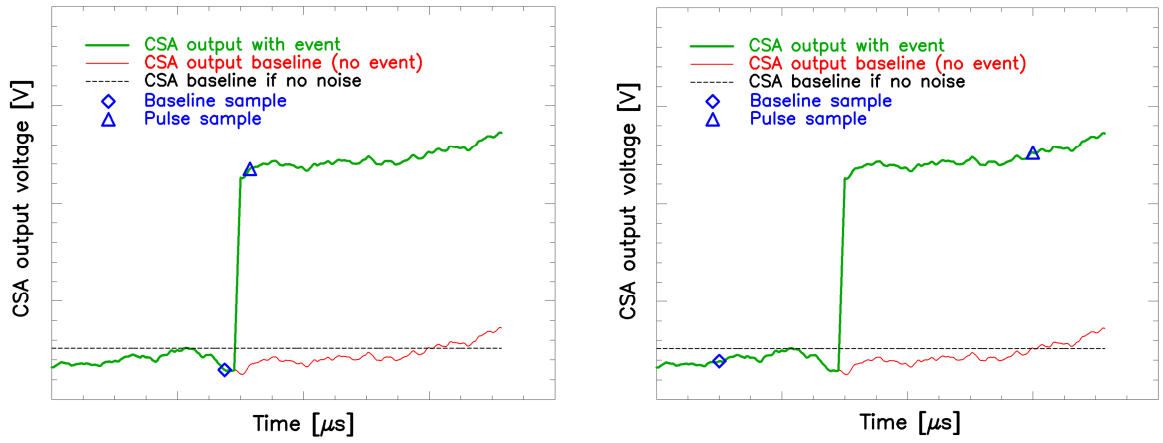


Figure 2.38 Illustration of a noisy CSA output and measurement of the output signal amplitude with Correlated Double Sampling (CDS). Two examples of different intervals are demonstrated. In A) where the interval is shorter, there is more correlation of noise between the two samples and the measurement is more accurate than in B) with much larger interval.

The CSA output voltage has three noise components (according to results from the paragraph 2.2.6). The low frequency noise, with PSD proportional to $1/f$ (due to the input flicker voltage noise) and $1/f^2$ (due to the input white current noise) is reduced by the double sampling. In these two cases the slowly decreasing correlations make the CDS filtering very efficient.

However there is also the white noise component (due to the input white voltage noise). In case of noise with a perfectly white PSD there is no correlation at all, since the autocorrelation function of the white noise is [69]:

$$R_{xx}(\tau): \begin{cases} \neq 0, \tau = 0 \\ = 0, \tau \neq 0 \end{cases} \qquad 2\text{-}89$$

This is not strictly true for the band limited white noise, as the one at the CSA output. In case of the band limited white noise, the autocorrelation can be observed for $\tau \neq 0$ however it decreases very rapidly with increasing τ [67][68].

To deal with the white voltage noise – a low pass filter is one way to reduce its contribution to the output noise power. It can be realized by reduction of the CSA bandwidth. However as the cutoff frequency decreases – the signal rise time increases. To be able to measure the full signal amplitude – the period between the two samples T_s must be higher than the signal rise time. However the increasing period results in lower correlation of the low frequency noise also present in the two samples. Consequently this method has certain limits.

2.3.5.2. Property of averaged samples – MCDS

Additional decrease of the white noise contribution can be achieved with averaging of multiple samples. In presence of an ideal white voltage noise source – averaging of k samples reduces the

output noise power by $1/k$ [69][75]. This principle is used in the MCDS processing. It is an extension to the CDS principle. In the MCDS each of the two CDS samples is composed of an average over k sub-samples: k samples before the event and k samples of the signal pulse. The MCDS procedure is depicted in Figure 2.39. It is performed with the following steps:

- Choose the number of samples k and the sampling period T_s
- Memorize k-samples before the event
- Calculate the average voltage $V_{AV\ base}$ over the baseline samples
- Memorize k-samples of the signal pulse
- Calculate the average voltage $V_{AV\ pulse}$ over the signal samples
- Perform the CDS, that is calculate the signal amplitude $V_{signal} = V_{AV\ pulse} - V_{AV\ base}$

In the rest of the text I will refer to this kind of processing, where $2k$ samples are involved, as the k-folded MCDS.

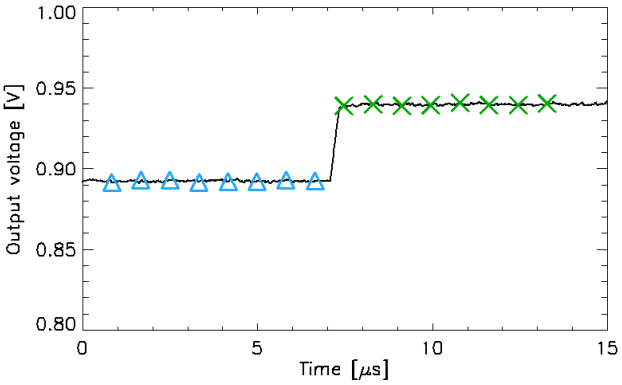


Figure 2.39 CSA noisy output – illustration of sampling for 8-fold MCDS ($k = 8$) with f_s set to 1200 kHz, blue triangles: 8 baseline samples (before event) to be averaged, green crosses: 8 signal samples (after event) to be averaged.

The interval between the last baseline sample and the first pulse sample is one more parameter to be adjusted. In the filter analysis, unless otherwise mentioned, this interval will be also set to T_s (the same as between any other consecutive samples). The presented process known as MCDS performs both low frequency and high frequency noise reduction. The following analysis aims determination of the noise parameters of this filter, so as to compare it with the optimal filter and with the CR-RC^N filter.

2.3.5.3. Time domain vs. frequency domain analysis

The CDS filtering is nowadays a mature technique and finds many applications. There are numerous publications of noise analysis and circuit measurements where the method is discussed. The CDS method is qualified into the category of time varying filters (definition in the paragraph 2.3.1). The justification is: only events covered by the weighting function around the discrimination trigger are processed. Other events (i.e. noise) are not processed. Only one output value per discrimination trigger is produced. Depending on the arrival with respect to the trigger the events around the trigger have different weights. The necessity for the time domain analysis of noise in time variant shapers is emphasized in [65] with the specific example of the CDS method based on the weighting function approach.

However there are also few other CDS noise calculation methods that can be found. For example these described in [80] and [81], where the autocorrelation function of the CSA output noise is first determined to calculate the noise after the CDS processing. In [68][79] and [82] the transient response of the system is first derived and then transformed into the frequency domain for noise calculation. The works [66] and [78] analyze CDS as a discrete system with approximation of the transfer function in the frequency domain through the z-transform. Finally, studying the subject of the CDS analysis – there are also examples of noise calculation purely in the frequency domain. Namely, in [61] the power spectrum of noise sampled at the CSA output is determined first, in order to perform then discrete operations in the frequency domain.

All these examples that treat CDS in the frequency domain are intuitive and comprehensive. However the mathematical reasoning for the frequency analysis of the time variant system is very often omitted. The publication [76] shows the link between the time variant filters and the fact they can be analyzed in the frequency domain, as long as the filter is linear. It is explained that the weighting function of the time invariant filters is equivalent to the impulse response, while in case of time variant filters the impulse response can be only defined temporarily: $H(j\omega, t_m)$. A temporary impulse response corresponds to a single measurement at the time t_m. This temporary function, defined with respect to the measurement time, is identical for each time of interest related to the gating signal. Therefore a common transfer function $H(j\omega)$ can be defined for all of these events. Basing on this principle, in [64] the CDS system is described by a weighting function and then is related to the frequency domain. The total output noise is then calculated and compared with the time domain result. A direct comparison of the time and the frequency domain analyses is presented also in [60], however through different arguments: the CDS is actually viewed as a time invariant system, being a sum of many events with identical processing scheme.

Concerning the more general MCDS processing there are fewer works to refer to. The MCDS noise analysis is presented in the time domain in [85]. The frequency domain MCDS transfer functions are shown in [78] for the 4-folded MCDS and for a general case in [85], but without noise calculations. On these foundations – I aim to describe the MCDS noise both in the time domain and in the frequency domain, for each of the three main noise components (white – parallel and series, and flicker series noise). The time domain analysis will be an extension of [65] and [85], based on the weighting function. Meanwhile the frequency domain analysis will be similar to the one described in [61]. In both cases the goal is to understand the effects of the parameters: CSA bandwidth B_w, sampling frequency $f_s = 1/T_s$, and the number of samples k.

The complete filter noise description with either approach can only be obtained numerically. This is the main reason why I perform the calculations with two different methods. I will be able to compare the results obtained with both procedures and to confidently conclude the noise parameters used in the general form of the ENC equation (equations *2-74*, *2-75* and *2-76* introduced in the paragraph 2.3.2). Finally, with the calculated parameters it will be possible to compare the MCDS with other filters used in the radiation detection, what is done in the paragraph 2.3.6. These results are used later in Chapter III and Chapter IV to optimize the final readout ASIC.

2.3.5.4. MCDS analysis in the time domain

MCDS is known as a time variant system. The measurement instants are not defined in advance, but are triggered by the gating signal upon an event. However the system assumes the same processing pattern in each measurement. The weighting function describes the influence of noise pulses on the output at the measurement time. In the first part of the time domain MCDS analysis – I will describe the filter's weighting function. For clarity I will start with the CDS weighting function to then continue with the general case of the MCDS. Secondly I will use the derived weighting function to determine the total noise $\overline{v_{nOUT}{}^2}$ at the output of the MCDS filter.

CDS weighting function

The CDS processing is the simplest form of MCDS with $k = 1$. Its weighting function $w(\tau)$ could be simplified to a sum of two weighting functions related to the two CDS samples. The first one $w_1(\tau)$, corresponding to the first sample taken at the time $\tau_1 = 0$ is expressed as:

$$w_1(\tau) = -\frac{1}{C_F}\left[1 - e^{(\tau - T_s)/\tau_{CSA}}\right] \cdot 1(T_s - \tau) \qquad 2\text{-}90$$

Where the time constant τ_{CSA} is related to the CSA and equals $1/2\pi B_w$ and T_s is the sampling period. The second elementary function $w_2(\tau)$ corresponds to the second sample taken at the time $\tau_2 = T_s$ with the negative weight:

$$w_2(\tau) = \frac{1}{C_F}\left[1 - e^{\tau/\tau_{CSA}}\right] \cdot 1(-\tau) \qquad 2\text{-}91$$

The complete weighting function describing the CDS process is defined as [65]:

$$w(\tau) = w_1(\tau) + w_2(\tau) = \begin{cases} \frac{1}{C_F}\left[1 - e^{\tau/\tau_c}\right] - \frac{1}{C_F}\left[1 - e^{(\tau - T_s)/\tau_{CSA}}\right], \tau \le 0 \\ -\frac{1}{C_F}\left[1 - e^{(\tau - T_s)/\tau_{CSA}}\right], 0 < \tau \le T_s \\ 0, \tau > T_s \end{cases} \qquad 2\text{-}92$$

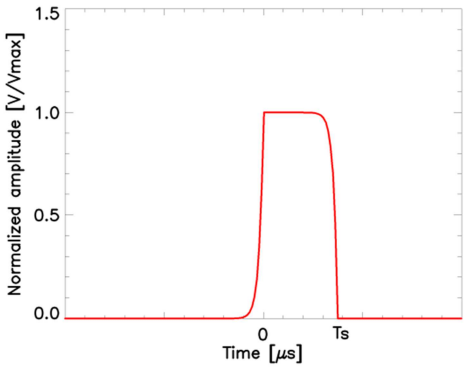


Figure 2.40 Normalized weighting function of the CDS filter $w_N(\tau)$.

The function $w(\tau)$ is valid for the complete electronic processing chain: the CSA and the filter. More often used however is its normalized form $w_N(\tau)$ where it is divided by the channel gain of: $\left[1 - e^{-T_s/\tau_{CSA}}\right]/C_F$. The normalized CDS weighting function is illustrated in Figure 2.40. Using this

function the system ENC can be calculated directly with equations *2-62*, *2-68* and *2-71* given in the paragraph 2.3.2.

MCDS weighting function

The CDS weighting function has been composed of two segments. Meanwhile the more general k-folded MCDS has $2k$ segments, meaning that it is a sum of this many elementary weighting functions. I will not write each elementary function separately, only provide the description of the complete $w(\tau)$. In order to simplify the notation, a function $p(\tau, k_n)$ will be first introduced:

$$p(\tau, k_n) = \frac{1}{C_F} \cdot \left[1 - e^{(\tau+(k_n-k)T_s)/\tau_{CSA}}\right] \cdot 1(k_n T_s - \tau) \qquad 2\text{-}93$$

Where k_n is an integer number between 1 and k, T_s is the sampling period and τ_{CSA} is the CSA time constant equal to $1/2\pi B_w$. The MCDS weighting function can be represented as:

$$w(\tau) = \begin{cases} [p(\tau,0)+..+p(\tau,k-1)] - [p(\tau,k)+..+p(\tau,2k-1)] & \tau \le -(k-1)T_s \\ [p(\tau,0)+..+p(\tau,k-1)] - [p(\tau,k)+..+p(\tau,k+k_n-1)] & -k_nT_s < \tau \le -(k_n-1)T_s \\ [p(\tau,0)+..+p(\tau,k-1)] - p(\tau,k) & -T_s < \tau \le 0 \\ [p(\tau,0)+..+p(\tau,k-1)] & 0 < \tau \le T_s \\ [p(\tau,0)+..+p(\tau,k_n-1)] & (k-k_n)T_s < \tau \le (k-k_n+1)T_s \\ p(\tau,0) & (k-1)T_s < \tau \le kT_s \\ 0 & \tau > kT_s \end{cases} \qquad 2\text{-}94$$

This few-lines long formula is a possibly compact description – but the form of the described function might not be obvious immediately. Therefore I will go on straight to its visualization. For that I use the normalized weighting function: divided by the channel gain, which is later used in the ENC calculations. In case of MCDS this gain is equal to $\sum_{i=1}^{k}\left(1 - e^{-i\cdot T_s/\tau_{CSA}}\right)/C_F$. The normalized weighting function $w_N(\tau)$ for a 4-folded MCDS is illustrated in Figure 2.41. The eight segments can be clearly distinguished: four "steps-up" and four "steps-down". On the same plot there are three $w_N(\tau)$ functions plotted, each with a different value of the ratio: T_s/τ_{CSA}.

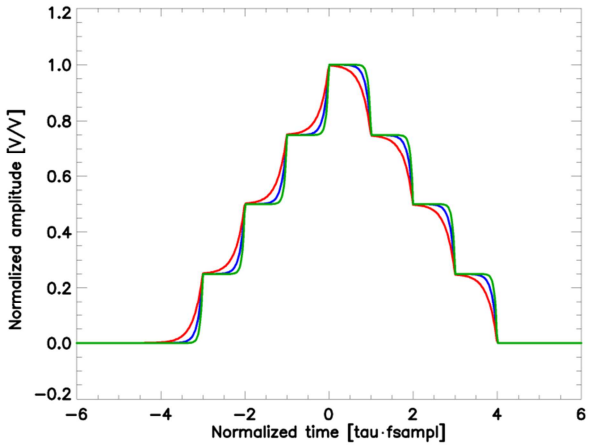
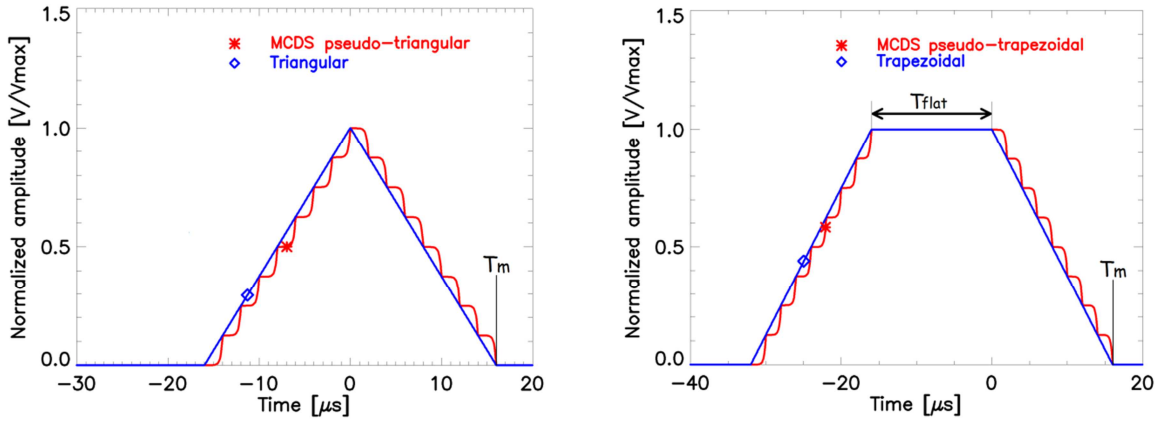


Figure 2.41 The weighting function for 4-folded MCDS, $k = 4$ with variable ratio T_s/τ_{CSA}, which is set to: 5 (red), 10 (blue), 20 (green).The most sharp shape corresponds to $T_s/\tau_{CSA} = 20$.

The highest value of the ratio T_s/τ_{CSA} in Figure 2.41 equals 20. In this configuration the MCDS resembles the most a multiple step function. Meanwhile for T_s/τ_{CSA} of much lower values a single step might not reach its maximum when the next step begins. According to the relationship between the CSA rise time and its time constant ($\tau_{CSA} = 1/2\pi B_w$), the value of T_s/τ_{CSA} should be at least 5 for the signal to achieve 0.99 % of its maximum value. With such a low T_s/τ_{CSA} (and ideally with a higher number of samples) the MCDS weighting function starts to resemble the weighting function of the triangular shaper, illustrated in Figure 2.42 A). This is valid with my initial assumption that the interval between the MCDS samples is always identical and equal to T_s. With this assumption the described MCDS shaper indeed resembles the triangular shaper. In many known applications however, the MCDS weighting function looks more like the trapezoidal filter with the additional flat top, as shown in Figure 2.42 B). For this reason MCDS is often referred to as a pseudo-trapezoidal shaper. The triangular shaper is only a variation of the trapezoidal, where the flat top duration T_{flat} is set to zero [43][70]. The flat top is introduced to avoid the influence of the charge collection time on the measurement and to assure a good measurement accuracy with the maximum signal gain despite the finite CSA bandwidth [10][71][73]. These are motivations for using longer trapezoidal weighting function rather than the triangular one. The drawback is that the flat top in the weighting function is responsible for an increase of the parallel noise contribution.



A) B)

Figure 2.42 Illustration of 8-folded MCDS as the pseudo-trapezoidal shaper. A) MCDS and triangular normalized weighting functions B) MCDS and trapezoidal normalized weighting functions both with identical flat-top duration of T_{flat}. In case of the MCDS the flat top is realized by the modified delay between the two middle samples: from T_s in the semi-triangular to $T_{flat} + T_s$ in the semi-trapezoidal. T_s/τ_{CSA} is set to 12.5.

Applications of MCDS with the flat-top are described in [84][86][88]. In my analysis of MCDS, however, it has been assumed that the sampling frequency is equal throughout the entire signal acquisition. This is mainly because of the perspective for the CdTe detector readout application, where the detector signal collection time is expected to be faster than the CSA time constant τ_{CSA}, posing no issue of ballistic deficit. Of course, when necessary, the presented MCDS weighting function could be modified to the pseudo-trapezoidal one by time shift of τ by T_{flat} in the last three lines of the $w(\tau)$ description *2-94*, that is to have:

$$w_{pseudo\ trapez}(\tau) = \begin{cases} w(\tau), for\ \tau \le kT_s \\ w(kT_s), for\ kT_s < \tau \le kT_s + T_{flat} \\ w(\tau - T_{flat}), for\ kT_s + T_{flat} < \tau \le 2kT_s + T_{flat} \end{cases} \qquad 2\text{-}95$$

In the function shape this would modify only the peaking part by making it long and flat, as shown in Figure 2.42 B). However, in the noise calculation, I will focus only on the special MCDS case with the pseudo-triangular weighting function. Having derived the weighting function of interest $w(\tau)$ defined in *2-94*, the next step in the channel analysis is the noise calculation.

Input parallel white noise contribution to ENC

The contribution of the input referred parallel white noise ${i_n}_p^2$ to the ENC of the detection chain with CSA and a filter has been derived in the paragraph 2.3.2 and it equals:

$$ {ENC_p}^2 = \frac{1}{q^2} \cdot 0.5 \cdot {i_n}_p^2 \cdot \int_{-\infty}^{\infty} [w_N(\tau)]^2 \, d\tau \qquad 2\text{-}96 $$

The equation can be interpreted geometrically as the scaled area under the $[w_N(\tau)]^2$ plot. For the MCDS weighting function, with its specific symmetry, the integral $\int_{-\infty}^{\infty}[w_N(\tau)]^2 d\tau$ can be written as $\left(2 \cdot \sum_{i=1}^{k} i^2/k^2 - 1\right) \cdot T_s$, which is equal to $T_s\,(2k^2+1)/3k$. This is illustrated in Figure 2.43 by superimposing a grid on the squared weighting function and by shading certain areas to indicate the complementary regions. The drawing on the right of Figure 2.43 shows the area which is equivalent to that under the $[w_N(\tau)]^2$ plot.

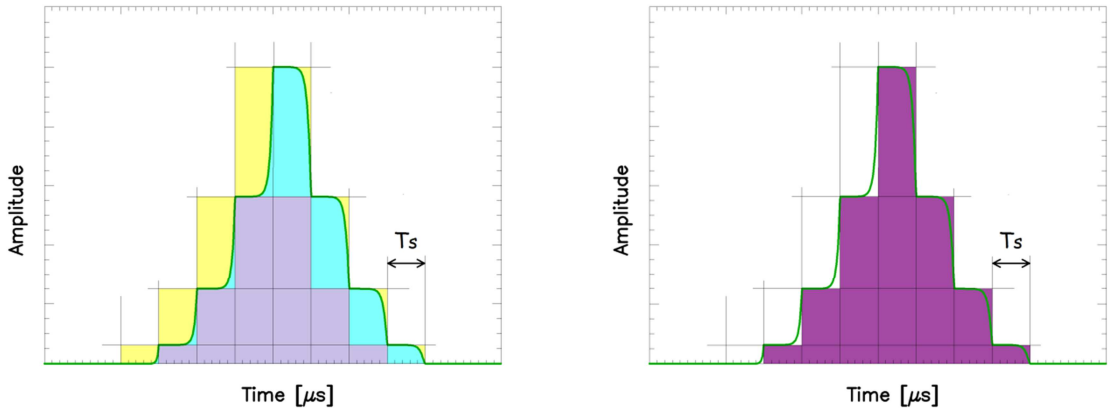


Figure 2.43 Geometrical illustration of the integral $\int_{-\infty}^{\infty}[w_N(\tau)]^2\, d\tau$ calculation in case of the 4-folded MCDS.

The result leads to the simplified expression of ENC due to the input parallel white noise, valid for the MCDS processing:

$$ {ENC_p}^2 = \frac{1}{q^2} \cdot 0.5 \cdot {i_n}_p^2 \cdot T_s \cdot \frac{2k^2+1}{3k} \qquad 2\text{-}97 $$

The ENC is found to be independent of the CSA time constant τ_{CSA}, it only varies with the number of samples k and with the sampling period T_s. The result is valid as long as T_s is longer than the rise time, which corresponds to $T_s/\tau_{CSA} \geq 5$.

The squared ENC is plotted as a function of k in Figure 2.44. From the illustration it is concluded, that with the increasing number of samples, the squared ENC contribution (that is ${ENC_p}^2$) increases almost linearly. The result can be explained by the decreasing noise correlation between the samples from which the MCDS is constructed. This is a consequence of the increasing time interval between the first and the last sample as k gets larger (assuming a constant value of T_s). This translates directly to the decreasing correlation between the samples, as the interval between samples increases.

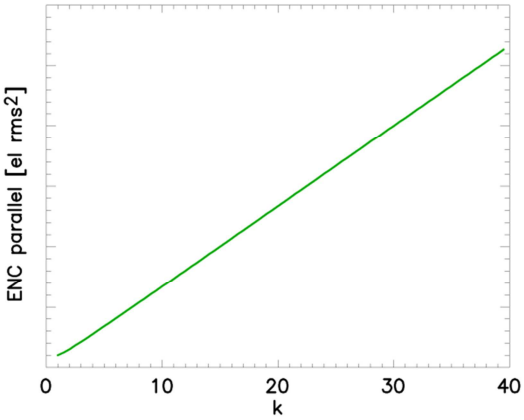


Figure 2.44 Illustration of the $ENC_p{}^2$ plot as the function of the number of samples k for a k-folded MCDS. The function is increasing according to the expression $2k^2 + 1/k$.

Input series white noise contribution to ENC

The derivative of the weighting function is plotted in Figure 2.45. It decides about filtering properties for the series white input noise. For the series noise it can be shown that the output integrated noise decreases by a factor of 2 as the CSA time constant τ_{CSA} is increased twofold. This is demonstrated by the calculation of the integral:

$$ENC_{n\,th}{}^2 = \frac{1}{q^2} \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot 0.5 \cdot \int_{-\infty}^{\infty} [w'_N(\tau)]^2 \, d\tau \qquad \text{2-98}$$

The equation contains the derivative of the weighting function. The derivative of the MCDS weighting function is illustrated in Figure 2.45, with three different values of the T_s/τ_{CSA} ratio. The examples are shown for the 4-folded MCDS. Its specific symmetry permits to analyze the integral in the ENC equation $\int_{-\infty}^{\infty}[w'_N(\tau)]^2 \, d\tau$ in a general MCDS case.

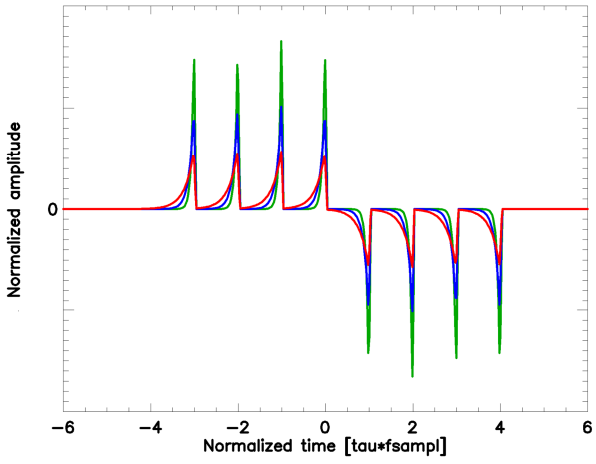


Figure 2.45 Derivative of the weighting function for 4-folded MCDS, $k = 4$ witth variable ratio T_s/τ_{CSA}: 5 (red), 10 (blue), 20 (green). The most sharp shape corresponds to $T_s/\tau_{CSA} = 20$.

If the ratio T_s/τ_{CSA} is higher than 5 (the sampling period is large enough) then the integral $\int_{-\infty}^{\infty}[w'_N(\tau)]^2 \, d\tau$ from the ENC equation can be approximated to a sum of $2k$ identical integrals $\int_0^{\infty}(1/k \cdot \left[1 - e^{-\tau/\tau_{CSA}}\right]')^2 \, d\tau$, what is illustrated in Figure 2.46. The $1/k$ factor is the consequence

of the changing amplitude of each "step" in the normalized weighting function (whose total amplitude is always: 1) as the number of samples k is changing. This can be concluded by comparison of the MCDS normalized weighting function in Figure 2.40, Figure 2.41 and Figure 2.42, with k set respectively to 1, 4 and 8.

In consequence, the solution of the integral from the ENC equation *2-98* can be written as:

$$\int_{-\infty}^{\infty} [w'_N(\tau)]^2 \, d\tau = 2k \cdot \int_0^{\infty} \frac{1}{k^2 \cdot {\tau_{CSA}}^2} \cdot e^{-2\tau/\tau_{CSA}} \, d\tau = \frac{1}{k \cdot \tau_{CSA}} \qquad 2\text{-}99$$

The integral is only dependent on the number of samples k and on the CSA time constant τ_{CSA} related to its bandwidth $\tau_{CSA} = 1/2\pi B_w$. Meanwhile the sampling period T_s is of no importance. Now I can rewrite the equation for the ENC due to input white series noise with the result obtained for the MCDS:

$$ENC_{n\,th}{}^2 = \frac{1}{q^2} \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot \frac{0.5}{k \cdot \tau_{CSA}} \qquad 2\text{-}100$$

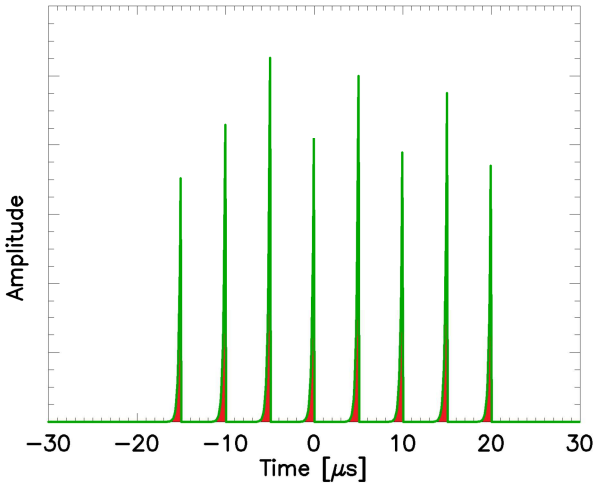


Figure 2.46 Geometrical illustration of the integral $\int_{-\infty}^{\infty}[w'_N(\tau)]^2\,d\tau$ calculation in case of the 4-folded MCDS: it is a sum of 8 integrals: $\int_0^{\infty} \cdot \left(\left[1 - e^{-\tau/\tau_{CSA}}\right]^2\right)' d\tau$ (provided that $T_s/\tau_{CSA} \geq 5$). The variable amplitude of each peak is a consequence of precision setup in the numerical calculations, theoretically all peaks should have equal amplitude.

The ENC expression *2-100* reveals that change in the sampling period T_s does not affect the white noise contribution to the output as long as the ratio T_s/τ_{CSA} is higher than 5. What is observed is that the proportionality of $ENC_{n\,th} \sim 1/\sqrt{k}$ occurs. This is in accordance with the initial theory of the white noise averaging, and consequently the choice of processing extended to multiple samples from the basic Correlated Double Sampling form. Further significant result which is important for the channel design – is the importance of the CSA parameters. Reducing its bandwidth (thus increasing the τ_{CSA} constant) also reduces ENC due to the input white noise: $ENC_{n\,th} \sim 1/\sqrt{\tau_{CSA}}$.

Input series flicker noise contribution to ENC

The contribution of the series flicker noise to the total ENC will be examined by analyzing the previously derived (paragraph 2.3.2) general equation in the time domain:

2.3. Noise filtering in the detection chain

$$ENC_f{}^2 = \frac{1}{q^2} \cdot v_{n\,f}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot 0.5 \cdot 2 \cdot \pi \cdot \int_{-\infty}^{\infty} \left[w_N{}^{(1/2)}(\tau)\right]^2 d\tau \qquad 2\text{-}101$$

The derivative of order $1/2$ of the weighting function describes contribution of the input-referred noise $v_{n\,f}^2$ with the $1/f$ distribution. I have examined the equation with respect to the MCDS processing by applying it in the numerical calculations. I have calculated the partial derivative $w_N{}^{(1/2)}(\tau)$ by applying the procedure described in 2.3.2 through the equation *2-72*.

First of all, in Figure 2.47 I show a plot of the fractional derivative $w_N{}^{(1/2)}(\tau)$ of the 4-folded MCDS weighting function, with a variable CSA constant τ_{CSA} and a fixed sampling period T_s. The plotted result resembles the case of the 3-folded MCDS fractional function reported in [53].

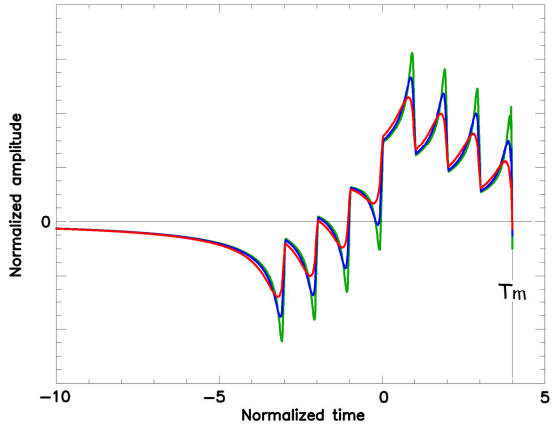


Figure 2.47 Derivative of the order 0.5 of the weighting function for 4-folded MCDS, $k = 4$ with a variable ratio T_s/τ_{CSA} set to: 5 (red), 10 (blue) and 20 (green). The most sharp shape corresponds to $T_s/\tau_{CSA} = 20$.

From Figure 2.47 it can be concluded that the highest influence on ENC is due to the noise within the time period equal to kT_s, preceding the measurement. The time period equal to kT_s, preceding the event arrival, contributes also the noise, however, in a significantly smaller amount. What is new in this analyzed case, on contrary to the parallel white and the series white noise cases: the contribution of the low frequency series noise "older" than kT_s before the event – is non-zero.

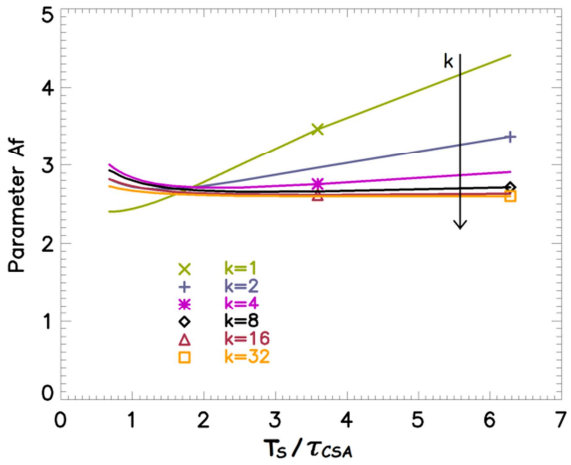


Figure 2.48 Characterization of the MCDS noise parameter A_f, equal to $\pi \int_{-\infty}^{\infty} \left[w_N{}^{(1/2)}(\tau)\right]^2 d\tau$, as a function of the ratio: T_s/τ_{CSA} and for different number of samples k. This is the result of numerical calculations using the MCDS weighting function.

Secondly, having not succeeded in finding an analytical solution, I have calculated the expression $\pi \int_{-\infty}^{\infty}\left[{w_N}^{(1/2)}(\tau)\right]^2 d\tau$ from the ENC_f equation numerically, for different values of the number of samples k and as a function of the ratio: T_s/τ_{CSA}. The expression describes the A_f noise parameter (defined in the paragraph 2.3.2). The results are illustrated in Figure 2.48, for k ranging from 1 to 32. The immediate conclusion is that the expression of interest is almost independent of the number of samples k, if k is higher than 4. Furthermore for high values of the ratio T_s/τ_{CSA} (on the x-axis) corresponding to the sampling period higher than the CSA time constant, what is typically the case in the applications, the expression $\pi \int_{-\infty}^{\infty}\left[{w_N}^{(1/2)}(\tau)\right]^2 d\tau$ becomes almost constant.

Noise parameters for ENC calculations obtained in time domain

The ENC equations derived in the paragraph 2.3.2 contain the noise parameters: A_p, A_{th} and A_f. Now having analyzed the ENC equations with respect to the MCDS filter, we can determine the values of these parameters. Below, I present the results of comparison of the ENC results obtained for each MCDS noise component with the already known general form ENC equations *2-74*, *2-75* and *2-76*:

$$ENC_p{}^2 = \frac{t_{peak}\cdot i_{n\,p}^2}{q^2}\cdot A_p \qquad where\ A_p = 0.5\int_{-\infty}^{\infty}[w_N(\tau)]^2\,d\tau \approx \frac{0.5\cdot(2k^2+1)}{3\cdot k^2} \qquad 2\text{-}102$$

$$ENC_{th}{}^2 = \frac{v_{nt}^2\cdot {C_{INnoise}}^2}{q^2\cdot t_{peak}}\cdot A_{th} \qquad where\ A_{th} = 0.5\int_{-\infty}^{\infty}[w'_N(\tau)]^2\,d\tau \approx \frac{0.5\cdot T_s}{\tau_{CSA}} \qquad 2\text{-}103$$

$$ENC_f{}^2 = \frac{v_{nf}^2\cdot {C_{INnoise}}^2}{q^2}\cdot A_f \qquad where\ A_f = \pi\int_{-\infty}^{\infty}\left[{w_N}^{(1/2)}(\tau)\right]^2 d\tau \qquad 2\text{-}104$$

Where $C_{INnoise}$ is equal to $C_F + C_{IN} + C_{CSA}$. The parameter t_{peak} in the k-folded MCDS processing is equal to kT_s and T_s is the sampling period. Previously, in the paragraph 2.3.2, I have defined the noise parameters as constants whose values depend on the shaper type. In case of the MCDS method the weighting function shape changes with the number of samples k and with the sampling period T_s, consequently also, the noise parameters are not strictly constant. I demonstrate it in Figure 2.49 and Figure 2.50, where my results of the noise parameters obtained through numerical calculations (involving numerical solution of the three integrals) are shown, respectively: as a function of the sampling period T_s and the number of samples k.

It is concluded that: the parameters A_p and A_f can be regarded as constant if the number of samples k is above 4. Also at this condition – the parallel noise parameter A_p approaches the value calculated for the triangular shaper [43][70]. The parameter related to the series white noise A_{th} shows a strong dependency on the sampling period T_s. However as T_s gets smaller – the parameter A_{th} tends to approach the value obtained for the triangular and the trapezoidal shaper [43][70]. Numerical simulations confirm that the parameter's value is independent of k. Finally in Figure 2.49 and Figure 2.50 the numerical calculations of the noise parameters described by the complete formulas A_p and A_{th} of are compared with the proposed analytical solutions. The values of both parameters closely follow those calculated numerically. However in case of A_{th}, where the assumption of $\mathrm{T_s}/\tau_{\mathrm{CSA}} \geq 5$ was made, the two plots significantly diverge when the sampling period T_s becomes too low with respect to τ_{CSA}.

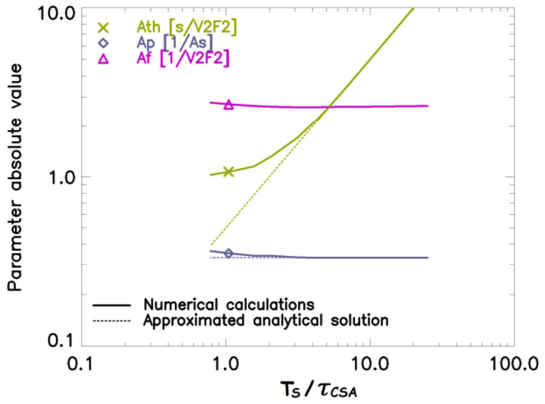


Figure 2.49 ENC parameters for MCDS as a function of the sampling period T_s. Number of samples is fixed to 16, the CSA bandwidth set to 0.8 MHz ($\tau_{CSA} = 200\ ns$). The results calculated numerically (from the corresponding integral containing the weighting function) are compared with the analytical solutions in the case of $T_s/\tau_{CSA} \geq 5$. No analytical solution for A_f.

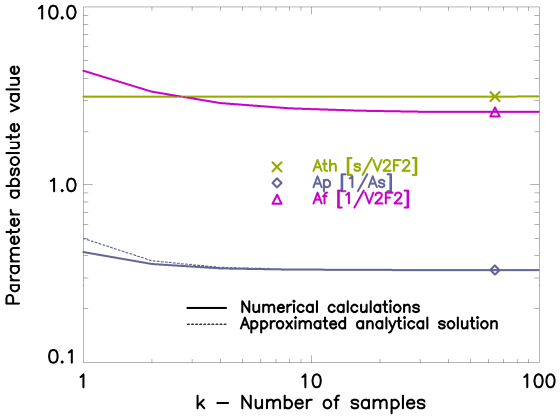


Figure 2.50 ENC parameters for MCDS as a function of number of samples k. Sampling frequency fixed to 0.8 MHz, the CSA bandwidth set to 0.8 MHz ($\tau_{CSA} = 200\ ns$). The results calculated numerically (from the corresponding integral containing the weighting function) are compared with the analytical solutions in the case of $T_s/\tau_{CSA} \geq 5$. No analytical solution for A_f.

MCDS processing with the lowest ENC

I have derived the analytic solutions (*2-102* and *2-103*) describing the contribution to ENC in the MCDS system of the parallel white and the series white input noise sources. In both expressions the number of samples k is of high importance. From the obtained results an optimum number of samples k_{opt} can be found –with the lowest value of the total ENC achievable in a detection system with the MCDS filter. The contribution of the flicker noise has a negligible dependence on the sampling period T_s and on the number of samples k – therefore it has a minor influence on the shaper optimization. Since ${ENC_p}^2$ increases almost linearly (Figure 2.44) with k and ${ENC_{n\,th}}^2$ decreases linearly with k – the lowest total ENC is achieved when ${ENC_{n\,th}}^2 = {ENC_{n\,p}}^2$. From this equality I can identify the optimal number of samples k_{opt}:

$$k_{opt} = \sqrt{\frac{3 \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2}{2 \cdot \tau_{CSA} \cdot {i_{n\,p}}^2 \cdot T_s}} - 0.5 \qquad \textit{2-105}$$

The obtained value k_{opt} indicates the optimal MCDS filter: k_{opt}-folded, where the total number of samples taking part in a single measurement is $2k_{opt}$. The optimal number of samples depends on

several parameters of the system: the input referred noise sources ${i_n}_p^2$ and $v_{n\,th}^2$, and the input impedance seen by these sources. Then the CSA characteristics that determine τ_{CSA} result in the requirement for a higher number of MCSD samples as the CSA time constant τ_{CSA} decreases, leading to a faster output rise time. This is the effect of increasing system's bandwidth and therefore also the noise bandwidth. It can be compensated by averaging a higher number of MCDS samples. Finally k_{opt} decreases as the sampling period T_s gets longer: this can be explained by the balancing noise correlation between the k-samples.

If the k_{opt} value determined with the described method is higher than 4 and the sampling period is set possibly high (but to maintain the condition of $\mathrm{T_s}/\tau_{\mathrm{CSA}} \geq 5$), then according to Figure 2.48, the result should indeed represent the optimal number of samples, leading to the lowest ENC achievable with the MCDS processing given by the equation:

$$ENC_{min}^{\ 2} = \frac{1}{q^2}\sqrt{\frac{2 \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot {i_n}_p^{\ 2} \cdot T_s}{3 \cdot \tau_{CSA}}} \qquad \textit{2-106}$$

The obtained minimum ENC can be directly compared with the performance of the optimal filter Cusp given in *2-80* (2.3.3). Assuming the most advantageous conditions in MCDS: $k = k_{opt}$ and $\mathrm{T_s}/\tau_{\mathrm{CSA}} = 5$ as well as neglecting the flicker noise contribution, ${ENC_{\min MCDS}}^2 = 1.8 \cdot {ENC_{\min Cusp}}^2$.

2.3.5.5. MCDS analysis in the frequency domain

The alternative to the time domain weighting function method, for analyzing noise of the MCDS system, is based on the frequency domain. I will propose the complete noise analysis based on this approach. Finally I will compare the ENC results obtained with both methods.

The detection chain for the MCDS processing can be represented by an equivalent circuit, which consists of a CSA, a sampling stage and a discrete filter, as shown in Figure 2.51. The real CSA with bandwidth B_w is represented here by an ideal CSA followed by the low pass filter. The sampling block output is a sequence of the samples with the interval $T_s = 1/f_s$. In the described system the $2B_w$ is the Nyquist rate f_{Nyq}. The sampled signal can be decomposed into a sum of sine waves with the maximum frequency B_w. Sampling with a frequency f_s lower than f_{Nyq} will cause aliasing of the frequency components in the range from $f_s/2$ to B_w. Very often in discrete systems – that condition is avoided. In the MCDS filtering this is however a situation that typically one has to deal with.

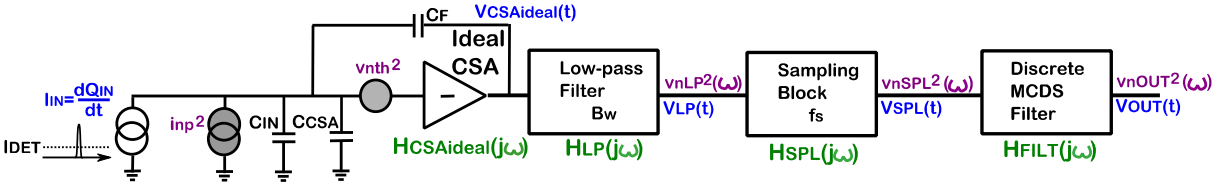


Figure 2.51 Signal processing channel for radiation detection with the ideal CSA, the low pass filter the sampling stage and the discrete MCDS filter. The system is equivalent to the one presented in Figure 2.37.

For a k-folded MCDS the channel gain, corresponding to the measurement time $t_m = k/f_s$, is described by the equation:

2.3. Noise filtering in the detection chain

$$V_{OUTmax}/Q_{IN} = \frac{\sum_{i=1}^{k}\left(1 - e^{-i\cdot 2\pi\cdot B_w/f_s}\right)}{k \cdot C_F} \qquad 2\text{-}107$$

To approach the target of calculating the ENC – the output noise PSD ${v_{nOUT}}^2$ must also be known. This task requires a more detailed analysis. I will go through the following steps related to the block description in Figure 2.51: starting with the low pass filter noise PSD ${v_{nLP}}^2$, followed by description of the sampled noise ${v_{nSPL}}^2$ and finally the noise PSD ${v_{nOUT}}^2$ at the discrete MCDS filter output.

The signal PSD at the CSA output assuming the detection chain composed of an ideal CSA and a low pass filter, can be written as:

$${v_{nLP}}^2(f) = {i_{nIN}}^2(f) \cdot |H_{CSAideal}(j\omega)|^2 \cdot |H_{LP}(j\omega)|^2 \qquad 2\text{-}108$$

Where ${i_{nIN}}^2(f)$ is the total input referred noise current, derived in the paragraph 2.2.6. It is described as the sum of the three noise contributors: ${i_{np}}^2$ and ${v_{nth}}^2/{Z_{INnoise}}^2$ and ${v_{nf}}^2/{Z_{INnoise}}^2$. $Z_{INnoise}(\omega)$ is the impedance seen by the input referred voltage noise sources also derived in the paragraph 2.2.6. The described noise PSD ${v_{nLP}}^2(f)$ is equivalent to noise PSD at the output of the real, band-limited CSA. The transfer functions of the CSA $|H_{CSAideal}(j\omega)|^2$ and the low-pass filter $|H_{LP}(j\omega)|^2$ are described respectively with the expressions: $1/(\omega C_F)^2$ and $1 + (\omega/2\pi B_w)^2$.

Noise sampling

The output of the low pass filter is next processed by the sampling block. The outcome is a discrete signal V_{SPL} with the sampling frequency equal to f_s. The sampled signal can be described with the equation [67]:

$${v_{nSPL}}^2(f) = {i_{nIN}}^2(f) \cdot sinc^2\left(\frac{\pi \cdot f}{f_s}\right) \sum_{n=0}^{+\infty} |H_{CSAideal}(f - nf_s)|^2 \cdot |H_{LP}(f - nf_s)|^2 \qquad 2\text{-}109$$

Where the expression $sinc^2(\pi f/f_s)$ is the Fourier transform of the rectangular window function of width $T_s = 1/f_s$ and is related to the sampling operation.

From the form of the equation *2-109*, it becomes more evident why the real band-limited CSA in the processing chain has been replaced with the ideal CSA followed by the low pass filter (Figure 2.37). The separation of the real CSA transfer function is done to isolate the aliasing effect of the baseband (when $f_s < 2B_w$). This phenomenon depends both on the low-pass filter bandwidth: B_w and the sampling frequency: f_s. Descriptions of the sampled noise power spectrum can be found in [67][68][77]. In [67] it is proposed to simplify the sum in range $n = [0, \infty]$ to $n = [0, N]$. The number N is the closest integer to the undersampling ratio defined as: $N_u = 2B_w/f_s$. The case of $N_u = 1$, corresponds to the Nyquist rate sampling. Below that value no aliasing takes place, however the high sampling frequency prevents the full CSA amplitude measurement, which is usually not the desired condition.

In case of $N_u > 1$ the sampled noise PSD ${v_{nSPL}}^2(f)$ is limited to the baseband frequencies from 0 to $f_s/2$ and the undersampling occurs. The aliased components of the CSA output PSD that are in the foldover frequency band $f_s/2$ to B_w are also present in the output PSD. These multiples of the $0..f_s/2$ band are shifted to the base band range. This effect is illustrated graphically in Figure 2.52.

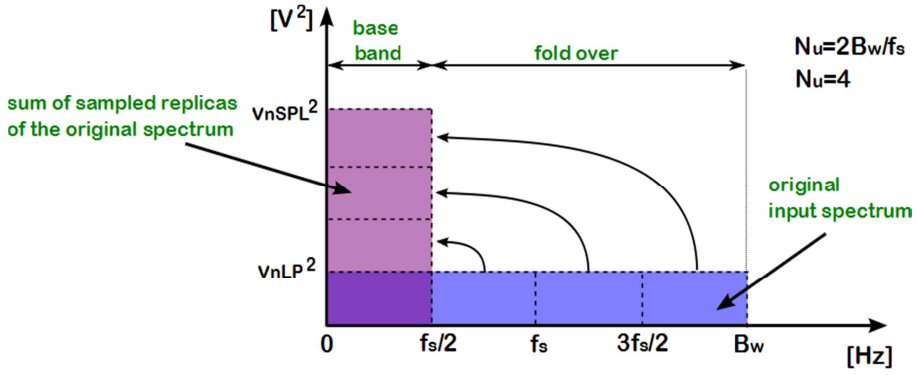


Figure 2.52 A simplified illustration of the aliasing effect caused by undersampling. The noise PSD $v_{nLP}{}^2$ at the output of a low-pass filtered CSA (only the ideally filtered white noise is shown) and the output PSD – of the sampled noise $v_{nSPL}{}^2$. The output PSD is limited to the baseband equal to $f_s/2$ and is constructed from shifted replicas of the original equal to the N_u-multiple of the input spectrum. In the example N_u is set to 4.

Finally the output noise PSD of interest $v_{nOUT}{}^2$ – of the complete MCDS detection system can be described with the equation using the obtained results:

$$v_{nOUT}{}^2(f) = v_{nSPL}{}^2(f) \cdot |H_{FILT}(j\omega)|^2 \qquad 2\text{-}110$$

Where $H_{FILT}(j\omega)$ - is the transfer function of the k-folded discrete MCDS process (Figure 2.51). Let's determine the transfer function.

MCDS transfer function

The transfer function for a multi correlated double sampling will be first described in the z-domain. It is represented by a difference of two sets of samples: $A_{v\,pulse} - A_{v\,base}$ (Figure 2.39). The first set $A_{v\,base}$ is the average of k-baseline samples: $(v_{base\,1} + v_{base\,2} + .. + v_{base\,k})/k$, where k is an integer higher than zero and corresponding to k-folded MCDS (or CDS in case of $k = 1$). The sampling interval between the samples is equal to $T_s = 1/f_s$, therefore the respective sampling times are $t_{base\,k} = (k-1)/f_s$ for each k-th baseline sample $v_{base\,k}$. The second set $A_{v\,pulse}$ is the average of k signal samples: $(v_{pulse\,1} + v_{pulse\,2} + .. + v_{pulse\,k})/k$. The corresponding sampling time instant is: $t_{pulse\,k} = k/f_s + (k-1)/f_s$ for each k-th signal sample $v_{pulse\,k}$. Consequently the z-transform of the k-folded MCDS system composed of the sequence of $2k$ samples can be written as [85]:

$$H_{FILT}(z) = \frac{1}{k} \cdot \sum_{i=0}^{k-1} \left(z^{-(k+i)/f_s} - z^{-i/f_s} \right) \qquad 2\text{-}111$$

Passing from the z-domain to the frequency domain with $z = e^{j\omega}$ yields the Fourier transfer function of the discrete MCDS shaper from Figure 2.51:

$$H_{FILT}(j\omega) = \frac{1}{k} \cdot \sum_{i=0}^{k-1} \left(e^{-j\omega\cdot(k+i)/f_s} - e^{-j\omega\cdot i/f_s} \right) = \frac{\left(e^{-j\omega\cdot k/f_s} - 1 \right)^2}{k \cdot \left(1 - e^{-j\omega/f_s} \right)} \qquad 2\text{-}112$$

In *2-112* I have performed simple transformations on the sequence of summed $2k$ elements – thus obtaining the simplified expression (with no additional approximations). With the given transfer function I can now calculate the noise power at the output of the detection channel from Figure 2.51.

MCDS output noise PSD

In the general case of k-folded MCDS the noise PSD at the detection chain output is the product of: the noise PSD at the input to the discrete MCDS ${v_{nSPL}}^2(f)$ and the module of the filter's squared transfer function $|H_{FILT}(j\omega)|^2$, that is:

$$ {v_{nOUT}}^2(f) = {v_{nSPL}}^2(f) \cdot \frac{2\left(1 - cos(\omega k/f_s)\right)^2}{k^2\left(1 - cos(\omega/f_s)\right)} \qquad \textit{2-113} $$

Substituting the sampled noise ${v_{nSPL}}^2(f)$ *2-109* into the expression derived above – the final equation describing the MCDS output noise power spectrum is finally obtained:

$$ {v_{nOUT}}^2(f) = \frac{{i_{nIN}}^2(f)}{{C_F}^2} \cdot \sum_{n=-N}^{+N} \left(\left(\frac{1}{2\pi(f - n \cdot f_s)} \right)^2 \cdot \frac{1}{1 + \left(\frac{f - n \cdot f_s}{B_w} \right)^2} \right) \cdot \frac{4 \cdot sin^4(\pi f k/f_s)}{(\pi f k/f_s)^2} \qquad \textit{2-114} $$

It is the product of the total input referred current noise and the transfer function $H_{system}(j\omega)$ of the overall detection chain from Figure 2.51, which is defined as $H_{CSAideal}(j\omega) \cdot H_{\mathrm{LP}}(j\omega) \cdot H_{\mathrm{SPL}}(j\omega) \cdot H_{MCDS}(j\omega)$. Using the described equations – I have implemented the system's transfer function in the IDL software for numerical computing. In Figure 2.53 the calculation results are shown illustrating the gain of the transfer function $H_{system}(j\omega)$. Three different plots are shown, each with a different value of the sampling frequency f_s and at fixed low-pass bandwidth B_w, yielding the undersampling ratios $N_u = 2\,B_w/f_s$ of 2, 4 and 8. The higher the ratio the more significant is the effect of aliasing of the high frequency components, manifested with a higher noise gain and in consequence – with a higher total output noise $\overline{{v_{nOUT}}^2}$. It should be noted that in these conditions the signal gain *2-107* remains constant. To signify the undersampling effect, I have chosen different values of the number of samples k, for each of the three MCDS transfer function plots. This results in identical band-pass frequencies in all the three cases, permitting direct observation of the undersampling effect.

When the squared transfer function $\left|H_{system}(j\omega)\right|^2$ multiplied by the input noise PSD ${i_{nIN}}^2(f)$ is integrated over the whole frequency – the total integrated noise is obtained:

$$ \overline{{v_{nOUT}}^2} = \int_0^\infty {v_{nOUT}}^2(f) df \qquad \textit{2-115} $$

Further mathematical transformations have been performed to simplify the equation *2-115* (taking into account *2-114*). First of all parameter ${i_{nIN}}^2(f)$ is the total input referred noise current, derived in the paragraph 2.2.6. It is described as the sum of the three noise contributors: ${i_{np}}^2$ and ${v_{nth}}^2/{Z_{INnoise}}^2$ and ${v_{nf}}^2/{Z_{INnoise}}^2$. $Z_{INnoise}(\omega)$ is the impedance seen by the input referred voltage noise sources also defined in the paragraph 2.2.6. Consequently the total output noise $\overline{{v_{nOUT}}^2}$ can be written as a sum of three integrals: $\overline{{v_{nOUTp}}^2}$, $\overline{{v_{nOUTth}}^2}$ and $\overline{{v_{nOUTf}}^2}$, related to the input noise sources: parallel white, series white and series flicker.

2.3. Noise filtering in the detection chain

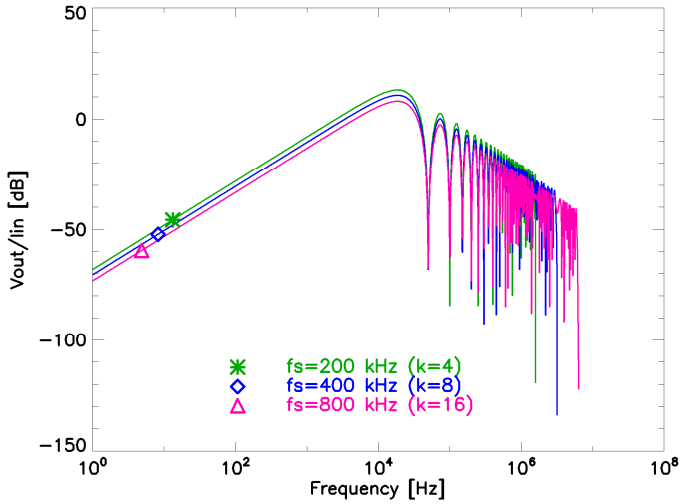


Figure 2.53 Illustration of the MCDS transfer function gain: $H_{system}(j\omega) = H_{CSAideal}(j\omega)H_{LP}(j\omega)H_{SPL}(j\omega)H_{MCDS}(j\omega)$, used to calculate the noise transfer: ${v_{nOUT}}^2/{i_{nIN}}^2$. The low-pass bandwidth B_w is set to $800\ Hz$. Three different plots correspond to different sampling frequencies f_s. Decreasing the sampling frequency value f_s results in an undersampling (aliasing) and consequently in an increased noise gain. The number of samples k is changing with f_s to provide identical bandwidth of the MCDS-filtered signal in all three cases.

In case of the series flicker noise and the parallel white noise – the power spectra at the CSA output have low frequency distributions. These contributors in many cases can be approximated, by neglecting the foldover component in the transfer function and by setting the number N in the sum in the equation *2-114* – equal to 0:

$$\overline{{v_{nOUTp}}^2} = 2 \cdot \left(\frac{k}{C_F \cdot f_s}\right)^2 \cdot \int_0^\infty {i_{np}}^2(f) \cdot \frac{sinc^4(\pi f k/f_s)}{1+(f/B_w)^2} df \qquad 2\text{-}116$$

$$\overline{{v_{nOUTf}}^2} = 2 \cdot \left(\frac{k}{C_F \cdot f_s}\right)^2 \cdot \int_0^\infty \frac{{v_{nf}}^2(f)}{{Z_{INnoise}}^2} \cdot \frac{sinc^4(\pi f k/f_s)}{1+(f/B_w)^2} df \qquad 2\text{-}117$$

This formulas result in less than 8% error when calculating the output noise $\overline{{v_{nOUTf}}^2}$ due to the series flicker contributor at the undersampling factor of $N_u = 8$, with error decreasing with a decreasing N_u. At the same condition the error in the $\overline{{v_{nOUTp}}^2}$ (due to the white parallel noise) is much below one percent.

ENC and noise parameters obtained for MCDS in frequency domain

Finally, knowing the expressions that describe the integrated output noise $\overline{{v_{nOUT}}^2}$ and the signal gain V_{OUTmax}/Q_{IN} at the measurement time $t_m = k/f_s$, the ENC of the detection system with the k-folded MCDS (Figure 2.51) can be written:

$$ENC = \frac{\sqrt{\overline{{v_{nOUT}}^2}}}{\frac{f_s}{C_F \cdot k} \cdot \sum_{i=1}^{k}(1 - e^{-i \cdot 2\pi \cdot B_w/f_s})} \cdot \frac{1}{q} \qquad 2\text{-}118$$

Where q is the electron charge, division by q sets the ENC units to $[electrons\ rms]$. The result has been obtained from the frequency domain characteristics. Having implemented the system transfer function numerically, I was also able to calculate the ENC formula for arbitrary input noise values of the input referred sources: ${i_{np}}^2$, ${v_{nth}}^2$ and ${v_{nf}}^2$. Consequently I could determine the noise

parameters: A_p, A_{th} and A_f from the ENC equations *2-74 - 2-76*. For calculation of each parameter only the relevant input referred source was set to a non-zero value, e.g. to calculate A_p the noise sources ${v_{nth}}^2$ and ${v_{nf}}^2$ were set to zero. Below I am presenting the obtained results in comparison with the parameters' values obtained with the time domain approach (*2-102 - 2-104*).

2.3.5.6. MCDS summary: results in the time and in the frequency domain

Noise in the detection system composed of the CSA and the MCDS filter has been analyzed both: in the time domain based on the weighting function approach, and in the frequency domain from the system's transfer function. In both cases I have derived the ENC equations and calculated the three noise parameters: A_p, A_{th} and A_f. In both cases, the expressions describing these parameters are contained under an integral – therefore I have performed numerical calculation to determine the parameters' values.

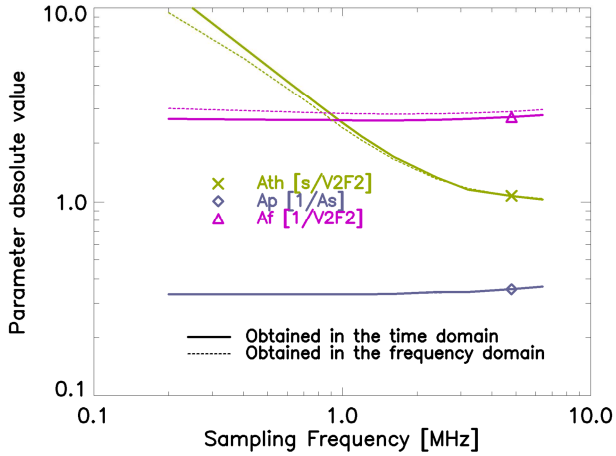


Figure 2.54 ENC parameters for MCDS as a function of the sampling frequency f_s. Number of samples is fixed to 16, CSA bandwidth is set to 0.8 MHz. Comparison between the numerical calculations of the solutions obtained in the time domain and in the frequency domain.

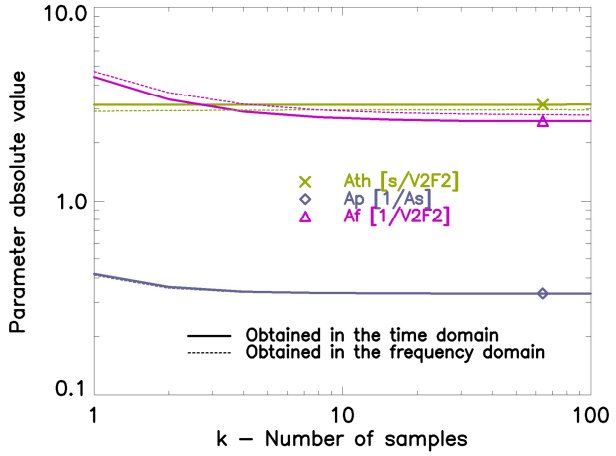


Figure 2.55 ENC parameters for MCDS as a function of number of samples k. The sampling frequency f_s fixed at 0.8 MHz, the CSA bandwidth B_w set to 0.8 MHz. Comparison between the numerical calculations of the solutions obtained in the time domain and in the frequency domain.

Consequently I could show that in the MCDS shaper the parameters might change with the sampling frequency or with the number of samples. The comparison of the obtained results of the time domain and the frequency domain expressions are plotted in Figure 2.54 and Figure 2.55. The results obtained with the two methods are almost identical in case of the A_p calculations. The noticeable difference in A_{th} and A_f parameters is mainly due to the chosen numerical step of the computed expressions. I have verified that with an increasing interval of the numerical integration in the frequency domain calculations – the parameter A_{th} approaches the time domain result. Concerning the A_f parameter it is mainly the time domain calculation that causes the small discrepancy observed in Figure 2.54 and Figure 2.55. This calculation involves the fractional derivative and the integration operation, which take a relatively long computing time. With a higher density in the numerical step (and thus even longer computing time) the resultant parameter value converges with the calculations based on the frequency domain.

The knowledge of the filter noise parameters: A_p, A_{th} and A_f is essential to model the ENC of a detection system. Having performed the noise analysis of the MCDS shaper both in the time domain and in the frequency domain, I can conclude this paragraph with recommendations for efficient noise parameters calculations for this type of shaper. In case of the parameters related to the input referred parallel white noise $i_{n\,p}^2$ and series white noise $v_{n\,th}^2$ I have derived analytical solutions describing A_p and A_f. Consequently the corresponding ENC contributions can be obtained with the following formulas:

$$ENC_p{}^2 = \frac{1}{q^2} \cdot t_{peak} \cdot i_{n\,p}^2 \cdot A_p, \qquad where\ A_p = \frac{0.5 \cdot T_s \cdot (2k^2+1)}{3 \cdot T_s \cdot k^2} \tag{2-119}$$

$$ENC_{th}{}^2 = \frac{1}{q^2} \cdot \frac{1}{t_{peak}} \cdot v_{n\,th}^2 \cdot C_{INnoise}{}^2 \cdot A_{th}, \qquad where\ A_{th} = T_s k \cdot \frac{0.5}{k \cdot \tau_{CSA}} \tag{2-120}$$

Where the capacitance seen by the series noise sources $C_{INnoise}$ is equal to the sum: $C_F + C_{IN} + C_{CSA}$, τ_{CSA} is the CSA time constant equal to $1/2\pi B_w$, $T_s = 1/f_s$ is the MCDS sampling period, k is the number of samples in the k-folded MCDS and the peaking time t_{peak} equals kT_s. These expressions are very accurate in the undersampling condition[4]: when the ratio $\mathrm{T_s}/\tau_{\mathrm{CSA}}$ is higher than 5, which is the typical condition in the MCDS processing.

I have not succeeded in finding the analytical solution of the flicker noise parameter A_f. It needs to be computed numerically. I have proposed simplifications to the formula obtained in the frequency domain to minimize the computing time: in case of the low frequency noise the effect of undersampling can be neglected yielding the following ENC approximation:

$$ENC_f{}^2 = \frac{2 \cdot \frac{k}{f_s}^4 \cdot \int_0^\infty v_{nf}^2 \cdot C_{INnoise}{}^2 \cdot \frac{sinc^4(\pi f k/f_s)}{1+(f/B_w)^2} df}{\left(\sum_{i=1}^{k}(1-e^{-i\cdot 2\pi \cdot B_w/f_s})\right)^2} \cdot \frac{1}{q^2} \tag{2-121}$$

From this equation the noise parameter A_f can be found. Of course, because of the simplification, the higher is the undersampling factor N_u, the higher is the error. I have verified that with $\mathrm{T_s}/\tau_{\mathrm{CSA}}$ as high as 25, the error is still below 8%. Consequently for fast modeling of the MCDS shaper's characteristics I can recommend this simplified formula.

[4] More precisely the undersampling condition occurs when $2T_sB_w = 1$, which corresponds to $\mathrm{T_s}/\tau_{\mathrm{CSA}} = \pi$.

Finally with the obtained results I was able to determine the optimal number of samples k_{opt} for a given system that uses the MCDS processing. From the analytical expressions of the ENC parameters A_p and A_{th}, related to the white current and voltage input noise sources, and from the fact that the flicker noise is found nearly independent of the number of samples k, the following conclusion arises:

$$k_{opt} = \sqrt{\frac{3 \cdot v_{n\,th}^2 \cdot {C_{INnoise}}^2}{2 \cdot \tau_{CSA} \cdot {i_{n\,p}}^2 \cdot T_s} - 0.5} \qquad 2\text{-}122$$

With a known input referred noise PSD: $i_{n\,p}^2$ and $v_{n\,th}^2$, a CSA time constant τ_{CSA} and the capacitances related to CSA and the detector: $C_{INnoise} = C_F + C_{IN} + C_{CSA}$, the optimal number of samples can be determined and optimized with respect to the sampling period T_s.

2.3.6. Comparison of shapers

Three shaping systems for radiation detector readout have been discussed: with the optimal filter Cusp, with the analog semi-Gaussian shaper CR-RC^N and with the discrete MCDS filter. The optimal filter is the reference for the best achievable energy resolution. The CR-RC^N semi-Gaussian filter is a widely used analog filter and very convenient in analog application. Finally the MCDS filter, whose shape is a good approximation of a triangular shaper, has very good properties for the correlated noise reduction. Weighting functions for the three filters are shown in Figure 2.56.

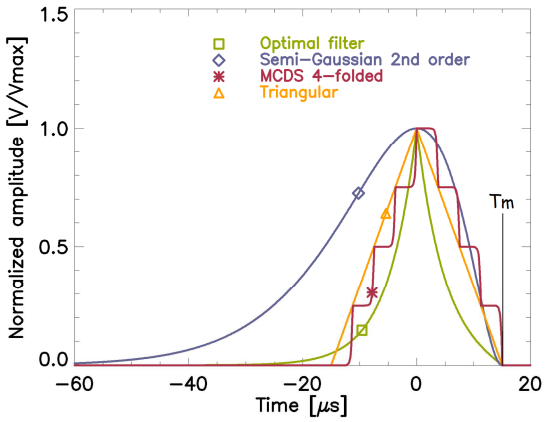


Figure 2.56 Weighting functions of four shapers: optimal filter – infinite cusp, CR-RC^2, pseudo-trapezoidal 4-folded MCDS (with no flat-top) and triangular. The peaking time t_{peak} is set to the same value t_m for each filter.

I have presented the known ENC expressions for the optimal filter and the semi-Gaussian in the form that enables extraction of the noise parameters: A_p, A_{th} and A_f. In case of the MCDS shaper I have derived the complete ENC formula using two methods: the time domain and the frequency domain approaches. With the double calculation there is a high confidence concerning the accuracy of the obtained MCDS noise parameters.

The noise parameters for all of the three discussed shapers are compared in Table 2.4. In addition – the triangular and trapezoidal shaping parameters [54] are included in the comparison as a reference

to the MCDS shaper, also referred to as a pseudo-trapezoidal. As predicted by the matched filter theory – the Cusp parameters indicate the best performance. Even though the result is shown for the truncated version with the measurement time t_{peak} limited to four times constants τ_{white} and despite the fact of being optimized only for the white noise sources, the Cusp parameters are still the most attractive. The second best filter of those presented in Table 2.4 is the triangular one, which is the nearest approximation of Cusp. Parameters of both filters are very similar, if only the measurement time t_{peak} is in range between τ_{white} and $2\tau_{white}$, what is in accordance with [44] where the optimal time of $\sqrt{3\tau_{white}}$ is given for the triangular shaper. The MCDS, considered without the flat-top (the period is constant along acquisition of all the baseline and the signal samples) shows to be a good pseudo-triangular approximation of the triangular shaper. The highest resemblance occurs when the sampling frequency exceeds the CSA bandwidth ($N_u < 1$), although for a maximum signal gain this condition is avoided. Finally the MCDS shaper, when compared with the CR-RC^N – shows better filtering capabilities for the parallel white noise and the series flicker noise, however the A_{th} parameter related to the series white noise is much lower in case of CR-RC^N.

Shaper	Weighting function	A_{th}	A_f	A_p
Truncated CUSP*	$t_{peak}/\tau_{white} = 1$	0.75	1.97	0.4
	$t_{peak}/\tau_{white} = 2$	1.08	1.83	0.24
	$t_{peak}/\tau_{white} = 4$	1.92	1.65	0.13
Triangular [43]	No flat top	1	2.76	0.33
Trapezoidal [70]	$t_{flat\ top} = t_{peak}$	1	4.33	0.83
CR-RC^N	1st order, $t_{peak} = RC$	0.92	3.69	0.92
	2nd order, $t_{peak} = 2RC$	0.85	3.41	0.64
	4th order, $t_{peak} = 4RC$	1	3.27	0.45
	8th order, $t_{peak} = 8RC$	1.34	3.21	0.32
MCDS**	$k = 4, f_s = 0.8\ MHz$	3.15	2.9	0.34
	$k = 16, f_s = 0.8\ MHz$	3.15	2.63	0.33
	$k = 16, f_s = 1.6\ MHz$	1.71	2.62	0.33

* the time constant τ_{white} is defined as: $(C_{IN} + C_{CSA} + C_F)\sqrt{{v_{n\,th}}^2/{i_{n\,p}}^2}$

** MCDS without flat-top, the peaking time t_{peak} is equal to kT_s, calculations for a fixed CSA bandwidth B_w of $0.8\ MHz$

Table 2.4 Comparison of shaping parameters of different filters used in radiation detection

Having obtained the noise parameters – the ENC achievable with each shaper can be calculated from the general equations, derived earlier in the paragraph 2.3.2:

$$ENC_p{}^2 = \frac{1}{q^2} \cdot t_{peak} \cdot i_{n\,p}^2 \cdot A_p \qquad 2\text{-}123$$

$$ENC_{th}{}^2 = \frac{1}{q^2} \cdot \frac{1}{t_{peak}} \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_{th} \qquad 2\text{-}124$$

$$ENC_f{}^2 = \frac{1}{q^2} \cdot v_{nf}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_f \qquad 2\text{-}125$$

Finally it is interesting to compare the shapers in terms of the optimal peaking time – that is the measurement time that results in the best ENC. For the Cusp the best resolution is achieved with an infinite time t_{peak}, or at least – a time possibly long in the truncated variant. In case of the other filters the optimal peaking time, resulting with the lowest ENC, is when the ENC due to white series noise is equal to ENC due to white parallel noise: $ENC_{th} = ENC_p$ (please refer to Figure 2.31 from

the paragraph 2.3.2). In case of the CR-RC^N filter, the optimal t_{peak} equals to the expression $N \cdot (C_F + C_{IN} + C_{CSA}) \cdot \sqrt{v_{n\,th}^2 / i_{n\,p}^2}$ for the 1^{st} order shaper, or multiplied by 1.15 or 1.5 for the 2^{nd} and 4^{th} order respectively. The optimal peaking time for the triangular shaper is the same expression but multiplied by $\sqrt{3}$ [70], which results in a longer measurement than with the optimal semi-Gaussian shaper. In case of the MCDS filter – the optimal shape is expected to be the nearest approximation of the optimal triangular shape. Consequently the optimal peaking time should be similar to the one obtained for the triangular shaper.

In the following chapter I will examine experimentally the semi-Gaussian and the MCDS shapers with respect to the achievable ENC in the radiation energy measurement. The employed CSA circuit is optimized for the readout of pixelated CdTe detector.

The detection chain has been described as a three stages structure: the sensor, the CSA and the noise filter. When the whole chain is well optimized, there are three dominating noise sources: the thermal and the flicker noise originating in the CSA, and the shot noise due to dark current in the sensor. I have shown that the energy resolution of an imaging instrument can be improved at each stage. Primarily the small dimensions of CdTe pixel are the key factor to reduce the sensor noise and effect of the electronic noise. Secondly the CSA can be optimized to directly minimize the electronic noise – this wide subject is expanded in the next chapter. Finally the filter stage limits the output bandwidth, consequently reducing the electronic noise power imposed earlier in the detection chain. The absolute noise floor is set by the material type (CdTe) and the Fano statistics, which can be considered as an ultimate noise source. The floor noise determines the lowest achievable noise of the imaging spectrometer instrument.

Several filters known from the literature have been analyzed with respect to the three noise sources and compared to the optimal filter. For each filter three noise parameters have been identified. They are the figure of merit in the filtering quality for the three noise sources respectively: thermal, flicker and shot. Of all presented filters, the analog semi-Gaussian CR-RC^N and the discrete Multi Correlated Double Sampling (MCDS) have received the highest attention. I have found the semi-Gaussian to be interesting because of its simple implementation in the electronic circuits and its maturity due to numerous applications, including the former designs in our group. The second method, MCDS gained popularity in the Correlated Double Sampling (CDS) version. The combination of possible ideas for the circuit realization in a relatively small silicon area and the encouraging noise parameters became the driving factors for the extensive analysis presented above. I have analyzed the filter performance with two different methods: in the time domain and in the frequency domain. Noise parameters expressions, which I have derived with both approaches, show consistent results in numerical calculations. Finally I have proposed the analytical formulas describing two of the noise parameters for the MCDS filter. This set of equations constitutes a powerful tool for the filter optimization, noise prediction and the user knowledge.

The noise parameters obtained for the filters of interest allowed comparison of the achievable spectral performance. I have concluded that whether it is the CR-RC^N or the MCDS who is better – depends on the type of the dominating input noise. In the presence of a high detector shot noise – the MCDS shaper predicts better filtering capabilities, if instead it is the white electronic noise dominating – the semi-Gaussian shaper brings an advantage. The filter for the dedicated detection system with the pixelated CdTe will depend mainly on the exact parameters of the CSA. The CSA design and determination of its optimal parameters (noise and capacitances) is the subject for the next chapter.

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CHAPTER III

The Caterpylar Testchip

In order to approach the Fano limits in the energy resolution of an imaging spectrometer – the electronic noise must be minimized down to a level far below the intrinsic capabilities of the sensing medium. In the Chapter I – the target detector has been chosen: the pixelated CdTe of 300 µm pitch. In the Chapter II – I have estimated that the pixel capacitance would range from 0.3 to 1 pF and also concluded that the dark current of a single pixel CdTe is expected below 5 pA. The high importance of a low input capacitance and a low dark current for a good energy resolution has also been discussed. Consequently these two are the driving parameters for the readout ASIC design optimization. The next step to improve the energy resolution is reduction of the electronic noise in the CSA stage.

In the CSA – the type, dimensions and drain current of the input transistor, have a great influence on the electronic noise. It only makes sense to speak about the noise optimization for the whole detection chain, i.e. with a given sensor and filter type. Therefore for the optimization I have chosen the reference filter: the semi-Gaussian with variable peaking time. Modification of the peaking time effectively shifts the bandwidth to higher or lower frequencies. This is true for any filter type. Consequently the peaking time appears as a new variable in the noise optimization, in addition to the input transistor parameters. Taking it into account, the CSA optimization in a given detection chain becomes a multi-dimensional problem. The optimal solution gives answer to: what is the achievable noise resolution for a given small pixel CdTe detector. I will respond to it with experimental results.

In this chapter my method of CSA optimization is described in the first place. It starts with identification of the best suited IC technology for the ASIC. With the chosen process XFAB 0.18 µm I have performed the optimization procedure. I have then analyzed the CSA at the transistor level. In consequence the best architecture and transistors' dimensions for the CSA have been determined for this specific technology through multi-dimensional simulations. The readout precision and the power consumption were the electrical key parameters to be optimized in the process. The first prototype called Caterpylar contains a set of over 20 CSA with the most interesting parameters: it has been designed and fully tested. In subsequent part of this chapter the experimental results of the achieved low ENC are demonstrated. Furthermore I describe extraction of the CSA input referred noise and capacitance from extensive measurements with an external second order semi-Gaussian shaper. Finally, in the last part of this chapter – I use the extracted CSA input referred noise and capacitance to determine the achievable ENC with various shapers. The calculations are based on the shaper's models derived in the Chapter II. This task is aimed to find the best suited filter for the new low power CdTe readout circuit.

3.1 Interest in the readout testchip

The direct bump-bonding of the pixelated detector and the readout ASIC appears to be the best way towards improving the spatial resolution and the energy resolution in the X-ray imaging spectrometry. While scaling down the detector dimensions – the input capacitance seen by each individual readout channel becomes smaller. Secondly with the bump bonding technique the parasitic capacitance of the detector-to-ASIC interconnections is expected lower than with the wire bonding. The consequent decrease of the electronic area matched to the pixel size, dictates restrictions in the power consumption: the electronics power density has to be maintained or even decreased with respect to the state of the art instruments. For a smaller area of the readout electronics this means: severely decreased power consumption per readout channel. The final objective of the new hybrid pixel is to improve the product of: energy resolution by dissipated power per channel.

In the previous chapter I have demonstrated that the ENC is highly dependent on the input capacitance. Reduction of the input capacitance through the hybridization method is the major step towards improvement in the energy resolution. However this relation suggests that any remaining capacitances intrinsic to CSA should also be minimized. Because of connections with other parameters (electronic noise and power consumption), the choice of the right CSA dimensions becomes a great concern. The design of the final ASIC for the CdTe readout grows to a complex project. These major challenges involve:

- Requirement for the CSA optimization – the most critical for the overall noise performance
- Necessity for integrating the noise filter, whose choice must be justified as the best suited for the application
- The power consumption concern on each single block level
- The overall complexity on the ASIC top level and its large dimensions

Because of the risks accompanying the new development – it is sensible to separate the project into smaller tasks. I have decided that for the higher confidence level it was sensible to develop an intermediate testchip: integrating only several CSA of different dimensions. In this paragraph I attempt to explain the advantages of doing this step. There are several motivations to it and much of useful information for the consequent development can be gained from this testchip. I will start with describing the IC technology choice for this circuit.

3.1.1 Technology choice

In the recent years most of the ASICs developed within our IRFU microelectronic group have been realized with the CMOS AMS $0.35\ \mu m$ IC technology. This trend includes the family of the previous IDeF-X circuits – what is understandable with the achieved high maturity of the technology: from the point of view of the noise models offered by the foundry as well as our internal understanding of the radiation hardness and the know-how in terms of the existing IP blocks or the radiation-hard layout cells. Despite all these advantages however, there is a strong motivation to move forward to a

technology featuring smaller dimensions in this specific development of the hybrid detector module for the pixelated CdTe. The first aspect is the power consumption: the more modern technologies offer devices operating at lower supply voltages. This is one of the keys in reducing the power consumption, very critical in the space-application. Secondly – with the severe limits of the single channel layout area, dictated by the CdTe pixel size, smaller transistor features are expected to highly facilitate the circuit design.

There were several criteria to be considered in the technology choice. One of the most important was naturally the cost. Especially with the perspective of the testchip production with a small number of samples, the possibility of the ASIC production through a multi-project wafer (MPW) is very important. This option permits to highly limit the fabrication costs. However submission of a design to the foundry through the MPW option imposes time constraints in the project development. If the option is available at all, the number of the MPW runs is usually limited to 6 per year or often even less than that. Within the subject of the time constraints – the fabrication time was also something that we could not neglect: even with the most efficient cooperation the production time: from submission to shipment of the ready product takes at least three months. This is already a rather long time, especially when comparing to the frame duration of the doctoral research. In case of some foundries however this production time was estimated much longer, therefore it would be not acceptable for this testchip. The next important criterion was the accessibility of the complete design kit, including: the complete transistors' and passive components' models with parameters for the Monte-Carlo simulations, availability of the standard cells (digital and IO) as well as a complete layout support for verification and for the digital place and route. The most ideal would have been a technology with the through-silicon-via (TSV) option, very desirable in hybridization between the sensor and the ASIC. Using TSVs the IO interface could be transferred onto the back-side of the ASIC, facilitating the 4-sided buttability of the final instrument with a minimized dead zone for detection. Unfortunately – none of the technologies accessible at the time when the choice was to be done would meet all these criteria. Eventually we had to choose one, which does not offer TSV but fulfills all the other requirements. At the testchip submission time the hybridization has been still an open subject, with several other possibilities (subcontracting the post-process TSV or using an interposer adapter to transfer the IO connections externally to the ASIC).

Having chosen all the available possibilities at that time – in consequence we have chosen the XFAB $0.18\,\mu m$ technology: the process with basic supply of $1.8\,V$ however also with $3.3\,V$ devices available.

3.1.2 The testchip goals

The large scale of the new instrument development project is the main reason why the intermediate step of a testchip design has been decided. The goal for the instrument has been detailed in the Chapter I: it is an imaging spectrometer for pixelated CdTe. It should contain an array of 256 channels, each providing high resolution X-ray detection and measurement. Meanwhile the content of the testchip has been fixed to be: a set of low power Charge Sensitive Amplifiers optimized for the readout of small CdTe pixels. The CSA block constitutes only a tiny part of the target ASIC. However I

will show that there are few principal reasons why this small step is extremely valuable in the whole development path.

3.1.2.1 IC technology validation

The technology chosen for this development is XFAB $0.18\ \mu m$ and it has been the first time in our group to design and fabricate an ASIC with this process. With the new technology – lots of new elements have appeared as needing a good understanding. The available process options (transistors types and passive devices) as well as the simulation tool-kit with the noise models are only some of the parameters strictly related to the technology choice. Realization of the testchip is the first experience with this technology. This step is undertaken with the perspective to develop the second ASIC containing the complete readout circuit with the same process. A successful testchip should help in the technology validation for our future purposes.

The measurements of the CSA blocks alone contribute to our knowledge about the most critical parameter of this application: noise. With the real circuit – a comparison of the simulation models with the experimental results could be carried out. The subject becomes even more interesting in the low power domain with transistors typically operating in the moderate or weak inversion. In this operation region there are lots of speculations concerning the most accurate models.

3.1.2.2 CSA optimization for small pixel CdTe readout

Naturally the fact of integrating a set of several CSA on the discussed testchip should result in nominating the most suitable one for the final application. There are several parameters within the CSA that need optimization to achieve the desired performance: the architecture, transistor types and dimensions as well as their bias currents and voltages. The CSA that appears to have the best performance according to simulations is not necessarily the best in measurements, although this would be true in the ideal case. Therefore a careful choice of the set of integrated CSA through simulations has to be validated with measurements. The characterization of the CSA noise performances is done with respect to parameters of a small pixel CdTe detector. Once the CSA offering the best compromise between noise, power and the other parameters (described in the paragraph 3.1.3) are determined – the ENC achievable with the dedicated CdTe detector can be also predicted.

3.1.2.3 Validation of the processing chain

The testchip architecture assumes the integration of several readout chains, each containing the CSA only, without integrated noise filter. Evidently this is not sufficient for a good measurement resolution. The motivation for that choice is: simplification of the circuit to the most critical part from the noise point of view.

The filter can be implemented externally to the test-ASIC. This brings a certain significant advantage: the ASIC with the noise imposed by the CSA can be tested experimentally with several filters. The ENC values achievable with different setups can be compared. The resulting experimental feedback is precious for choosing the most suitable filter to be integrated in the final ASIC (described in the Chapter IV). Comparison of the filtering methods implemented off-chip is therefore the third of the

principal purposes of the testchip. The main actors of this evaluation will be the semi-Gaussian and the MCDS shaper.

3.1.3 The readout testchip input parameters

Having defined the clear goals of the testchip, the next step is the specification of its detailed functionality and performance. This section contains a review of the testchip requirements. They are imposed by the application character discussed in the previous chapters (mainly in the sections 1.3 and 2.1). The parameters' list presented below is adapted to the fact that at this point it is only the CSA block design that is discussed. In consequence there are two driving aspects for the specification list: the detector characteristics and the IC technology constraints. The first one determines: the signal polarity, the input dynamic range as well as the CdTe and the stray capacitances C_{IN} and the detector dark current I_{DET} for which the CSA has to be optimized. Meanwhile the technology has an impact on the output dynamic range and on the supply voltage strictly related to the power consumption.

3.1.3.1 Signal polarity

The principal polarity of the front end circuit (the CSA) is determined by the fact that the readout of charge signals takes place on the anode side. Because of the advantages discussed in Chapter I – the pixelated electrodes are on the positively polarized electrode, where the electron charge is collected. The negative charge is thus fed to the CSA input. The inverting nature of the CSA amplifier results in the positive output voltage step due to the instantaneous negative charge.

3.1.3.2 Input capacitance

The input capacitance seen by the readout circuit is the parallel combination of the CdTe pixel and parasitic capacitance due to bonding between the detector and the electronics. The pixel capacitance of CdTe alone has been estimated (in the paragraph 2.1.3) to $100\ fF$. It has been calculated taking into account the electric field distribution in a pixelated planar detector with $300\ \mu m$ pitch. Also, the capacitance of gold stud bonding and the standard bonding pad of the ASIC have been accounted. However dependency of geometries and materials, as well as presence of inter-pixel capacitance put the estimate in question. In similar application [1] with CdTe hybrid pixel of similar size an input capacitance of $0.4\ pF$ has been obtained. Therefore in the CSA design optimization discussed in this application I assume the spread in the total input capacitance: between $0.3\ pF$ and $1\ pF$.

3.1.3.3 Detector dark current

The detector dark current depends on several parameters: starting from the CdTe crystal fabrication methods, through its geometry and architecture (presence of the Schottky contact or guard-ring), ending up at the operating conditions (bias voltage and temperature). In the paragraph 2.1.2 I have extrapolated the available results (based on the past experiments performed within our team or based on others' reports) for a CdTe detector with $300\ \mu m$ pitch. According to my evaluation the dark current is expected to be below $0.5\ pA$. However there are additional aspects whose influence

is difficult to quantify: radiation damage, operating conditions' spread (beyond the evaluated parameters) or domination of the guard-ring/pixel surface current. Consequently an additional rise or even current polarity change must be taken into account. The CSA simulations are thus performed with a broader range – with the detector current modeled up to $5\,pA$, which corresponds to a negative current oriented from the CSA input to the detector. Furthermore the functionality must provide operation also for a positive orientation of the dark current.

3.1.3.4 Energy range

The input energy range of hard X-rays is in order of 300 to $400\,keV$. For CdTe, where the electron-hole pair creation energy w is equal to $4.42\,eV$, this corresponds to a maximum input charge $Q_{in\,MAX}$ of approximately 10 to $15\,fC$. This value has to be translated through the CSA transfer function to an output voltage in a reasonable range.

3.1.3.5 Output dynamic range and feedback capacitance

In the chosen IC technology the main power supply is set to $1.8\,V$, the output dynamic range must be inferior to it. However its value should be as high as possible: with high signal amplification the signal to noise ratio immediately improves (for details please refer to the paragraph 2.2.5). Prior to design I have estimated the highest feasible output signal to a value between $0.5\,V$ and $1\,V$. The maximum input charge and the output dynamic range – are related with the feedback capacitance by the CSA transfer function:

$$V_{out\,MAX} = \frac{Q_{in\,MAX}}{C_F} \qquad 3\text{-}1$$

In addition the feedback capacitance should be small when compared to the total input impedance seen by the CSA series noise $Z_{INnoise}$ (defined in the paragraph 2.2.6). This requirement is there to avoid a significant amount of additional capacitance seen be the input referred series noise sources. Typically C_F is chosen at least twenty times smaller than the input capacitance.

I have set the feedback capacitance C_F to $25\,fF$, which fits the demands. In this case the CSA closed loop gain equals to $40\,mV/fC$, which is relatively high. Concerning the contribution to the equivalent input capacitance that scales up the effect of the series noise, the chosen value is 12 to 40 times smaller than the input capacitance, which is in range of $0.3\,pF$ to $1\,pF$.

The CSA gain is set by the capacitance C_F. For the gain stability the value should have limited deviations with the process spread. A metal "sandwich" capacitance available in the chosen IC process has a large enough area (of approximately $0.1\ fF/\mu m^2$) to ensure a sufficient stability of the capacitor value.

3.1.3.6 CSA power consumption

I have already set the power consumption target for the final ASIC containing the complete multichannel readout (in the paragraph 1.3.4) to: $0.18\ mW/channel$. For reference the Caliste HD [41] with the IDeF-X HD ASIC [2] has been considered. IDeF-X HD is a very low power circuit qualified for space borne experiments and recognized for high demand applications like the STIX instrument for the Solar Orbiter [4]. The 32-channels IDeF-X HD fits an active silicon area of approximately

$13\ mm^2$ (excluding peripheral circuits) and its average power consumption is $0.8\ mW/channel$. The current consumption of a single CSA in the IDeF-X HD is adjustable between 50 and $100\ \mu A$, which results in about 20% contribution to the channel power consumption. When considered in the Caliste HD CdTe-based spectro-imaging instrument power density is $2\ mW/mm^2$ of the detector surface. The power quote includes peripheral circuits common to all channels – therefore the calculations are approximated.

In the new pixelated detector with $300\ \mu m$ pitch, a single channel area is $0.09\ mm^2$. To maintain the power density a single channel should correspondingly consume power of less than $180\ \mu W$. The best aid to reduce the power consumption is to lower the supply voltage: in IDeF-X HD designed in $0.35\ \mu m$ IC process it was $3.3\ V$, in the new development with the $0.18\ \mu m$ technology the typical operating voltage is $1.8\ V$. However not everything can scale down simultaneously: the percentage contribution of the CSA to the total channel power should be estimated lower than 20%. This is because of the low noise demand of the shaping stage which becomes more critical for the two following reasons:

- **Lower absolute noise of the shaper**
  The noise of the new CSA will naturally decrease in the hybrid CdTe pixel with very low input capacitance. For the filter however the design may be found to be another challenge – since it should contribute no additional noise to the CSA.
- **Lower channel gain**
  If the input dynamic range is maintained, the lower supply voltage inevitably leads to lower channel gain. In effect noise has to be further improved. In case of the output signal amplitude twice smaller – the shaper's squared voltage noise has to be divided by four.

The discussion concludes with extreme CSA power reduction to 10% of maximum channel power consumption, that is to $18\ \mu W$. Nevertheless it is intended that the current is adjustable in the first test prototype – in order to analyze the energy resolution and power dissipation trade-off.

3.1.3.7 Parameters summary

I have proposed the realization of a testchip as an intermediate step in the design of the complete readout ASIC for the new spectro-imaging instrument. The most significant purposes for the testchip have been defined. The IC technology chosen for this development is XFAB $0.18\ \mu m$ and the first experimental measurements are aimed to qualify the process for the further development. The testchip is intended to contain a set of CSA optimized for the small pixel CdTe. These circuits should be proposed relying on simulations. Later measurements should indicate the most suitable one for the final application together with the best operating conditions.

The general CSA design parameters are summarized in Table 3.1. One parameter that has not been mentioned so far is the layout area of the CSA designed for the testchip. I do not give a clear specification, but let's remember that in the application of destination, a complete single readout channel must fit in the area corresponding to the CdTe pixel size, that is $300 \times 300\ \mu m^2$. There, the CSA layout area should be only a fraction of the total channel size. However the internal structure for this final circuit is supposed to be determined relying on the outcome of the discussed testchip. Because of these mutual dependencies – it is difficult to set the CSA layout area. In the testchip

development my goal is to make the CSA as compact as possible, to fit it in a fraction of the destination channel area.

Parameter	Unit	Value
IC technology		CMOS XFAB 0.18 µm
Total external input capacitance	pF	0.3 … 1
Detector dark current	pA	<5
Detector current polarity		positive and negative
Detector signal polarity		negative – anode readout
Maximum input dynamic range	fC	10 … 15
Maximum output dynamic range	V	0.5 … 1
Feedback capacitance	fF	25
Supply voltage	V	1.8
Max. CSA power consumption	µW	18

Table 3.1 Parameters determined for a single CSA integrated in the testchip. Specifications have been chosen to match the requirements for the final ASIC, dedicated to readout the pixelated CdTe detector with 300 µm pixel pitch.

The testchip with the integrated CSA can be used for noise evaluation with one of the potentially applicable shaper networks: the semi-Gaussian or the MCDS. In the measurements the shaper can be connected externally. This highly simplifies the testchip design and increases flexibility of the experimental methods.

In the next section 3.2 I describe the CSA structure, after review of the possible architectures. I also analyze noise sources. With this electronic background I can then justify the CSA optimization through the simulations, what is described in 3.3. That section concludes with the description of the Caterpylar testchip submitted for an MPW run in March 2011. In 3.3 and 3.4 I present and discuss the obtained experimental results and their contribution to the further development.

3.2 Inside the CSA

It is time to look at the internal structure of the CSA. First of all I will review the most common architectures. Immediately each solution will be regarded with respect to the previously listed design properties that are of the highest concern in the readout circuit, that is:

- Noise
- Power consumption
- Layout area
- Output dynamic range

Then I will perform the transistor level noise analysis for the most interesting candidate. The conclusion of this discussion will have impact on my method for the optimization of the CSA noise presented afterwards.

3.2.1 CSA architectures: from simple common source to folded cascode

In the previous chapter the symbol of the CSA has been represented as shown in

As one could have noticed from the previous chapter – I have already assumed use of a single-ended input type of CSA. This paragraph shows comparison of two structures and explains my motivation. Transistor level examples of both amplifier types are illustrated: differential input in Figure 3.2 A) and single-ended input Figure 3.2 B).

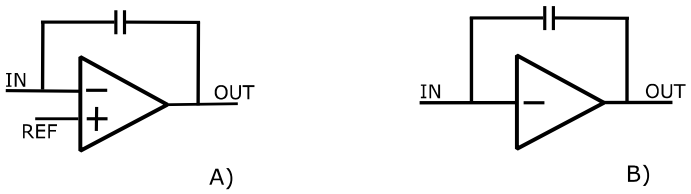


Figure 3.1 B): it is an inverting amplifier with capacitance C_F in the feedback loop. In the paragraph 2.5.5 I have shown that a high value of the CSA open loop gain A is critical. It is important to remember the significance of this parameter: for each of the CSA architectures the open loop gain will be calculated. The obtained expressions will be helpful to determine how to design each of the transistors for the best noise performance.

3.2.1.1 Differential vs. single-ended input

In the first classification the CSA architectures can be divided into:

- Differential input amplifiers (Figure 3.1 A)
- Single-ended input amplifiers (Figure 3.1 B)

As one could have noticed from the previous chapter – I have already assumed use of a single-ended input type of CSA. This paragraph shows comparison of two structures and explains my motivation. Transistor level examples of both amplifier types are illustrated: differential input in Figure 3.2 A) and single-ended input Figure 3.2 B).

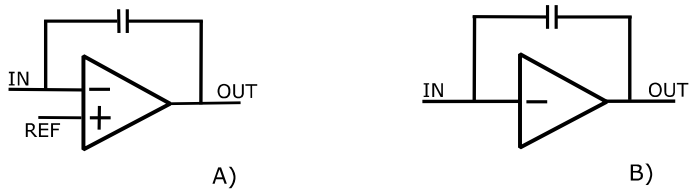


Figure 3.1 Two possible CSA applications: A) differential input, B) single-ended input.

Each of the differential pair input transistors in Figure 3.2 A) has W and L dimensions and drain current equal to I_{BIAS}. The single input transistor of the common source amplifier in Figure 3.2 B) also has dimensions W and L and the same bias current I_{BIAS}. With the given conditions, the input transistor from Figure 3.2 B) has the same gate related voltage noise ${v_n}^2$ as each of the differential pair transistors from Figure 3.2 A). The CSA input referred noise contributed by the input stage is ${v_n}^2$ for the single-ended amplifier and $2 \cdot {v_n}^2$ for the differential one. Simultaneously the total current consumption is twice lower for the simple common source amplifier. A CSA based on the single-ended input amplifier is superior to differential amplifier in terms of noise, power consumption and layout area, typically dominated by the input transistor size. The noise reduction with respect to differential amplifier is achieved with half of the current that two identical differential transistors would consume.

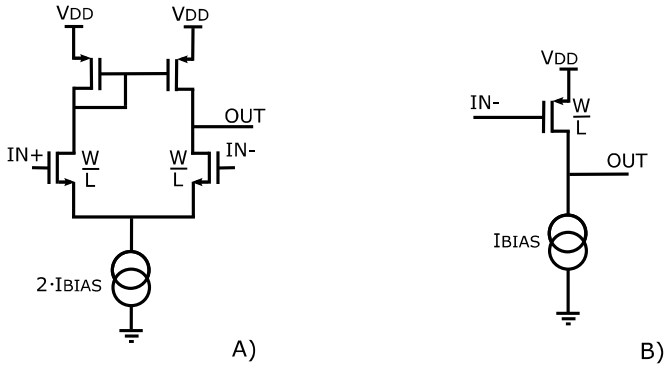


Figure 3.2 Examples of CSA amplifier architectures: A) differential input, B) single-ended input.

On the other hand what may be perceived as a drawback is a single input DC operating point of the common source amplifier. There is no flexibility to control it with an external reference as it would be in case of the amplifier with positive and negative inputs, what is illustrated in Figure 3.1

In the low power pixelated CdTe readout circuit the priorities have been set to low noise and to minimized power consumption. Moreover the CSA layout area is also a concern since the complete readout channel has to fit in the limited surface of $300\,\mu m \times 300\,\mu m$. Consequently the single-ended input architecture is preferred. However the remaining issues of the input reference and the supply rejections have to be addressed. The input reference has to be set already by the design. It is fixed by evaluating at the same time the reset stage that actually provides the input operating point

and the dynamic range at the output; these parameters are all related. The supply rejection is poor in the selected architecture. Physical separation of the supply lines in the layout between the low noise CSA and the aggressor circuits (like comparators, digital blocks or high current output buffers) reduces the danger of noisy supply.

3.2.1.2 Common source amplifier

A source follower amplifier from Figure 3.3 A) and B), is the simplest architecture of the single-ended input amplifier with adjustable bias current. Both transistors: the input $M0$ and the current source $M1$ operate in the saturation region. The amplifier open loop gain is obtained from the equivalent small signal model [55]:

$$A = -g_{m0} \cdot (r_{o0} \parallel r_{o1}) \qquad 3\text{-}2$$

where g_{m0} is the transconductance of the input transistor $M0$, r_{o0} and r_{o1} are the small signal resistances of $M0$ and $M1$ respectively.

When the small signal resistance of the current source is much larger than that of the input transistor, the equation can be simplified to:

$$A \approx -g_{m0} \cdot r_{o0} \qquad 3\text{-}3$$

As explained in the previous chapter, ideally, the open loop gain A should be infinite. In the practical case the intension is to make it as high as possible. The current source, $M1$ small signal resistance is high by definition of the current source. In case of the input transistor, there is a design compromise between g_{m0} and r_{o0}. This is the first reason to introduce the cascode stage.

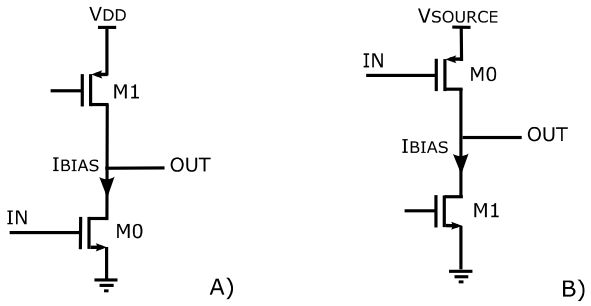


Figure 3.3 Common source single input amplifier: A) NMOS input, B) PMOS input.

Before changing the architecture to one that enables a higher open loop gain I would like to discuss the subject of the input reference voltage for the simple common source amplifier. Let's consider the amplifier with a PMOS input transistor from Figure 3.3 B). The bias current I_{BIAS} is set by the current source $M1$. Only a specific value of the input transistor gate-source voltage V_{GS} can support the current I_{BIAS}, it corresponds to the highest g_{m0} achieved in saturation. The voltage V_{GS} of the transistor defines the input reference voltage level, and is typically in the range from $0.4\,V$ to $0.7\,V$. With the source supply V_{SOURCE} equal to $1.8\,V$ this results in the input reference in range $1.1\,V$ - $1.4\,V$. If for some reason the input reference has to be changed the source supply, can be modified to value different (lower) than the main supply V_{DD}. Unfortunately the proposed change means a reduced output dynamic range and an additional supply in the circuit. Evolutions of the cascode stage discussed below will show how the issue of the output dynamic range can be tackled down.

Another solution to modify the input voltage value would be to use the amplifier with an NMOS input transistor shown in Figure 3.3 A). With its source connected to the substrate potential the similar V_{GS} voltage, as previously considered, results in the input reference in range $0.4\,V$ - $0.7\,V$. Unfortunately with no control over the process and with temperature variations, only an approximate input reference is set with these operations.

The reason of the input reference discussion is the link with the output dynamic range. In the pixelated CdTe readout the input signal is a negative charge. In the CSA conversion stage it results in a positive voltage step at the output. For a high dynamic range the CSA baseline is desired as low as possible with the maximum positive swing. The two CSA node voltages: input and output are related with the reset network, which is responsible for setting the operating point. If for example the reset is realized as a switch (described in the paragraph 2.2.4) – the output baseline is equal to the input reference. Therefore the reset structure has to be reconsidered simultaneously with the CSA amplifier architecture.

3.2.1.3 Telescopic cascode

The gain of the source follower can be improved by adding the cascode transistor $M2$ between the high transconductance transistor $M0$ and the output. One way to do this is placing the cascode $M2$ in series in the main current path, as shown in Figure 3.4. The cascode separates the output node from the lower impedance node X. The open loop gain of the amplifier is now:

$$A = -\frac{g_{m0} \cdot r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2})}{r_{o1} + r_{o2} + r_{o0} \cdot (1 + g_{m2} \cdot r_{o2})} \qquad 3\text{-}4$$

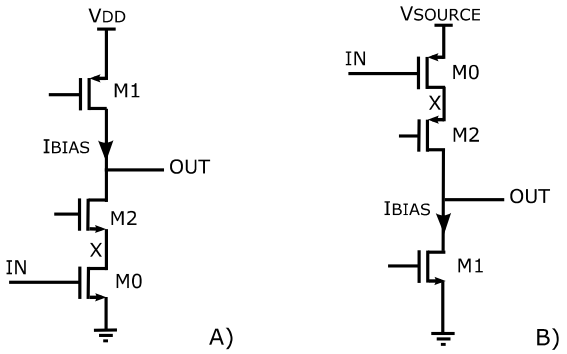


Figure 3.4 Common source amplifier with the telescopic cascode: A) NMOS input, B) PMOS input.

Since generally $r_{o0} \cdot (1 + g_{m2} \cdot r_{o2}) \gg r_{o1} + r_{o2}$, the open loop gain can easily be simplified to:

$$A \approx -g_{m0} \cdot r_{o1} \qquad 3\text{-}5$$

In the presented CSA internal architecture – it is the current source transistor that determines the output resistance. With the cascode the principal small signal parameters of the amplifier: the transconductance and the output resistance – can be set almost independently. In consequence the open loop gain can be much higher than in the simple common source amplifier from Figure 3.3, what is confirmed by comparison of the equations *3-3* and *3-5*.

3.2.1.4 Folded cascode

In the discussed common source amplifiers the current I_{BIAS} flowing through the transistor $M0$ is intended to be as high as possible, to minimize its thermal noise (described in the paragraph 2.5.5). In the arrangement with the telescopic cascode the current I_{BIAS} highly influences the equivalent small signal output resistance, where r_0 decreases with a higher current I_{BIAS}. It would be desirable to control separately the cascode $M2$ current and the input transistor $M0$ current. The improvement is achieved with the folded cascode architecture shown in Figure 3.5.

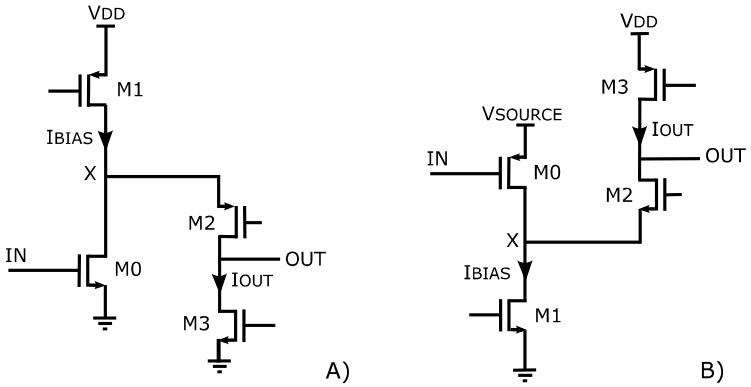


Figure 3.5 Common source amplifier with the folded cascode: A) NMOS input, B) PMOS input.

The folded cascode amplifier is composed out of four transistors: the input transistor $M0$, two current sources $M1$ and $M3$ and the cascode transistor $M2$. The current for the output stage I_{OUT} is set independently of the total current I_{BIAS}. The output current is intended to be low in order to increase the cascode small signal resistance r_{o2} in the output stage, whereas the input stage current I_{BIAS} is set to a high value magnifying the input transistor transconductance g_{m0}. The input current is limited by the CSA power budget. Meanwhile the output current is compromised between high output resistance and limited slew rate of the output signal.

The small signal open loop gain of the folded cascode amplifier is:

$$A = -\frac{g_{m0} \cdot r_{o0} \cdot r_{o1} \cdot r_{o3} \cdot (1 + g_{m2} \cdot r_{o2})}{(r_{o0} + r_{o1}) \cdot (r_{o2} + r_{o3}) + r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2})} \qquad 3\text{-}6$$

When the two currents (in $M0$ and $M2$) are not too much unbalanced, their transconductances are much higher than the small signal channel resistances and one can simplify *3-6* to:

$$A \approx -g_{m0} \cdot r_{o3} \qquad 3\text{-}7$$

By changing $M1$ to $M3$, the simplification leads to the same equation as *3-5* obtained for the telescopic cascode architecture: the open loop gain is the product of the transconductance of the input transistor by the output resistance of the output transistor.

If the two currents are too much dissymmetric and $I_{OUT} \ll I_{BIAS}$ the same simplification cannot be made and the open loop gain is:

$$A = -g_{m0} \cdot r_{o3} \frac{1}{1 + \frac{r_{o0} + r_{o1}}{g_{m2} \cdot r_{o0} \cdot r_{o1}}} \qquad 3\text{-}8$$

It has been revealed that the input stage supply voltage is not always the main ASIC supply. For this reason the input transistor source supply in Figure 3.5 is defined as V_{SOURCE} which is not necessarily the same as V_{DD}. In case of telescopic cascode (or with no cascode at all), the voltage swing between supplies and the output dynamic range are limited by V_{SOURCE}. The folded cascode structure folds the output signal back to the V_{DD} domain. This operation increases the output dynamic range.

Naturally, the folded cascode has some drawbacks compared to the telescopic one. If the two amplifiers would have the same total current consumption, in case of the folded cascode, the output drive is much lower due to $I_{OUT} \ll I_{BIAS}$. The fact is that the slew rate of the folded cascode is much lower and limited by the current source $M3$. This might severely limit output rise time in case of the NMOS cascode or fall time in case of the PMOS cascode. Consequently, in the circuit design, a special care must be taken to minimize the output load capacitance (and to choose the best amplifier polarity with respect to the signal polarity).

In summary, there are two reasons why the folded cascode is preferred to the common source stage. First of all it increases the output dynamic range comparing to a single inverting stage. Secondly the folded cascode separates the CSA into two stages, with no additional stability issues, allowing a high output impedance and maintaining a high transconductance of the input stage. Consequently a higher open loop gain can be achieved. The disadvantage is the limited output slew rate due to relatively small value of the output current I_{OUT}.

3.2.1.5 Unfolded cascode

An alternative architecture to the folded cascode that also brings similar open loop gain advantages is the unfolded cascode. It is shown in Figure 3.6. The signal path through the amplifier is not folded, like in the telescopic cascode. However the DC current paths are separated as in the folded cascode. This structure has an identical small signal model as the folded cascode. Consequently, the gain is described with the same equation *3-6*, or the simplified *3-7* and *3-10* This kind of amplifier is worth considering as an alternative to the folded cascode, again with respect to: voltage headroom, dynamic range and rise time.

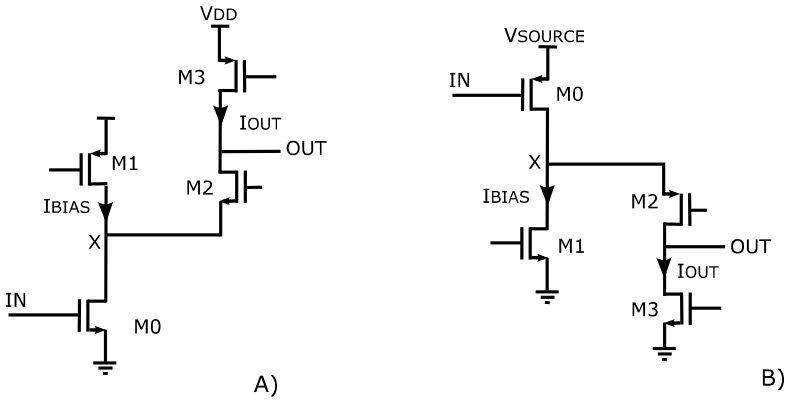


Figure 3.6 Common source amplifier with unfolded cascode: A) NMOS input, B) PMOS input.

3.2.1.6 CSA architectures summary

Several solutions for the CSA amplifier have been described. The discussion results are summarized in Table 3.2, where the most important design parameters are compared. For the CSA in the pixelated CdTe readout circuit, the power consumption and noise are the parameters that bring a substantial advantage to the single-ended input over the differential input amplifier.

Among the discussed single-ended amplifiers, the most interesting are the folded cascode and the unfolded cascode architectures. In Table 3.2 it is indicated that their output slew rate is rather poor, which is explained by the low value of the output current source $M3$. The issue has to be precised by distinguishing between PMOS and NMOS output current source polarities. With the PMOS output current source, Figure 3.5 B) and Figure 3.6 A), it is the rise time that is vulnerable to a limited slew rate at low I_{OUT}. The fall time is less of a concern since it is determined by a typically much higher current I_{BIAS}. In contrast, in amplifiers with the NMOS output current source, Figure 3.5 A) and Figure 3.6 B), it is the fall time where the low slew rate might become an issue at low I_{OUT} values.

CSA amplifier architecture	Open loop gain	Output slew rate	Output dynamic range	Input reference level	Noise	Power Cons.	Supply rejection
Differential input Active load	+	+	+	+	-	-	+
Single-ended input Common source	-	+	-	-	+	+	-
Single-ended input Telescopic cascode	+	+	-	-	+	+	-
Single-ended input Folded cascode	++	-	+	-	+	+	-
Single-ended input Unfolded cascode	++	-	+	-	+	+	-

Table 3.2 Comparison of the basic CSA architectures.

Concerning the folded and the unfolded cascode arrangements, a design parameter that also needs additional comment is the output dynamic range. More precisely the subject involves the input transistor type (PMOS and NMOS) and the cascode type (folded and unfolded). The cascode separates the output from the X node. Typically the current source $M1$ requires much higher voltage headroom than the input transistor $M0$ to operate in saturation. Therefore the node X potential is preferably set to a possibly high value with the PMOS input transistor and to a possibly low value with the NMOS input. It is the cascode polarity and its gate bias that impose the voltage at X, thus the input transistor polarity and the cascode stage type (folded or unfolded) should be considered simultaneously. It should be also remembered that the voltage headroom at the node X and indirectly the output dynamic range – both depend on the value of the V_{SOURCE} voltage.

The proposed architectures are the basic ones used for the CSA design. Each of them can be further improved with respect to the considered parameters. As one possibility, the telescopic and folded cascode can be used at the same time. Also an amplified folded cascode can be introduced, as demonstrated in [5]. Both actions are meant to increase the open loop gain A. Furthermore additional techniques can be introduced (like cascoding the current mirrors) to improve the current sources and to increase the small signal resistance (transistors $M1$ and $M3$). There are also practices

that recommend adding one more stage at the amplifier output, to separate the subject of the open loop gain and the output slew rate. This can be realized for example with an output source follower (which has little influence on the stability). The suitable solution however is mostly determined by the available resources: noise budget, power consumption and voltage headroom. In the application for which I consider the CSA design: with the low power consumption and rather low voltage headroom, the most attractive solutions are the folded and the unfolded cascode architectures.

3.2.2 Noise in folded and unfolded cascode CSA

Since the small signal models of the folded cascode and the unfolded cascode are the same, as well as the expressions describing the open loop gain – the following discussion is valid for both architectures. In the basic structures both amplifiers (Figure 3.5 and Figure 3.6) are constructed analogically with the four transistors:

- the input transistor $M0$
- the current source $M1$ for the input transistor bias current I_{BIAS}
- the cascode transistor $M2$
- the current source $M3$ for the output stage with cascode I_{OUT}, typically $I_{OUT} \ll I_{BIAS}$

Each of the transistors $M0 \,..\, M3$ is characterized with an inherent electronic noise v_{n0}^2 .. v_{n3}^2, referred to its gate. Localization of the four noise sources is illustrated in Figure 3.7. The noise sources include both the thermal and the flicker component. In this paragraph, the individual equivalent input noise contributions referred to the CSA input v_{nIN0}^2 .. v_{nIN3}^2 are calculated for each transistor [55]. They all add up to the total CSA input referred voltage noise:

$$v_{nIN}^2 = v_{nIN0}^2 + v_{nIN1}^2 + v_{nIN2}^2 + v_{nIN3}^2 \qquad 3\text{-}9$$

The CSA input-referred voltage noise ${v_{nIN}}^2$ corresponds to the CSA series noise analyzed in terms of the power distribution in the paragraph 2.2.6. The contribution of the gate-referred noise of each transistor is analyzed in Annex II.

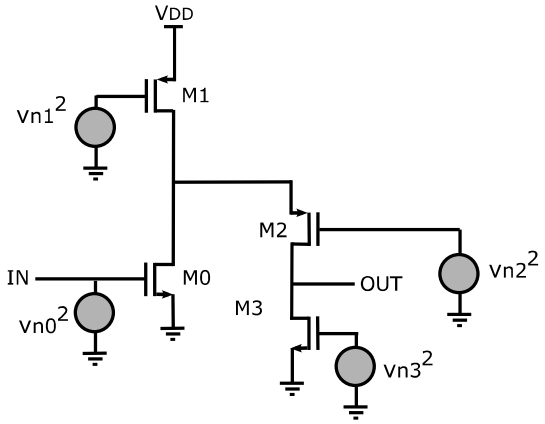


Figure 3.7 Transistor-level CSA: the NMOS-based folded cascode arrangement. Illustration of noise contributions from each transistors. Each noise is referred to the gate of a corresponding transistor.

Also, in the Annex II, I obtain the complete expression describing the total CSA input voltage noise:

$$v_{nIN}^2 = v_{n0}^2 + \frac{v_{n1}^2 {g_{m1}}^2}{{g_{m0}}^2} + v_{n2}^2 \left(\frac{r_{o0} + r_{o1}}{g_{m0} \cdot r_{o0} \cdot r_{o1}}\right)^2 + v_{n3}^2 \frac{{g_{m3}}^2}{{g_{m0}}^2} \left(\frac{r_{o0} + r_{o1}}{g_{m2} \cdot r_{o0} \cdot r_{o1}} + 1\right)^2 \quad 3\text{-}10$$

The calculations were carried out without distinguishing between the thermal noise and the flicker noise within the transistor gate referred voltage noise v_{ni}^2. Taking these two contributors into account each voltage noise v_{ni}^2 can be written as:

$$v_{ni}^2 = v_{ni\,th}^2 + v_{ni\,f}^2 \quad 3\text{-}11$$

Where $v_{ni\,th}^2$ is the thermal noise with flat power density and $v_{ni\,f}^2$ is the flicker noise with PSD proportional to $1/f$. When the two noise sources, with their characteristic spectral distributions, are distinguished – the following dependencies occur for each i-th transistor:

$$v_{ni\,th}^2 \sim \frac{1}{g_{mi}} \quad 3\text{-}12$$

$$v_{ni\,f}^2 \sim \frac{1}{W_i \cdot L_i} \quad 3\text{-}13$$

I will next show the consequences of these relations in the process of the CSA design optimization.

3.2.2.1 Low noise CSA – design recipe

The presented noise analysis leads to a set of guidelines for the design of the folded (and unfolded) cascode CSA. They are summarized in Table 3.3. A consequence of the noise amplification along the detection chain predicted in the paragraph 2.2.5 is significant already at the transistor level – within the internal CSA structure. From equation *3-10* I conclude that the transistor $M0$ has the most significant influence on the total noise in the CSA, and consequently on the total noise in the entire conversion chain.

Transistor	Parameter	Value	Effect
Input transistor $M0$	g_{m0}	High	Low noise High open loop gain
Cascode transistor $M2$	g_{m2}	High	Low noise High open loop gain
Both current mirrors $M1$ and $M3$	g_{m1} and g_{m3}	Low	Low noise
	r_{o1} and r_{o3}	High	High open loop gain
Input stage current mirror $M1$	I_{BIAS}	High	High open loop gain
Output stage current mirror $M3$	I_{OUT}	Low	Low noise High open loop gain
All transistors $M0\,..\,M3$	$W_i \cdot L_i$	High	Low noise

Table 3.3 Guidelines for designing a low noise CSA with the folded (unfolded) cascode architecture.

By applying the guidelines from Table 3.3 the most desirable situation can be achieved, where: $M0$ dominates the CSA input referred series noise while other transistors have negligible noise contribution. With the chosen CSA architecture the focus in the CSA optimization turns to the careful selection of the input transistor $M0$. Its desired low noise and high transconductance are both functions of the channel area (W and L) and of the current consumption I_{BIAS}. The determination of $M0$ dimensions and operating point that fulfill the best ENC performance of the whole detection

channel – is the successful choice. Because the optimal solution depends on the CdTe detector parameters (already set), on the CSA intrinsic capacitances, on the shaper type (let's assume it is predefined) and on the peaking time – the optimization of the transistor $M0$ is found to be the most critical part in the CSA design. The issues in the input transistor selection as well as my proposed approach in search for the optimal solution are described in the following section.

3.3 Multi-dimensional optimization

From the given parameters in a readout chain, the following dictate the total noise:

- The detector dark current I_{DET} and the resulting shot noise
- The total input capacitance C_{IN} and C_{CSA} (associated with the detector, the CSA and the physical connection between them)
- The CSA input transistor – the transistor type, its dimensions W, L and its bias current I_{BIAS}
- The filter type and peaking time

The CSA input transistor is the most important element that needs to be optimized, since different parameters of the detection channel (Figure 3.8) are related to its choice. First of all the input transistor dimensions define the input series noise power density (thermal and flicker). Meanwhile its gate oxide capacitance, also set by W and L, dominates the input capacitance C_{CSA} – so important in the ENC equations (discussed in paragraphs 2.3.2 - 2.3.6). This is the most interesting relation in the optimization process and I will discuss it in the first place. Secondly the MOS transistor: flicker noise, transconductance and capacitance per unit area are determined by technology parameters. Among several types of transistors available in the chosen IC technology XFAB $0.18\ \mu m$, each may have individual noise characteristics. Selection of the most appropriate transistor type is part of the optimization. Finally the shaper transfer function and the characteristic peaking time determine how much each noise component is filtered. In a given filter the optimal peaking time (where the lowest ENC is achieved) changes with proportions of the three dominating noise sources, that is: ${i_n}_p^2$ (dominated by the detector shot noise), ${v_n}_{th}^2$ (dominated by the CSA input transistor thermal noise) and ${v_n}_f^2$ (dominated by the CSA input transistor flicker noise).

The thermal noise of the input transistor highly depends on the bias current. Therefore it is intended to feed the transistor with the maximum available current. I have established the upper limit for the CSA power consumption to $18\ \mu W$ (from Table 3.1). However in order to well understand tradeoffs of this analog challenge, I also consider the I_{BIAS} variations in the transistor optimization.

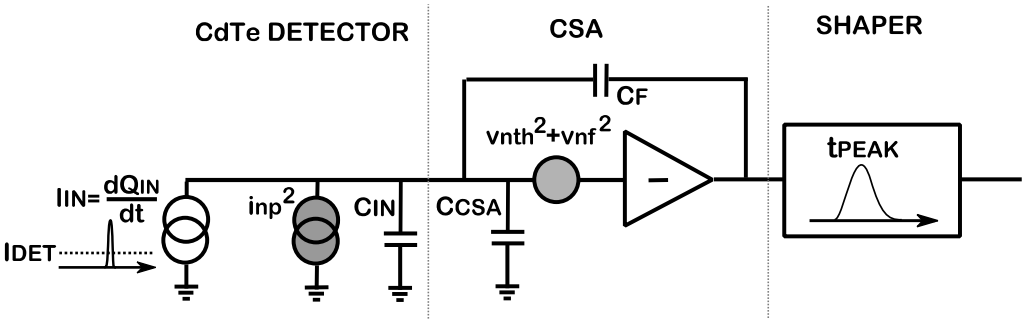


Figure 3.8 Detection chain with: the $300\ \mu m$ pitch CdTe detector model, the CSA and the shaper with the characteristic peaking time t_{peak}.

3.3.1 Capacitive matching

In the Chapter II, the significance of the CSA intrinsic input capacitance C_{CSA} on the system ENC has been highlighted. However I have postponed the profound discussion on origins and value of this capacitance until now. The gate capacitance of the CSA input transistor has a substantial contribution to the capacitance C_{CSA}. In fact, all other capacitive parasitics (mainly related to routing of the internal metal paths and the reset network) can be assumed negligible. If the input transistor operates in the strong inversion – the capacitance C_{CSA} can be described with the dominating gate oxide capacitance [55]:

$$C_{CSA} = \frac{2}{3} \cdot C_{OX} \cdot W \cdot L \qquad 3\text{-}14$$

Where C_{OX} is the gate oxide capacitance per unit area $[fF/\mu m^2]$; its value depends on the device type used as the input transistor. The capacitance C_{CSA} varies with the dimensions of the CSA input transistor: W and L.

Meanwhile the detector is also characterized with a specific capacitance C_{IN}, set by the application. I have estimated it (in the paragraph 2.1.3) to be in range between $0.3\,pF$ and $1pF$. It has been demonstrated [6][7][8][9] that the capacitive matching between the CSA (C_{CSA}) and the detector (C_{IN}) is one of the first rules in the noise optimization. The input capacitance is present in equations describing ENC due to both series noise contributors: ENC_{th} and ENC_f. By analyzing the corresponding equations, the optimum transistor dimensions, that minimize the two ENC components, can be determined:

$${ENC_{th}}^2 = \frac{1}{q^2} \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot \frac{1}{t_{peak}} \cdot A_{th} \qquad 3\text{-}15$$

$${ENC_f}^2 = \frac{1}{q^2} \cdot v_{n\,f}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_f \qquad 3\text{-}16$$

The equations have been derived in the paragraph 2.3.2. A_{th} and A_f are noise parameters and depend on the filter type (for exact values please refer to the paragraph 2.3.6). Let's consider at first each of the equations separately. Then I will compare the analyzed outcomes.

3.3.1.1 Capacitive matching – thermal noise

In case of ENC_{th} it is the term $v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2$, from the equation *3-15*, that needs to be optimized. It is done by evaluating the two parameters: $v_{n\,th}^2$ and C_{CSA}. Both of them are functions of the input transistor dimensions.

- C_{CSA} – in the saturation region the gate capacitance is given by the equation *3-14*.
- ${v_{n\,th}}^2$ – the noise power reduces with the increasing transconductance, which, in the saturation region, is proportional to the ratio W/L:

$${v_{n\,th}}^2 \sim \frac{1}{g_m} \approx \frac{1}{\sqrt{2 \cdot \mu \cdot C_{OX} \cdot I_D \cdot \frac{W}{L}}} \qquad 3\text{-}17$$

With a lower transistor length both the thermal noise and the gate capacitance get smaller. Therefore the best ENC_{th} can be obtained with the length fixed to the minimum L_{MIN}, which is set by the technology.

Further optimization is left to the transistor width. Its optimal value W can be found from the derivative of ENC_{th} as a function of the transistor. The desired W is the one corresponding to the minimum ENC_{th}, what can be found from the equation:

$$\frac{dENC_{th}(W)}{dW} = 0 \qquad 3\text{-}18$$

It can be shown that this occurs when the total input gate capacitance is [9]:

$$C_{CSA} = \frac{C_{IN} + C_F}{3} \qquad 3\text{-}19$$

This condition is referred to as the thermal noise capacitive matching. Assuming that the CSA input transistor operates in the saturation region – the optimal transconductance g_m and the gate capacitance of the input MOS C_{CSA} are achieved with the width of:

$$W = \frac{C_{IN} + C_F}{2 \cdot C_{OX} \cdot L} \qquad 3\text{-}20$$

Where L is preferably set to L_{MIN}.

In the CSA design discussed in this chapter I have estimated its power consumption to $18\ \mu W$. With the maximum supply voltage of $1.8\ V$ (imposed by the chosen IC technology), the CSA bias current should be in the order of $10\ \mu A$. With the relatively large W/L ratio – the high gain input transistor is likely to enter the moderate or the weak inversion operating region. In this case its transconductance would become nearly independent of the geometry [55]:

$$g_m \sim I_D \qquad 3\text{-}21$$

In this case the inversion charge starts to disappear from the channel and the input capacitance becomes dominated by the bulk capacitance. At this condition the expression *3-14*, describing the capacitance C_{CSA}, is no more accurate. Especially on the border of the two operating regions, an analytical optimization of $ENC_{th}(W, L)$ becomes quite a complex problem, therefore it is left for a numerical solution. The paragraph 3.3.2 is dedicated to the description of the procedure. Even once the optimal width W is found, such to ensure the thermal noise capacitive matching, it does not guarantee the lowest noise. There is still the second ENC component related to the flicker noise, for which the capacitive matching W and L conditions also need to be found. In the end, the lowest ENC is a compromise between the two: thermal and flicker noise matching conditions.

3.3.1.2 Capacitive matching – flicker noise

The ENC due to flicker noise is optimized by analyzing the term: $v_{n\,f}^2 \cdot (C_F + C_{IN} + C_{CSA})^2$ from the equation *3-16*. Again there are two parameters that depend on the input transistor geometry:

- The capacitance C_{CSA}, which as in case of the ENC_{th}can be approximated by the expression *3-14* if the CSA input transistor operates in the saturation region.

- The flicker noise, which in many models has been shown to be inversely proportional to the total gate area:

$$v_{n\,f}^2 \sim \frac{1}{W \cdot L} \qquad 3\text{-}22$$

Assuming that this flicker noise model is valid, the minimum ENC_f is found when the following condition is met:

$$\frac{dENC_f(W \cdot L)}{d(W \cdot L)} = 0 \qquad 3\text{-}23$$

Once the equation is solved, the optimum gate capacitance for minimizing effects of the flicker noise is found to be:

$$C_{CSA} = C_{IN} + C_F \qquad 3\text{-}24$$

This condition provides the capacitive matching for the flicker noise.

Again, in this calculation the strong inversion operation has been assumed. The expected CSA operation at the edge of weak inversion, together with the uncertainty of the correct flicker noise model – lead to the necessity for numerical optimization in simulations.

ENC_{th} and ENC_f can be both optimized by selecting an appropriate geometry of the CSA input transistor. In both cases the conclusion of this analysis is that the best W and L dimensions cannot be found analytically. Consequently I have performed the numerical simulations, which find the optimal geometry where the sum of ENC_{th} and ENC_f is the lowest. The simulations address also the question over the best peaking time – where the total ENC, including the parallel noise contribution ENC_p, is the lowest.

3.3.2 Numerical solution to parameterized ENC equation

In fact the balance in the CSA input transistor dimensions has to be found through multidimensional simulations, more complicated than the two-dimensional transistor geometry (W, L) predicted above from the capacitive matching.

3.3.2.1 The large scale simulation

The primary parameter is the detector capacitance that has a certain spread, which has been established to the range from $0.3\ pF$ to $1\ pF$. The input transistor width and length must be chosen to match this capacitance. This means, that there are at least two optimal geometries, each matching one extreme. Assuming that these two CSA would be integrated on the testchip, there is still the uncertainty of the outcome if these CSA operate with the C_{IN} lying in between the given range, for example $0.6\ pF$. The answer must be found through simulations.

The number of the simulations is further increased by the number of the transistor types available in the chosen IC process, which I would like to analyze. In the XFAB $0.18\ \mu m$ the PMOS and NMOS transistors both exist with different oxide thicknesses, resulting in different C_{OX}. The obvious

implication is that the optimal geometry will not be necessarily identical for these different transistors. The task becomes even more complicated once one notices that there are two transistor models provided by the foundry: BSIM3v3 and SPICE2. It will be shown later, that the two models do not give identical results. This makes the choice of the final CSA dimensions even more difficult to finalize.

The next simulation parameter could be the detector dark current. Here I have decided to consider only the worst case of $5\ pA$, where the shot noise is the highest. Finally the shaper stage for the ENC calculations is fixed to the 4^{th} order semi-Gaussian. In terms of the shaper paramaters: A_p, A_{th} and A_f, it is a compromise between an N-th order semi-Gaussian and an MCDS shaper, whose noise parameters are not that far apart. For the fixed filter stage – the peaking time is set as a variable to determine the absolute minimum ENC with the given shaper. Finally I have included the bias current I_{BIAS} as a simulation parameter. Its nominal value has been set to $10\ \mu A$. Simulations at, at least, two different current levels are necessary to understand how sensitive is the ENC (mainly the thermal component) to the current variations.

Only having the answer to the ENC behaviour with respect to all listed parameters, I could decide about the input transistor CSA dimensions and move on to the complete CSA design.

Parameter	Optimization corner values
Total external input capacitance	0.3 pF 1 pF
CSA bias current	2 µA 10 µA
Input transistor types	PE – thin oxide PMOS (1.8V) PEI – thin oxide isolated PMOS (1.8V) PE3 – thick oxide PMOS (3.3 V) NE – thin oxide NMOS (1.8V) NEI – thin oxide isolated NMOS (1.8 V) NE3 – thick oxide NMOS (3.3 V)
Input transistor width	50 – 1000 µm
Input transistor length	0.18 – 3 µm
Peaking time of the shaper	0.1 – 40 µs
Transistor noise model	BSIM3v3 SPICE2

Table 3.4 Parameters varied in the numerical optimization of the CSA. The leakage current $5\ pA$*, the temperature* 25 ℃ *and the feedback capacitance* $25\ fF$ *are fixed.*

3.3.2.2 Pseudo-ideal CSA for input transistor optimization

In the input transistor optimization, I have used a pseudo-ideal CSA, where only the noise from the input transistor was taken into account. All eventual noise contributions due to the cascode and the current mirrors were excluded – I made the assumption that their contribution to the total noise would be negligible. This highly simplified the whole procedure. The simulated CSA contains: the input transistor (the model provided by the foundry), the bias current source realized with an ideal current source and an ideal amplifying stage realized with a voltage controlled voltage source. The schematic of the pseudo-ideal CSA is illustrated in Figure 3.9.

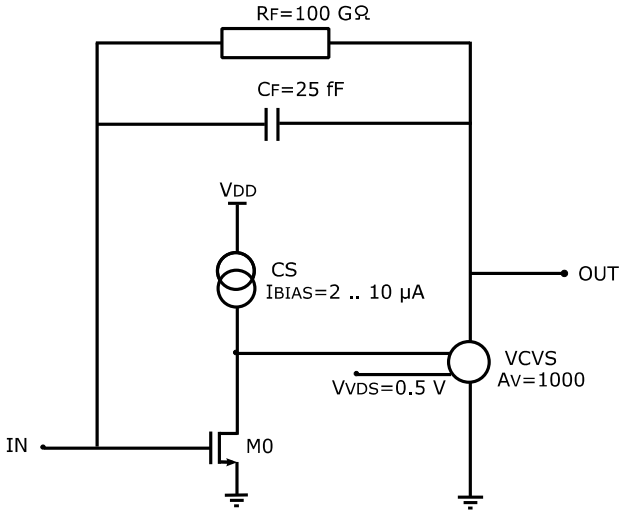


Figure 3.9 The pseudo-ideal CSA schematic used in simulations for the CSA input transistor optimization. As the input transistor M0 – one of the transistors from the design kit is used. The transistor bias current I_{BIAS} is set with the ideal current source CS. The CSA gain is ensured by the amplifying element realized with the voltage controlled voltage source VCVS with the voltage gain A_V set to 1000. The CSA operating point is set by the reference voltage V_{VDS}, with a high CSA open loop gain of approximately $g_{m0} \cdot A_V$ – the drain of M0 is regulated at the level of V_{VDS}.

The described CSA was simulated in a detection chain together with the CdTe detector model (defined in 2.1) and with the 4^{th} order CR-RC shaper with variable peaking time t_{peak}. The CSA input transistor noise is defined by the operating point and its dimensions. With a geometry W and L, the bias current I_{BIAS} and the V_{DS} voltage regulated around the feedback loop to the value V_{VDS} – the ENC at the channel output can be calculated. It has been shown (in 2.3) that: the ENC due to thermal noise is inversely proportional to peaking time, the ENC contribution of the flicker noise is constant with the peaking time, finally the parallel white noise contribution to ENC increases with the peaking time. All three components are plotted in Figure 3.10 as a function of the peaking time. The total ENC that is a squared sum of the listed contributors is a nonlinear function of the peaking time. A minimum ENC_{MIN} exists that corresponds to optimal peaking time $t_{peak\,OPT}$. This is what the optimization task is looking for. A change of CSA dimensions, and thus its noise would change the balance between the three contributors. Therefore the optimum peaking time is strongly related to the CSA dimensions.

I have performed a three-dimensional simulation, where the input transistor width W, length L and shaper peaking time t_{peak} were parameterized. In each sub-simulation the noise at the shaper output $\overline{v_n^2}$ and its transient response $y_{LN\,max}(t)$ to a given input charge Q_{IN} were determined. ENC was calculated for each point (W, L, t_{peak}) according to the formula:

$$ENC(W, L, t_{peak}) = \frac{Q_{IN}}{q} \cdot \frac{\overline{v_n^2}}{y_{LN\,max}(t)} \qquad 3\text{-}25$$

For each series of parametric simulations with fixed W and L – the ENC was calculated. Then the minimum value $ENC_{min} = ENC(t_{peak\,OPT})$, with corresponding peaking time $t_{peak\,OPT}$ were found.

3.3. Multi-dimensional optimization

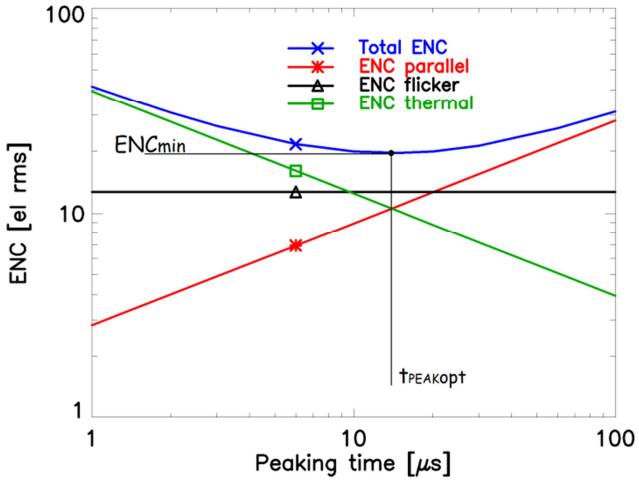
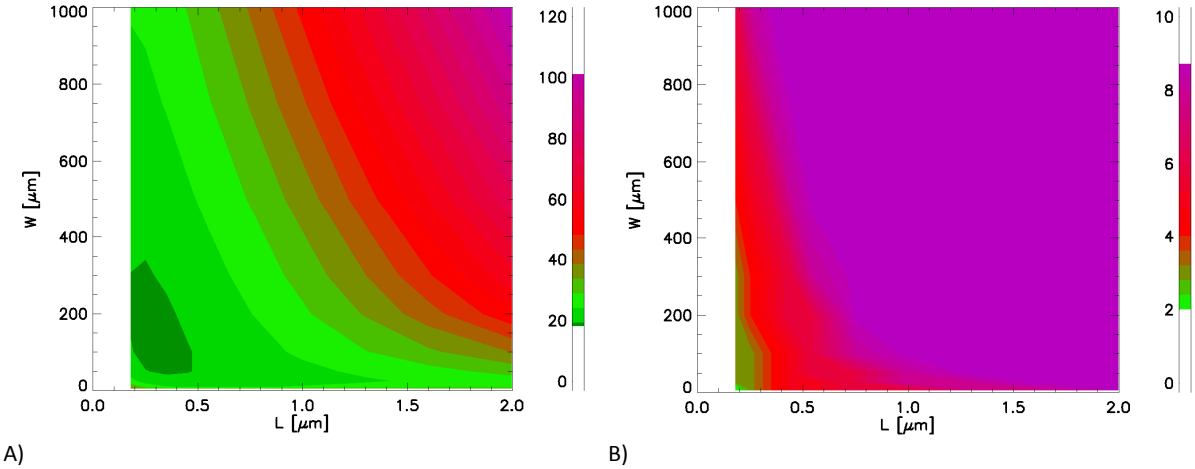


Figure 3.10 Simulation result: ENC of CSA with a semi-Gaussian shaper as a function of the peaking time. Detector dark current is set to $1\ pA$ *nd its capacitance to* $0.3\ pF$*. The total ENC as well as its individual contributors (parallel white noise , thermal noise and flicker noise) are presented.*

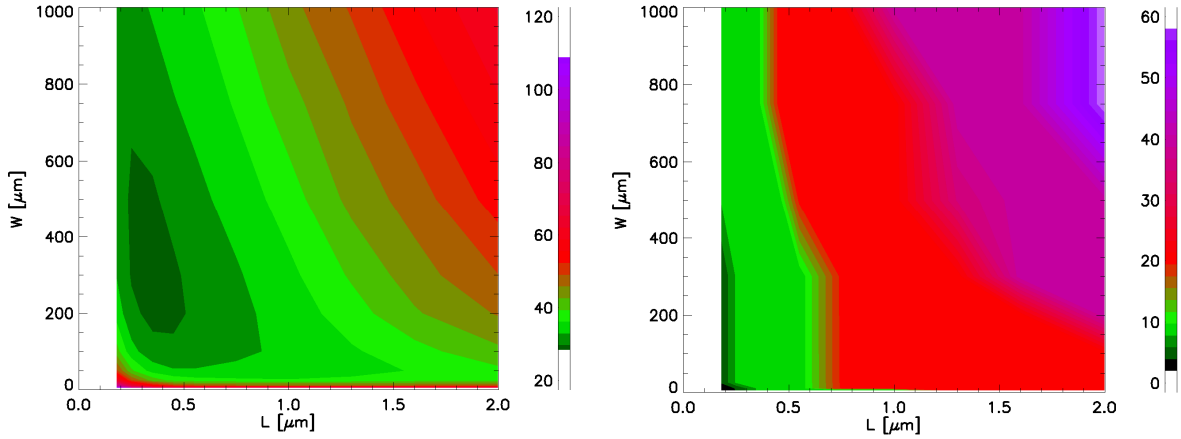
In this three-dimensional simulation the peaking time and the input transistor dimensions were varied automatically to check ENC at different values of these parameters. With the aid of a dedicated script the optimal point (W_{OPT}, L_{OPT}, $t_{peak\ OPT}$) was extracted from all the elementary simulations. This point corresponds to the lowest ENC achievable at the given simulation conditions (the detector parameters, the bias current, the transistor type and the simulator model).

Finally I have generated an ENC map to visualize the evolution of the minimum ENC with the varying width and length. Because of the interest to find the minimum ENC at different simulation conditions, including most of the combinations from Table 3.4 – I have repeated the described optimization procedure multiple times. The simulation conditions were also varied, according to Table 3.4, resulting in a set of 48 three-dimensional simulations.



A) B)

Figure 3.11 A) Minimum ENC [electrons rms] as a function of the transistor width W *and length* L*. The absolute minimum ENC occurs around the dark shaded spot. In this particular case, with a CSA based on the PMOS PE with* $10\ \mu A$ *bias current and at* $\underline{300\ fF}$ *input capacitance – the minimum ENC of* $18.1\ el\ rms$ *and is found at* $W = 100\ \mu m$*,* $L = 0.25\ \mu m$ *and* $t_{peak} = 3\ \mu s$*. B) Corresponding optimum peaking time* $t_{peakOPT}\ [\mu s]$*.*



A) B)

Figure 3.12 A) Minimum ENC [electrons rms] as a function of the transistor width W and length L. The absolute minimum ENC occurs around the dark shaded spot. In this particular case, with a CSA based on the PMOS PE with $10\ \mu A$ bias current and at $1\ pF$ input capacitance – the minimum ENC of $28.3\ el\ rms$ and is found at $W = 300\ \mu m$, $L = 0.35\ \mu m$ and $t_{peak} = 9\ \mu s$. B) Corresponding optimum peaking time $t_{peakOPT}\ [\mu s]$.

Figure 3.11 and Figure 3.12 show example of the result of one of the multi-dimensional simulations with the ENC map. Both have been obtained for the input transistor PE. In Figure 3.11 the input parameters are: the thin oxide PMOS PE with $10\ \mu A$ bias current, the detector input capacitance of $300\ fF$. Its dark current set to the most pessimist value of $5\ pA$. The presented plot shows the minimum $ENC(t_{peak\ OPT})$ calculated for each $[W, L]$ combination. In the given example the darkest area on the ENC map indicates the transistor geometry where the lowest ENC can be achieved. In the example, using the BSIM3v3 noise model, the very best result is obtained for $W/L = 100\mu m/0.25\mu m$ with $ENC = 18.1\ el\ rms$. In each $[W, L]$ pair simulation the peaking time corresponding to the minimum ENC has been monitored. In the given example when W and L are set to the optimum dimensions – the minimum ENC is obtained with $3\ \mu s$ peaking time. The results from Figure 3.12 show the optimization of the same transistor type PE also biased at $10\ \mu A$, at the same detector dark current of $5\ pA$. In this case however the ENC of the pseudo-ideal CSA is calculated to match the detector capacitance of $1\ pF$. In this case the best ENC is $28.3\ el\ rms$ at $t_{peakOPT} = 9\ \mu s$.

3.3.3 CSA optimization summary

The CSA input transistor has been optimized at different detector conditions and bias conditions, according to Table 3.4 (in 3.3.2). Six different input devices offered by the XFAB $0.18\ \mu m$ have been taken into account. In Table 3.5 I have summarized all of the results obtained with a single MOS noise model: BSIM3v3 [11]. The most important features observed from the presented numbers are:

- The optimum width W ranges from $100\ \mu m$ to $750\ \mu m$ and length from $0.25\ \mu m$ to $1.6\ \mu m$.
- The optimum length is about four times higher in the NMOS-based CSA.
- For a given transistor type the optimum width is always higher at a higher detector capacitance (as predicted by the capacitive matching).
- The lowest ENC achieved in simulations corresponds to the PMOS transistor PE3 with thick oxide.
- In most cases the optimal dimensions remain constant with the bias current.

The last conclusion is especially interesting from the point of view of integrating the CSA in the testchip. A single CSA with adjustable bias current can be experimentally tested with respect to the power consumption. Simultaneously the transistor dimensions always remain very close to the optimal value.

Conditions: C_{DET}=1pF, I_{BIAS}=10µA			
Transistor type	ENC_{MIN} $[el_{rms}]$	$t_{peak\,OPT}$ $[\mu s]$	W_{OPT}/L_{OPT} $[\mu m/\mu m]$
PE	28.3	9	300/0.35
PEI	28	8	300/0.35
PE3	21	6	500/0.3
NE	33.1	8	300/1.6
NEI	34.1	10	200/1.6
NE3	39.5	10	750/1
Conditions: C_{DET}=0.3pF, I_{BIAS}=10µA			
Transistor type	ENC_{MIN} $[el_{rms}]$	$t_{peak\,OPT}$ $[\mu s]$	W_{OPT}/L_{OPT} $[\mu m/\mu m]$
PE	18.1	3	100/0.25
PEI	17.7	3	200/0.25
PE3	13.9	3	200/0.3
NE	22.1	4	100/1.3
NEI	22.5	5	100/1.3
NE3	27	4	500/0.75
Conditions: C_{DET}=1pF, I_{BIAS}=2µA			
Transistor type	ENC_{MIN} $[el_{rms}]$	$t_{peak\,OPT}$ $[\mu s]$	W_{OPT}/L_{OPT} $[\mu m/\mu m]$
PE	35.3	15	300/0.35
PEI	34	13	300/0.35
PE3	26.5	12	300/0.3
NE	35.5	12	300/1.6
NEI	39.2	16	200/1.6
NE3	42.5	17	300/1.6
Conditions: C_{DET}=0.3pF, I_{BIAS}=2µA			
Transistor type	ENC_{MIN} $[el_{rms}]$	$t_{peak\,OPT}$ $[\mu s]$	W_{OPT}/L_{OPT} $[\mu m/\mu m]$
PE	22.1	6	100/0.25
PEI	21.3	6	100/0.35
PE3	17.4	6	200/0.3
NE	23.4	6	100/1.3
NEI	25.1	8	100/1.3
NE3	27.2	6	200/1

Table 3.5 Minimum ENC values obtained in multi-parametric simulations, each line corresponds to $ENC(W, L, t_{peak})$ optimization with the 4^{th} order semi-Gaussian shaper and shot noise due to $5\ pA$ detector leakage current. Results presented for two values of the detector capacitance: $0.3\ pF$ and $1\ pF$ and two values of the bias current: $2\ \mu A$ and $10\ \mu A$. Noise model BSIM3v3 is used in simulations.

I have performed an identical set of simulations with the second of the MOS noise models provided by the foundry: SPICE2 [11]. Consequently the two sets of optimum conditions, obtained with: BSIM3v3 and SPICE2 have been compared. The minimum ENC and the corresponding optimal W and L dimensions are summarized in Table 3.6.

Conditions: C_{DET}=1pF, I_{BIAS}=10µA				
Transistor type	Noise model: SPICE2		Noise model: BSIM3v3	
	ENC_{MIN} $[el_{rms}]$	W_{OPT}/L_{OPT} $[\mu m/\mu m]$	ENC_{MIN} $[el_{rms}]$	W_{OPT}/L_{OPT} $[\mu m/\mu m$
PE	33.1	100/0.55	28.3	300/0.35
PEI	33.5	100/0.75	28	300/0.35
PE3	29.9	200/0.35	21	500/0.3
NE	40	100/2	33.1	300/1.6
NEI	38.8	100/2	34.1	200/1.6
NE3	47.8	500/0.75	39.5	750/1
Conditions: C_{DET}=0.3pF, I_{BIAS}=10µA				
Transistor type	Noise model: SPICE2		Noise model: BSIM3v3	
	ENC_{MIN} $[el_{rms}]$	W_{OPT}/L_{OPT} $[\mu m/\mu m]$	ENC_{MIN} $[el_{rms}]$	W_{OPT}/L_{OPT} $[\mu m/\mu m$
PE	20.5	50/0.35	18.1	100/0.25
PEI	20.8	50/0.45	17.7	200/0.25
PE3	18.4	100/0.3	13.9	200/0.3
NE	25.9	100/1.3	22.1	100/1.3
NEI	25.3	50/1.3	22.5	100/1.3
NE3	31.5	300/0.55	27	500/0.75

Table 3.6 Comparison of two noise models in ENC optimization: SPICE2 and BSIM3v3. Each line corresponds to $ENC(W, L, t_{peak})$ optimization with the 4^{th} order semi-Gaussian shaper and shot noise due to 5 pA detector leakage current. Bias current set to 10 µA. Results presented for two values of the detector capacitance: 0.3 pF and 1 pF

Because of the similar observation for both models: that the bias current does not influence the optimal geometry – I present the comparison only for I_{BIAS} of 10 μA. The following conclusions are drawn from this comparison:

- The optimum width indicated by the SPICE2 noise model is always lower than with BSIM3v3.
- The values of the minimum ENC differ by about 20 % and are consistently lower with the BSIM3v3 noise model.

Regardless of the noise model, the thick oxide PMOS PE3 still points the way towards the lowest ENC, whereas the NE3, which is also a thick oxide device shows the worst noise performance. This is consequence of: the flicker noise parameters and the gain factor: $\mu \cdot C_{OX}$ in the transconductance formula appearing in *3-17*, which differ between the transistor types.

The obtained results were carefully analyzed to determine which transistor dimensions should be chosen for the final implementation on the testchip. Because of different dimensions with different noise models, a general question on the models' accuracy has been raised. In consequence, despite poorer performance of some transistor types, I considered their integration in the ASIC for experimental verification.

3.3.4 Caterpylar ASIC

The performed optimization was meant to determine the CSA input transistor type and the geometry that would provide the best ENC with the small pixel CdTe detector. The best CSA became the first candidates to integrate in the developed testchip. Although the two available transistor models have shown different results concerning the optimal dimensions, in both cases it has been the PE3

transistor type that provided the best readout resolution according to simulations. To understand the process better through measurements I have decided to integrate CSAs with different input transistor types on the testchip, however excluding the isolated devices PEI/NEI which appear to be very similar to PE/NE and excluding the noisy NE3. The different geometry outcomes from the two noise models resulted in the dilemma: which one should be followed. This is how I have approached the solution: knowing that the BSIM3v3 model [11] is more recent and more parameterized than SPICE2, intuitively I selected this model as a reference. For each transistor type of interest I have decided to design CSAs with the optimal dimensions obtained with BSIM3v3. However I extended the number of CSA dedicated for testchip implementation to additional ones with the input transistor width plus/minus variations from the optimal dimensions.

The carefully selected input transistors were inserted into real amplifiers, where the bias current sources and the cascode have been designed to add the possibly lowest additional noise. Because of the low total current consumption and thus a limited transconductance of the input stage this additional noise is noticeable, especially with the lower bias current value of $2\ \mu A$. Consequently the noise contribution of the input transistor has been found to be in a range between 60% and 90%. Nevertheless these calculations, based on the squared voltage noise, prove that in the CSA's optimization, the input transistor noise is still the most important element, justifying use of the proposed pseudo-ideal CSA from Figure 3.9 in the procedure. Correspondingly, in simulations of the complete CSA, I have found that the ENC increases by up to 20% in comparison to the pseudo-ideal CSA from Figure 3.9. To cross-check that the input transistor dimensions were still correct in the complete design – I have performed additional multi-dimensional ENC simulations (on much smaller scale) with the real amplifiers.

3.3.4.1 Top-level circuit description

The outcome of the CSA optimization is the testchip design. The ASIC is called IDeF-X Caterpylar and it contains 26 CSAs dedicated to experimental verifications. The ASIC does not include the filter stage, any additional processing as well as the pulse discrimination has to be performed externally. The general top-level architecture is illustrated in Figure 3.13. All CSA channels are multiplexed to a common output stage, thus only one channel can be monitored at a time. The readout path can be selected between: an output source follower buffer and a differential amplifier based buffer with either unity gain or $\times\ 4$. Before the output buffer, the supply domain is $1.8\ V$, where the best was done to utilize a maximum output dynamic range. The common output buffer which enables additional amplification is realized in the $3.3\ V$ domain.

Each of the 26 channels has a different CSA, the variety includes three different architectures and different types and dimensions of the input transistor. I have already described (in the paragraph 3.3.3) the selection process of the CSA input devices – on the testchip one can identify three types: thin oxide PMOS and NMOS and thick oxide PMOS. Their dimensions have been chosen to cover the proximity of the minimum ENC simulated with two noise models (BSIM3v3 and SPICE2). Additional CSA of dimensions beyond the optimum have been included to investigate the effect of variable W and L on the flicker noise and the thermal noise as a function of the W/L ratio. The complete list of CSAs integrated on the IDeF-X Caterpylar testchip is presented in Table 3.7.

3.3. Multi-dimensional optimization

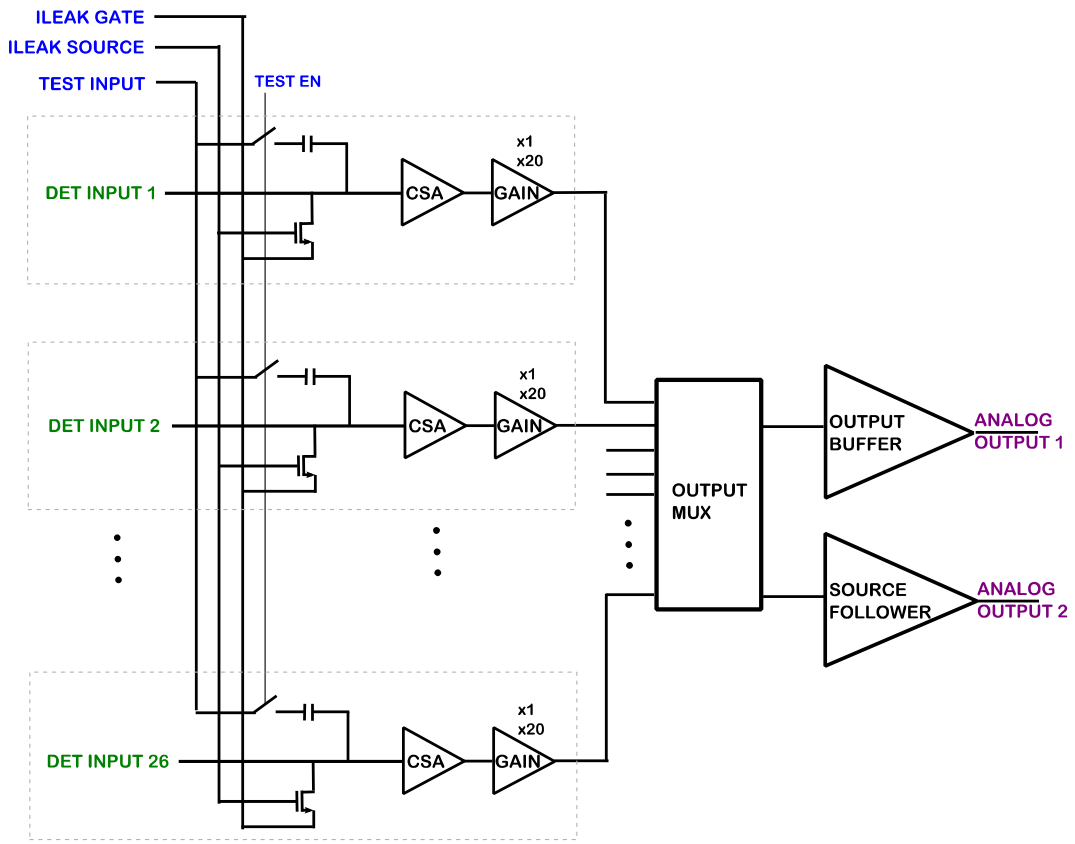


Figure 3.13 General architecture of the Caterpylar ASIC: 26 channels with CSA multiplexed to the common output stage.

No	Input transistor type	CSA type	Size [µm/µm]
T1	PE thin oxide	Folded	100/0.18
T2	PE thin oxide	Folded	100/0.25
T3	PE thin oxide	Folded	100/0.45
T4	PE thin oxide	Folded	100/0.55
T5	PE thin oxide	Folded	300/0.18
T6	PE thin oxide	Folded	300/0.25
T7	PE thin oxide	Folded	300/0.45
T8	PE thin oxide	Folded	300/0.55
T9	PE3 thick oxide	Folded	100/0.3
T10	PE3 thick oxide	Folded	100/0.45
T11	PE3 thick oxide	Folded	100/0.55
T12	PE3 thick oxide	Folded	300/0.3
T13	PE3 thick oxide	Folded	300/0.45
T14	PE3 thick oxide	Folded	300/0.55

No	Input transistor type	CSA type	Size [µm/µm]
T15	NE thin oxide	Folded	100/0.8
T16	NE thin oxide	Folded	100/1
T17	NE thin oxide	Folded	100/1.3
T18	NE thin oxide	Folded	200/1.3
T19	NE thin oxide	Folded	200/1.6
T20	NE thin oxide	Folded	200/2
T21	NE thin oxide	Unfolded	100/0.8
T22	NE thin oxide	Unfolded	100/1
T23	NE thin oxide	Unfolded	100/1.3
T24	NE thin oxide	Unfolded	200/1.3
T25	NE thin oxide	Unfolded	200/1.6
T26	NE thin oxide	Unfolded	200/2

Table 3.7 Dimensions of 26 CSA integrated on the IDeF-X Caterpylar test chip. The values correspond to optimum obtained in simulations.

Two different polarities (PMOS and NMOS) have determined the implementation of two folded cascode architectures: with PMOS input and NMOS input. Furthermore the same NMOS input transistors were copied into a third CSA architecture – the unfolded cascode. All CSA sharing the same architecture have identical core structure, where only the input transistor dimensions are variable. For example all the folded cascode PMOS CSA: $T1$ to $T14$ are identical except for the variable input transistor geometry. This is true also in terms of layout. There are also certain structures that are common for all CSA, that is:

- reset feedback PMOS transistor
- input test structure for charge injection
- input current compensation circuit
- buffer with gain: $\times 1$ or $\times 20$

Below I describe details of the Caterpylar ASIC architecture.

3.3.4.2 Caterpylar three CSA architectures

The three inner CSA architectures that one can identify on the testchip are depicted in Figure 3.14: the PMOS input folded cascode, the NMOS input folded cascode and the NMOS input unfolded cascode. The CSA are intended to read out signals from the anode of a CdTe detector. Therefore their functionality provides higher amplitude of the positive output voltage step, resulting from negative charge signal. All CSAs have been optimized to the appropriate DC operating point and output dynamic range of approximately $0.6\,V$. However the possibility of external analog adjustment of the cascode gate bias brings flexibility to adapt the dynamic range also for measurements with the cathode readout.

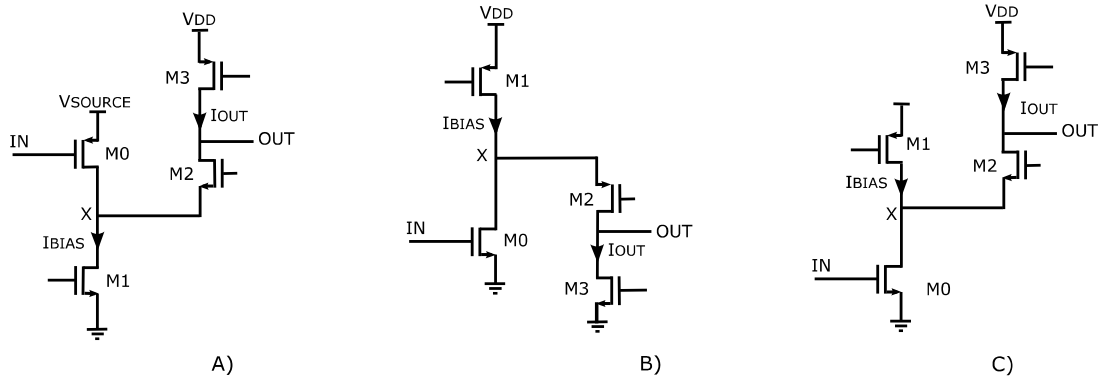


Figure 3.14 Three CSA architectures implemented on the IDeF-X Caterpylar testchip: A) Folded cascode PMOS input, B) Folded cascode NMOS input, C) Unfolded cascode NMOS input.

Each CSA has adjustable bias currents: I_{BIAS} in the input transistor is between $2\ \mu A$ and $12\ \mu A$ and I_{OUT} in the output stage ranges from $100\ nA$ to $700\ nA$. The first current source influences mainly the thermal noise contribution to ENC, whereas the second one I_{OUT} controls the CSA bandwidth.

3.3.4.3 Test injection

Most of the planned Caterpylar lab tests have been aimed for the pure electrical characterization. Therefore it has been designed to be able to operate without any detector, but with the signal

charge injected by some other electronic means. There are certain important reasons to this characterization approach. Operating with a detector imposes requirements on the lab environment (e.g. controlled temperature) and adds additional difficulties in the setup handling. Furthermore the charge signal is originating from the X-rays photons absorbed in the detector, whose energy cannot be adjusted (except for X-ray generators).

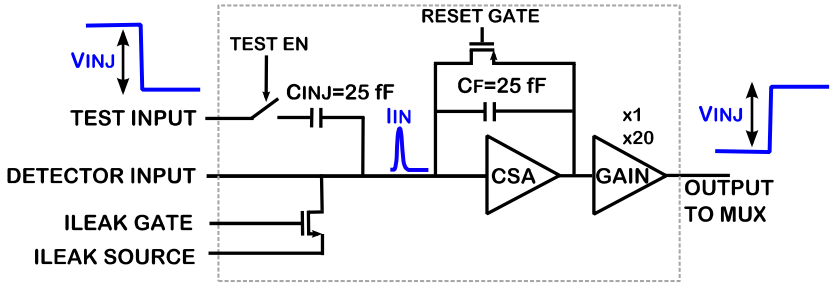


Figure 3.15 A structure common to all channels: input test injection, input current compensation (ILEAK), feedback capacitance and reset as well as the output gain stage selectable between $\times 1$ *and* $\times 20$.

A special test input has been included in each readout channel with CSA to enable a controlled charge transfer. The input signal is injected through a series capacitance C_{INJ} shown in Figure 3.15. The $TEST\ INPUT$ is common to all CSA, but each channel has an individual injection capacitance C_{INJ}. If necessary each channel may be disabled individually by deselecting the control signal $TEST\ EN$. Applying a negative voltage step V_{INJ} on the test capacitance input results in injection of a negative charge at the CSA input, equal to $V_{INJ} \cdot C_{INJ}$. The capacitance has the same value as the feedback capacitance C_F of $25\ fF$, therefore the expected CSA response is a positive step of amplitude equal to V_{INJ}. The two capacitances C_F and C_{INJ} are carefully matched to reduce gain errors in the measurements.

3.3.4.4 CSA reset

The reset is realized with a PMOS transistor. With an external access to its gate, as shown in Figure 3.15, it can be operated in two modes: as continuous reset by applying a DC voltage or as switched reset by controlling the gate with a digital signal. More details on these two reset types can be found in the paragraph 2.2.4.

The transistor dimensions are more critical in the continuous operation. Therefore they are primarily optimized for this reset mode, to provide a high equivalent resistance and low noise during the signal acquisition.

Continuous reset operation

The continuous reset is achieved by applying a DC voltage to the feedback transistor gate. Typically the value is around $0.7\ V$ for PMOS input CSA and $0.45\ V$ for NMOS input CSA. The transistor operates in the subthreshold region, its equivalent resistance is in the order of tens of $G\Omega$. Because of the PMOS type reset transistor, the feedback current can only flow in one direction through the feedback: from the CSA output to the CSA input. Consequently it can provide a current path only for the detector anode dark current drawn “out of the CSA input”.

In case where the circuit operates in the continuous feedback mode, the output baseline voltage must be higher than the CSA input. It is a consequence of the V_{DS} voltage drop on the PMOS in the feedback loop. This voltage depends on the amount of current through the reset PMOS transistor. This is important to consider because of its strong relation with the output dynamic range. With the NMOS as the CSA input transistor the voltage at the CSA input is equal to its V_{GS}, which is only few hundred millivolts above the ground. Since the output has to be higher than the input – the output dynamic range becomes critical, to give place to the positive output signal. In case of the PMOS based CSA, in order to keep the input voltage relatively low the V_{GS} voltage is shifted down from the positive supply. This means that instead of using also V_{DD} of $1.8\ V$, a lower supply V_{SOURCE} has to be provided. This additional supply domain is illustrated in Figure 3.14 A). Its typical value is $1.3\ V$, what ensures the output dynamic range comparable to the NMOS-based CSA.

The pole-zero cancellation structure (detailed in the paragraph 2.2.4) matching the CSA feedback network has not been included on the Caterpylar ASIC. All measurements in the continuous reset configuration are performed with an external shaper, which has its own PZ cancellation network.

Continuous reset noise

The continuous-reset is a source of noise since a DC current flows through the transistor channel. Similarly with the shot noise, its contribution is represented as within the parallel noise source ${i_n}_p^2$ at the CSA input, shown in Figure 3.8. When referred to the CSA input – the reset noise contribution has the power density ${i_n}_{rst}^2$, which is a white noise dominated by the thermal origins.

Its character is similar to the detector shot noise [12]. This theory has been confirmed by one of the two available simulation noise models – SPICE2 [11]. I have later validated the shot-like behaviour with the experimental results with the Caterpylar ASIC [14], what is demonstrated in 3.4.4. Consequently the noise contribution ${i_n}_{rst}^2$ due to the reset current I_{rst} can be predicted by the shot noise equation:

$$ {i_n}_{rst}^2 = 2 \cdot q \cdot I_{rst} \qquad 3\text{-}26 $$

In a typical application with the detector anode connected to the CSA input – the current through the reset transistor I_{rst} equals to the detector dark current I_{DET}. According to this model it can be stated that the reset transistor “doubles” the shot noise.

Switched reset operation

The CSA reset operates in the switched mode when the feedback transistor gate (shown in Figure 3.14) is controlled with a digital signal, as illustrated in Figure 3.16. During the reset phase the transistor is switched on, shorting the CSA input and output. The action sets the output baseline to a value equal to the CSA input voltage, the latter one is regulated by the input transistor bias current I_{BIAS} and the V_{SOURCE} voltage. The duration of the reset phase is in the order of a microsecond. Afterwards the acquisition phase starts, where the reset transistor is switched off. Throughout this time the CSA can receive input charge signals, however there is no DC path for the detector dark current continuously being drawn from the CSA input node. Therefore the CSA output voltage linearly increases with rate:

$$\frac{\Delta V_{CSA}}{\Delta t} = \frac{I_{det}}{C_F} \qquad 3\text{-}27$$

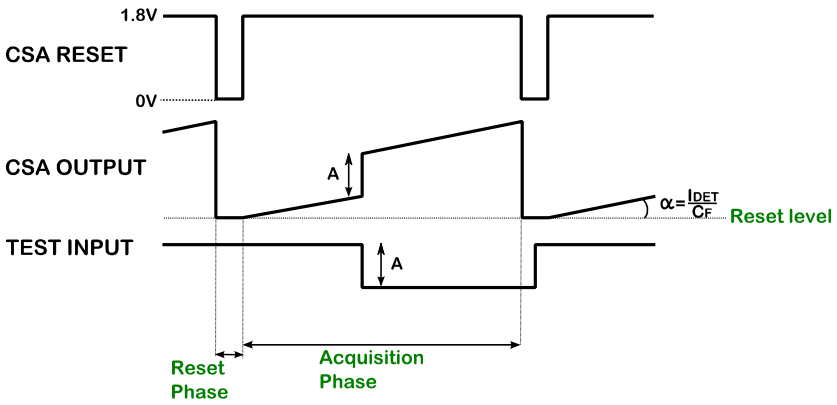


Figure 3.16 Timing diagram of CSA operation with switched reset

To avoid the CSA saturation – the entire reset cycle should be limited in time. Its duration is estimated between one and few hundreds milliseconds, depending on the input dark current from the detector (or from the compensation transistor). Saturation may occur also due to pile-up of several high energy X-ray events. It is prevented by either forcing the reset phase after each event or by further decreasing the reset period with respect to source activity to reduce the pile-up likelihood.

Switched reset noise

During the acquisition phase the reset transistor is switched off and generates no noise. However during the reset-on phase it represents an equivalent resistance of a very low value and thus it becomes source of a high thermal noise current.

Without this additional noise – the CSA output voltage during the reset phase would be equal to the CSA input V_{CSAin}. However the noise current in the reset-on state adds uncertainty to the baseline value, which cannot be eliminated. At the time instant when the reset transistor is being switched off – the voltage across the feedback capacitance is not equal to zero, but it has a random value. Its root mean square value V_{OSkTC} is described by the kT/C noise (detailed in the paragraph 2.2.5). It results from the parallel arrangement of: the feedback equivalent resistance and the feedback capacitance C_F. With the capacitance of $25\ fF$ the baseline offset due to the kT/C noise is $0.4\ mV_{rms}$. By its character – this integrated rms noise is independent of the equivalent feedback resistance of the switch. At the moment when the reset switch passes to the off-state, the baseline value at the CSA output memorized on the feedback capacitance is equal to:

$$V_{CSAout} = V_{CSAin} + V_{OSswitching} + V_{OSkTC} = V_{CSAin} + V_{OSswitching} + \frac{k \cdot T}{C_F} \qquad 3\text{-}28$$

Where $V_{OSswitching}$ is an additional DC offset resulting from the switching action of the feedback switch. The switched reset option of the Caterpylar CSA is used during measurements with the MCDS filter. There the double sampling operation cancels out the offset due to $V_{OSswitching}$ and the kT/C noise.

3.3.4.5 Input current compensation

In case of the CSA feedback PMOS operating as the continuous reset – the proper operating point for the CSA is guaranteed only when some current I_{rst} flows through the feedback transistor, as indicated in Figure 3.17. In the designed CSA dedicated for CdTe readout – this condition is fulfilled once the detector anode is connected to the CSA. The dark current I_{DET} is flowing through the feedback PMOS and there is no issue concerning the CSA operating point. However there are two situations when the functionality of the CSA has to be maintained by other means:

- if there is no detector connected to the ASIC
- if the detector dark current has an inversed polarity

A current compensating circuit has been introduced to polarize the feedback reset in any of these circumstances. It is realized with an isolated NMOS transistor with its bulk connected to the common substrate. The source and the gate terminals can be controlled externally with analog adjustment of the current I_{comp}.

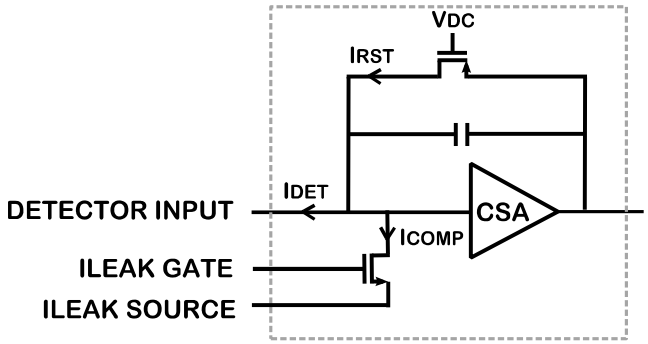


Figure 3.17 Currents related to the CSA input node: detector dark current, reset current and compensation transistor current

The isolated transistor with adjustable source potential has two control terminals:

- NMOS gate, with $V_{ILEAK\ gate}$ voltage
- NMOS source, with $V_{ILEAK\ source}$ voltage

By increasing the gate voltage with respect to source:

$$V_{GS} = V_{ILEAK\ gate} - V_{ILEAK\ source} \qquad 3\text{-}29$$

a current flows out of the input node into the compensation NMOS drain. Meanwhile, a decrease in the drain to source voltage V_{DS} by adjusting $V_{ILEAK\ source}$ reduces the leakage current component independent of the V_{GS} voltage. In order to further minimize the unintended leakage – the compensating transistor has a long channel. When the V_{GS} voltage is set to a negative value and the V_{DS} to $0.3\ V$ - $0.6\ V$ the leakage current is negligible. In consequence the current I_{comp} can be set to any value between $\sim 200\ fA$ and few hundred pA. Concerning the transistor dimensions, despite the long channel, its small width and thus small drain area minimizes the additional capacitance at the sensitive CSA input node.

The current compensating function primarily allows performing tests that verify the purely electrical performance. These measurements are typically realized without the detector connected. Once the

detector is connected to the CSA for the anode readout and the ASIC operates in the continuous reset mode – the current compensation can be set to the minimum. When necessary – the implemented structure also supports the readout of the cathode signals, even though the feedback reset has been primarily designed for the anode readout. When the cathode side is connected to the CSA the input structure can compensate for the detector dark current in the reversed direction ("into the CSA", which according to the current orientations in Figure 3.17 means $I_{DET} < 0$). In this case the absolute current through the compensating transistor has to be increased to value just above the cathode dark current (with the negative sign) to ensure the current flow through the PMOS reset:

$$I_{rst} = I_{comp} + I_{DET} > 0 \qquad 3\text{-}30$$

Compensation transistor noise

The compensation transistor is also a source of noise. Same as the detector shot noise it is represented as the parallel noise source at the CSA input, with the power density is denoted as ${i_{n\,comp}}^2$.

If a DC current flows through the compensation transistor channel, it generates a parallel current noise similar to the detector shot noise [12]. The current is typically in the order of up to a few pA, therefore the transistor operates in a deep subthreshold. Consequently its noise can be modeled similar as the reset transistor in the continuous mode. That is – the noise contribution of the compensating transistor ${i_{n\,comp}}^2$ due to its drain current I_{comp} is predicted by the shot-like noise equation:

$${i_{n\,comp}}^2 = 2 \cdot q \cdot I_{comp} \qquad 3\text{-}31$$

3.3.4.6 CSA buffer

On the output of each CSA there is a buffer, shown in Figure 3.15. It is implemented to drive signals along the metal line to the common output stage. The buffer has an option of two gain selections: $\times 1$ and $\times 20$. With the simple unity gain configuration the CSA dynamic range can be measured. The high gain is aimed for the noise characterization. Once the CSA output signal is amplified with the gain $\times 20$ any noise contributions from the consecutive stages in the measurement chain are surely negligible.

3.3.4.7 Slow Control

The circuit functionality is managed with the digital Slow Control. It provides access to the following adjustments:

- CSA bias current I_{BIAS}
- CSA output stage current I_{OUT}
- In-channel gain: $\times 1$ or $\times 20$
- Activation of test injection for individual channels
- Selection of the channel to be monitored readout
- Choice of the analog output: output buffer or source follower

The Slow Control block is accessed through a parallel interface, which includes the read/write clock and the data stream.

3.3.4.8 Caterpylar testchip summary

After the thorough optimization procedure, I have designed the Caterpylar ASIC (shown in Figure 3.18). Since it is the first ASIC of the group designed in this technology and since the design kit includes no IP except PADs and individual digital cells, I had to design all the analog (buffers, source followers, multiplexors…) and digital stages (Slow Control). This testchip is an integral part of the new hybrid spectro-imager development.

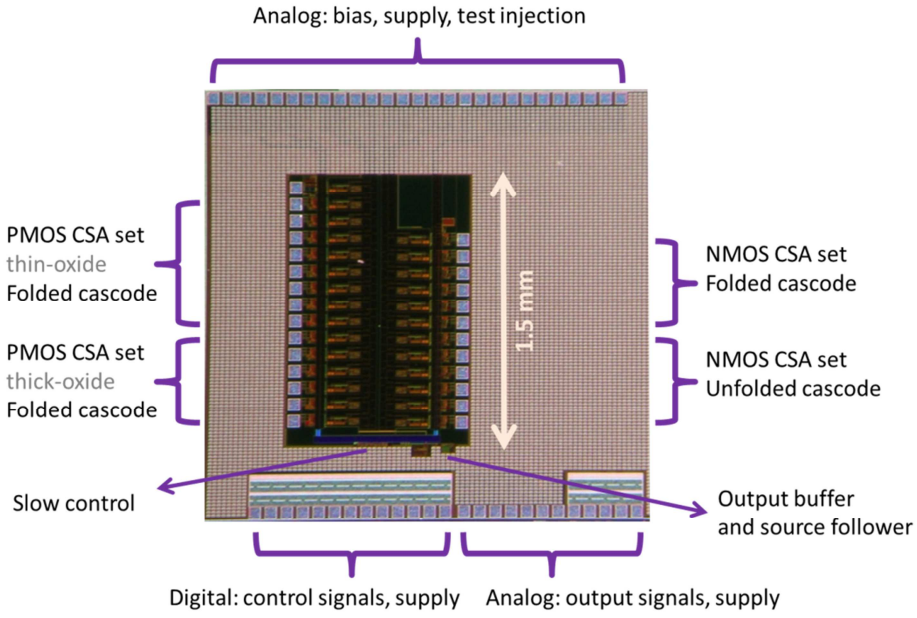


Figure 3.18 IDeF-X Caterpylar ASIC photograph with indication of PMOS CSA – on the left, NMOS CSA – on the right, as well as the digital Slow Control, analog output stage (including the output buffer and the source follower) and IO pads.

The main targets of the Caterpylar circuit are: experimental confirmation of the most suited CSA for pixelated CdTe detector readout, estimation of the achievable energy resolution, verification of the new IC technology and comparison of the two identified filter techniques with real data.

The testchip has been realized with dedicated circuit structures integrated around each of the 26 CSA channels to ensure facility of the measurements. Many parameters can be adjusted with programmable slow control registers. Probably the most important among them are: the CSA main bias current I_{BIAS} and the cascode branch current I_{OUT} as well as the possibility to disable the injection to unused channels. Furthermore several strategic node potentials, like the cascode and the reset transistor gates or the compensation transistor terminals, are adjustable with the analog access. All features when considered together – provide a high flexibility with a wide range of applicable operating conditions. This is essential for the characterization of the integrated CSAs with respect to the target application in a low power and Fano-limited readout system for pixelated CdTe. The experimental outcomes are presented in the next section 3.4.

3.4 Caterpylar: experimental results

In 3.3 I have presented the noise optimization procedure as well as the complete design of the low power readout ASIC: IDeF-X Caterpylar. This section is dedicated to the experimental results obtained with the testchip.

3.4.1 Overview of the measurements

The measurements with Caterpylar ASIC are organized in four parts:

First of all there are those that confirm the desired functionality: in the paragraph 3.4.2 the characteristics related to CSA only are presented, whereas in the paragraph 3.4.3, I describe two methods of external noise shaping, that involve: the 2^{nd} order semi-Gaussian filter and the Multi-Correlated Double Sampling. Both filter setups lead to successful measurement results of very low ENC when no detector is connected.

Secondly I present the complete noise characterization for the set of CSA integrated on the Caterpylar. With the CR-RC^2 the electronic noise of each CSA has been measured as a function of the peaking time and as a function of the external input capacitance. I show how the measurements are used to study the input noise parameters of the integrated CSA circuits. One of the principal objectives of the Caterpylar ASIC is the determination of the optimum CSA for the small pitch pixelated CdTe readout. I will use the extracted series noise parameters to analyze (in the section 3.5) the ASIC performance with different pulse shapers to find out which CSA is recommended for which shaper.

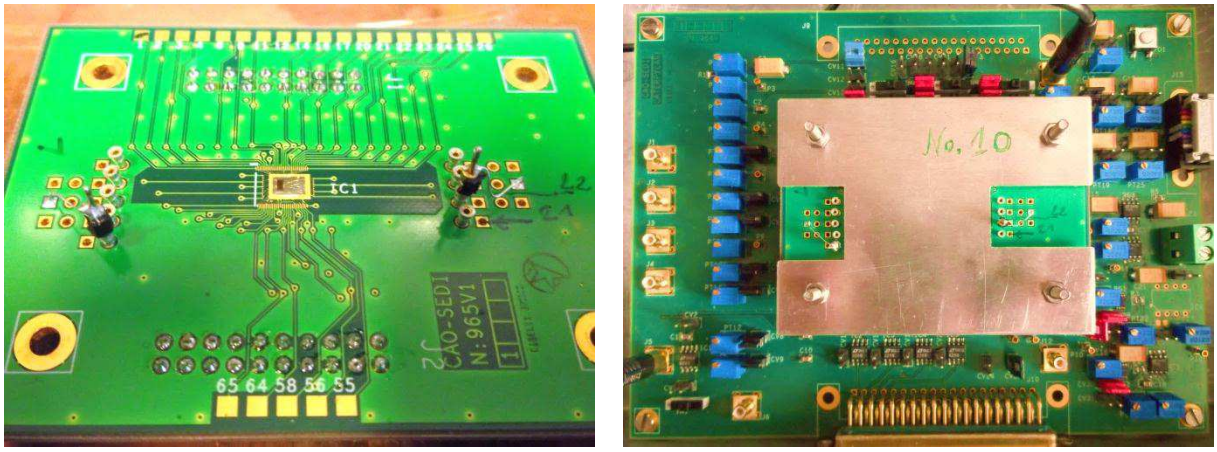
Following the electronic noise characterization – in the paragraph 3.4.5 I demonstrate the ASIC capabilities as a readout circuit in high resolution spectrometry. The measurements performed with one of the CSA connected to a silicon diode are reported and discussed. The results include the spectroscopy measurements with a gamma rays source. Measurements have been done with both of the proposed shaping methods: CR-RC^2 and MCDS. With both methods, FWHM resolutions of $400\ eV$ were obtained at energies of few keV with a CSA power consumption of only $14\ \mu W$.

Finally the experimental results from the irradiation tests are presented in the paragraph 3.4.6. These tests took several months. They constitute the first part of the IC technology qualifications for the space-borne instrument. The functionality and noise performance has been studied for the total dose of $\sim 1.2\ MeV$ gamma-rays up to $1\ Mrad$.

3.4.1.1 Experimental setup

In all measurements the following general setup has been utilized. The bare-die Caterpylar ASIC is bonded on a socket PCB, shown in Figure 3.19 A). Then the socket PCB is mounted on the main board, depicted in Figure 3.19 B), which contains supplies and regulators. The main board includes a PC interface. The link is used to program the ASIC internal registers that control: the CSA bias current

I_{BIAS} and the output current I_{OUT}, the CSA buffer gain as well as the selection of the active CSA readout channels.



A) B)

Figure 3.19 Measurement boards: A) IDeF-X Caterpylar ASIC bare die bonded on socket PCB B) main supply PCB with metal-shielded socket PCB mounted on top.

3.4.2 Functional results

The primary functional results are related to the CSA electrical characteristics. These measurements were performed without any detector connected to the CSA. The input signal charge was provided through the test input structure, described in the paragraph 3.3.4. In these tests it was the CSA output that was directly observed, only passing through the multiplexer and the integrated output buffer.

3.4.2.1 Output pulse

Figure 3.20 shows voltage signal on the CSA output. It is result of an input voltage step V_{INJ} of $-30\ mV$ applied at the test injection capacitance (shown in Figure 3.15 in the paragraph 3.3.4). The records show the output voltage of two CSA: with PMOS and with NMOS as the input transistor. The DC baseline offset is not included to compare the two waveforms in one plot in terms of the dynamic behaviour. The baseline voltage levels vary between $0.6\ V$ with NMOS to $0.9\ V$ with PMOS input transistor. The difference in rise time is mainly due to the input transistors capacitances.

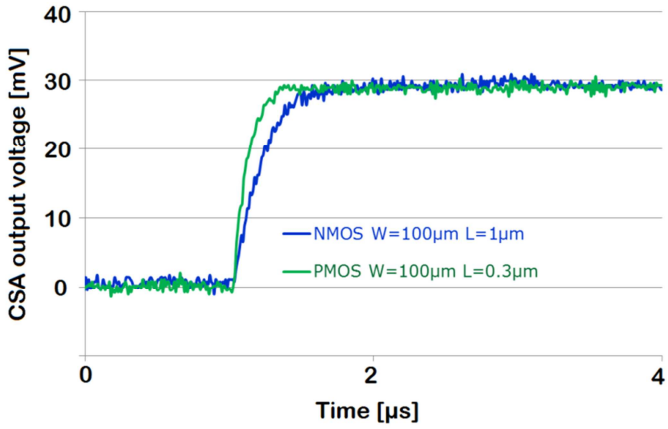


Figure 3.20 The output responses to the input test signal V_{INJ} of: $-30\ mV$ of PMOS- and NMOS based CSA. In both cases the CSA bias currents are set to: $I_{BIAS} = 10\ \mu A$ and $I_{OUT} = 100\ nA$. No detector is present in at CSA inputs.

3.4.2.2 Rise time

Ideally the CSA output voltage would be a step. However with the CSA finite open loop gain and with a limited bandwidth the waveform is smoothed. This is observed in Figure 3.20 with the behaviour similar to a low pass filter effect on a voltage step. For a first order low pass filter with the time constant τ it can be shown that the output signal rise time from 10% to 90% resulting from the input step equals:

$$t_r = 2.2 \cdot \tau \qquad 3\text{-}32$$

Where τ is the time constant of the CSA. The time constant corresponding to the CSA with the bandwidth limited at high frequencies has to be found. The open loop gain of the CSA with the folded cascode architecture is expressed with the equation (derived in the paragraph 3.2.1):

$$A \approx -g_{m0} \cdot r_{o3} \qquad 3\text{-}33$$

In order to analyze the rise time – the open loop gain has to be taken into account in the CSA output voltage equation, derived for CSA with a non-zero input capacitance that was described in the paragraph 2.2.3. By inserting *3-33* in the output voltage expression, one obtains:

$$V_{CSAout} = Q_{IN} \cdot \frac{1}{\left(\frac{C_{IN} + C_{CSA}}{A} + C_F\right)} \cdot \frac{1}{1 + r_{o2} \parallel r_{o3} \cdot (C_F + C_L) \cdot \frac{C_{IN} + C_{CSA}}{A \cdot C_F}\omega} \qquad 3\text{-}34$$

The equation describes the output voltage of a low pass filtered CSA with time constant dependent on the input capacitance $C_{IN} + C_{CSA}$, the feedback capacitance C_F and the load capacitance C_L, as well as on the total CSA transconductance. The term $r_{o2} \parallel r_{o3}$ is the output resistance of the amplifier. In result, by analogy with the low pass filter and the equation *3-32*, the output rise time equals:

$$t_r = 2.2 \cdot \frac{r_{o2}}{r_{o2} + r_{o3}} \cdot (C_F + C_L) \cdot \frac{C_{IN} + C_{CSA}}{g_{m0} \cdot C_F} \qquad 3\text{-}35$$

The rise time is directly proportional to the input capacitance and the output load. It is inversely proportional to the total CSA transconductance and it also depends on the output stage small signal resistance r_{o2} and r_{o3}.

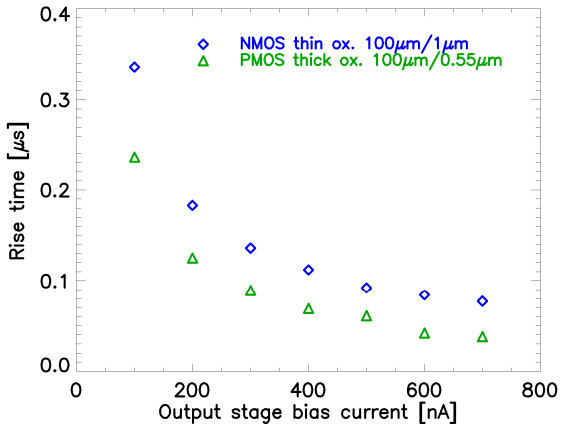


Figure 3.21 Measured CSA output voltage rise time (10%-90%) as a function of the output stage bias current. $I_{BIAS} = 10\ \mu A$, I_{OUT} varied in range 100 to 700 nA. The characteristics are shown for two CSA input types PMOS based folded cascode and NMOS based unfolded cascode. No detector is present in at CSA inputs.

I have examined the CSA output pulse rise time as a function of the output current I_{OUT}. The measurements are demonstrated in Figure 3.21. The current I_{OUT} can be adjusted in the range from 100 to $700\,nA$. It is observed that with the increasing current – the rise time decreases. It is the consequence of the equation *3-35*. The CSA output stage small signal resistances: r_{o2} and r_{o3} strongly depend on the output current I_{OUT}. The difference between measurements of CSA with the NMOS and with the PMOS input transistors comes from the fact of their different dimensions. However both characteristics agree that the best compromise between the output current and the rise time is the I_{OUT} value of $\sim 400\ nA$. For higher currents only little speed improvement is achieved.

From the obtained results and from the definition of the CSA time constant in *3-32*: $\tau = 1/2\pi B_w$ – I can also derive the CSA's bandwidth. It is approximately in the range between $1\ MHz$ and $7\ MHz$ and it increases together with I_{OUT}.

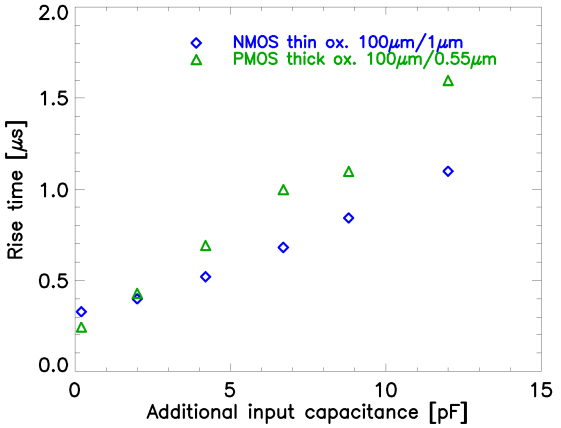


Figure 3.22 Measured CSA output voltage rise time (10%-90%) as a function of additional input capacitance up to $10\ pF$. $I_{BIAS} = 10\ \mu A$, $I_{OUT} = 100\ nA$. The characteristics are shown for two CSA input types: PMOS based folded cascode and NMOS based unfolded cascode. No detector is present at the CSA inputs.

The same two CSAs have been analyzed as a function of the additional input capacitance, with I_{OUT} set to minimum of $100\ nA$. An external capacitance with value between 0 and $10\ pF$ was connected to the CSA input in the consecutive measurements. As predicted with the rise time equation *3-35* –

the CSA output increases linearly with the input capacitance. All of the Caterpylar CSA amplifiers have the same feedback capacitance and output load due to the consecutive buffer stage. Differences in the rise time plots are mainly related to the different dimensions of the input transistors (especially at low value of the additional external input capacitance) and to the different small signal parameters between the PMOS and the NMOS structures.

The understanding of rise time is important later in the noise characterization presented in the paragraph 3.4.4, where the ENC is measured as a function of the input capacitance with an external shaper. In these measurements a special case occurs at the smallest CR-RC^2 filter peaking times t_{peak}: with the increasing external capacitance the CSA rise time approaches the value of t_{peak}. This must be taken into account in the noise parameters' analysis to minimize any calculation errors.

3.4.2.3 Dynamic range

The dynamic range has been experimentally verified for the three CSA architecture types integrated on the Caterpylar testchip: the PMOS folded cascode, the NMOS folded cascode and the NMOS unfolded cascode. The measurement results are demonstrated in Figure 3.23. A voltage step that reaches nearly $600\ mV$ can be obtained at the CSA output in all three cases. This corresponds to maximum input charge of $15\ fC$ and consequently meets the dynamic range expectations given in Table 3.1 in the paragraph 3.1.3.

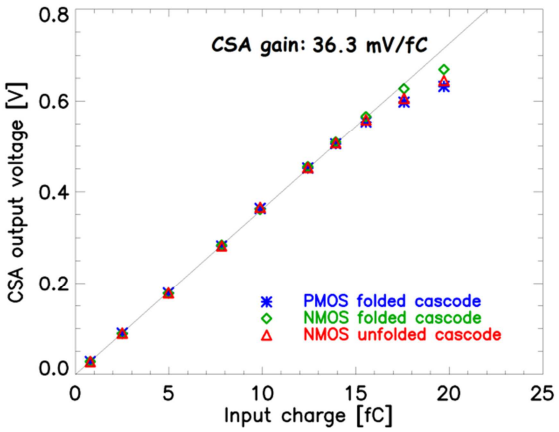


Figure 3.23 Dynamic range: CSA output voltage as a function of the input charge. $I_{BIAS} = 10\ \mu A$, $I_{OUT} = 100\ nA$. The characteristics are shown for three CSA architectures: the PMOS-based folded cascode and NMOS-based folded cascode and the NMOS-based unfolded cascode. No detector is present in at CSA inputs. The CSA gain is found to be $36.3\ mV/fC$. The resulting Integral Nonlinearity (INL) is below one % within the dynamic range up to $15\ fC$.

With each CSA, a similar gain of $36.3\ mV/fC$ has been found in electrical measurements. Although with the feedback capacitance of $25\ fF$ it is expected to be $40\ mV/fC$, however, the reset transistor in the feedback network, identical for all channels, adds an additional parasitic feedback capacitance. This results in the systematic gain offset, which must be taken into account in the ENC characterization. Later, a calibration with a known radioactive source (setup described in 3.4.5) indicated that the gain is slightly lower: $35.7\ mV/fC$. This value excludes mismatch between the test injection capacitance C_{INJ} and the feedback capacitance C_F.

3.4.3 ENC measurement

The Caterpylar testchip contains 26 parallel channels, each containing a different CSA. With the intention to characterize each of them in a complete detection chain in terms of ENC – I have prepared two measurement setups. They correspond to two filtering methods: the 2^{nd} order semi-Gaussian and the MCDS shapers. I introduce both approaches and compare results obtained in both cases, at the identical operating conditions: the filter peaking time, the CSA type and the CSA bias.

3.4.3.1 ENC measurements with CR-RC²

The first setup, illustrated in Figure 3.24, was built for ENC measurements with the analog semi-Gaussian filter. This external shaper is a CR-RC^2 from Ortec and constitutes measurement equipment especially for use in the radiation detection chains. Its peaking time is adjustable in range between $1\ \mu s$ and $11\ \mu s$. The filter has an internal pole-zero cancellation, which can be adjusted to match the CSA. This feature was important in this setup, since in this case, all CSA were configured to operate in the continuous reset mode. The equipment was connected to the output of the Caterpylar ASIC. The reset transistor gate potentials: one common to all PMOS channels and one for NMOS channels, were set to the appropriate DC values.

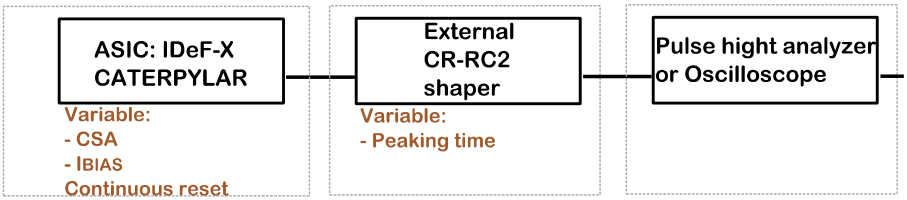


Figure 3.24 Diagram of the Caterpylar measurement setup with the CR-RC^2 processing.

In most measurements there was no detector connected to the CSA and thus the input signal was provided through the test injection input (described in the paragraph 3.3.4 with Figure 3.15). The CSA output was typically monitored with a level triggered oscilloscope. The oscilloscope was used as an event discriminator as well as to measure the output signal value. However when the detector was connected for studies of the energy spectrum – a 13-bit Wilkinson ADC with integrated variable threshold event discriminator and a pulse height analyzer (from Canberra), was connected to the CR-RC^2 shaper output instead. The ADC output data were then analyzed with dedicated software in a real time.

Figure 3.25 shows two sets of ENC measurements characterized with the external CR-RC^2 as a function of its peaking time, obtained for two CSA. Both CSA are based on a thick oxide PMOS input device, however with different geometries: one optimized for $0.3\ pF$ and the other for $1\ pF$. The results were acquired without any input capacitance, the CSA bias current was set to 10 µA and the leakage current compensation tuned to the minimum of approximately $0.2\ pA$. The lowest achieved ENC values are $12\ el\ rms$ and $30\ el\ rms$, measured respectively with the CSA $T9$ and $T12$ optimized for C_{IN} (due to detector and stray capacitances) in a range between $0.3\ pF$ and $1\ pF$. Because of the negligible parallel noise contribution in each case the best measurement corresponds to $11\ \mu s$ peaking time, which is the maximum reachable with the particular shaping equipment.

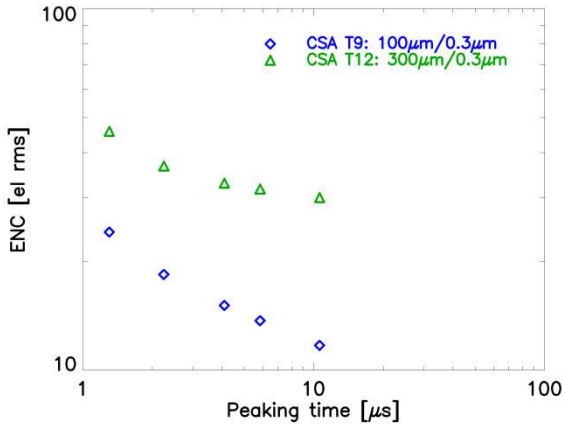


Figure 3.25 The floor ENC of CSA T9 and T12 measured with the 2^{nd} order semi-Gaussian shaper. Conditions: $I_{BIAS} = 10\ \mu A$, $I_{OUT} = 100\ nA$, there is no detector, no additional input capacitance and no input compensation current.

Of all other CSAs measured at the same conditions, those optimized for $0.3\ pF$ showed the lowest floor ENC. It is in the order of 10 - 12 electrons rms with both thin and thick oxide PMOS input. The value obtained with the NMOS-based CSA, also optimized for $0.3\ pF$ input capacitance is higher: 20 electrons rms.

3.4.3.2 ENC measurement with MCDS

The second measurement setup is shown in Figure 3.26. It was realized with a fast 14-bit external ADC that digitized directly the CSA output with sampling data rate of $250\ Msps$. For each event the voltage was memorized in a data frame of length between 16 and $260\ \mu s$. The ADC memory has been tuned in such a way that approximately a half of the data frame width contains information before the event: that is the CSA baseline, while the second part of the frame contains the baseline plus the signal information.

In the described setup the CSA reset was operated in a pulsed mode. The reset pulse of few micro seconds duration was programmed to a fixed rate chosen individually in each measurement within the range of $1\ ms$ to $100\ ms$.

The noise filtering was realized with a discrete post-processing, once a large number of data were acquired. The calculations have been done off-line mainly due to the fact that the time it takes to memorize a single frame with the ADC is much longer than the frame duration itself.

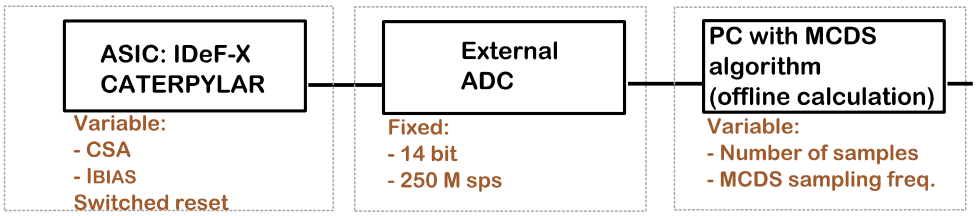
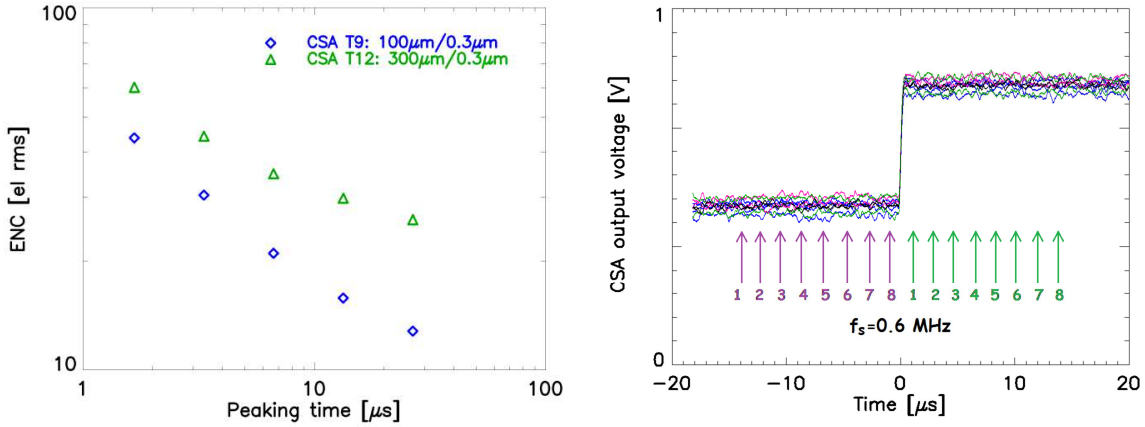


Figure 3.26 Diagram of the Caterpylar measurement setup with the MCDS processing.

The discrete filtering was performed by applying the MCDS algorithm to the output data. From a single data frame only the relevant samples would be chosen, i.e. for an 8-fold MCDS the total of 16

data points where chosen with spacing of approximately $2.5\ \mu s$. The process could be considered inefficient comparing to the analog setup from Figure 3.24, because of much longer acquisition time. However once data is stored with the high output oversampling rate of $250\ MHz$ – then a characterization of ENC at different number of samples and different frequencies is possible with a single data set.



A) B)

Figure 3.27 A) The floor ENC of CSA T9 and T12 measured with the MCDS shaper. Conditions: $I_{BIAS} = 10\ \mu A$, $I_{OUT} = 100\ nA$, MCDS sampling frequency $f_s = 0.6\ MHz$, variable number of MCDS samples k from 1 to 16, there is no detector, no additional input capacitance and no input compensation current. The peaking time is defined as $t_{peak} = k/f_s$. B) CSA output data from multiple acquisitions, which after sampling is processed numerically to perform the MCDS filtering – example with 8-folded MCDS ($k = 8$).

The floor ENC measurement example is presented in Figure 3.27. In the example two PMOS-based CSAs are chosen: one optimized for $0.3\ pF$ of the input capacitance and one for $1\ pF$, the same as in the previous example with the analog shaper in Figure 3.25. Therefore the two characteristics can be directly compared. The minimum ENC of 12 electrons rms has been measured with the 16-fold MCDS in case of the CSA optimized for $0.3\ pF$ and 26 electrons rms for the CSA optimized for $1\ pF$. Because of the negligible parallel noise contribution – further increase in the number of samples would further decrease the ENC.

With each of the described Caterpylar measurement setups a characterization of the CSA electronic noise can be done as a function of the detection chain parameters: the CSA bias current, the external input capacitance imitating the detector capacitance C_{IN} and the shaper parameters to adjust the peaking time. In case of the semi-Gaussian shaper – there is the complete set of analytical ENC expressions described in the paragraph 2.3.4 that facilitate the noise analysis. It is mainly for this reason that I have used the first, analog setup, to perform a complete measurement characterization of the ASIC to then extract the noise parameters of each CSA. The paragraph 3.4.4 is dedicated to description of this work.

3.4.4 Measurements and extraction of CSA noise parameters with CR-RC²

The equivalent noise charge (ENC) measured in a detection chain with a specific CSA depends on the filter type. Knowing the filter parameters and understanding the noise sources of the CSA – the input

noise parameters can be extracted from a series of ENC measurements. I have discussed these aspects in Chapter II. From the comparison of the two measurement methods available with the Caterpylar – it is the analog shaper that provides a faster acquisition time. In a large series of measurements it has an advantage of direct monitoring whether the noise read-outs are correct. Any eventual errors can be rapidly detected and eliminated. More important, however, is the fact that the semi-Gaussian shapers have very simple mathematical description when compared to MCDS. This feature makes the CR-RC^2 shaper the main tool of the Caterpylar noise analysis.

3.4.4.1 Extraction strategy

I have studied the intrinsic ENC of the Caterpylar CSA circuits with the CR-RC^2 shaper. This complete characterization was done: as a function of peaking time and additional input capacitance. All these measurements, however, were performed with no detector connected to the electronic circuit.

Having obtained the measurements and knowing the mathematical description of ENC for the detection chain with CR-RC^2 shaper – I could extract the CSA input-referred series noise sources and its intrinsic CSA input capacitance. The purpose of this operation is explained by reminding the general ENC equations derived in the paragraph 2.3.4:

$$ENC_p{}^2 = \frac{1}{q^2} \cdot t_{peak} \cdot i_{n\,p}^2 \cdot A_p \qquad 3\text{-}36$$

$$ENC_{th}{}^2 = \frac{1}{q^2} \cdot \frac{1}{t_{peak}} \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_{th} \qquad 3\text{-}37$$

$$ENC_f{}^2 = \frac{1}{q^2} \cdot v_{n\,f}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_f \qquad 3\text{-}38$$

Where $i_{n\,p}^2$, $v_{n\,th}^2$ and $v_{n\,f}^2$ are the input referred noise sources, C_{IN} is the total input capacitance, C_{CSA} is the internal capacitance of the CSA (including the pad) mainly related to the gate oxide of the input transistor, C_F is the CSA feedback capacitance. Finally the parameters A_p, A_{th} and A_f denote here the noise parameters of the 2^{nd} order semi-Gaussian shaper and are equal to: 0.64, 0.85 and 3.41 respectively.

There are three types of parameters describing the ENC in the equations *3-36*–*3-38* :

- Detector-dependent: C_{IN} and $i_{n\,p}{}^2$ (due to detector dark current)
- CSA-dependent: C_{CSA}, C_F, $v_{n\,th}{}^2$ and $v_{n\,f}{}^2$
- Shaper-dependent: A_p, A_{th} and A_f

The detector-related parameters as well as the shaper parameters have been evaluated in the Chapter II. Additional knowledge of the CSA-related parameters would open the way to calculate ENC for any given shaper, any detector capacitance and any detector dark current. Unfortunately not all of these CSA parameters are known. If, on the other hand, the ENC value was known with fixed detector parameters – then the CSA parameters could be calculated. I will use this reversed approach to obtain the parameters: C_{CSA}, $v_{n\,th}{}^2$ and $v_{n\,f}{}^2$. The capacitance C_F is known from the design.

3.4.4.2 Parallel noise extraction

The ENC measurements dedicated to the noise parameters extraction have been performed without a detector and with no external capacitance connected to the CSA input. This of course eliminates the detector shot current noise from the detection chain. However there are two other noise sources contributing to the input referred current source ${i_{n\,p}}^2$ from the ENC equation *3-36*. They are related to the CSA structure:

- ${i_{n\,rst}}^2$ due to reset transistor noise operating in the continuous mode
- ${i_{n\,comp}}^2$ due to current compensation transistor noise

In the measurements with the CR-RC^2 shaper the reset transistor is configured to continuous mode operation and it constitutes path for the input current coming from the compensation transistor. Although it is intended that this current I_{comp} is close to zero, its minimum value is estimated to $200\ fA$ and is related to uncontrolled leakage current. In our measurement setup I_{rst} is equal to I_{comp} (Figure 3.15 in the paragraph 3.3.4).

Shot noise theory in MOS transistor in weak inversion

With the drain currents in the pA range both transistors: the reset PMOS and the compensation NMOS, are expected to operate in the deep subthreshold region. I have previously mentioned (in the paragraph 3.3.4) that the drain current noise in this case is expected to have the shot-like behaviour [12]. I have decided to verify this theory, since with shot noise PSD – the compensation transistor at the CSA input could replace the effect of the detector dark current I_{DET} with shot noise PSD described as $2 \cdot q \cdot I_{DET}$. If the shot-noise theory is right the two parallel noise sources due to reset and due to compensation transistors would have PSD defined as:

$$ {i_{n\,rst}}^2 = 2 \cdot q \cdot I_{rst} \qquad 3\text{-}39 $$

$$ {i_{n\,comp}}^2 = 2 \cdot q \cdot I_{comp} \qquad 3\text{-}40 $$

Confirmation of this noise model would be very helpful in the channel noise characterization and in estimation of performance expected with the CdTe detector, before even connecting the detector.

The theoretical contribution of the parallel noise ${i_{n\,p}}^2$ to the total ENC is obtained by inserting the expressions *3-39* and *3-40* into the ENC equation *3-36*:

$$ {ENC_p}^2 = {ENC_{rst}}^2 + {ENC_{comp}}^2 = \frac{1}{q^2} \cdot t_{peak} \cdot 2 \cdot q \cdot \left(2 \cdot I_{comp}\right) \cdot A_p \qquad 3\text{-}41 $$

Where A_p is the shaper parallel noise parameter and in case of CR-RC^2 is equal to 0.64.

Experimental verification of parallel noise and comparison with theory

In parallel I have obtained experimental results of parallel noise related to the reset and the compensation transistors (Figure 3.15 in the paragraph 3.3.4). In Figure 3.28 few sets of ENC measured as a function of peaking time are shown, they have been obtained with the CR-RC^2 shaper. Each set corresponds to a different value of the input compensation current ranging from 0.4 to $20.8\ pA$.

3.4. Caterpylar: experimental results

The ENC characteristics from Figure 3.28 confirm the influence of the parallel noise with increasing I_{comp}, which is especially strong at the highest peaking times. Consequently, in the parallel noise analysis I have focused on the maximum peaking time. Figure 3.29 shows the same ENC measurements but now as a function of the input compensation current at the highest peaking time of $11\ \mu s$.

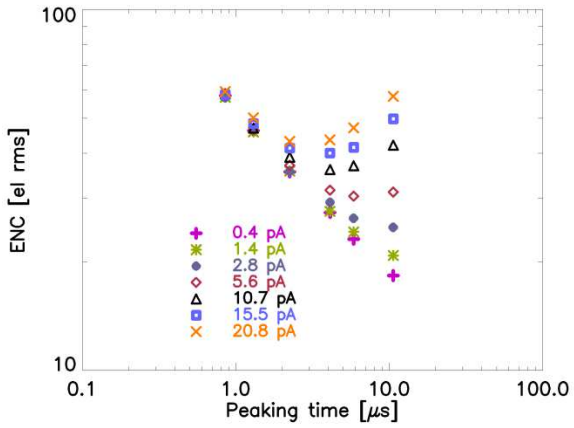


Figure 3.28 Illustration of the parallel noise effect, due to the reset transistor ${i_{n\,rst}}^2$ and the compensation transistor ${i_{n\,comp}}^2$. ENC as a function of the peaking time measured at different values of the input compensation current, CSA used in measurements: T5 $300\ \mu m/0.18\ \mu m$ with bias current of $10\ \mu A$. The compensation current was calculated by monitoring the discharge rate of the feedback capacitance with reverse biased reset transistor.

The results are compared with theoretical values of ENC_p at the corresponding drain current obtained with the equation:

$$ENC_p = \sqrt{{ENC_{rst}}^2 + {ENC_{comp}}^2} \qquad 3\text{-}42$$

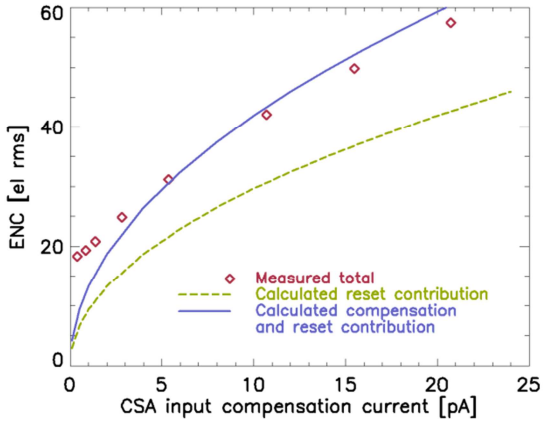


Figure 3.29 Illustration of the parallel noise effect, due to the reset transistor ${i_{n\,rst}}^2$ and the compensation transistor ${i_{n\,comp}}^2$. ENC_p as a function of the CSA input compensation current at the highest peaking time of $11\ \mu s$: comparison of measurements from Figure 3.28 with theoretical calculations of ENC due to reset and compensation noise. In addition a theoretical plot of ENC due to single contributor $ENC_{rst} = ENC_{comp}$ is shown for reference. Calculations of reset and compensation transistors noise (operating in deep inversion), were done with the shot-like model described in the paragraph 3.3.4.

Following the discussion on the Caterpylar parallel noise in the paragraph 3.3.4 – according to the shot-like noise model of a MOS transistor operating in deep subthreshold, theoretical values of

ENC_{comp} and ENC_{rst} should be identical. A single MOS contribution to ENC is equal to $2Iq$. The theoretical noise contribution of both transistors (reset and compensation) is indicated in Figure 3.29 with the continuous line.

Measurement of the compensation transistor current

The value of current through the compensation transistor I_{comp} has been adjusted through the external analog control of the $V_{ILEAK\ gate}$ and $V_{ILEAK\ source}$ Caterpylar IO terminals. By applying a large voltage step at the test input causes an equal negative step at the CSA output, resulting in reverse bias of the reset transistor (Figure 3.30). Consequently the discharge rate of the CSA feedback capacitor depends only on the current I_{comp} and the value of the feedback capacitance C_F. The compensation current was obtained by monitoring the CSA output and was calculated from the relationship:

$$I_{comp} = C_F \cdot \frac{\Delta V_{CSA}}{\Delta t} \qquad 3\text{-}43$$

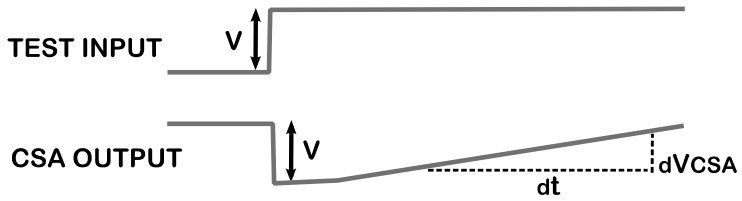


Figure 3.30 Illustration of the compensation current I_{comp} measurement method. The corresponding schematic is shown in Figure 3.15. The CSA output was monitored with an oscilloscope.

Conclusions regarding parallel noise in the detection chain

What has been demonstrated in Figure 3.29 – at low values of the compensation current of 1-2 pA the theoretical curve of ENC due to parallel noise is much below the measured total ENC. With increasing current however – the two characteristics converge. This is simply because of the fact that the series noise contribution does not change and the parallel becomes dominating. Once the series noise contribution becomes negligible – the measurements are in agreement with the shot-like noise model in MOS transistor in deep subthreshold.

Consequently in all ENC calculations presented later in the text, where the parallel noise may be significant, I utilize the $2Iq$ model to include the parallel noise contribution. The results obtained with the CR-RC^2 shaper show that the compensation transistor can be used to mimic the effect of the CdTe detector in the electrical characterization of an ASIC with an integrated shaper of any kind [14].

3.4.4.3 Series noise extraction

The CSA parameters were extracted from a set of measurements with the CR-RC^2 shaper. For each CSA a set of measurements has been performed – to characterize the ENC as a function of the peaking time and of the input capacitance: $ENC(t_{peak}, C_{IN} + C_{CSA})$. The shaper peaking time is adjustable with six steps ranging from 1 to 11 μs. Measurements were realized without detector and using the injection test input as a source of the input signal. Characterization has been performed in three arrangements related to the input capacitance:

- Without bonding, the input capacitance was simply:

$$C_{IN} = 0 \qquad 3\text{-}44$$

This configuration was used to measure ENC as a function of the peaking time with no additional input capacitance $ENC(t_{peak}, C_{CSA})$.

- In the second arrangement an additional wire bonding was realized between the Caterpylar ASIC and PCB. It connects the CSA input pads on the ASIC to one of the dedicated on-board metal paths. The other end of the PCB metallization is organized in a way that external capacitance C_{add} can be mounted. However in the discussed measurement set, no additional capacitance is present. Thus the total input capacitance equals:

$$C_{IN} = C_x \qquad 3\text{-}45$$

Where C_x is the capacitance of the dedicated PCB metal path. This configuration was used to measure ENC as a function of the peaking time: $ENC(t_{peak}, C_{CSA} + C_x)$.

- Finally a series of ENC measurements with additional external capacitance C_{add} was performed. The total input capacitance in this case is:

$$C_{IN} = C_x + C_{add} \qquad 3\text{-}46$$

The values of the additional capacitance are ranging from $2.2\ pF$ to $10\ pF$. For each of four different C_{add} values the characterization of ENC against peaking time was performed: $ENC(t_{peak}, C_{CSA} + C_x + C_{add})$.

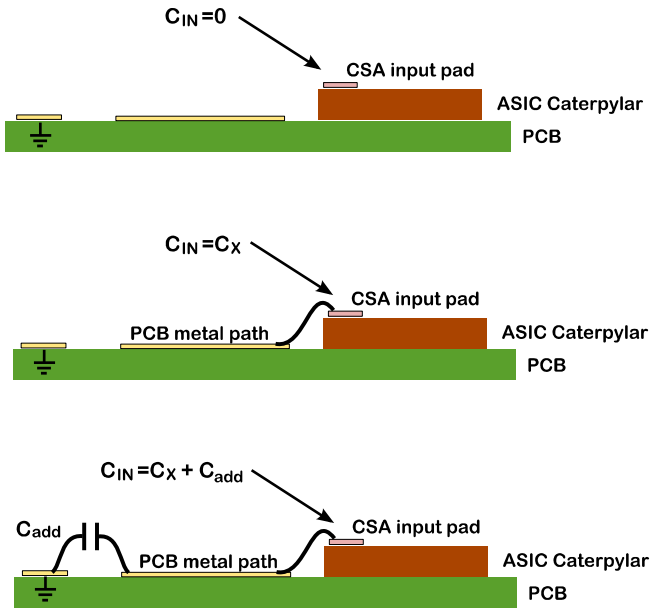


Figure 3.31 Illustration of three different arrangements of the CSA input pad connection: with $C_{IN} = 0$, $C_{IN} = C_x$ and $C_{IN} = C_x + C_{add}$.

Normally in a complete detection chain with the detector, the capacitance C_{IN} would comprise the detector and stray capacitances. However in the noise characterization described here – it is instead a sum of the additional external capacitance C_{add} and the stray capacitance C_x:

$$C_{IN} = C_{add} + C_x \qquad 3\text{-}47$$

The measurement setup is organized in such a way that C_{add} can be set to any value with a hybrid passive component, however in the absence of C_{add} – the capacitanceC_{IN} is non-zero and equal to C_x. The capacitance C_x is parasitic and therefore it is difficult to assess. However it is possible to estimate it by comparing measurements of two ASICs: one with bonding to the socket PCB containing the C_{add} insertion structure and with one, where no bonding is realized and thus C_{IN} is equal to zero.

The Caterpylar ASIC includes 26 CSA. Most of them were characterized with the described set of measurements. Because of the size limitation the socket PCB has been designed with only 9 dedicated metal paths for external capacitance connection. Therefore only 9 CSA could be characterized with a single PCB. Consequently several socket PCBs were realized with three different bonding diagrams. Each arrangement was dedicated for characterization of another CSA group. These metal paths can be seen on the image in Figure 3.19 A) in the paragraph 3.4.1 – they are located on the right and on the left side of the ASIC, on the socket PCB.

Measurements: ENC as a function of the peaking time

The discussion on the ENC measurement continues, because of the interest in the remaining variables present in the ENC equations *3-37* and *3-38*, namely: ${v_n}_{th}^2$, ${v_n}_f^2$, C_{CSA} as well as C_x. A set of ENC measurements as a function of the peaking time is shown in Figure 3.32, this time with the parallel noise set to a negligible level (with the minimum I_{comp} of $0.2\ pA$). Instead, the total input capacitance $C_{IN} = C_x + C_{add}$ is different in each measurements set, what is achieved by changing the additional external capacitance C_{add}.

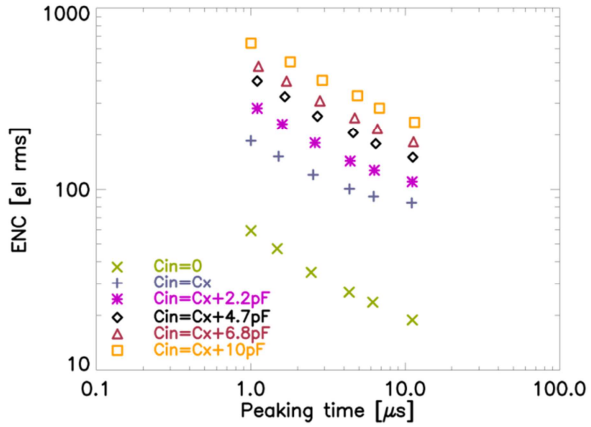


Figure 3.32 Example of the CSA $ENC(t_{peak}, C_{add})$ characterization for the extraction parameters of the series noise: the ENC with CR-RC² shaper as a function of the measured peaking time for input capacitance C_{IN} ranging from $0\ pF$ to $C_x + 10\ pF$. CSA T6 with thin oxide PMOS $300\mu m/0.25\mu m$ input transistor, the bias current set to $10\ \mu A$. The value of $C_x = 2.7\ pF$ is found in the parameter extractions described later in this chapter.

The example in Figure 3.32 shows characterization from Caterpylar testchip of only one CSA: T6 with thin oxide PMOS $300\ \mu m/0.25\ \mu m$ as the input transistor at fixed bias current of $10\ \mu A$. As expected – the strong influence of the input capacitance is observed in the ENC characteristics. Primarily the CSA thermal and flicker noise multiplied by the total input capacitance $(C_{IN} + C_F + C_{CSA})$ cause an increase of the ENC. Furthermore, because of the input capacitance effect on the CSA output rise time (highlighted in the equation *3-35*), the peaking time measured at the shaper output individually for each measurement point – deviates from the nominal value set by the external shaper CR-RC^2. Regardless of the capacitance value, the ENC characteristics follow the behaviour predicted

previously (with the equation *3-37* and with the illustration in Figure 3.10): the ENC decreases with the increasing peaking time. This behaviour is characteristic to the thermal noise (at negligible parallel noise power). The presence of flicker noise, constant with peaking time (described with the equation *3-38*), is not so obviously present at the first glance, however, a deeper analysis described below permit its estimation.

In the Annex III – I have described the full-fit model used for extraction of the CSA noise parameters. The outcome of the model for a single CSA is the set of parameters:. $v_{n\,th}^2$, $v_{n\,f}^2$, C_{CSA} and C_x. I use this model as a tool to analyze the obtained ENC measurements. It has been applied to all of the characterized CSAs from the Caterpylar ASIC. The analysis has the following purpose:

- Calculate the optimum ENC for the proposed small-pixel CdTe readout system with the input capacitance (comprising the detector and the stray capacitances) of $0.3\,pF$ - $1pF$ and for a given detector dark current with $I_{DET} < 5\,pA$. Consequently the best CSA can be identified for the specified system.
- Link the measurements with the simulation results. There are two noise models available in the moderate inversion MOS, each showing different ENC results (Table 3.6 in the paragraph 3.3.3). It is uncertain how precise the simulation models are and which one is the more accurate. The experimental ENC characterization should provide more information in this subject.

In this profound analysis – the noise parameters are extracted from the full set of measurements $ENC(t_{peak}, C_{add})$. This rather complex analysis provides results for more general use: the extracted CSA parameters apply to calculations with any other shaper.

The best ENC with Caterpylar and the CR-RC^2 shaper

Using the full-fit model detailed in Annex III, which uses the ENC model described with the equations *3-36* - *3-38* – I have obtained the parameters: $v_{n\,th}^2$, $v_{n\,f}^2$, C_{CSA} and C_x, for most of the CSA from the Caterpylar ASIC. I have determined the CSA that is the most suitable in the application of interest with this new analysis method. The pixelated CdTe detector is expected to contribute to an input capacitance C_{IN} between $0.3\,pF$ and $1\,pF$ with a maximum dark current of $5\,pA$. In the given range of the expected detector input conditions, CSA T10 and T11 appear to be the best candidates. They are both PMOS based CSA, where the input transistor has thick oxide and gate dimensions of $100\,\mu m/0.45\,\mu m$ and $100\,\mu m/0.55\,\mu m$ respectively [17]. The expected minimum ENC and corresponding optimal peaking times are almost identical for both transistors and equal to:

- $28\,el\,rms$ at 4 μs peaking time with $C_{IN} = 0.3\,pF$
- $40\,el\,rms$ at $8\,\mu s$ peaking time with $C_{IN} = 1\,pF$

In the calculations, in addition to the detector shot noise, I have included also the reset contribution to the parallel noise with the reset drain current of $5\,pA$. I believe that the presented noise extraction method is as precise as possible, since nearly all of the measurement points are employed in the full-fit model. The important point to note is the actual CSA indicated as the most suitable for the final application with the extraction procedure. It is the CSA with thick oxide PMOS as the input transistor, with a width of $100\,\mu m$ and a length of 0.45-$0.55\,\mu m$.

For me, the most important outcome of this model is the fact that it can be used to calculate ENC with any shaper described by the noise parameters A_p, A_{th} and A_f. This includes all those described in the Chapter II, with the parameters' values summarized in the paragraph 2.3.6. This conclusion is a result of the general description of this model with the equations *3-36 - 3-38*. The known noise parameters A_p, A_{th} and A_f of the CR-RC^2 shaper participating in the measurements have been used to extract the remaining unknown parameters. Once the parameters are known – ENC can be predicted for any other shaper. Consequently this model plays an important role in the further development of the readout ASIC for the dedicated pixelated CdTe.

3.4.4.4 The approach to compare ENC measurements with simulations

Finally, I have compared the measurements with the simulation results. This was done indirectly: by means of the ENC full-fit model parameters. A set of simulations was performed for each of the Caterpylar CSAs (the same as measured). The ENC values were obtained at various peaking times t_{peak} and input capacitance values C_{IN}. The capacitance C_{CSA} included also the capacitance of the bond pad which had to be extracted from the layout (in the measurements this capacitance was also a part of C_{CSA}). Using the simulation data set $ENC(t_{peak}, C_{IN})$ an identical procedure for the full-fit model parameter extraction was performed. The output parameters $v_{n\,th}^2$, $v_{n\,f}^2$ and C_{CSA} (in simulations the parameter C_x is equal to zero) resulting from the calculations could be directly compared with the corresponding parameters extracted from the measurements for the same CSA.

The simulation data should have no faulty data related to measurements. Nevertheless the percentage error obtained with the SPICE2 noise model was up to 0.15%. The resulting extraction errors for all CSAs are shown in Figure 3.33.

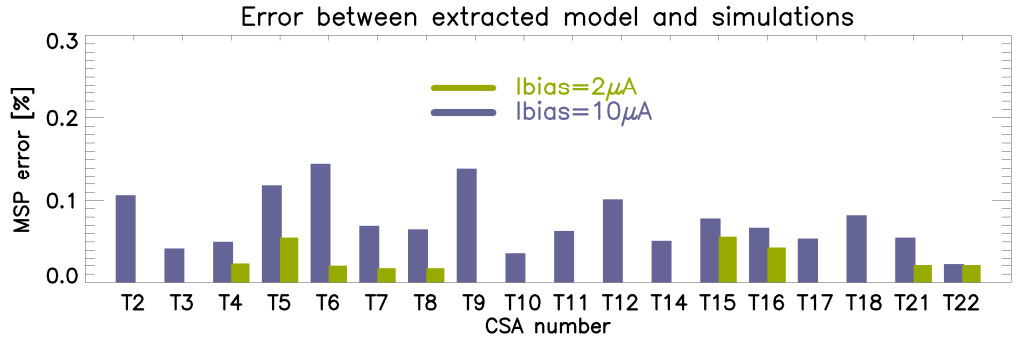


Figure 3.33 Mean square percentage error of model with extracted parameters compared to simulations with SPICE2 noise model. Values are shown with $I_{BIAS} = 10\ \mu A$ and for chosen CSA also with $2\ \mu A$.

3.4.4.5 Studies of the extracted noise parameters

The large number of different characterized CSA allows analysis of noise parameters: C_{CSA}, $v_{n\,th}^2$, $v_{n\,f}^2$ and C_x as a function of the CSA input transistor gate dimensions. It is especially interesting in case of the extracted noise: in theory described with several mathematical models. It is not obvious which one fits the most the given application. More significantly, what was interesting for me in this exercise, is the confirmation – which of the simulation models corresponds better with the obtained measurements: BSIM3v3 or SPICE2. Both noise models are available in the simulation kit of the chosen technology XFAB $0.18\,\mu m$ and in the simulations they have demonstrated ENC values

considerably far apart (paragraph 3.3.3). The importance of the noise characterization is empowered by the fact that the MOS operates between the moderate and the weak inversion. This transition region with low drain current densities is rather difficult to model.

Among the obtained results on the top of the variety of physical dimensions, there are also measurements of CSA at two different values of the input transistor bias current. These bring additional conclusions. Table 3.8 provides list of parameters that I took into account in the results analysis with indication: which design variables are relevant.

Parameter	I_{BIAS}	W	L	W/L	$W \cdot L$	$W \cdot L^2$
C_{CSA}					✓	
$v_{n\,th}^2$	✓	✓		✓		
$v_{n\,f}^2$	✓		✓		✓	✓

Table 3.8 Extracted CSA noise parameters: analysis of CSA design parameters with respect to mathematical models.

The complete analysis of the results is described in Annex IV. Below I only summarize the most important results which indicate how the simulation noise models correspond with the measurement results.

Thermal noise

The input series thermal noise is the second of the three parameters extracted for the CSA from the IDeF-X Caterpylar. Typically, models of the transistor thermal noise state that the voltage noise depends inversely proportionally on the transconductance [11][19][55]: $v_{n\,th}{}^2 \sim 1/g_m$. The transconductance has a known dependency on the bias current and transistor dimensions. In the strong inversion the transconductance fulfills the relation *3-48* whereas in the subthreshold it depends only on the bias current according to *3-49* [19]:

$$g_m \sim \sqrt{I_{BIAS} \cdot W/L} \qquad 3\text{-}48$$

$$g_m \sim I_{BIAS} \qquad 3\text{-}49$$

My target was to find out which of the expressions *3-48* or *3-49* better describe the operating region and which of the thermal noise models: SPICE2 or BSIM3v3 reflect the measurements more accurately.

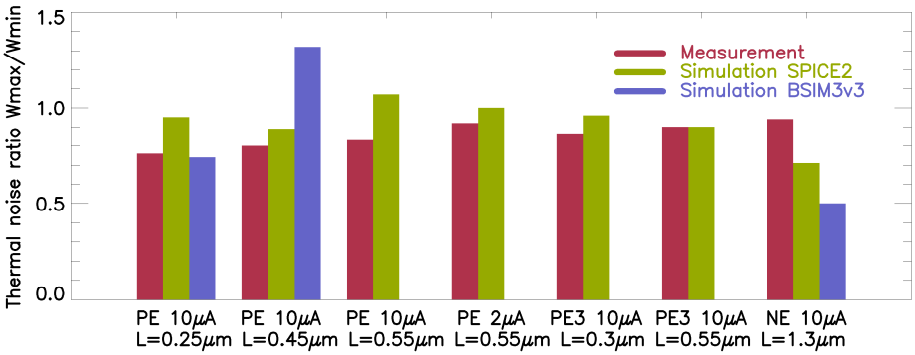


Figure 3.34 Ratio of thermal noise at 300 µm and 100 µm width (200 µm and 100 µm for NMOS). Each ratio is calculated for two CSA of identical input transistor type and length, with a fixed bias current.

3.4. Caterpylar: experimental results

Figure 3.34 shows the thermal noise ratios of two CSA with the same length and different widths. The measurement-based values are nearly constant for all input transistor types. Simulations results show similar effect only when the SPICE2 model is used. Meanwhile the theoretical ratio ${v_{n\,th\,300\mu m}}^2/{v_{n\,th\,100\mu m}}^2$ calculated for the saturation g_m model is:

- for PMOS CSA $\frac{{v_{n\,th1}}^2}{{v_{n\,th2}}^2} = \frac{g_{m2}}{g_{m1}} = \frac{\sqrt{100\ \mu m}}{\sqrt{300\ \mu m}} = 0.58$
- for NMOS CSA $\frac{{v_{n\,th1}}^2}{{v_{n\,th2}}^2} = \frac{g_{m2}}{g_{m1}} = \frac{\sqrt{100\ \mu m}}{\sqrt{200\ \mu m}} = 0.71$

In subthreshold regime, the theoretical ratio would approach the value of 1 in both cases. The ratios obtained in reality from the measurements lie always in between the two results (Figure 3.34). The additional results shown in Figure 3.35 give supplementary arguments towards the subthreshold g_m model. The chart shows thermal noise ratios, each obtained for the same CSA with different bias current. The theoretical values predicted from respective operating region models are:

- saturation model $\frac{{v_{n\,th1}}^2}{{v_{n\,th2}}^2} = \frac{g_{m2}}{g_{m1}} = \frac{\sqrt{2\ \mu A}}{\sqrt{10\ \mu A}} = 0.45$
- subthreshold model $\frac{{v_{n\,th1}}^2}{{v_{n\,th2}}^2} = \frac{g_{m2}}{g_{m1}} = \frac{2\ \mu A}{10\ \mu A} = 0.2$

Meanwhile the ratios obtained from the measurements oscillate between 0.2 and 0.25, resolutely following the weak inversion model. Meaningful is the fact that the SPICE2 model shows again results that are consistent with the measurements.

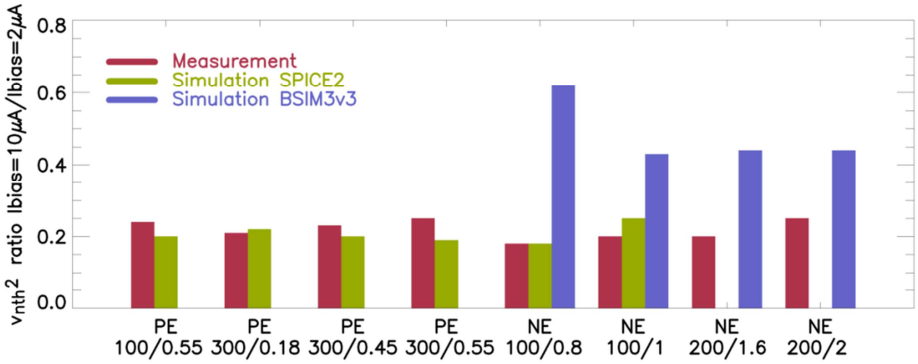


Figure 3.35 Ratio of thermal noise at two values of I_{BIAS}: $10\ \mu A$ and $2\ \mu A$ for a given CSA with fixed input transistor dimensions. Characterization of PMOS and NMOS CSA of various W and L dimensions.

In conclusion, the analyses of the thermal noise show that the overall CSA noise behaviour is too complex to be characterized with any of the simplified transconductance models (*3-48* and *3-49*). The important and extremely useful outcome of this analysis – is the consistency between the thermal noise obtained experimentally and the simulation results using the SPICE2 model. The indicated simulation model provides results of the squared noise ${v_{n\,th}}^2$ well within an order of magnitude. This conclusion has a key consequence in the future development of the complete readout ASIC, where the power consumption is set to be very low. In design of the final application with current densities expected to be very low – the selected thermal noise model: SPICE2 is expected to ensure a good precision.

Flicker noise

In the analysis of the noise parameter: $v_{n\,f}{}^2$ in case of the PMOS-based CSAs the extracted noise shows certain systematic properties, which made it interesting to analyze with respect to channel width and length. In case of the NMOS-based CSA however the parameters are not consistent. Most likely, the parameters extraction from measurements was not precise enough. In case of NMOS-based CSA I expect that the measurements were done at peaking times, where the thermal noise still has a dominating influence over the flicker noise. Extending the peaking time used in measurements to much higher values should increase the $v_{n\,f}{}^2$ extraction precision, if only the parallel noise contribution could be still neglected.

In pursuit of the PMOS transistor's flicker model, I have studied its inverse proportions with respect to: L, WL or WL^2. The analysis with respect to gate dimensions would not indicate a specific noise model that follows the measurements. However the last proportion: WL^2, shows an interesting behaviour. In parallel it should be noticed that the BSIM3v3 flicker noise model constitutes a sum of two terms: $A \cdot \frac{I_{BIAS}{}^2}{C_{ox} \cdot W \cdot L^2}$ and $B \cdot \frac{I_{BIAS}}{C_{ox} \cdot L^2}$, whereas the SPICE2 flicker model is only described by $C \cdot \frac{I_{BIAS}}{C_{ox} \cdot L^2}$ [11]. Because in the extracted parameters the width appears to be of high importance, not alike in the SPICE2 model, I have decided to compare the measurements only with the BSIM3v3 model simulations. Figure 3.36 shows flicker noise comparison: between the measured and the simulated values.

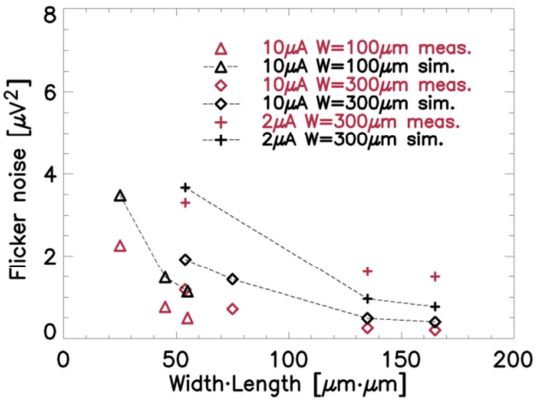


Figure 3.36 Comparison of flicker noise extracted from simulations and from measurements. Presented results for thin oxide PMOS input transistor at different width (100 μm and 300 μm) and bias current (2 μA and 10 μA). BSIM3v3 has been used as the noise model in simulations.

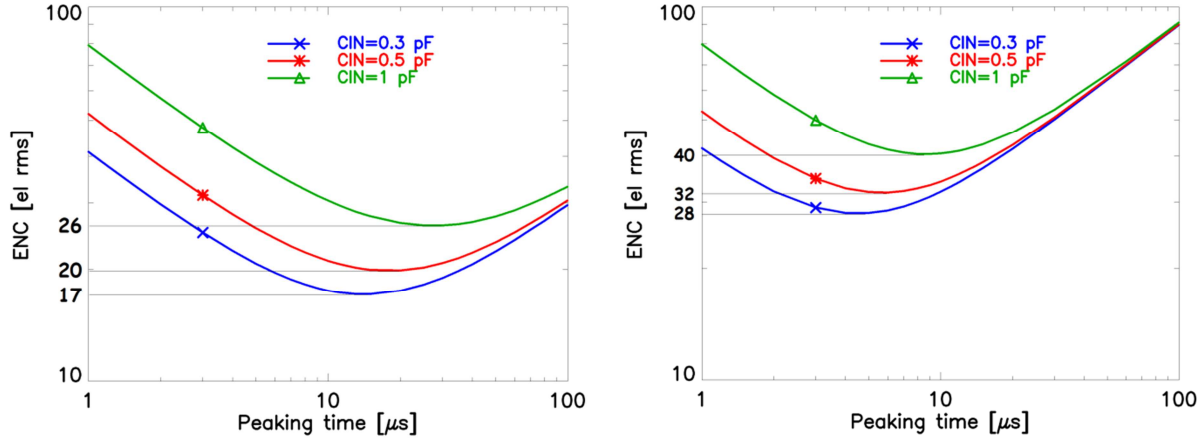
Systematically the absolute value is slightly higher in simulations, yet the extrapolated profiles appear very similar in case of the measured and the simulated points. In consequence the BSIM3v3 noise model of the flicker noise is chosen for design and simulations of the final readout ASIC.

3.4.4.6 Conclusions on extracted noise parameters

I have performed a complete set of ENC measurements with the CR-RC^2 shaper for almost all of the CSA integrated on the Caterpylar testchip. The data set was sufficient to be able to extract the CSA-related parameters: C_{CSA}, $v_{n\,th}{}^2$ and $v_{n\,f}{}^2$ – necessary to calculate the ENC of a given CSA with any other shaper. The extracted values have been compared to simulations. The complete analysis of this comparison is described in Annex IV. The analyses lead to following essential conclusions:

- SPICE2 model has been found accurate to predict the thermal noise behaviour,
- BSIM3v3 has been proved to be an accurate reference in case of the flicker noise,

The conclusions on the noise model however are valid and confirmed only for CSAs with a PMOS input transistor. The simulation tool offers separate model setting for each noise type: thermal and flicker. The defined configuration can serve for any future low noise low power circuit characterization in the given IC technology. Finally, from the group of parameters obtained for each CSA, I have calculated the expected ENC for applications with CdTe detectors. If it is the CR-RC^2 shaper that is considered – the best suited CSA is found to be the one with the thick-oxide PMOS and dimensions: $W = 100\ \mu m$ and $L = 0.45\ \mu m$ (or $0.55\ \mu m$).



A) $I_{DET} = 0.5\ pA$ B) $I_{DET} = 5\ pA$

Figure 3.37 Expected ENC due to electronics comprising the CdTe detector, the optimal CSA PMOS-(based with dimensions $W/L = 100\ \mu m/0.45\ \mu m$) and the CR-RC^2 filter. ENC calculated for three values of the detector capacitance C_{IN}: the worst case $1\ pF$, for $0.5\ pF$ and for $0.3\ pF$, as well as for two values of the detector dark current: A) $I_{DET} = 0.5\ pA$, B) $I_{DET} = 5\ pA$, which is the worst case value.

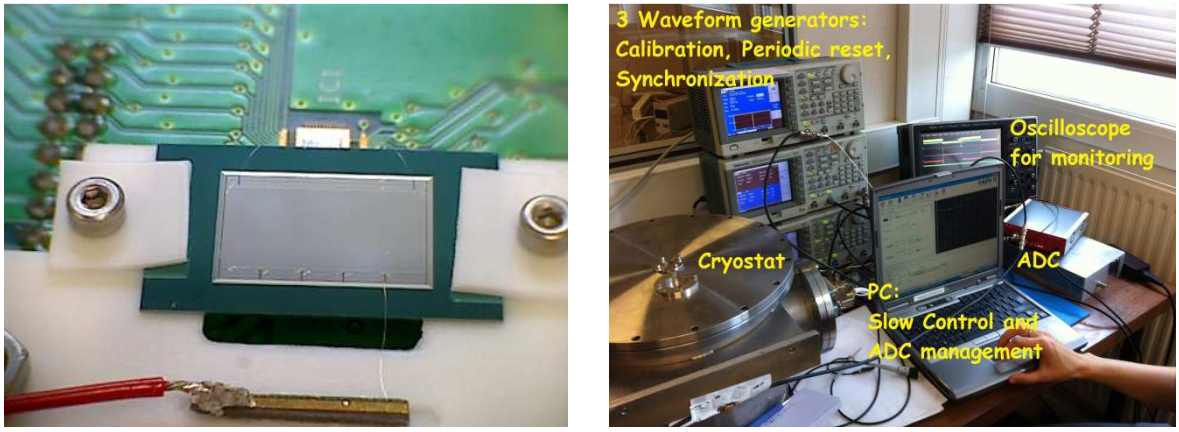
The resulting minimum achievable ENC in a detection chain comprising pixelated CdTe detector, the optimal CSA (T10) and the CR-RC^2 filter is expected to be below $40\ el\ rms$. This is the value obtained for the worst case parameters of the detector: the input capacitance C_{IN} of $1\ pF$ and the dark current of $5\ pA$. Being more optimistic, if the capacitance and the dark current are lower, what is very likely since I assumed high safety margins in their estimations (in the paragraphs 2.1.2 and 2.1.3) – the ENC could be even below $20\ electrons\ rms$. Various possible scenarios of the detector input parameters (C_{IN} and I_{DET}) are illustrated in Figure 3.37. From these results I can estimate that in the best case, it is feasible to realize a Fano-limited instrument based on such detection chain with CdTe detector, where the FWHM resolution would be in the order of $0.5\ keV$ up to X-ray energies of $30\ keV$.

3.4.5 Measurements with Si detector

In addition to purely electrical characterization presented in the previous section, the Caterpylar ASIC has also been tested in a setup dedicated to X-ray photons spectroscopy. A dedicated measurement board was realized where a radiation detector was connected to the IDeF-X Caterpylar ASIC on the PCB socket, Figure 3.38 A). The detector used in the experiment is a silicon diode. On one side of the

diode there is a common anode and on the other – several smaller cathodes of various sizes. The smallest pixels have dimensions of $0.8\ mm \times 0.67\ mm$ – these were the pixels of interest in the Caterpylar experiment, since the input capacitance is similar to the one expected with the CdTe detector in the target application. The detector is based on the same fabrication technology as the larger one characterized in [18]. Therefore its input capacitance can be extrapolated correspondingly to the relative dimensions. Consequently the input capacitance of the smallest pixels is estimated to 0.3 pF. The smallest pixel is connected to one of the Caterpylar CSA inputs through a direct bond wire between the cathode and the CSA input bond pad. The common anode is biased at $65\ V$. The input transistor of the CSA T12 is a thick oxide PMOS with dimensions $W/L = 300\ \mu m/0.3\ \mu m$.

The socket PCB with the detector and ASIC together with the mother board containing the associated bias circuitry was placed in a cryostat, shown in Figure 3.38 B), and cooled down to: -10 ℃. At this temperature the measured detector dark current I_{DET} of $0.5\ pA$ was measured. The system in the described configuration was illuminated with a ^{57}Co source to realize a spectrum.



A) B)

Figure 3.38 The measurement setup of the Caterpylar ASIC configured as the Si detector readout circuit. A) Image of the detector with two bondwires and the socket PCB, the ASIC appears in the background. B) The measurement bench with the cryostat (on the left) and the control equipment.

Separate sets of spectroscopic measurements have been performed with two pulse shaping methods, described in the paragraph 3.4.3. Both are realized externally to the Caterpylar ASIC. The first one engages the analog CR-RC^2 shaper. In this case the CSA reset has been operating in a continuous mode. In the second setup the MCDS filtering has been performed off-line on the discrete data acquired by an ADC at the CSA output. In this case the CSA reset has been operating in the pulsed mode. In both cases a single X-ray photon event resulted in a single output voltage value translated to the photon energy.

In the measurements the CSA was biased with the current I_{BIAS} of $10\ \mu A$. Since in the PMOS based CSA there are two power supplies: $V_{SOURCE} = 1.3\ V$ and $V_{DD} = 1.8\ V$ the total power consumption is estimated to only $14\ \mu W$.

With the cathode readout of the Si detector the dark current seen by the CSA flows in the opposite direction than supported by the continuous PMOS reset. Therefore the leakage current compensation circuit had to be employed. Its adjustable terminals have been tuned to provide a sufficient current sink in the opposite direction to the dark current. The current has been increased to a value where the CSA would achieve the optimal DC operating point. The issue is relevant to the

analog filtering setup with CR-RC^2 and the continuous PMOS reset. The second consequence of the cathode-side readout, important in both setups, is the signal charge polarity. Just as the dark current, for which the Caterpylar has been primarily designed, it has also an inversed polarity with respect to the target CdTe anode-readout application. With the cathode readout, the CSA output dynamic range is lower for the positive input charge, imposing low limits on the maximum photon energy.

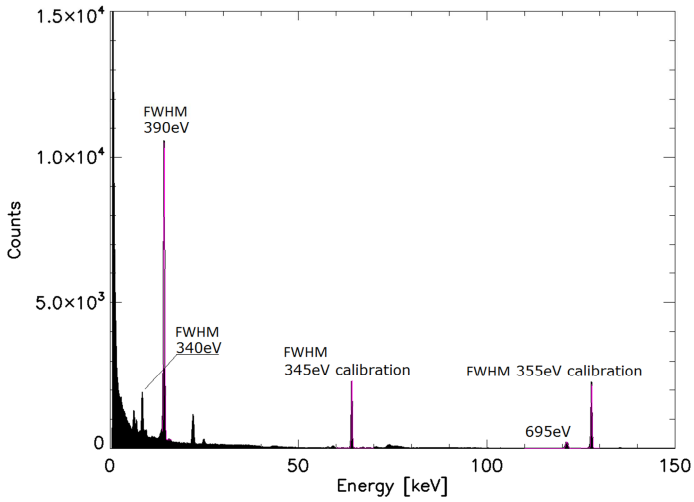


Figure 3.39 Spectroscopy measurements with indicated FWHM values of main peaks, source: ^{57}Co gamma rays, detector: Si diode $0.8\ mm \times 0.67\ mm \times 0.33\ mm$, CSA T12 with power consumption of $14\ \mu W$, filtering: analog shaper CR-RC^2 with peaking time $11\ \mu s$, temperature: -10 °C.

The spectroscopy plots realized with the two filtering methods are shown in Figure 3.39 for CR-RC^2 and Figure 3.40 for the MCDS shaper. The results have been calculated with constant values of the electron-hole pair production energy in silicon of $3.63\ eV$ and the Fano factor of 0.11 [19]. In both spectrums obtained for the radioactive source of ^{57}Co, the Compton edge is observed at the energy of approximately $40\ keV$.

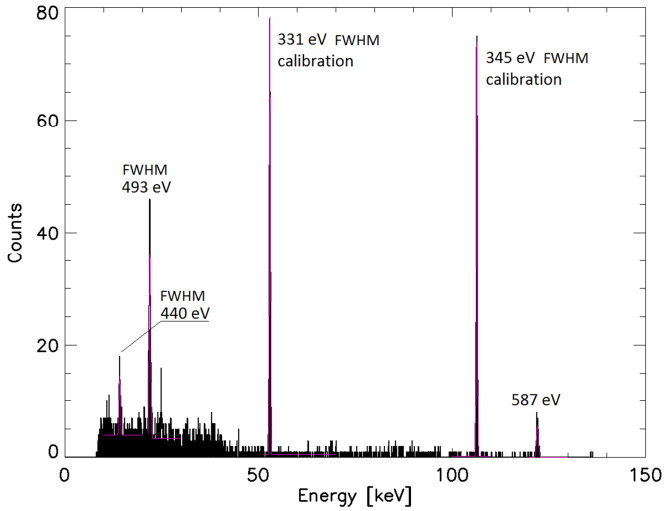


Figure 3.40 Spectroscopy measurements with indicated FWHM values of main peaks, source: ^{57}Co gamma rays, detector: Si diode $0.8\ mm \times 0.67\ mm \times 0.33\ mm$, CSA T12 with power consumption of $14\ \mu W$, filtering: discrete 16-fold MCDS shaper with sampling frequency $700\ MHz$, temperature: -10 °C.

The characteristic energy peaks related to the setup and the emitted ^{57}Co gamma are found at $8\ keV$, $14\ keV$ and $122\ keV$. The FWHM values obtained with the analog shaper are respectively:

$340\ eV$, $390\ eV$ and $695\ eV$ with the peaking time set to the highest adjustment of $11\ \mu s$. With the MCDS filter the corresponding resolutions are: $440\ eV$, $493\ eV$ and $587\ eV$ obtained with a 16-folded processing at $0.7\ MHz$ sampling. The results are summarized in Table 3.9.

Shaper type:	FWHM resolution $[eV]$ at: $8\ keV$	$14\ keV$	$122\ keV$	calibration peak
CR-RC^2 at $11\ \mu s$	340	390	695	345
16-fold MCDS at $0.7\ MHz$	440	493	587	331

Table 3.9 Summary of the FWHM resolutions achieved in the ^{57}Co spectroscopy experiment with the IDeF-X Caterpylar CSA T12 connected to Si diode cathode side of dimensions: $0.8\ mm \times 0.67\ mm \times 0.33\ mm$, with the input capacitance estimated to $0.3\ pF$ and dark current of: $-0.5\ pA$ compensated with the on-chip ILEAK structure.

The calibration peaks present in both plots have a better FWHM resolution than peaks related to the emission lines, partly because of the absence of Fano noise contribution. However at the higher energy peaks the degradation of the resolution is also related to the limited dynamic range (and thus decreasing gain in that region). Because of the different acquisition methods, the total number of counts obtained with the MCDS is lower than with CR-RC^2. The MCDS processing with the off-line algorithm is more time consuming and requires a large amount of data to produce the output value being a measure of single event energy. Furthermore the detection threshold is significantly higher in this case than with the analog setup. This is because, in contrast to the CR-RC^2 trigger method, the discriminator for the MCDS is based on a comparator connected directly to the CSA output, without any filtering.

The obtained experimental results have shown excellent spectroscopic capabilities of the CSA included on the Caterpylar. Despite the cathode readout and the necessity to compensate for the inversed polarity detector dark current simultaneously adding parallel noise (due to the compensation transistor) – the measured energy resolution is very good. The electronic noise estimated from the calibration peak, not burdened with the Fano statistics, is $38\ el\ rms$. This includes a strong parallel noise contribution. It should be noted, that the CSA used in the experiment, T12 has dimensions $W/L = 300\ \mu m/0.3\ \mu m$, significantly different from the optimum CSA selected for the CR-RC^2 shaper, whose dimensions are $100\ \mu m/0.45\ \mu m$. Initially I have attempted to carry out the measurements also with the selected CSA T10. However because of the setup handling difficulties (and the consequent damages) as well as the limited number of detectors to repeat the hybridization with the ASIC, the measurements with the chosen CSA have not been pursued.

3.4.6 Total ionizing dose tests up to 1 Mrad

In this last paragraph dedicated to the experimental results with the IDeF-X Caterpylar, I describe the first steps towards the space qualifications of the chosen IC technology and the CSA circuit. The test presented here aimed at the investigation of the radiation effects on the electronics. A dose of ionizing radiation has been delivered to the circuit in the amount that would be encountered in a space environment during a long mission. The ASIC has been irradiated with the ^{60}Co source in the COCASE facility of CEA (Figure 3.41). The source emits $1.17\ MeV$ and $1.33\ MeV$ gamma rays. The photons energies are sufficiently high to trigger the principal damage mechanisms known in the semiconductor circuits: atom displacement and oxide ionization. Both effects lead to modification of

the electrical characteristics of the substrate and more importantly – the integrated transistors. The radiation damages are related to the amount of the total dose rather than to energy or type of the emitted particles [21]. Researchers show that the amount of damage depends on the technology and on transistors' geometry [22].

A) B)

Figure 3.41 The measurement setup with the Caterpylar ASIC at the COCASE facility at CEA. A) A PCB with the Caterpylar chip, in front of the ^{60}Co gamma source. The photograph was taken in the last measurement phase with the smallest distance to the source. B) The supplies, control and the monitoring equipment placed in the protected area, not exposed to the gamma rays.

The ASIC performance has been monitored as a function of the total absorbed ionizing dose. The setup for this measurement included a board with the Caterpylar ASIC, with a complete adjustment of the operating point and with the CSA current set to $10\ \mu A$. Tests have been carried on for several months leading to accumulation of the total dose in the range of $1\ Mrad$. During this time there were 10 short irradiation suspensions forced regularly every few weeks. During each pause that lasted typically a few hours – the total dose was read out and the ENC was measured on selected CSA to observe the noise evolution upon irradiation. In total 12 sets of measurements have been performed, where the first one was done before irradiation, and all were spread over 360 days of the experiment. Out of 26 CSA integrated on the Caterpylar ASIC, five of them have been chosen for characterization. The choice includes devices of different width, oxide thickness, polarity and architecture:

- T1: thin oxide PMOS, $W/L = 100\mu m/0.18\mu m$, folded cascode
- T6: thin oxide PMOS, $W/L = 300\mu m/0.25\mu m$, folded cascode
- T10: thick oxide PMOS, $W/L = 100\mu m/0.45\mu m$, folded cascode
- T16: thin oxide NMOS, $W/L = 100\mu m/0.8\mu m$, folded cascode
- T21: thin oxide NMOS, $W/L = 100\mu m/0.8\mu m$, unfolded cascode

At the beginning of tests the ASIC has been placed at a distance $r = 33\ cm$ away from the radioactive source. During the first hundred days of the experiment the ENC did not noticeably change, meanwhile the absorbed dose reached $100\ krad$. At this point the ASIC was shifted towards the source, down to $17.5\ cm$ away from it – in order to increase the exposure rate. The second

increase in exposure took place after another 150 days at the total dose of $250\ krad$: the distance has been decreased down to $11\ cm$. The dose measured at intermediate pauses as a function of the experiment time duration is shown in Figure 3.42. The respective distances from the source to the board with the Caterpylar ASIC are also indicated with scale on the right side Y-axis. The intensity of the radioactive source, regarded as a point source, follows the inverse square law. If at the distance r_1 from the source the radiation dose rate is X_1 $[rad/h]$, the dose rate X_2 at a distance r_2 is calculated from the following equation:

$$X_2 = X_1 \left(\frac{r_1}{r_2}\right)^2 \qquad 3\text{-}50$$

The relationship explains the steep increase in the total dose rate after the first 100 hundred days of the experiment.

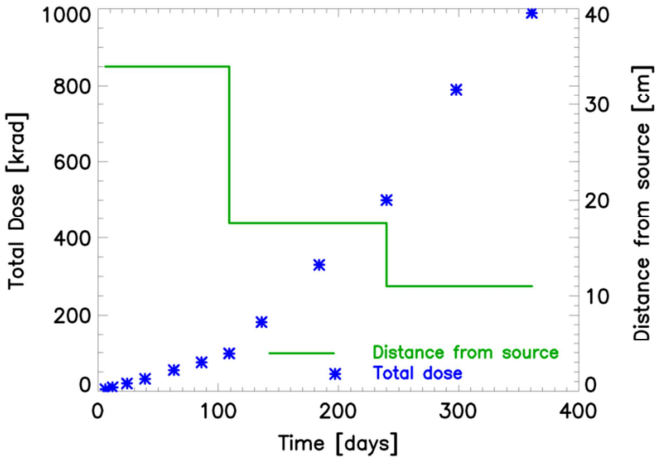


Figure 3.42 Total dose absorbed by the Caterpylar ASIC during irradiation tests with ^{60}Co source and distance between the ASIC and the source – both shown as a function of the experiment time.

The primary parameter of interest was ENC and it was monitored at each pause, indicated in Figure 3.42. Every time the ENC was measured with two shapers: 1^{st} order and 2^{nd} order semi-Gaussian. The CR-RC^2 has a peaking time adjustable in range: 1 to $11\ \mu s$. Meanwhile the CR-RC supports tests at higher peaking times from $18\ \mu s$ to approximately $1.2\ ms$. However, there are also other CSA parameters that have been monitored: gain, rise time, C_F discharge time and the baseline voltage level. No major and consistent variations in gain and rise time have been observed. Concerning the DC value of the baseline measured at the CSA output, it steadily increases throughout the tests. This is valid for all five CSA circuits subjected to regular observations. The results are shown in Figure 3.43.

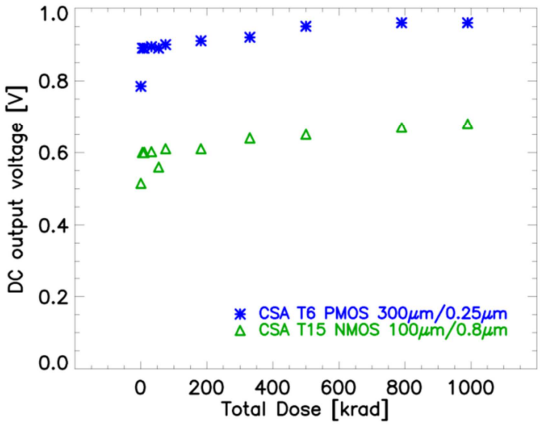


Figure 3.43 CSA output DC baseline as a function of the total ionizing dose for PMOS and NMOS based CSA. Measurements conditions: CSA bias current $10\ \mu A$*, minimized compensation current* I_{comp}*.*

The second parameter that also changes with the applied ionizing dose is the discharge time of the CSA feedback capacitance C_F. This parameter is measured as follows: a voltage step of $30\ mV$ is applied at the test input (shown in Figure 3.15 in the paragraph 3.3.4). It results in the step signal at the CSA output with the amplitude also close to $30\ mV$. Since the CSA are operating in the continuous reset mode during these tests – the current through it slowly discharges the feedback capacitance, causing the output voltage to fall down to the baseline level. The parameter is measured as a discharge time from 100% to 50% of the output voltage after the event. Plot as a function of the total dose is shown in Figure 3.44 for PMOS and NMOS type input devices, showing the parameter evolution.

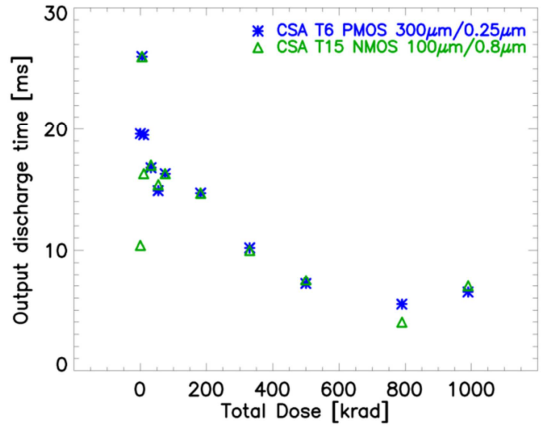


Figure 3.44 Discharge time from 100% *to* 50% *of the CSA output voltage (after the* $30\ mV$ *output step signal) shown as a function of the total ionizing dose for PMOS and NMOS based CSA. Measurements conditions: CSA bias current* $10\ \mu A$*, minimized compensation current* I_{comp}*.*

Finally in Figure 3.45 the ENC as a function of peaking time is presented. This particular plot shows CSA T1 in a few of the experiment phases: before irradiation, after $75\ krad$ dose and in all consecutive measured points. Up to the value of $75\ krad$ no change in ENC was observed. Then with increasing dose, the ENC increases and the effect is pronounced at high peaking times. Very similar characteristics have been observed for other four measured CSA circuits.

3.4. Caterpylar: experimental results

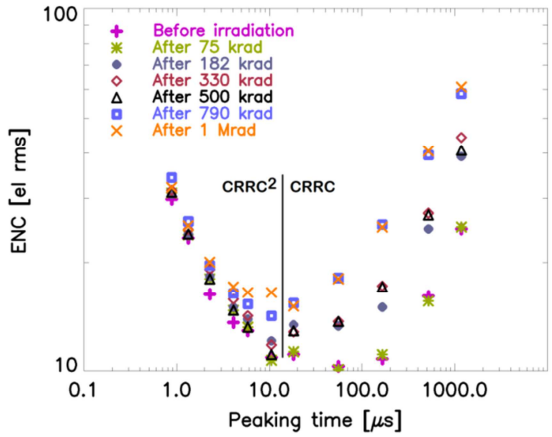


Figure 3.45 ENC as a function of peaking time. Evolution of the characteristic with increasing total ionizing dose up to $1\ Mrad$*. Measurements conditions: CR-RC² shaper (for* $t_{peak} < 11\ \mu s$*) CR-RC shaper (for* $t_{peak} > 18\ \mu s$*), CSA bias current* $10\ \mu A$*, no input capacitance, minimized compensation current.*

Figure 3.46 shows comparison of all five examined CSA as a function of the total dose at the lowest and the highest peaking time value. The plot in Figure 3.46 A) shows the ENC measured at each irradiation experiment step with the lowest peaking time of $1\ \mu s$ with the CR-RC² shaper. Figure 3.46 B) shows ENC monitored along the tests with the CR-RC shaper and the peaking time set to the maximum value of $1.2\ ms$.

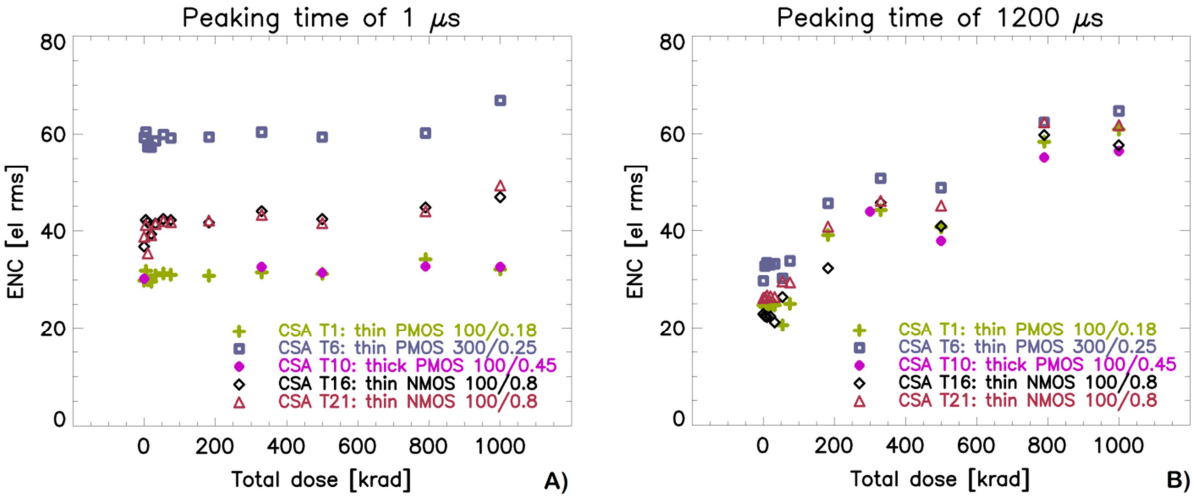


Figure 3.46 ENC as a function of the total ionizing dose for different CSA with peaking time set to A) $1\ \mu s$ *B)* $1200\ \mu s$*. Measurements conditions: CR-RC² shaper, CSA bias current* $10\ \mu A$*, no input capacitance, minimized compensation current.*

Measurements at the low peaking time show little dependency of ENC on the total dose. In this region the ENC_{th} due to thermal series noise is dominating the total ENC. The fact that these characteristics are relatively flat indicates that the thermal noise does not depend on the total dose up to $1\ Mrad$. However at high peaking times, where the ENC is dominated by the parallel noise, it gradually increases to achieve nearly 200% difference: before the irradiation and at the end of the experiment at $1\ Mrad$. The obtained results indicate increase in the ENC related to the parallel noise. While the detector is not connected to any CSA during tests and measurements, there are still two possible sources of the parallel noise:

- noise of the reset transistor, increases with decreasing channel resistance

- noise of the current compensation transistor and the reset transistor, increase with increasing drain current of the compensation transistor

Results from Figure 3.43 and Figure 3.44 confirm the notion of interest in these noise sources: the CSA output voltage DC level increases with the ionizing dose, while the C_F discharge time gets shorter. Both effects are observed in the CSA with the PMOS and with the NMOS as the input transistor. What could cause such a change in both parameters? The CSA output DC voltage increases with a lower reset resistance R_F related to a static function $V_{CSAout}(I_{comp})$ with a nonlinear equation [23]. Similarly the output voltage discharge time is related to the function $V_{CSAout}(I_{comp}, Q_{in}, t)$ but in the dynamic conditions. Consequently a faster discharge rate can be related to the same root causes. In all tests the current compensation transistor has the following setup: the transistor gate voltage is set to $0\ V$, while source is at $0.4\ V$ in the NMOS-based CSA and at $0.6\ V$ in the PMOS-based CSA. It results in the negative V_{GS} voltage, meaning that any possible presence of the current I_{comp} is due to the uncontrolled leakage current. Thus, the possible event that might have caused the modification of these two parameters and simultaneous increase of the parallel noise is either: a higher value of the leakage current through the compensation transistor I_{comp} or a direct modification of the threshold voltage in the feedback reset PMOS. Both effects are likely to appear with the gradual oxide damage upon irradiation.

The observed shifts in the monitored electrical parameters do not cause any serious performance degradation in this particular application. The result from this test is the important information on the robust functionality and maintained low noise of the Caterpylar CSA subjected to a high ionizing dose. These initial space qualification results keep the way open for the chosen IC technology to participate in further developments of the CdTe readout circuit for the X-rays spectro-imaging camera.

3.5 Filter studies using extracted CSA parameters

This chapter has been dedicated to the optimization, the design and measurements of the Caterpylar ASIC. One of the principal motivations for realizing this testchip was: to gain a deep understanding of the achievable CSA noise with the given technology. I have met this target by doing a complete characterization of each of the integrated CSA. The ENC points at variable test conditions (t_{peak} and C_{IN}) were measured with the external CR-RC^2 shaper. The outcome of this procedure is the set of extracted parameters for each CSA: internal input capacitance C_{CSA}, thermal noise PSD ${v_{n\,th}}^2$ and flicker noise PSD ${v_{n\,f}}^2$. The extraction method was described in the paragraph 3.4.4. There, I have also presented the optimal CSA that should give the best results with the CR-RC^2 shaper. This is the one with PMOS transistor as the input device with dimensions set to $W/L = 100\ \mu m/0.45\ \mu m$. It has been selected out of 26 CSA blocks integrated on the Caterpylar testchip. The conclusion is based on calculations employing the extracted parameters.

The acquired knowledge should serve as an important support in the development of the complete CdTe readout circuit, including an array of detection channels, each with a pulse shaping capability. However, in the target detection chain, there is a choice of which filter should be implemented. In the Chapter II – two potential candidates have been introduced: the CR-RC^2 and the MCDS shapers. For each of them the noise parameters for ENC calculations have been obtained: A_p, A_{th} and A_f. The noise parameters were compared also with other commonly known shapers. The outcome has been summarized in the paragraph 2.3.6.

At this point with the complete set of information on each detection stage:

- CdTe detector: C_{IN} and I_{DET}
- CSA: C_{CSA}, ${v_{n\,th}}^2$ and ${v_{n\,f}}^2$
- Shaper: A_p, A_{th} and A_f

it is possible to analyze the possible ENC scenarios with any of the available CSA (from the Caterpylar ASIC) and with any chosen shaper. To calculate the ENC – it is enough to insert the appropriate parameters' values into the ENC equations *3-36 - 3-38*.

There are two remaining questions of the highest interest. First of all, it must be determined: which of the CSAs is the most suitable for the corresponding shapers. The answer is known already in case of the CR-RC^2 shaper. However because each CSA has different proportions of the thermal-to-flicker noise – shapers with different filtering capabilities (defined with A_p, A_{th} and A_f) might need a different CSA to achieve the best possible readout resolution. Secondly, for the selected CSA-Shaper pairs it is essential to quantify the actual best achievable performance in terms of ENC and the corresponding optimal peaking time t_{peak}.

3.5.1 The best CSA

To address the remaining issues I have analyzed each of the shapers discussed in the paragraph 2.3.6 with all CSA from the Caterpylar ASIC. For each CSA, with parameters corresponding to the current I_{BIAS} of $10\ \mu A$, the total ENC was calculated as a function of the peaking time using the equations *3-36 - 3-38*. Because of the large spread in the detector capacitance C_{IN} – every time, there were two extreme cases considered: with $0.3\ pF$ and with $1\ pF$ at the input. The following shapers have been considered:

- Semi Gaussian: 1^{st}, 2^{nd} and 4^{th} order.
- MCDS in two variants: with variable sampling frequency f_s at number of samples k set to 16 and with variable number of samples at fixed f_s to $0.8\ MHz$. The peaking time has been calculated as $t_{peak} = k/f_s$.
- Truncated Cusp with the truncated interval determined by the measurement (peaking) time set in range from 0.25 to 8 times the noise time constant τ_{white}, defined as $(C_{IN} + C_{CSA} + C_F)\sqrt{{v_n}_{th}^2/{i_n}_p^2}$ (for more details please refer to the paragraph 2.3.3).
- Triangular.

The ENC calculation spreadsheet containing all these calculations led to the simple conclusion: the optimal CSA is the same in case any of the shapers. It is again the T10 from the Caterpylar ASIC whose input thick-oxide PMOS dimensions are: $W/L = 100\ \mu m/0.45\ \mu m$. In fact at the condition of the higher input capacitance $C_F = 1\ pF$ the Cusp, the triangular and the CR-RC^2 shapers indicated the CSA with slightly longer channel of the input transistor: $W/L = 100\ \mu m/0.55\ \mu m$, however the negligible difference in the resolution of a fraction of $electron\ rms$ permits to omit this result in practice. Let's have a look on the exact ENC numbers.

3.5.2 Achievable ENC with various filters

With all considered filters the best CSA is always T10 with dimensions $W/L = 100\ \mu m/0.45\ \mu m$ or T11 with slightly longer channel of $L = 0.55\ \mu m$. With the known CSA selection, I will now speak only about the shaper choice and the corresponding minimum ENC that can be achieved. The summary of the obtained results is presented in Table 3.10. The calculations show that the best results in energy resolution can be obtained with the truncated Cusp. Assuming the most optimistic detector capacitance of $0.3\ pF$ and worst case dark current of $5\ pA$ the minimum achievable ENC with the CSA T10/T11 would be as low as $19\ el\ rms$. The best ENC with this particular shaper is achieved with an infinitely long peaking time. However if the peaking time equals to only 8 times the noise constants τ_{white} the ENC results would be only 5% higher than the absolute minimum.

The second interesting result, which offers much shorter optimal peaking time is the triangular shaper. The best possible ENC is $21\ el\ rms$, again with the lower extreme of C_{IN} and $5\ pA$ dark current.

3.5. Filter studies using extracted CSA parameters

There are also the two shapers of the greatest interest in terms of the future implementation in the readout ASIC: the semi-Gaussian and the MCDS filters. The semi-Gaussian has been analyzed in four cases: with a single differentiator – CR-RC, with double – CR-RC^2, the 4^{th} order – CR-RC^4 and finally the 8^{th} order – CR-RC^8. Among them the 2^{nd} order shaper is the best compromise between the minimum ENC and the optimal peaking time. Nevertheless with the noise PSD present at the CSA output it appears from the demonstrated results in Table 3.10 that the ENC improves with the shaper order.

Shaper type	$C_{IN} = 0.3\ pF, I_{DET} = 5\ pA$		$C_{IN} = 1\ pF, I_{DET} = 5\ pA$	
	ENC_{MIN} $[el\ rms]$	$t_{peak\ OPT}$ $[\mu s]$	ENC_{MIN} $[el\ rms]$	$t_{peak\ OPT}$ $[\mu s]$
CR-RC	31.1*	4	44.6	8
CR-RC^2	28.1*	4	40.4	8
CR-RC^4	27.4*	8	39.3	16
CR-RC^8	26.4*	8	37.9	16
MCDS $k = 16$	24.1	10	40.1	10
MCDS $f_s = 0.8\ MHz$	32.1	40	39.6	40
Truncated Cusp	19	Infinity $\tau_{white} = 5.8\ \mu s$	27	Infinity $\tau_{white} = 11\ \mu s$
Triangular	21.2	8	30.7	16

* Contribution of the parallel noise due to reset feedback transistor is included. It assumes the simple active continuous reset as used in the Caterpylar ASIC with the noise PSD at the pA current range of $2 \cdot q \cdot I_{drain}$ [14].

Table 3.10 The minimum ENC achievable with the different shapers presented with the corresponding optimal peaking times. In the calculations it is always either the T10 ($W/L = 100\ \mu m/0.45\ \mu m$) or the T11 ($W/L = 100\ \mu m/0.55\ \mu m$) CSA from the Caterpylar ASIC that is found the best suited for the small pixel CdTe readout (there would be only small differences in results if only T10 was considered). Two extreme cases of the detector capacitance value are evaluated. The CSA considered here are all biased with $I_{BIAS} = 10\ \mu A$.

Let's finally discuss the MCDS shaper ENC results. Its performance has been calculated for two cases:

- At fixed number of samples k[5] equal to 16 and the optimal peaking time adjusted by changing the sampling frequency
- At the sampling frequency set to $0.8\ MHz$ and the variable number of samples.

A glance at this two different views of the ENC as a function of the peaking time show (Figure 3.48 and Figure 3.49), that MCDS can have comparable performance with results obtained with the semi-Gaussian shaper. The indicated minimum ENC achievable with the 16-folded MCDS of $24\ el\ rms$ (at the lower C_{IN} extreme) is close to the absolute best result with this kind of shaper. I must refer back to the MCDS discussion from the paragraph 2.3.5 to clarify it. Because of the following MCDS properties (for details please refer to paragraph 2.3.5):

- ENC_{th} is independent on the sampling period (as long as the $T_s/\tau_{CSA} \geq 4$)
- ENC_{th} decreases with the number of samples k
- ENC_p decreases with decreasing sampling period

thus the minimum total ENC is achieved when the sampling frequency approaches the CSA time constant τ_{CSA}. The time constant for the PMOS-based CSA can be estimated, according to rise time measurements and the related calculations from the paragraph 3.4.2. At the CSA output stage

[5] The number of samples k in the MCDS algorithm, just as it was described in Chapter II, means the number of averaged samples (k – before the event and k – after the event). Therefore the total number of samples in a k-folded MCDS is equal to $2k$.

current of $100\ nA$ set in all ENC measurements, τ_{CSA} is equal to $\sim 100\ ns$, which corresponds to the CSA low pass cut-off frequency in the order of $1\ MHz$. The optimal number of samples k is achieved when $ENC_{th} = ENC_p$ and can be determined with the expression derived in the paragraph 2.3.5:

$$k_{opt} = \sqrt{\frac{3 \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot f_s}{2 \cdot \tau_{CSA} \cdot {i_n}_p^2}} - 0.5 \qquad 3\text{-}51$$

The equation *3-51* indicates the best number of samples at a chosen sampling frequency. The number of samples as a function of the chosen f_s is plotted in Figure 3.47 for the MCDS parameters calculated for the analyzed CSA T10 from the Caterpylar ASIC. If it would be the number of samples that is fixed in the application – the optimal sampling frequency is not the one concluded from the equation *3-51*. Instead a possibly high sampling frequency should be chosen, comparable with the CSA bandwidth, to minimize the parallel noise contribution.

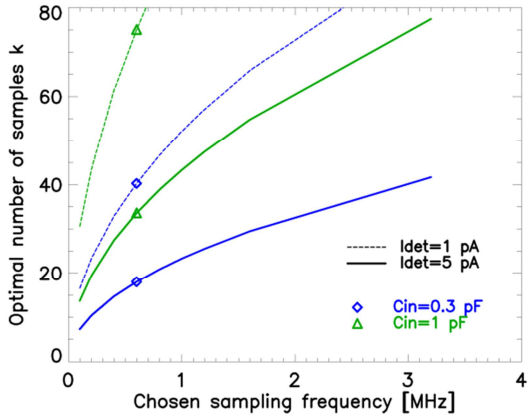


Figure 3.47 The optimal number of samples k_{opt} in the MCDS processing for a chosen sampling frequency f_s. If this is the number of samples that is fixed – the corresponding value on the x-axis it is not necessarily the best frequency, usually the optimal frequency is the one that is possibly high, until approaching the CSA time constant related to its intrinsic bandwidth. The plots are illustrated for two values of C_{IN}: $0.3\ pF$ and $1\ pF$ and for two values of I_{DET}: $1\ pA$ and $5\ pA$.

In the example given in Figure 3.47 in case of the lower extreme of the expected detector capacitance of $0.3\ pF$ and the most pessimistic dark current value of $5\ pA$ – the optimal number of samples is found at the frequency corresponding to the CSA bandwidth limit. With this frequency estimated close to $1\ MHz$ – the optimal number of samples is 20. The second, more general, interesting conclusion from Figure 3.47 is the fact that with much higher detector capacitance or much lower dark current – the MCDS algorithm would require a significantly larger number of samples. In such cases, the MCDS would become impractical in a real application. The particular values of the small pixel CdTe detector parameters – make the MCDS shaper an interesting candidate for the readout circuit.

3.5.3 Conclusions on the best detection chain

To conclude the discussion on the optimal shaper – in Figure 3.48 in Figure 3.49 I present all of the discussed shapers (summarized in Table 3.10) as a function of the peaking time, that is: CR-RC^2, MCDS, Cusp and Triangular. All results have been obtained for the CSA T10 from the Caterpylar ASIC

(for details please refer to Table 3.7 in the paragraph 3.3.4). The first illustration Figure 3.48 shows calculations for the detector capacitance C_{IN} of $0.3\ pF$ and the dark current I_{DET} of $5\ pA$. Figure 3.49 shows corresponding results but at higher detector capacitance of $1\ pF$.

The ENC plot obtained with the truncated Cusp is located at the lowest values and in theory represents the best system for the small pixel CdTe. Unfortunately this shaper is not realizable with analog circuitry. One of the known realizations [55] involves discrete processing, which in case of this filter requires a high oversampling rate and significant calculation time. This is not applicable in the target readout realization: on a single multi-channel chip and with low power consumption. The triangular shaper shows the best results among the other discussed shapers whose weighting function is an approximation of the Cusp. This kind of shaper is the best recommended in analog applications. Unfortunately it is difficult to realize it in a system, like in the astrophysics detection, where a self-trigger upon photon arrival is necessary to process an event.

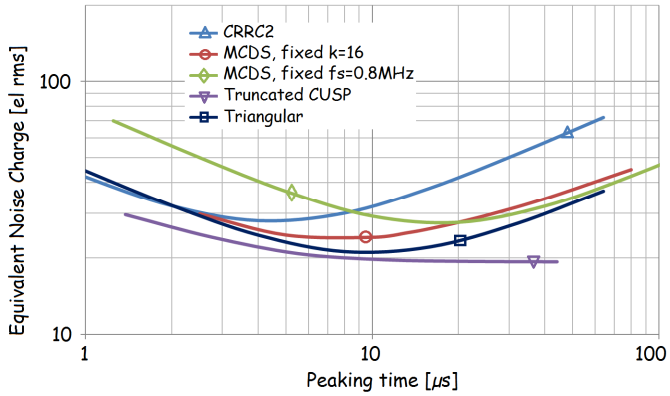


Figure 3.48 Model of the ENC as a function of the peaking time for different shapers. The input conditions are: the detector input capacitance $0.3\ pF$ and the dark current $5\ pA$, the CSA T10 with the input transistor thick oxide PMOS of dimensions $W/L = 100\ \mu m/0.45\ \mu m$ and biased with the current $I_{BIAS} = 10\ \mu A$. The noise parameters have been extracted with the Caterpylar ASIC.

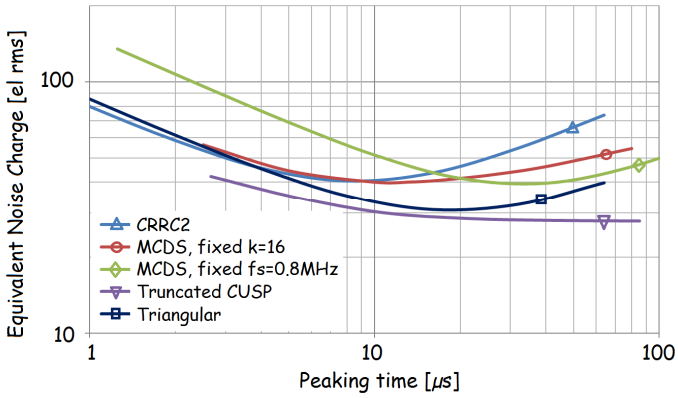


Figure 3.49 Model of the ENC as a function of the peaking time for different shapers. The input conditions are: the detector input capacitance $1\ pF$ and the dark current $5\ pA$, the CSA T10 with the input transistor thick oxide PMOS of dimensions $W/L = 100\ \mu m/0.45\ \mu m$ and biased with the current $I_{BIAS} = 10\ \mu A$. The noise parameters have been extracted with the Caterpylar ASIC.

The triangular shaper not only shows promising ENC results but can also exhibit excellent performances with real analog implementation as it has been demonstrated in the VERITAS ASIC described in [25], for DEPFET and pnCCD detectors readout. In fact, in the cited application it has been realized as a trapezoidal filter with flat top. The drawback of the architecture in terms of use in

the astrophysics detection with the CdTe detector – is that the event measurement time must be known a priori by the processing system, since at the photon arrival instant the processing of the signal must be initiated. This was not an issue in case of VERITAS used with the DEPFET and pnCCD detectors, which do not need to be read out instantaneously. Another possible trapezoidal shaper architecture has been proposed in [26] for the readout of Silicon Drift Detector. This kind of detector, as for CdTe detectors needs an instantaneous processing. The issue has been solved with four parallel processing channels (Concurrent Wheel Technique), realized, as shown in Figure 3.50. However if the trapezoidal function has to be optimized by decreasing the flat top (for example to minimize the parallel noise contribution), the system soon would need a much higher number of concurrent channels, making the implementation significantly more complex.

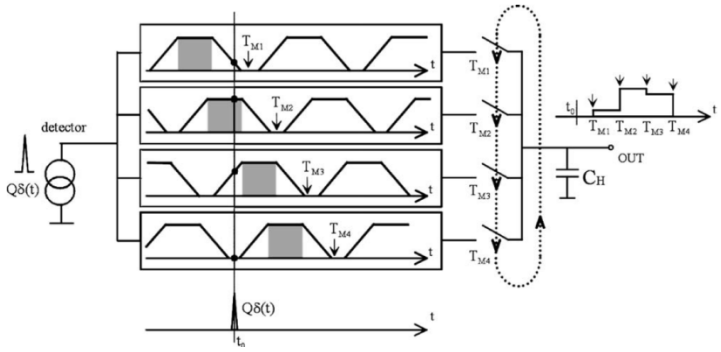


Figure 3.50 Illustration of the Concurrent Wheel Technique (CWT) presented in [26] suitable for realizing the trapezoidal shaper with the Switched Current Technique or the pseudo-trapezoidal with Multi Correlated Double Sampling.

Finally among the discussed shapers there are also the semi-Gaussian and the pseudo-trapezoidal MCDS. They offer similar ENC resolutions, but slightly worse than in case of the two previously discussed shapers. Especially the semi-Gaussian shaper is interesting for practical analog implementation, because of its analogy as a filter with the CR-RC network. I have been equally interested in the MCDS shaper because of the perspectives to realize it with an analog circuit, with an alternative technique to the CWT (from Figure 3.50), introduced in Chapter IV. Pointing towards the semi-Gaussian and the MCDS shapers as the potential candidates in the target CdTe readout ASIC – I conclude the discussion on the ENC performance (with the pixelated detector and CSA T10) as a function of the shaper type. The final choice between the CR-RC^N filter and the MCDS is left to strictly architectural considerations which is the subject of the next chapter.

The presented contents result from the strongly motivated request for producing a testchip with CSA before the final readout ASIC. The testchip was inspired by the following three aspects: understanding of the new IC technology XFAB 0.18 µm, selection of the most suitable CSA for the final application, validation by measurement of the pulse processing system by means of external shapers.

Integration of only the CSA block on the Caterpylar ASIC was justified with the theoretical demonstration – that the CSA and especially the choice of the input transistor is the most critical element in the electronic readout channel design. Noise of this particular transistor has the highest impact on the overall ENC performance. Especially in an ultra-low power CSA the input transistor could contribute up to 90 % of the total noise. For this reason the noise optimization task was in the first place performed in simulations with a detection chain composed of the small pixel CdTe detector model, an idealized CSA with noise contribution only from the input transistor and the filter of reference: the second order CR-RC^2 filter with variable peaking time. Through a set of systematic noise simulations, over several dimensions related to design parameters, I have proposed the optimal width and length of the input transistor, which theoretically should result in the lowest ENC achievable with the given CdTe detector. Several transistor types, available in the chosen technology, have been considered as the CSA input transistor. Also a possible spread in the detector input capacitance has been accounted, resulting in a few possible solutions for the best CSA candidates. Using these optimization results I completed the design of a set of 26 most suitable CSAs and I have implemented them all into the Caterpylar testchip. Each CSA has been planned for an ultra-low power consumption ranging from $3\ \mu W$ to $18\ \mu W$.

During the foundry run, I prepared a custom test bench for my testchip. Then I successfully characterized the ASIC in the laboratory. Most of the ENC measurements were performed with an external 2nd order CR-RC filter with variable shaping time. The known filter characteristics permitted to extract the values of the CSA electrical noise for different input transistor dimensions and bias current conditions. The results were used to build a model to calculate the expected energy resolution in the future imaging spectrometer: with the CdTe detector followed by a complete detection chain. From these results I could determine the best CSA architecture that ensures the lowest achievable ENC with the most suited shapers: semi-Gaussian and MCDS. Through experimental results with a silicon detector, I have confirmed excellent spectroscopic capabilities of the Caterpylar CSA with the power consumption of only $14\ \mu W$. Finally my measurements contributed to an extensive characterization of the chosen IC technology. One of the achievements is the validation of the chosen CSA architecture in the technology of interest with the Total Ionizing Dose tests up to $1\ Mrad$, with the ENC performance almost unchanged after the experiment at the peaking times of interest. The second important technology-related issue is the result of the systematic comparison between the ENC measurements and simulations. The remarkable fact is that the SPICE2 thermal noise model has been found to be very accurate in the subthreshold MOS operation. In consequence the final ASIC design, presented in the next chapter, can rely on this model with high confidence in the simulation results.

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CHAPTER IV

The Readout ASIC D^2R_1

All the subjects discussed so far converge to the main point: the actual design of the complete readout ASIC for pixelated CdTe. The issues related to the detector, the CSA and the shaper have been covered to finally consider the optimal detection chain in practice. The desired performances of the circuit have been discussed in Chapter I. The ASIC should support readout of multiple channels each with limited size, proposed to $300\ \mu m \times 300\ \mu m$. The design should be scalable to large arrays of identical pixels and to be compatible for stacked assembly with the CdTe detector. The principal functionality constraints include the capability to self-trigger upon a photon arrival and to measure its energy in range from $2\ keV$ up to $250\ keV$. One of the major parameters that determine accuracy of this measurement is a low electrical noise. What I have set as a goal is: to meet these requirements with the power consumption per detector area maintained with respect to the existing Caliste HD instrument, previously developed in our group, with $2\ mW/mm^2$ of the CdTe area. The main difficulty lies in balancing between the last two issues: the power resources and the low noise requirement.

In the previous chapter I have presented optimization of the CSA stage for the best energy resolution at limited power consumption. The procedure has been performed with perspective of implementing it in the new readout ASIC discussed in this chapter. The CSA power consumption of $14\ \mu W$ is low enough to comply with the overall power budget. Also the CSA layout size is only a fraction of the total pixel area, leaving sufficient layout flexibility for the filtering stage and the discriminator. Through experimental characterization of the circuit I have established an ENC calculation model. With the model I have demonstrated that ENC of the indicated CSA in a system with CdTe detector and with the semi-Gaussian or the MCDS shaper – should be between $25\ el\ rms$ and $40\ el\ rms$. The lower ENC limit corresponding to CdTe capacitance of $0.3\ pF$ is a very promising result: readout chain with the proposed CSA could be Fano-limited at energies below $40\ keV$.

The main question that appears now is: what is the low-power channel architecture that would obey these semi-theoretical results without degrading the energy resolution already foreseen. In terms of the filtering methods there are two candidates that already appeared on the scene, the semi-Gaussian and the MCDS shapers. Both approaches have shown very promising experimental outcome, when realized as off-chip shapers. The final shaper choice is strongly related with two other aspects: what is the possible event discrimination scheme for each approach? And how the CSA reset realization would influence the overall architecture? My decision is driven by: the power consumption and the layout area. In this chapter I present feasibility studies for the full readout system on-chip implementation. The complete readout ASIC architecture is proposed and discussed. I will conclude this chapter with experimental results of the new readout ASIC D^2R_1.

4.1. Challenges in design concept

Throughout the previous chapters, the necessary background has been collected to identify the main requirements for the new ASIC. In section 1.3, I have defined the most important functions of the circuit to read signal from a pixelated CdTe detector. The derived characteristics of a single CdTe pixel in section 2.1 lead to understanding of the noise challenges that each detection channel has to meet, in order to approach the Fano limit in the energy resolution. The feasibility has been confirmed in the analysis of the experimental results with the Caterpylar ASIC presented in section 3.5. I have demonstrated that severe power consumption constraints set for the final ASIC, are compliant at the CSA-level with the low noise demands. Excellent spectroscopy results with Caterpylar, where the electronics ENC contribution in $38\ el\ rms$ despite the cathode readout, have confirmed the right direction in the readout chain development. The next goal is to achieve comparable results with a similar detection scheme but in the fully integrated version of a low power ASIC. I will now remind the required features and summarize the experience from the Caterpylar testchip, to show how far progress has been done. Secondly I will point out the remaining challenges to go through during the ASIC design.

4.1.1. Desired functionality and performance

The main requirements for the new readout ASIC have been derived from the target detector type in Chapter I. The pixelated CdTe detector has been chosen to meet the astrophysicists' demands for the future X-rays telescopes. Its characteristics have consequence on the functionality and performance needed in the ASIC.

Parameter	Value / Characteristics
Detector type	Pixelated CdTe array with pixel pitch of $300\ \mu m$
Self-trigger with low detection threshold	Detection threshold $2\ keV$
Dynamic range upper limit	$250\ keV$
Low noise in charge measurement	ENC between $25\ el\ rms$ and $40\ el\ rms$ (for CdTe capacitance in range $0.3\ pF - 1\ pF$)
Multi-channel electronics	Proposed initial size of 16×16 channels with possibility to scale up the array
Position sensing	Event localization in x and y dimensions
Readout channel polarity	Anode readout
Single channel layout area	$300\ \mu m \times 300\ \mu m$
Power consumption	Total of $2\ mW/mm^2$, what corresponds to $180\ \mu W/channel$
Peripheral circuits area	Minimized, because of necessity for the CdTe guard-ring, it is proposed to be a $300\ \mu m$ wide ring around the pixels array
Radiation hardness	Sustainable at high level of Total Ionizing Dose and immune to Single Event effects

Table 4.1 The principal parameters required for the new readout ASIC D^2R_1.

Especially the detector dimensions of fixed size pixels with $300\ \mu m$ pitch impose a strict geometrical specification for the ASIC layout. The consequences are related both to a single channel area as well as to layout space available for the shared peripheral blocks. The exact matching between the ASIC

and the detector is fundamental to create the hybrid module: with stacked assembly between the CdTe matrix and the integrated array of readout circuits. The principal ASIC parameters are listed in Table 4.1.

One parameter that is not directly related to the detector is the power consumption. It is required to be as low as possible, to limit the power dissipation into the system. I have reviewed the existing ASIC solutions – today's applications in the domain of X-ray detection in astrophysics based on CdTe (details of the review in the paragraph 1.2.5). From the reported parameters I have concluded to set the power consumption to $2\ mW/mm^2$ so that the dissipation per detector area would not exceed the reference module: Caliste HD [41] based on the IDeF-X HD ASIC [42] designed for larger CdTe pixel pitch. In case of the new ASIC, designed for stacked assembly with detector – this parameter is equivalent to power consumption per ASIC area.

The overview on the ASIC design parameters from Table 4.1 indicates the key challenges. The main difficulty in the circuit concept is the tradeoff between three parameters: the low power consumption, the ultra-low noise and the limited layout area. I face the task by taking advantage from the promising results already obtained with the Caterpylar testchip to then study the possible architecture of the integrated readout chain.

4.1.2. D^2R_1 foundations based on experience with Caterpylar ASIC

The starting point in development of the new ASIC, the main actor of this chapter, has been established by the promising outcomes from the Caterpylar ASIC presented in Chapter III. That circuit constitutes an intermediate step in creation of the core of the future spectro-imaging camera: the integrated array of readout chains.

4.1.2.1. CSA choice

The Caterpylar testchip includes a set of 26 CSAs of different dimensions and polarities, all optimized for readout of the small pixel CdTe detector. Through systematic measurements and their analysis I have determined the most suitable CSA that should provide excellent ENC results with the proposed detector. I have also found that that no matter which of the considered noise filters would be used, the CSA stays always the same. In consequence for the D^2R_1 ASIC the folded cascode CSA is proposed where the input transistor is a thick oxide PMOS and the overall low noise is consequence of its optimal dimensions of $W/L = 100\ \mu m/0.45\ \mu m$. The CSA is capable to read signal from CdTe with an excellent resolution between $25\ el\ rms$ and $40\ el\ rms$ (depending on the detector capacitance) with power consumption of only $14\ \mu W$.

4.1.2.2. Shaper

For ENC measurements of the CSA integrated in Caterpylar an external shaper has been employed. The experimental results included two types of shapers: the 2^{nd} order semi-Gaussian and the MCDS, both with adjustable peaking time parameters. Both filters participated in two important tests with the testchip:

- Floor ENC measurement with no external capacitance seen by the CSA input ($C_{IN} = 0$)
- Spectroscopy of ^{57}Co source with the Si detector, who represents capacitance $C_{IN} = 0.4\ pF$, similar to the target CdTe detector

In each case the results obtained with both shapers were very similar, showing that both are potential candidates for the on-chip implementation in D^2R_1. The final confirmation was done by calculating the theoretical ENC using extracted noise parameters of the chosen optimal CSA with the input PMOS dimensions of $W/L = 100\ \mu m/0.45\ \mu m$. According to these results both shapers are equally interesting in terms of achievable resolutions in the X-ray energy measurement.

4.1.2.3. Reset circuit

Together with two shapers, the Caterpylar's CSA was tested with two reset circuits. A single PMOS integrated in the CSA stage as a feedback transistor was used in two modes: continuous reset and switched reset. Two entirely different operating modes could be performed on the same structure thanks to the external access to the MOS gate. The two alternative operations are described in the paragraph 3.3.4 more in detail.

The reset mode in the specific measurements has been strictly related with the shaper type used in each setup. The continuous reset was very appropriate in measurements with the semi-Gaussian shaper. This external filter being equipped with adjustable pole-zero cancellation stage provided smooth pulse shape of the output signal. Meanwhile in the tests involving MCDS the same continuous reset was not suitable for the amplitude measurement. Therefore the switched reset was used instead.

I have predicted in the paragraph 2.2.4 that the two reset types, the most suitable for the small pixel CdTe readout are these two circuits: continuous reset and switched reset. In comparison with other commonly used CSA reset circuits, these two single MOS solutions are particularly interesting with respect to the three major aspects in the project: power consumption, layout area and noise.

Justifying from the excellent results with Caterpylar the final choice of the reset mode in the D^2R_1 ASIC only depends now on the shaper type: the continuous reset with semi-Gaussian shaper or the switched reset with MCDS shaper.

4.1.2.4. Technology

Among all of the Caterpylar achievements the most important are the conclusions on the IC technology chosen for the testchip: the CMOS XFAB $0.18\ \mu m$. The ENC measurements obtained with Caterpylar have been compared with corresponding simulations. The outcome has provided evidence of a good correspondence between the MOS transistor SPICE2 thermal noise model and the reality. The significance of this result is even more pronounced with the discrepancy between two noise models accessible in the XFAB process (SPICE2 and BSIM3v3) observed in the subthreshold operation of MOS transistors. Since the power consumption of the new ASIC D^2R_1 should be severely limited, the moderate/deep inversion is a likely operating region of many MOS transistors in the design, also in other blocks than CSA. Choosing the same process XFAB $0.18\ \mu m$ for this new ASIC – all noise simulations can be performed with the SPICE2 model, with high confidence in the noise performance of the final circuit.

The second prerequisite for staying with the XFAB IC technology is the promising result of the dose measurements obtained with the Caterpylar ASIC. Several CSA circuits from the testchip, including the optimal one, have been characterized before and after irradiation of the Total Ionizing Dose of $1\,MRad$. The ENC performance was almost unchanged at the peaking times of interest. Shift in certain parameters related to increase of the parallel noise had only a minor influence on the ASIC functionality.

In consequence of the results obtained with Caterpylar together with the practical advantages pointed out in the paragraph 3.1.1 – I have chosen the same process XFAB $0.18\,\mu m$ for designing the ASIC D^2R_1.

4.1.3. Shaper choice: MCDS vs. semi-Gaussian

In consequence of the Caterpylar experimental results presented in section 3.4 and their analysis in section 3.6, I have concluded to use one of the two possible shapers in the D^2R_1 readout ASIC: semi-Gaussian or MCDS.

4.1.3.1. Semi-Gaussian architecture

As I have already pointed out – the IDeF-X HD ASIC [2], developed in our group, is a reference for the new circuit D^2R_1 in terms of low noise and low power. It uses a semi-Gaussian processing method – therefore, in my consideration over this type of shaper, I use the IDeF-X HD architecture as inspiration. A single channel block-schematic is illustrated in Figure 4.1 [2].

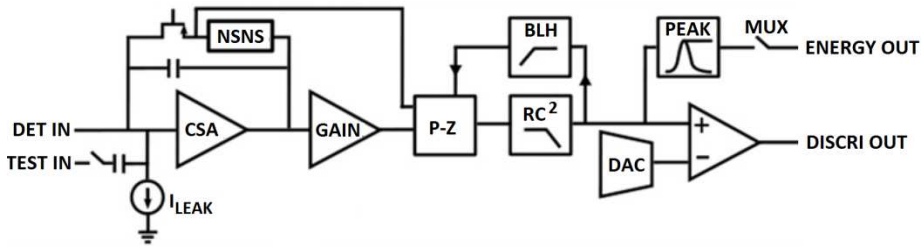


Figure 4.1 The readout channel architecture in the IDeF-X HD ASIC [2]. It is the CSA with continuous reset equipped in Non-stationary noise suppressor (NSNS) and with gain. The first stage is followed by the pole-zero cancellation (P-Z) and the Sallen-Key 2^{nd} order low pass filter. The baseline holder (BLH) keeps baseline at a constant level. Peak detector memorizes the peak amplitude as energy measurement. The event arrival is notified by a discriminator with an adjustable reference (DAC).

It is composed of a CSA with continuous reset equipped with Non-Stationary Noise Suppressor (NSNS), which significantly reduces the noise component variable with the signal amplitude – issue related to the nonlinearity of the MOS transistor relevant to a continuous reset. The pole-zero cancellation stage ensures a rapid return to baseline after each pulse. It constitutes a high-pass filter of the CR-RC^2-equivalent structure. Meanwhile the 2^{nd} order low-pass block is realized with the Sallen-Key topology. The shaped pulse on its output enters two blocks: the peak detector, which stores the maximum signal pulse value and the discriminator, which notifies about the actual arrival of the signal pulse. The low detection threshold of the discriminator is possible as it is placed after

the semi-Gaussian filter, where the signal detection is performed at limited noise power. The result could not be possibly that good if the discriminator was located directly at the CSA output. The overall reference level is controlled by the baseline holder (BLH) block. It is a desirable structure to address the consequences of the pole-zero cancellation (P-Z), stage. The P-Z block sets up a DC path between the CSA output and the RC^2 filter input, where the current equal to a scaled value of the dark current is flowing. The BLH suppresses baseline variation upon long-term fluctuations in the detector dark current (e.g. resulting from change in the operating temperature).

It has been decided to realize D^2R_1 with a different technology than IDeF-X HD (XFAB $0.18\ \mu m$ instead of $0.35\ \mu m$ AMS process used by IDeF-X HD) and scaled-down technology – the similar processing chain would need to be designed for a nearly twice lower supply of $1.8\ V$ rather than $3.3\ V$ in IDeF-X HD. Additionally, with the fact that the power consumption per channel should be over four times lower in the new ASIC to maintain the same power consumption per detector area – the realization of a similar circuit topology becomes a challenge. Furthermore with respect to the reference ASIC: IDeF-X HD, the channel area is now much more limited and the noise contribution of the shaper must be carefully considered to make sure it would be transparent at the ENC level of $25\ el\ rms$. Among the advantages of this solution I should mention: the completely analog character of the CR-RC architecture. The discriminator, which commutes only once per event, is the only block in the channel that brings a risk of parasitic digital disturbance during the signal acquisition. Additionally the fully analog structure makes it very simple to determine the circuit's noise performance. With the validated simulation noise model SPICE2 the processing chain can be optimized, designed and fabricated with a high confidence of the final experimental outcomes to be comparable with the initial simulations.

4.1.3.2. MCDS architecture

Illustrated in Figure 4.2, I propose the architecture for MCDS processing with self-trigger capability. It is composed of a CSA with switched reset. The CSA output voltage enters into two functional structures: the discriminator and the MCDS filter. The filter is realized in two steps. First of all, there are blocks that sample the CSA output and produce two average values: from the baseline samples and from the pulse samples. In the second step – both average values are commuted one-by-one to the CDS block. This circuit produces the final analog output (ENERGY OUT), which is a single voltage level: $V_{AV\ pulse} - V_{AV\ base}$ proportional to energy of the measured X-ray event. The CSA output enters also into the discriminators structure. This circuit comprises two comparators. Each of them is based on the architectures similar to those reported in [4][5]: with the offset cancellation involving the preamplifier stage and with the dynamic latch. A voltage step at the CSA output is detected by one of the comparators and results in the trigger signal pulse. The discriminators work in parallel, however with interleaved phases of control signals (CLK and $\overline{CLK}$ with corresponding delayed latch pulses $\overline{CLK(t+1)}$ and $CLK(t+1)$). This topology means that there is no dead time for detection during the clock period. Despite the fact that the comparators are located directly at the CSA output, the detection threshold can be greatly reduced with their offset cancellation capability which suppresses the low noise components.

What has not been specified in the MCDS channel architecture concept from Figure 4.2 is the control logic. This additional block is necessary to supervise the comparators with appropriate phases. It must also handle the event MCDS processing in response to the discriminator pulse: by commanding

the sampling, the averaging and the CDS operations. One of the smart-control functions of the logic is to ensure a continuous acquisition of the baseline until arrival of X-ray event, to make sure that the average of the most recent k-baseline samples could be produced at any time.

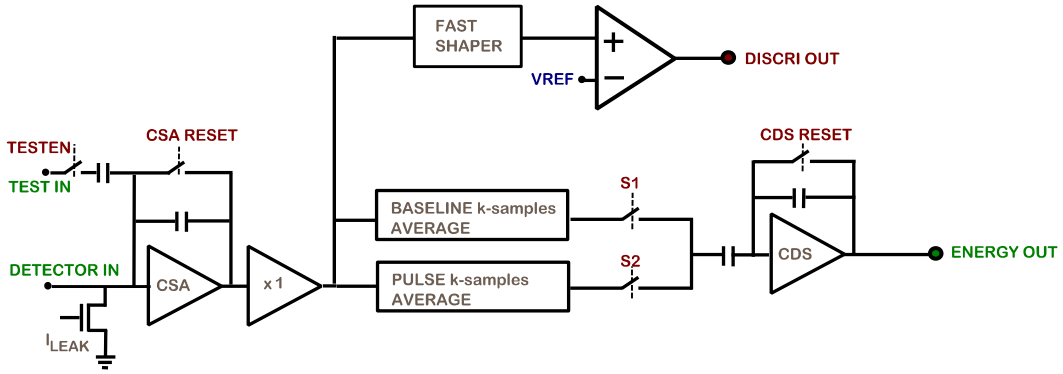


Figure 4.2 Concept of the integrated MCDS processing. It includes a CSA with switched reset, the pulse and baseline sampling blocks that also perform averaging and the CDS amplifier. The pulse discrimination is done by two parallel dynamic comparators, whose interleaved operating phases ensure a continuous detection coverage.

In case of the MCDS architecture a similar difficulty arises as in case of the semi-Gaussian shaper: how to fulfill the low noise requirement at limited voltage headroom. The noise contribution limit that I consider for the shaper is $10\ el\ rms$. Assuming that the MCDS filter would contribute that high additional noise when referred to CSA input, the noise referred to the shaper input should be below $64\ \mu V_{rms}$. This calculation holds when there is no additional gain stage after the CSA and with the CSA closed loop gain $1/C_F$ of $40\ mV/fC$. The low noise requirement imposes challenges at the MCDS block-level design. Especially the CDS amplifier and the output buffer, whose noise bandwidth limits are not reduced by the MCDS processing, would be critical in terms of noise. The second inconvenience of this system is the switching noise of the sampling blocks: it is very difficult to simulate. The effect of the noise averaging and the CDS noise reduction (technique also used by the comparators) would have to be quantified through transient noise simulations, which are extremely time consuming. This leaves the only possibility of a noise estimation from the CSA noise parameters obtained experimentally with the Caterpylar ASIC and the MCDS model calculations demonstrated in the paragraph 2.3.5. Discussing the subject of noise in the circuit, there is one other issue: the sampling blocks dimensioning with respect to thermal noise. The sampling capacitors need a high layout area of $4\ pF$ per cell to make sure that the kT/C noise contribution would be transparent at the ENC level of $25\ el\ rms$. With this requirement the given readout channel layout area becomes tight if the number of cells would have to fulfill possibility of realizing the 16-folded MCDS (highly desirable optimum number according to shapers' summary from the paragraph 3.5.2). One more significant disadvantage of the MCDS circuit in the analog realization is the presence of digital control signals nearly at every stage in the chain. It makes a high risk for the digital noise to appear in the analog signal: through capacitive coupling or through the common substrate. In consequence the transistor-level concept and the layout should be done with exceptional attention to reduce the risk.

The proposed MCDS architecture is new for a self-triggered readout ASIC dedicated to CdTe. Everything that is new puts in question the unexplored risks, although they might be possible to overcome. After assessment of the main difficulties, I would like to highlight the advantages of this solution. The processing scheme is relatively simple and should provide very good linearity. The

output baseline is set only by the CDS amplifier. The control logic interacting with each block requires only few adjustments to enhance the operation in additional processing modes (e.g. with variable number of k-samples) and a full test access. Once the circuit is connected with the detector – it is desirable to adjust the peaking time in search for the optimal ENC. In the MCDS shaper it is an easy parameter to be modified simply by modifying the sampling frequency. Another advantage is seen in terms of its functionality with respect to the detector dark current polarity. In case of a dark current of inverse polarity, the circuit still operates normally. This event is likely to occur in applications of small-pixel detectors: the fraction of dark current originating from the CdTe bulk and received by the pixel could be dominated by surface current between pixels. It must be noted though that with the switched reset – the offset calibration is necessary with dark current fluctuations.

4.1.3.3. Comparison of the two solutions

In response to the promising theoretical results obtained with the semi-Gaussian and the MCDS shapers (presented in Chapter III) – I have proposed two channel architectures corresponding to the respective methods: in Figure 4.1 and in Figure 4.2. The main issues as well as advantages have been identified. They are summarized in Table 4.2, in a form of comparison between the two alternative approaches.

With the challenging specification list from Table 4.1 (presented earlier in 4.1.1) my confidence to enter the design phase has not been fully satisfied with any of the structures. There are certain risks that could become an issue at the block-level concept, appear not feasible at the layout level, or would only pop up in the measurements. In terms of layout the highest concern is the surface budget needed for large capacitances. In case of the semi-Gaussian the large capacitance in order of few tens of picofarads is required for ability of high peaking time, desirable to minimize ENC in the likely case of the detector dark current being lower than the pessimistically predicted value of $5\ pA$, e.g. at I_{DET} of $0.5\ pA$ the optimal peaking time is above $30\ \mu s$. In case of MCDS at least 32 sampling cells would be required for the 16-folded processing, which would mean the total in-channel capacitance of over $128\ pF$ for negligible kT/C noise contribution. In both cases the layout area required for capacitances can be saved using the T-MIM option (Triple Metal-Insulator-Metal) offered in the XFAB $0.18\ \mu m$ process. It permits use of high stability capacitances integrated in small surfaces of up to few $fF/\mu m^2$. In case of MCDS there is the second aid to spare the layout area: through the possible re-organization of its architecture, where a k-folded processing could be achieved with only $k+1$ sampling cells. With this concept (presented in the next section 4.2) I could afford to fit the 16-folded MCDS in the given layout area. The total required capacitance of $70\ pF$ is expected to cover surface of nearly 30% of the space available for a single channel (it is seen in the final pixel layout illustrated in Figure 4.22).

A second possible improvement in MCDS, this time in terms of noise, is the possibility of increasing the output dynamic range without significant losses in the power consumption. Let me explain the concept with reference back to Figure 4.2. The most critical blocks in the given topology in terms of noise – are the last two: the CDS amplifier and the shared output buffer (not indicated in the illustration Figure 4.2). They both have broad noise bandwidths, not influenced by the MCDS processing. Increase in the supply voltage at these last two stages from $1.8\ V$ to $3.3\ V$ enables to implement a gain of $\times 4$ in the CDS amplifier, making its noise and the output buffer's noise to be less significant contributions to the total channel noise. This strategy is possible in the chosen IC

process with thick oxide transistors that support the $3.3\,V$ supply, like for example the low-noise PMOS chosen to be the CSA input transistor. All blocks before the CDS amplifier (including CSA) can carry on operation in the $1.8\,V$ domain, to ensure low power dissipation. In case of the semi-Gaussian architecture from Figure 4.1 – the additional power supply is not recommended for the following reason. The noise advantage could be realistically achieved with a higher power supply in the low-pass filter CR^2 by increasing gain of that stage. Consequently also the BLH, the discriminator, the peak detector and the common output buffer (not indicated in Figure 4.1) would have to be operated at $3.3\,V$. This would lead to even 2-fold increase in the total power consumption, which is unacceptable. In this case the advantage of using the $1.8\,V$ process would be lost.

Functional issues in the detection chain	Semi-Gaussian	MCDS	Comments
Control logic	+	–	In MCDS it is a large and complex digital block; in semi-Gaussian it is a fairly simple logic
Peaking time control	–	+	Semi-Gaussian requires variable capacitance adjustment; in MCDS it is enough to modify sampling frequency
Total capacitance area	–	–	In semi-Gaussian: to achieve high peaking time; in MCDS to reduce the kT/C noise
Inversed dark current polarity	–	+	Semi-Gaussian would not work at this condition – it requires additional compensation current adding parallel noise; for MCDS it is of no consequence but it needs a regular offset calibration in any case
Noise simulations	+	–	The switching noise in MCDS takes too long to predict it with transient noise simulation – the estimation must be done with other means; in the analog semi-Gaussian the typical AC noise analysis is possible, it is rapid and accurate (with the indicated noise model)
Risk of digital noise	+	–	Semi-Gaussian is purely analog with the only digital signal from discriminator; MCDS based on commuted capacitances requires extreme attention to prevent coupling to sensitive nets
Power consumption	–	+	Because of the higher number of functional blocks the semi-Gaussian option might require a higher power consumption, especially if realized as 4^{th} order CR-RC shaper

Table 4.2 Comparison of two channel architectures: with semi-Gaussian and with MCDS shaper.

Considering the discussed issues of the two proposed architectures I have decided to carry on design of the new ASIC D^2R_1 with the MCDS processing approach. Detailed examination has shown that together with the suggested improvements of the compact sampling block with $k+1$ sampling cells and with the additional gain in the CDS stage imposing the second power domain at the channel output – the MCDS architecture is feasible fulfilling the set of requirements listed in Table 4.1. The most difficult subject to face is the noise estimation in the switched capacitors topology.

4.2. ASIC design

The D^2R_1 circuit contains 256 identical readout channels. They are arranged in 16×16 array to precisely match the CdTe detector of identical dimensions in a stacked assembly. The design is discussed in two parts: at the pixel level and at the top level. First of all the process of the signal detection and the MCDS measurement is detailed at the lower hierarchy level. I also explain the whole procedure of X-ray event handling through chronograms of the strategic control signals. Secondly the ASIC is described in the global view of the top-level architecture. This description is especially interesting from the system point of view, before passing to the next section (4.3) dedicated to the experimental results. The ASIC design is concluded with a description of the final layout arrangements: at the pixel and at the top level.

4.2.1. Pixel level

A single pixel in the D^2R_1 architecture is an electronic unit containing a complete detection chain. Measurement of the input charge signal is realized with MCDS processing, implemented in analog circuitry. In typical operations the measurement outcome is a single analog voltage level with value proportional to the signal amplitude. Through individual descriptions of each processing block separately, I will explain the functionality and the overall performance of the readout channel.

4.2.1.1. Top-down description of the pixel architecture

The block-level diagram with the readout channel topology is illustrated in Figure 4.3. It consists of analog and digital parts. The analog blocks include the CSA with switched reset followed by the unity gain buffer. Its output is routed to two architectural units: shaper and discriminator. The MCDS shaper is realized in two steps: with the set of 17 parallel sampling cells connected through a unity gain buffer to the CDS amplifier input. The discriminator is composed of two dynamic comparators, which continuously compare the CSA output signal with the reference level adjustable in each comparator with individual DACs. Their interleaved control phases ensure continuous detection coverage in case of arrival of the signal step at the CSA output. The last of the analog block is the multiplexer, where the output to be observed can be chosen:

- CDS output – in the normal mode
- CSA output or the sampling block output – in the special operating modes

The digital section also implemented within the individual channel includes: the control logic and the slow control. The control logic continuously supervises the channel operation by commanding signals to: discriminators, sampling circuit, CDS amplifier and multiplexer. Meanwhile the slow control block typically remains static during the signal acquisition. Its purpose is to communicate with external link the programmable settings, specific to the pixel. For example desired values of the discriminators' DACs can be written and memorized in this block.

Let's now review the channel functionality step-by-step.

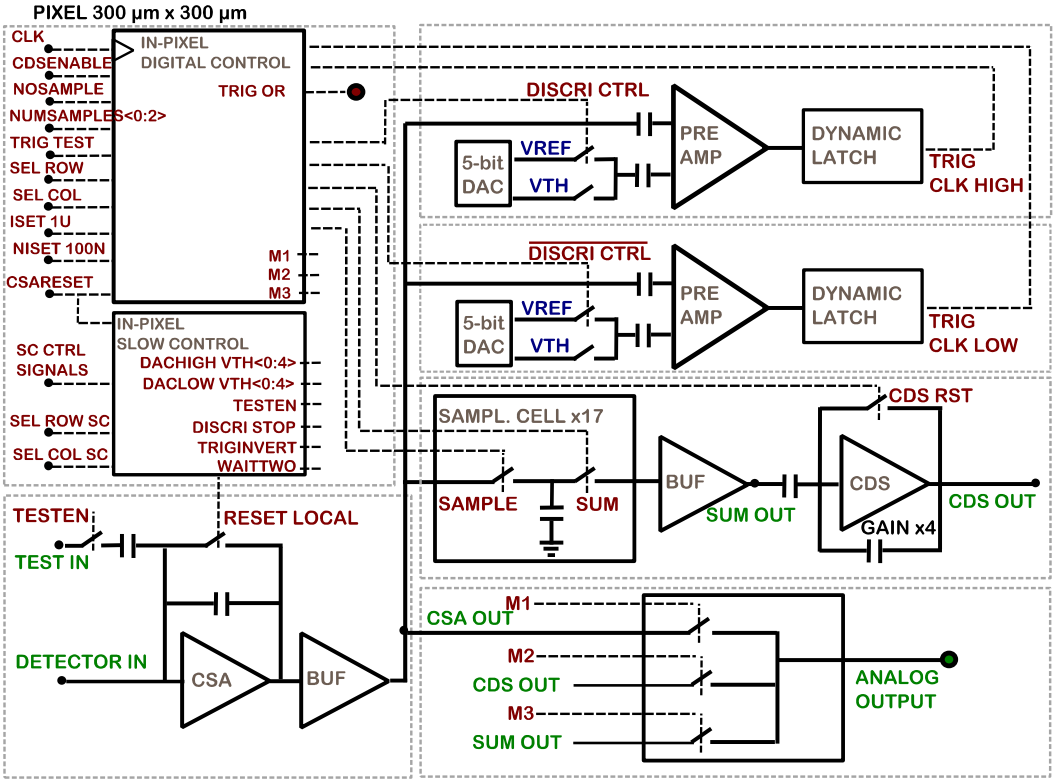


Figure 4.3 Illustration of the readout channel architecture on the block-level. The pixel includes: a CSA with switched reset, followed by a unity gain buffer, MCDS shaper with 17 parallel sampling cells and CDS amplifier, output multiplexer, two discriminators operating in interleaved phases each with individually adjustable threshold, digital control logic block and digital slow control block.

CSA

The first detection stage of the D^2R_1 readout chain has been carefully chosen through measurements of the IDeF-X Caterpylar testchip (Chapter III). The CSA is a single-ended input amplifier with switched reset, input current compensation transistor and two capacitances: the feedback capacitance and the test injection capacitance, both set to $25\,fF$. At the CSA output there is a unity gain buffer. It is needed to provide a sufficient driving speed for the sampling cells in the next stage.

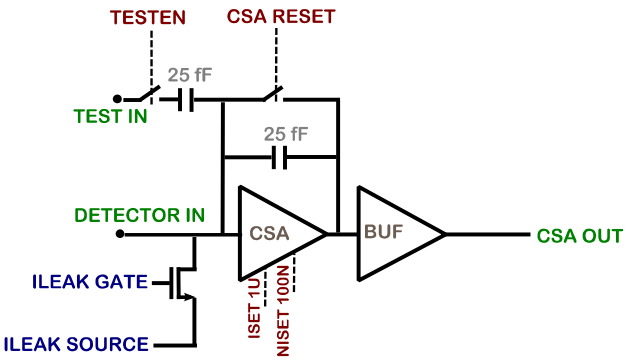


Figure 4.4 Schematic of the CSA in the D^2R_1 detection chain.

The CSA general structure is shown in Figure 4.4, while Figure 4.5 illustrates the internal topology of the amplifier. It has a thick oxide (for up to $3.6\,V$) PMOS input transistor with $W = 100\,\mu m$ and $L = 0.45\,\mu m$. These are the optimal dimensions, which permit to achieve the lowest ENC with the

MCDS processing at the input capacitance between $0.3\,pF$ and $1\,pF$. This is the capacitance expected for the small pixel ($300\,\mu m \times 300\,\mu m$) CdTe detector including margin for the stray capacitance incertitude.

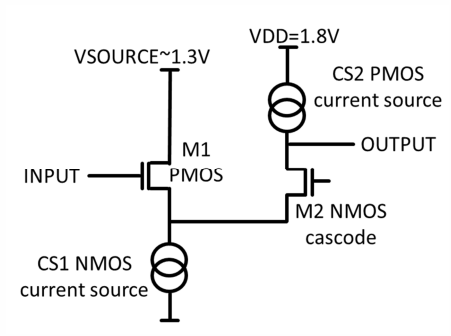


Figure 4.5 Internal structure of the CSA block from Figure 4.4. It is a PMOS-based single-ended input folded cascode amplifier.

The amplifier from Figure 4.5 has two current sources: the input transistor bias adjustable between $4\,\mu A$ and $20\,\mu A$ and the output stage bias, which can be set between $100\,nA$ and $800\,nA$. The choice of the input transistor current enables to find an optimum between the power consumption and noise. The second current source decides about the CSA dynamic characteristics: higher current means faster rise time and also wider bandwidth. With the nominal supply voltages indicated in the schematic (Figure 4.5) the CSA power consumption is between $5.5\,\mu W$ and $27.5\,\mu W$, depending on the current settings. The buffered CSA output signal is then routed to two core blocks of the detection and measurement system: the discriminators and the MCDS shaper.

Signal discriminators

There are two parallel discriminators in each D^2R_1 readout pixel. Both have exactly the same structure, but interleaved phases: one is controlled with CLK signal, the other with $\overline{CLK}$. Each discriminator performs double sampling of the buffered CSA output voltage and then comparison at a specific clock edge. Two discriminators are used in order to cover a continuous monitoring of the CSA output, to be able to detect a step signal at any time.

Each of them has a fully-differential structure of dynamic comparator, equipped with double preamplifier and dynamic latch. The general topology illustrated in Figure 4.6 is inspired with the low offset comparators reported in [4] and [5]. The signals that are compared by the circuit are:

- CSA output voltage variation between two control phases: $(V_{CSA\ OUT\ @\ PH2} - V_{CSA\ OUT\ @\ PH1})$
- Amplitude between the reference voltages: $(V_{TH} - V_{REF})$, which is adjustable individually in each discriminator in range between: $-15\,mV$ and $+15\,mV$, with a 5-bit DAC.

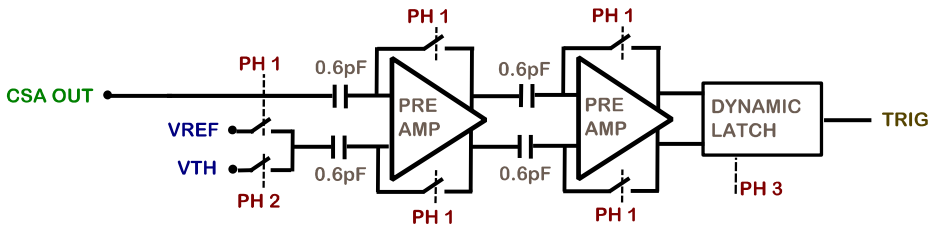


Figure 4.6 Block diagram of a single discriminator in the D²R₁ readout channel. Each channel contains two identical discriminators, operating with interleaved clock phases.

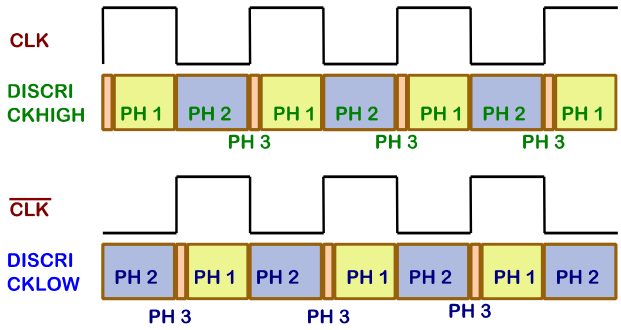


Figure 4.7 Chronogram of control phases of two parallel discriminators of D²R₁ readout channel. One supervised by the CLK signal and one by the $\overline{CLK}$ signal.

The CSA output is recorded twice at the discriminator's input: $V_{CSA\,OUT\,@\,PH1}$ in the phase $PH1$ (offset storage) and $V_{CSA\,OUT\,@\,at\,PH2}$ in the phase $PH2$ (sampling mode). Simultaneously in the phase $PH1$ the voltage V_{REF} is stored to set the reference level and in the phase $PH2$ the voltage V_{TH} is sampled to memorize the desired threshold. Double preamplifier before the dynamic latch circuit amplifies the difference between the two signals of interests. Despite an additional current consumption of 4 μA, I have decided to use a double preamplifier instead of a single one, to achieve high gain of the compared voltages. In consequence, the influence of the discriminator's intrinsic noise on the detection threshold is minimized. In the third very short phase PH3, with duration of about $30\,ns$, the final comparison of the amplitudes: $(V_{CSA\,OUT\,@\,PH2} - V_{CSA\,OUT\,@\,PH1})$ and $(V_{TH} - V_{REF})$ is done by the dynamic latch. In order to minimize coupling from the in-pixel discriminator trigger to nearby sensitive analog nets – the CMOS level has been converted to a current mode signal, not shown in Figure 4.6. In Figure 4.7 the respective control phases $PH1$, $PH2$ and $PH3$ are illustrated as a chronogram of two parallel discriminators: controlled with CLK and $\overline{CLK}$ signals. It also illustrates the detection coverage over the whole clock period.

Two possible signal detection scenarios are illustrated in Figure 4.8 and Figure 4.9. The difference lies in the X-ray event time arrival t_0 with respect to the clock phase. If the photon arrives as the clock CLK is low, the discriminator controlled the CLK by this signal is already in the phase $PH2$, ready to compare two input signals at the incoming (rising) clock edge. This situation corresponds to Figure 4.8. If, on the contrary, the X-ray event occurs as the clock CLK is high – the second discriminator, controlled by the signal $\overline{CLK}$ would trigger, as illustrated in Figure 4.9. In both cases the discriminator output signal $TRIG\ DISCRI$ duration is equal to one clock cycle. In case of high energy events arriving at the transition between two clock cycles – it could occur that both discriminators trigger.

The discriminator design is the first case, where I have met the difficulty related to noise calculation. With the switched capacitors circuits, the AC noise simulation cannot be performed. Circuit simulators offer transient noise analysis option, however as soon as there are few transistors in the

considered schematic, the computing time becomes too long. However the noise estimation was necessary to estimate the expected detection threshold of D^2R_1. Two contributors to this key parameter are: the CSA noise (discussed in the paragraph 2.2.6) and the discriminator intrinsic noise. Let's consider these noise PSDs referred to the CSA output (that is: to discriminator input). Both noise contributors experience the low noise reduction through CDS performed by the comparator. Within the discriminator structure from Figure 4.6 the first differential preamplifier dominates the total noise (the noise of the second amplifier and of the dynamic latch is divided by gain of two preamplifier). I have determined that the first preamplifier has a noise of $110\ \mu V_{rms}$ referred to the CSA output. This elementary calculation is possible through the AC noise analysis. The preamplifier noise is negligible compared to the $900\ \mu V_{rms}$ of the CSA contribution referred to the CSA output.

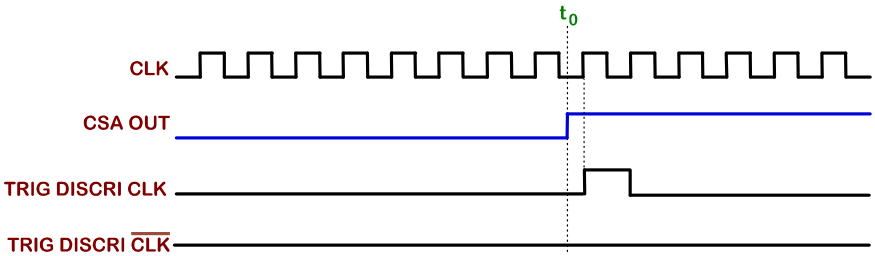


Figure 4.8 Chronogram illustrating a scenario, where the CSA step signal is detected by the first of the two parallel discriminators, controlled by CLK.

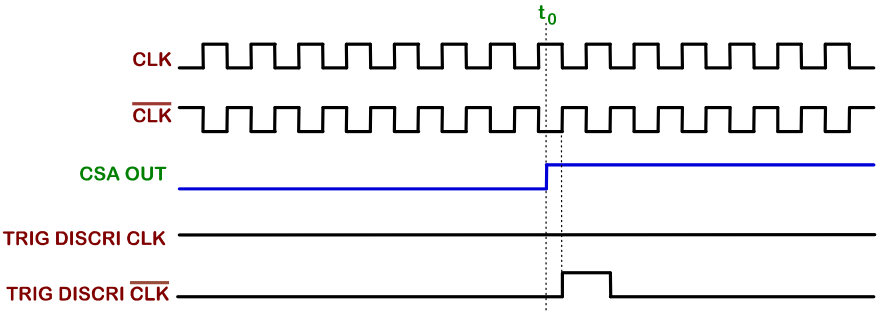


Figure 4.9 Chronogram illustrating a scenario, where the CSA step signal is detected by the second of the two parallel discriminators, controlled by $\overline{CLK}$.

I have performed measurements on a very similar CSA amplifier integrated on the Caterpylar ASIC, with the only difference that its input transistor length is $0.55\ \mu m$ instead of $0.45\ \mu m$ (according to results from the paragraph 3.4.4 the two CSA: T10 and T11 yield almost identical ENC results). The CSA had an external capacitance of $2\ pF$ connected to its input pad. The following measurement has been: CDS processing at different frequencies. This is the same operation that the D^2R_1 discriminator does. The resulting noise referred to the channel input expressed in ENC was between $115\ el\ rms$ and $130\ el\ rms$. This should correspond to an energy detection threshold lower than of $3.1\ keV$ - $3.5\ keV$, calculated for 6-sigma. That is the level where there is only 0.00034% chance of false event detection with an input capacitance level twice higher than the one foreseen in the target application. Through CDS processing, most of the low frequency noise has been attenuated – the thermal noise dominates the result. This noise contribution is directly proportional to the CSA input capacitance. Since the input capacitance used in the experiment is twice higher than the maximum predicted with the CdTe detector ($0.3\ pF$ - $1\ pF$), I expect the detection threshold of the D^2R_1 ASIC to be twice smaller than the measured results.

MCDS shaper, part 1: sampling and averaging block

The MCDS shaper consists of two parts: the sampling block capable of averaging a certain number of stored samples and the CDS amplifier. The sampling block is illustrated in Figure 4.10. It contains 17 parallel sampling cells. The number of cells used in the M-CDS processing depends on the number of MCDS samples k and can be adjusted to comply with the 1-, 2-, 4-, 8- or 16-folded MCDS. The number of cells that participate in the respective variants equals to $k + 1$. Each cell contains a $4\ pF$ Triple-MIM capacitance and two switches: sampling and averaging. The capacitance value has been chosen to minimize the kT/C contribution to the total channel noise. The sampling is performed during half of a clock period. At each clock period a different sampling cell is commuted to the CSA output, commanded by the signals $SAMPLE_1$ .. $SAMPLE_{17}$.

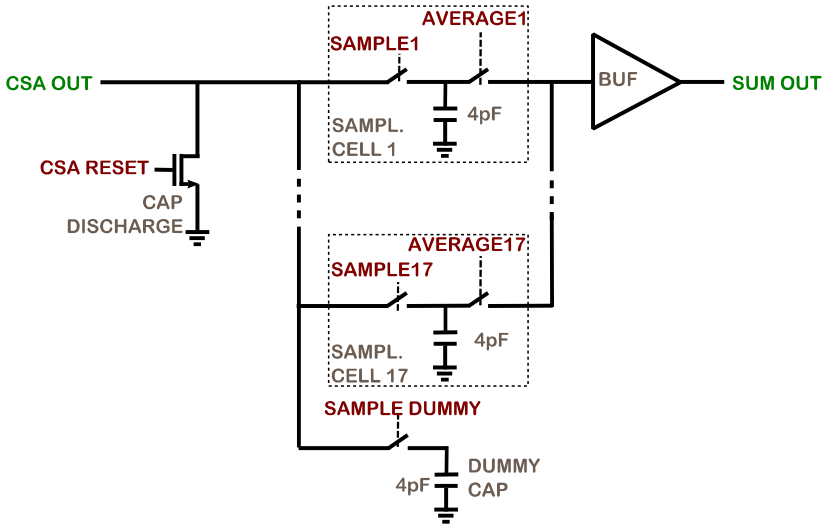


Figure 4.10 Sampling block composed of 17 *parallel cells. It is the first part of the MCDS shaper in the* D^2R_1 *ASIC.*

Every time during the remaining non-sampling half of the clock period the dummy capacitor is commuted to the CSA output. It ensures stability of the unity gain buffer in the CSA stage. The dummy is realized as $4\ pF$ PMOS oxide capacitance. In the designed circuit the averaging is done by summing charge of k capacitors, this action is controlled with the $AVERAGE_1$ .. $AVERAGE_{17}$ signals. With the presented scheme a great care must be taken to minimize the parasitic capacitance in the summing node common to all averaged cells. For this reason I have included the unity gain buffer in the discussed block. The output signal $SUM\ OUT$ is still in the $1.8\ V$ domain.

There are two modes of operation that the block can perform. The first is the principal one, used for the MCDS processing in the D^2R_1 detection chain. In this mode the output of the circuit are two consecutive voltage values of the averaged CSA output. They arrive in sequence: first – the average of the CSA baseline samples and then – the average of CSA step signal samples. The first average is produced upon trigger from one of the discriminators informing about X-ray event arrival. It is composed of the last k-samples before the trigger. The averaged voltage is maintained at the sampling block output for one clock cycle. In the meantime the acquisition continues with the free sampling cell: $k + 1$. Once the first average is released, the sampling of the CSA output signal pulse is carried on for another $k - 1$ clock cycles. It is concluded by the second average produced at the sampling block output. Figure 4.11 illustrates the process of CSA output sampling and the result of

average voltage produced at the $SUM\ OUT$ output. The example shows the case of 4-folded MCDS, where 5 samples take part in the acquisition.

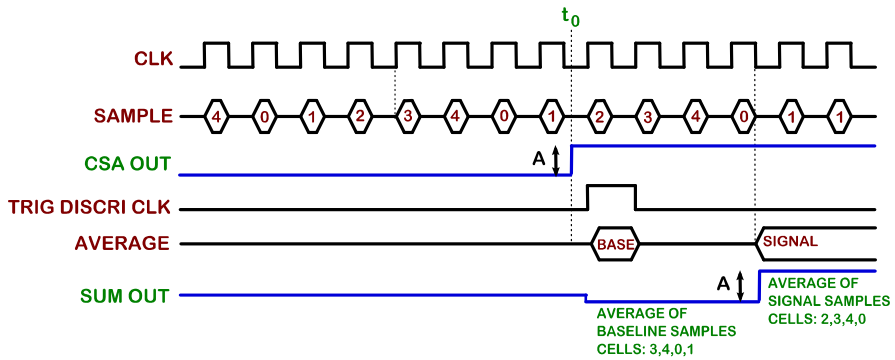


Figure 4.11 Chronogram of the sampling block principal operation. It performs sampling of the CSA output. As the discriminator signalizes the event arrival, the first average of four CSA baseline samples is produced and maintained for one clock cycle. Meanwhile CSA output sampling continues to collect the step-signal samples. Once this is done – the second average of the signal samples is produced at the output. The example involves 5 cells used for 4-folded MCDS. The sampling block operation can be extended up to 17 cells for 16-folded MCDS.

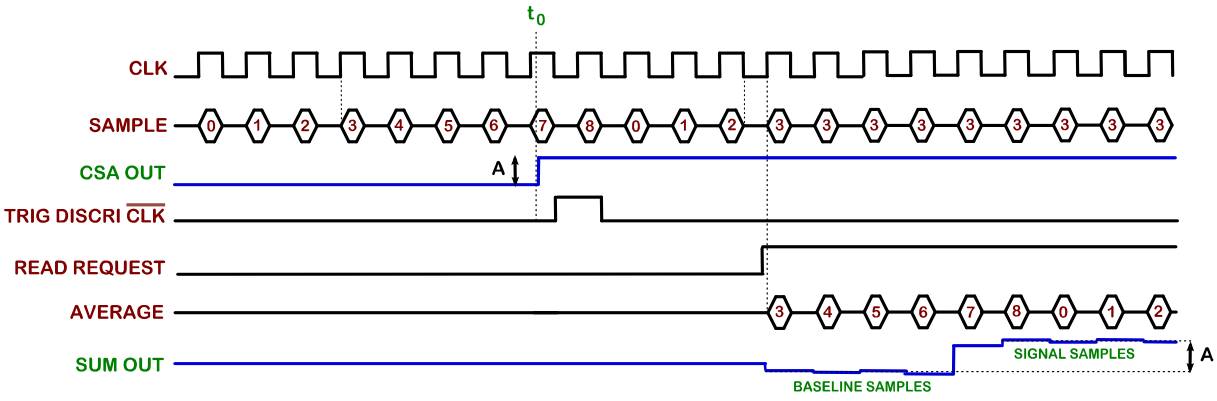


Figure 4.12 Chronogram of the sampling block second operating mode, where the acquired CSA samples are transmitted to the output. The transmission occurs upon the READ REQUEST signal. The samples can be read out by an external ADC and used for off-line MCDS processing. This operation mode has been developed mainly for test access into the readout channel. In the shown example, 9 cells participate in the sampling operation, they can be used to perform off-line the 4-folded MCDS. The sampling block operation can be extended up to 17 cells for an externally realized 8-folded MCDS.

The second operating mode enables to read all the acquired samples individually at the D^2R_1 ASIC output. It constitutes an alternative test mode. This option enables the MCDS processing to be performed off-line, for example in order to compare it with the integrated MCDS realized on-chip. The reference event for the ASIC is again the discriminator trigger. The $k/2$ samples before the trigger contain the information about the CSA baseline. All the remaining ones store the sampled CSA signal pulse level. Since k is in range from 1 to 16 – the total number of output samples is between 3 and 17. The maximum number is limited by the size of the sampling block containing 17 cells. In consequence when performing the off-chip MCDS the maximum size of 8-folded processing can be realized.

The samples are read upon the external signal $READ\ REQUEST$. In case that the CSA rising edge due to event arrival would occur during the sampling interval, when CLK is high, the sample is still kept. Knowing which of the two discriminators has triggered such an event can be recognized and the unwanted sample can be erased, leaving the remaining k samples for the amplitude calculation. This

discriminator information is available to the external user. In case of the previously discussed operating mode of the sampling block from Figure 4.11, used for the in-channel MCDS processing – the channel automatically recognizes the unwanted sample of the CSA rising edge and repeats sampling with the same cell one clock period later. This function is illustrated in the chronogram of the complete pixel illustrated in Figure 4.18.

MCDS shaper, part 2: Correlated Double Sampling block

The second part of the D^2R_1 MCDS shaper is the CDS block, illustrated in Figure 4.13. This switched-capacitor circuit contains: an amplifier with a serial capacitance at the input, feedback capacitance and feedback switch. Similar to the CSA stage – it is based on a single-ended input amplifier. This reduces the noise by a factor of $\sqrt{2}$ and also reduces the current consumption by a factor of 2, when compared to a differential solution. The internal topology is very similar to the CSA amplifier from Figure 4.5, however the supply voltages of the input transistor and in the output stage are set to $3.3\ V$. The CDS block capacitances ratio is set to $4{:}\,1$. This results in voltage amplification $\times\ 4$ in this stage. It is also the main reason for the increased supply voltage of $3.3\ V$ with respect to the previous stages supplied with $1.8\ V$. Thanks to the gain increase, the noise of the CDS block has negligible contribution to the total channel noise. This is especially important since the noise of this wide-band amplifier is not a subject to noise reduction through averaging or CDS processes, what is the case in all the previous stages.

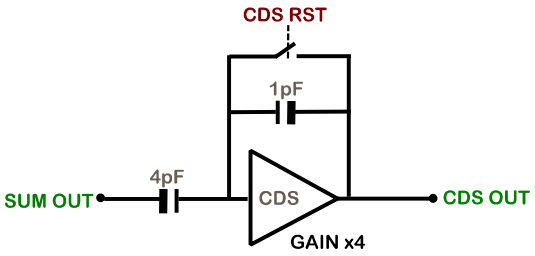


Figure 4.13 CDS amplifier – the second part of the MCDS shaper implemented in each processing chain in the ASIC D^2R_1.

The CDS operation performed by this block is illustrated in Figure 4.14. It receives in sequence two averaged values from the sampling block: CSA baseline level ($BASE$) and CSA signal level ($SIGNAL$). Initially the CDS input and output are shorted with the feedback switch. As the first value of interest $BASE$ is active – the CDS reset is released: $CDS\ RST = 0$. This action establishes the CSA baseline level to be a reference for the AC-coupled CDS block. After a certain time the second averaged value $SIGNAL$ is ready and appears at the CDS input. From now, the CDS output is ready to be measured. The reference for the CDS output voltage $CDS\ OUT$ voltage is the reset level $V_{CDS\ REF}$. It corresponds to the $CDS\ OUT$ output measurement of a zero charge signal at the CSA input. Because CDS is an inverting block, an X-ray event producing a non-zero charge at the CSA input, when read out on $CDS\ OUT$ – the resultant output voltage level is lower than that the reset level $V_{CDS\ REF}$.

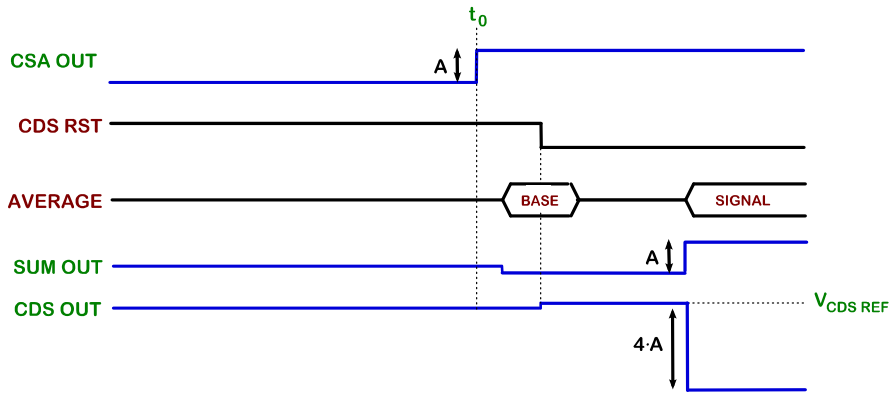


Figure 4.14 Chronogram illustrating operation of the CDS block, the second part of the D^2R_1 MCDS shaper.

Digital sequencing

Two parts of the MCDS shaper have been discussed: the sampling block and the CDS block. They are both based on switched capacitances. To ensure the described functionality – the control signals for the switches must arrive in a specific order. The operation is strictly related to the response of the discriminators and to the external CSA reset signal. The whole process is synchronized with the clock CLK. To supervise the operation of these switched analog circuits – a dedicated digital block is integrated in each detection chain of the D^2R_1 ASIC. It controls the sequence of sampling and the discriminators' phases. When necessary, it is capable to handle the arrival of X-ray event. Finally it also provides the order of the readout sequence, important both on the pixel and on the top level. These functions are supported in four different operating modes of the pixel. All in total makes it to be a cell of a substantial size. The digital control logic block illustrated in Figure 4.15 indicates the strategic input and output signals.

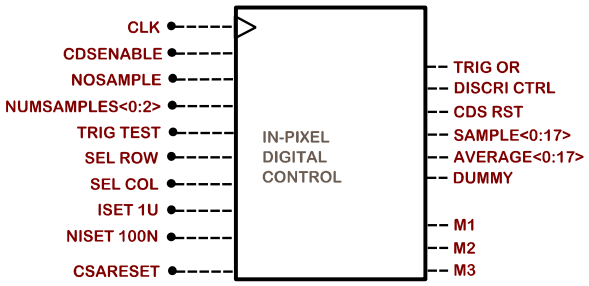


Figure 4.15 In-pixel digital control logic included in each channel of the D^2R_1 ASIC. It manages the dynamic operation of the analog blocks.

Digital slow control

Presence of the sequencing logic discussed above explains how handling of the continuous readout chain functionality is maintained in D^2R_1. However in each pixel there is also a second digital block: Slow Control, where desired settings of the analog circuits can be memorized. It contains a 15-bit register that influences the following functions:

- Adjust individual threshold in each discriminator with a 5-bit DAC
- Disable CSA, e.g. in case of a noisy pixel
- Disable discriminators, e.g. in case of use of an external trigger

- Enable test injection
- Invert the discriminator polarity to detect cathode signals of the detector (in this mode the dynamic range is significantly limited)
- Do not erase the "bad" sample in MCDS processing (with this option the sample $No.1$ of the CSA signal in Figure 4.18 would not be repeated)

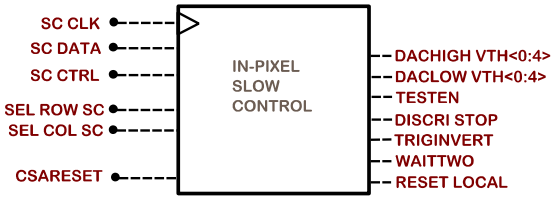


Figure 4.16 In-pixel Slow Control logic included in each channel of the D^2R_1 ASIC. Functionality settings are memorized in it's 15-bit register. The applied settings are individual for each channel.

All these settings can be set separately in each pixel. The Slow Control block is typically programmed through an external interface after the circuit power-up. Once it is set up, the desired registers' values are memorized. However, if necessary, they can be modified. There is a top-level Slow Control block which supervises the In-Pixel Slow Control register. The main Slow Control supervision is common to all readout channels. The access to individual pixel settings is explained in the top-level description of the D^2R_1 ASIC, in the paragraph 4.2.2.

4.2.1.2. Complete pixel functional operation of the MCDS detection chain

The complete diagram of the readout channel is depicted in the introduction to this paragraph (4.2.1) in Figure 4.3. The main blocks composing the analog channel are: the CSA with switched reset, two parallel discriminators with thresholds set by individual 5-bit DACs, 17 sampling cells with averaging switch and the voltage buffer, CDS amplifier with gain $\times 4$ and the output multiplexer. The digital part is split into two blocks: the in-pixel digital control that supervises the operation and the in-pixel Slow Control block where all pixel specific settings can be adjusted individually from pixel to pixel.

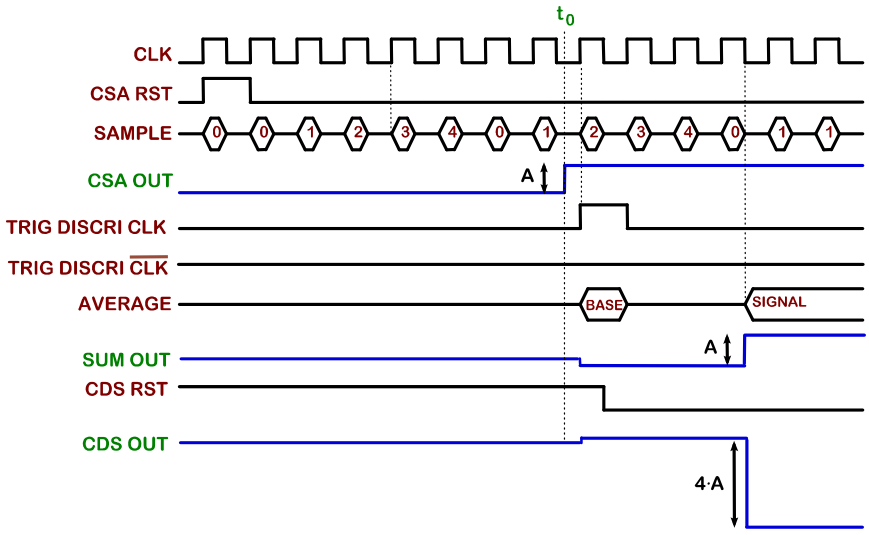


Figure 4.17 Chronogram illustrating the event handling in the D^2R_1 detection chain with 4-folded MCDS. The event arrives as the global clock CLK is low – in result it is the discriminator controlled by the CLK signal that triggers. This fact has influence on the processing sequence (the other possibility is illustrated in Figure 4.18, where the second discriminator triggers).

In the principal operating mode of k-folded MCDS processing, the acquisition sequence is as follows: Once the CSA reset is released – the CDS reset switch is short-circuited ($CDS\ RST = 1$) and the output voltage of the CSA is sampled every clock cycle. The baseline samples are acquired cyclically on the $k + 1$ sampling cells, where k can be set to 1, 2, 4, 8 or 16. The channel is ready to receive signal from detector (or test input) after $k + 1$ clock cycles from the CSA reset occurrence. From this time, the two parallel discriminators are actively awaiting an X-ray event, by monitoring the CSA output. Each discriminator performs CDS of the CSA output, once every clock cycle. The sampling rate is twice higher than the global clock frequency. The discriminator controlled with CLK compares the CSA output at the CLK high level with the CSA output at CLK low level. The comparison takes place at each CLK rising edge. The second discriminator controlled with the inverted clock $\overline{CLK}$ performs discrimination at each CLK falling edge: sampling the CSA output first at CLK low then at CLK high. When an event arrives it is detected at the nearest CLK edge, by one of the discriminators. The processing sequence is simpler in the first case where the event arrives when CLK is low, depicted in Figure 4.17. The illustration shows an example of event processing with 4-folded MCDS. Once the discriminator detects the step signal at the CSA output – the most recently sampled 4 cells are kept as the baseline samples. They are averaged at the CDS input with the corresponding $AVERAGE$ signals, while the 5^{th} "oldest" sampling cell stores the first signal sample. At the end, there will be also 4 signal samples. The baseline average is available for one clock cycle at the $SUM\ OUT$ node (shown in Figure 4.3). In the middle of this period the CDS reset is released. The reference level has been stored. At this time the remaining sampling cells can be reused for the CSA signal sampling. In the particular case from Figure 4.17 it is performed within the $k - 1$ consecutive clock cycles (in this case: 3 cycles). Once all four signal samples are stored, the respective $AVERAGE$ signals are activated producing again an average of the most recent 4 samples at the CDS input (the $SUM\ OUT$ node). The pixel remains in this state, ready for readout. Once the readout request signal is active in the given pixel – the CDS output signal is commuted through the in-pixel multiplexer to the line readout buffer. The value is available to be readout until the CSA reset is performed again. The CSA reset signal serves also as reset for the supervising in-pixel digital control.

The second scenario is when the event arrives during CLK high half-period, as depicted in Figure 4.18, again on the example of 4-folded MCDS. In this case, it is the discriminator controlled by the $\overline{CLK}$ signal that triggers. At this time, the value most recently sampled into the sampling block does not contain the pure baseline voltage but it is corrupted with the signal slope. In this case they are the "oldest" 4 samples that are averaged as the baseline samples. Again, as in the previous case – the average is available for one clock cycle at the $SUM\ OUT$ node and the CDS reset is released in the middle of this period. At the same time the most recent "corrupted" sampling cell repeats the CSA output signal sampling. This time it is certain to store the pure signal value. One clock cycle later – the other sampling cells are available to store additional 3 signal samples. Then the sampling stops and the second average is performed and appears at the CDS amplifier input. The charge is immediately integrated at the CDS output and the final amplitude is available to read out through multiplexer and the line buffer, upon the read request.

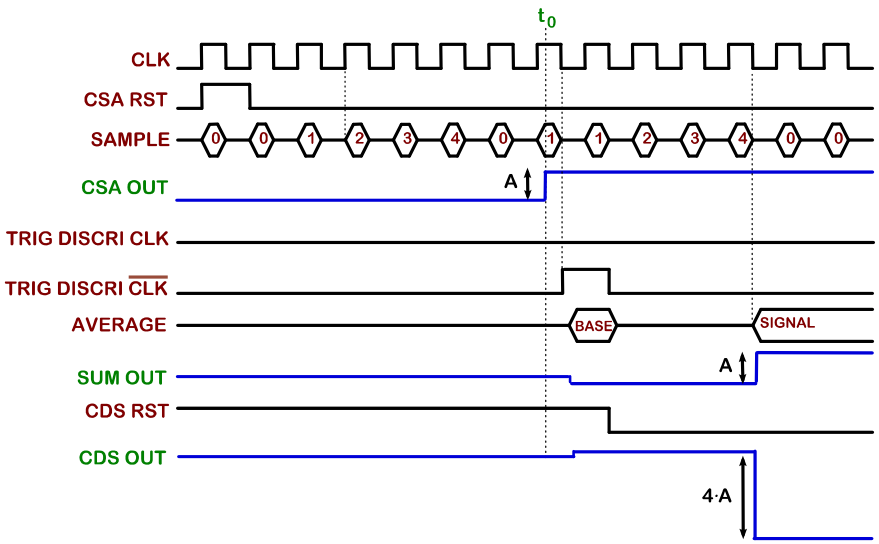


Figure 4.18 Chronogram illustrating event handling in the D²R₁ detection chain with 4-folded MCDS. The event arrives as the global clock CLK is low – in result it is the discriminator controlled by the CLK signal that triggers. This fact has influence on the processing sequence (the other possibility is illustrated in Figure 4.17).

With both presented possible scenarios of the event arrival, detection and processing – the k-folded MCDS can be realized with k set to 1, 2, 4, 8 or 16. In each case the processing scheme is identical, but involves $k + 1$ sampling cells allowing averaging at maximum k-samples simultaneously.

4.2.1.3. Channel power consumption

The described above D²R₁ detection channel was designed with a special care to meet the initially set power dissipation target: below $2\ mW/mm^2$. For a channel with dimensions of $300\ \mu m \times 300\ \mu m$ this means that the maximum power allowed is $180\ \mu W/channel$. Both architecture and the block-level concept were optimized to achieve possibly low power consumption. The summary of the current consumption and voltage supply of the corresponding in-pixel blocks is presented in Table 4.3. The total power dissipated by these in-pixel contributors is $117\ \mu W$.

Block	Current consumption $[\mu A]$	Supply voltage $[V]$	Current compromise
CSA	4 - 20 (adjustable, typ. 10) 0.1 - 0.7 (adjustable, typ. 0.1)	1.3 1.8	Noise Dynamic response
Unity gain buffer BUF (× 2)	6	1.8	Dynamic response
CDS amplifier	11	3.3	Noise Dynamic response
Discriminator DAC (× 2)	1	1.8	Settling time
Discriminator preamplifier (× 4)	4	1.8	Detection threshold Dynamic response
Discriminator dynamic latch (× 2)	$I_{DC} = 0$, peak current $0.4\ mA$	1.8	-
Discriminator CMOS trigger conversion to current mode (× 2)	2	3.3	Not critical
In-pixel digital control logic	$I_{DC} = 0$, peak current $3\ mA$	1.8	-
In-pixel Slow Control	$I_{DC} = 0$	1.8	-
Total DC power consumption: 117 µW			

Table 4.3 Power consumption in a single channel of the D²R₁ ASIC.

In the same list I have indicated the parameters that are compromised with the current consumption. Because the total estimated power per channel is significantly lower than the maximum allowed – therefore one can afford, for example, to increase the adjustable CSA input stage current, expected to have the highest influence on the total ENC. However there are also other blocks outside the pixel that also need to be accounted in this total power budget. Namely these are the shared peripheral blocks on the top level, like the output buffers, digital drivers or current references. The top level ASIC design is discussed in the paragraph 4.2.2. However before moving on to the higher hierarchy, there is one more fundamental subject to discuss at the pixel level: the expected noise at the given power supply level.

4.2.1.4. Channel noise estimation

One of the essential difficulties in design of the presented D^2R_1 readout channel is the noise estimation. The fact that its architecture is based on switched capacitances makes it impossible to perform a noise analysis of a complete readout chain. I have already explained the difficulty in this paragraph (4.2.1) through the issue of the discriminator threshold prediction. In case of that block, the specific experimental results were used, where contribution of the parallel noise with the condition of CDS noise reduction could be neglected. However, in case of the MCDS processing chain – this source of noise cannot be ignored.

Block	Noise referred to the block output $[\mu V\ rms]$	ENC contribution $[el\ rms]$	Noise estimation method
CSA at I_{DET} of 5 pA C_{IN} set to 0.3 pF	-	24	Experimental noise analysis with the Caterpylar ASIC
CSA at I_{DET} of 5 pA C_{IN} set to 1 pF	-	40	Experimental noise analysis with the Caterpylar ASIC
Unity gain buffers	100	-	AC noise simulation. ENC contribution assumed negligible with the MCDS filter in the noise transfer path.
Averaging of k sampling cells kT/C *	$32 \cdot \sqrt{k}/\sqrt{k}$	5	kT/C calculation of sampling cells, noise averaging statistics of k samples
CDS internal amplifier	120	5	Noise simulation through AC analysis, ENC calculations based on channel gain: $4/C_F = 160\ mV/fC$
CDS reset noise kT/C	64	2.5	kT/C calculation of the reset noise, ENC calculations based on channel gain: $4/C_F = 160\ mV/fC$
Total with C_{IN} set to $\mathbf{0.3\ pF}$	-	**25**	
Total with C_{IN} set to $\mathbf{1\ pF}$	-	**41**	

* In the expression kT/C: k symbolizes the Boltzmann constant, otherwise this symbol is reserved for number of samples

Table 4.4 Noise calculation for the 16-folded MCDS processing performed by the D^2R_1 detection chain.

The expected noise of the CSA has been already estimated in the paragraph 3.5.2 with the extracted CSA noise sources and with known MCDS noise parameters obtained numerically. The obtained result of $24\ el\ rms$ at $0.3\ pF$ ($40\ el\ rms$ at $1\ pF$) assumed that the MCDS processing adds no significant noise. This was proved to be true (also in Chapter III) with the external shaper. The question now is: what is its contribution in the described on-chip implementation.

In order to predict ENC of the complete detection chain I have considered each noisy block in the signal path and estimated its contribution to ENC referred to the channel input. There were different calculation methods that I used, sometimes combined together: theoretical noise calculation, block-level AC noise simulation, averaging statistics and deduction. In consequence I have obtained the following results demonstrated in Table 4.4. According to these estimations – the ENC of the 16-folded MCDS processing should not increase more than $1\ el\ rms$ in comparison to the predictions based on the Caterpylar testchip measurements.

It must be noted that the presented noise estimation does not include the signal degradation due to: coupling from digital to sensitive nets, nodes discharge upon leakage currents and channel crosstalk. This secondary noise sources have been minimized through design and layout by introducing: separate analog/digital power nets, shielding, dummy switches and careful dimensioning. These techniques are discussed more in detail in 4.2.3.

4.2.2. Top level

The D^2R_1 ASIC contains an array of identical pixels. Each of them constitutes a complete detection chain. I have already described the architecture of this elementary unit in 4.2.1. In this paragraph I explain how the top-level circuit is organized to manage input control signals and the output readout of these numerous readout channels.

4.2.2.1. General description of the ASIC

The ASIC D^2R_1 can be described in three parts:

- The core with a matrix of 256 pixels
- Digital control logic that handles the discriminators' signals and redistributes the control I/O across the chip
- Top-level unit of the digital Slow Control system

The ASIC operates with two power-supply domains $1.8\ V$ and $3.3\ V$. In order to reduce the overall power consumption the initial part of each readout channel is supplied with $1.8\ V$, as explained in the paragraph 4.2.1. This is where there is a strong tradeoff between the transistor current and the transistor noise. However, the last in-pixel stage and the shared output buffers belong to the $3.3\ V$ domain.

The readout channels are organized in an array of 16×16 pixels. Figure 4.19 shows a diagram with a single line of 16 pixels. Each line has an individual analog output buffer with adjustable gain: $\times 1$ or $\times 4$. Most of the input signals are shared by all pixels in one line. The exceptions are the detector inputs and the column address signals: the readout address and the address to program the in-pixel Slow Control. Concerning the output signals, there is one analog output per line. The single net connects all analog outputs with the common buffer. Each pixel has also two identical trigger output signals from its internal discriminator. The signals are transmitted to the top-level trigger registers in current mode. The current mode not only saves the routing, allowing for only one trigger net per line

and one per column, but also it is a good alternative to noisy CMOS mode that could add lots of disturbance when routed across the chip.

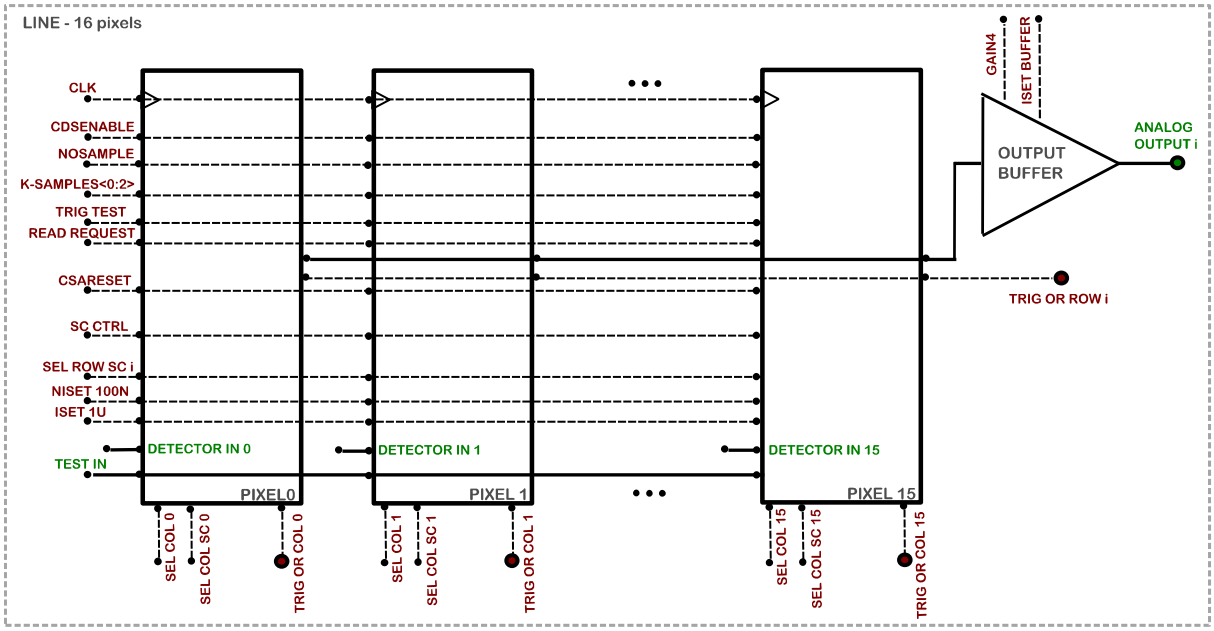


Figure 4.19 Line of 16 pixels in the D^2R_1 ASIC

In case of an event, in order to read out its energy, there is a global external read request input signal that must be selected to activate the output buffers. The ASIC is also equipped with an external 4-bit address input, to indicate the column for readout. This address is demultiplexed to a 16-bit code, one bit per column. A single address bit is common for the corresponding column in all 16 lines therefore, even though there are 16 line buffers, they can read only one column at a time. How do we know that an event occurred in the ASIC and in which pixels? – This is the job of the discrimination network to provide this information to an external user.

4.2.2.2. Event discrimination

The discrimination network is distributed between all the pixels of the readout ASIC D^2R_1. So far I have explained how the trigger signal is generated in a single pixel: by the double-discriminators located in each readout channel. This individual trigger information is collected from pixels across the chip and managed by the top-level circuitry to provide two principal functions:

- It produces the global trigger signal to communicate that a hit event occurred somewhere in the matrix.
- It delivers information of the hit location. The hit location is stored in the column hit register and the line hit register.

To explain how the discrimination system is realized I first move back to its in-pixel origins.

Current mode distribution of the trigger signal

The event discrimination signal inside the pixel results from the comparison of the CSA output analog voltage with the reference. In consequence a CMOS signal is produced, where a one-clock-cycle high-

level pulse indicates the event arrival. The CMOS signal is then converted to two identical current mode signals, which constitute two trigger outputs from the pixel: $TRIG\ OR\ COL$ and $TRIG\ OR\ ROW$.

For pixels arranged in one line the $TRIG\ OR\ COL$ signals are connected in a common net. Similar organization is realized for pixels arranged in one column, this time this are the $TRIG\ OR\ ROW$ current signals that constitute a common net. This topology is illustrated in Figure 4.20. Each row and each column have individual circuits converting the summed current mode signal back to CMOS. Eventual occurrence of the re-converted CMOS trigger pulse results in immediate storage of the value "1" in the corresponding binary register cell.

The peripheral register cells are identified at the top-level as two hit registers: the line hit register and the column hit register. Since there are 16 lines and 16 columns - each of the two hit registers contains 16 memory cells. Both registers can operate as shift registers, consequently the data can be read out with only two serial outputs from the ASIC.

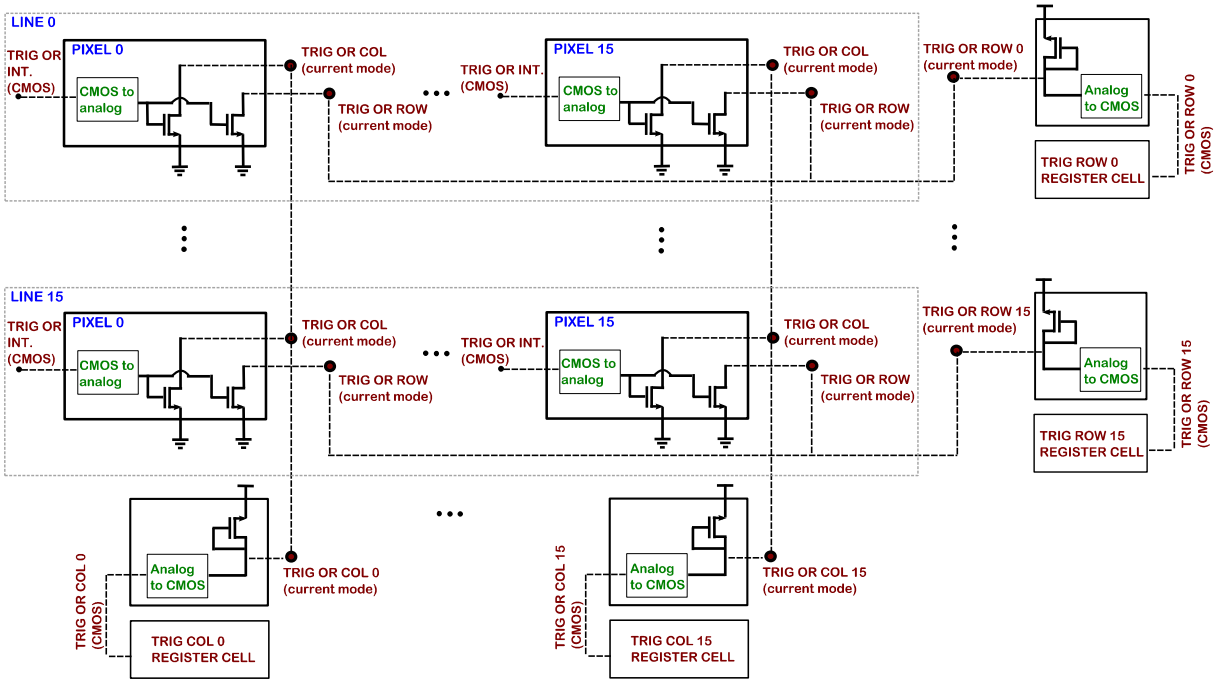


Figure 4.20 Discrimination network: from the pixel level to the top-level CMOS hit-registers. The current mode distribution of the trigger signals across each line and each column is illustrated.

Discriminator global OR and the hit-pixel localization

In addition to two serial outputs for the hit registers readout, there is one more ASIC output related to event discrimination: the 1-bit $Global\ OR$. It is realized with an OR gate that performs the logic operation over all register cells, what is illustrated in Figure 4.21. The trigger signal generated in case of an event by the in-pixel discriminator is a pulse of one clock cycle duration. Therefore pile-up of multiple events can be detected on the global trigger signal when multiple pulses or a single long pulse is observed.

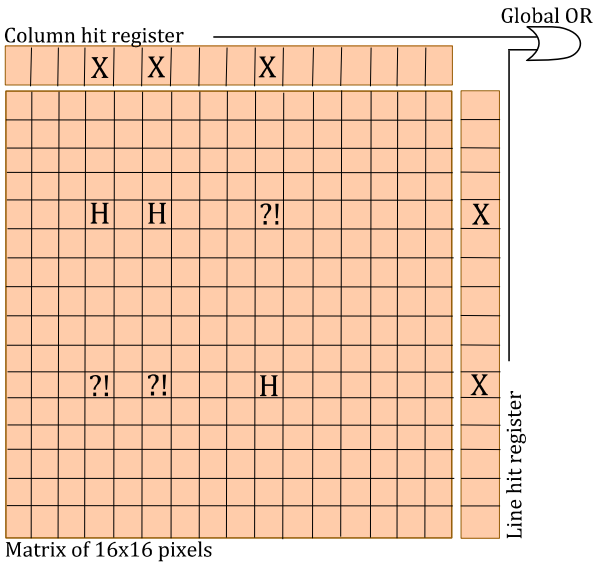


Figure 4.21 Discrimination scheme in the D^2R_1 ASIC. The event location is memorized in the corresponding column hit and line hit registers. Generation of a 1-bit $Global\ OR$ signal to inform about occurrence of an event.

Once a pixel has been hit – the cell in the line hit register that corresponds to the pixel line is tagged. Simultaneously the corresponding cell in the column hit register is tagged. The scheme is depicted in Figure 4.21. The example shows three pixels where a hit event has occurred marked with "H" symbol; two of them are in the common line. In effect there are three cells tagged in the column hit register and two cells in the line hit register with the "X" symbol. In the given example the incertitude of this discrimination scheme is demonstrated. By reading the column and line hit registers – the external user cannot tell unambiguously – which pixels were hit by an X-ray photon. This issue arises every time when two pixels, from different lines and different columns, are hit simultaneously.

Despite the fact that the D^2R_1 ASIC is designed to read out signals from a pixelated detector: with the described above discrimination scheme, there is a similar situation of the position uncertainty as in case of strip detectors. With this architecture, the specific advantage of a precise localization of multiple events by using a pixelated detector is vanished (for details please refer to the paragraph 1.2.3). I have decided to implement the discrimination scheme in the presented form to gain on the system simplicity, layout area and to minimize the power consumption (of the CMOS to current mode and inversed conversions). In the example from Figure 4.21, reading out all six possible hit-locations still permits to determine the event arrival. It is enough to measure the analog output levels of these pixels.

4.2.2.3. LVDS interface

In the D^2R_1 ASIC there are several strategic IO signals that provide an interface between the ASIC control circuitry and the external user and are dedicated to events processing and readout. They include ten inputs: global clock, CSA reset, read request, 4-bit column address, test trigger input, the hit registers enable and the scan clock. There are also three output signals from the ASIC: $Global\ OR$ and two serial hit registers outputs. These digital signals are strictly related with the detection, measurement and readout operations. If they were transmitted through the IO pins in CMOS levels – they could cause interference into sensitive analog nets, especially these at the PCB level, resulting in additional noise. To prevent it – all of the signals are converted to LVDS (Low Voltage Differential

Signaling). This implies presence of high power drivers and receivers at the ASIC level. These blocks are the main source of additional current consumption among all the peripheral circuits. In order to gain flexibility in the power management, the three LVDS output signals' drivers are capable to operate at three different bias current conditions. The most suitable mode can be chosen in the final application. The LVDS drivers are also inefficient in terms of IO pads: for transmission of a single signal – two analog IO pads are required. The price however is worth the robustness of digital signals transmission – almost invisible for the analog part.

4.2.2.4. Common Slow Control block

One more block that should be distinguished in the D^2R_1 ASIC is the top-level Slow Control. The Slow Control is used to apply functional settings to the circuit. It is a set of 6 registers programmed with a serial data input and a dedicated clock. Five of them are common registers located in the top hierarchy and are a part of the peripheral circuit. They contain general settings regarding the ASIC operation:

- Number of samples in MCDS processing
- Operating mode
- Output buffer gain $\times 1$ or $\times 4$
- CSA input transistor bias current
- CSA output stage bias current
- Bias current control for output buffers and LVDS drivers
- Synchronization choice for external trigger and CSA reset input signals
- Selection of channel/channels to program their In-Pixel Slow Control register

The last point is related to the 6^{th} register. That register is distributed, or in other words 256 copies of it exist – one in each pixel. This is the in-pixel Slow Control, which has been already described in the paragraph 4.2.1. Whether the in-pixel register is programmed it is decided with selection of the column and the line of interest in a 32-bits register (16 bits for column and 16 bits for line address). In this way, for example, the DAC thresholds can be set individually in each readout channel by addressing each pixel separately. Alternatively multiple pixels, up to the whole matrix, can be addressed simultaneously to apply identical in-pixel settings.

The overall Slow Control design integrates a dedicated output flag signal for ionizing radiation induced Single Event Upset detection. An identical general architecture has been used in other ASICs developed in our group. Any error due to change in registers' settings caused by ionizing radiation should be notified at the dedicated ASIC output. Consequently actions can be taken to re-program the ASIC providing the desired settings in the experiment.

4.2.2.5. Operating modes

The readout mode is set globally for all pixels by the top level Slow Control unit. There are four modes of operation, all listed in Table 4.5. The first two do not involve sampling. They are available to monitor the internal analog signals: either the CSA unity gain buffer output or the average buffer output where one dedicated sampling cell has always the switches $SAMPLE$ and $AVERAGE$ switched on, all the others sampling cells are disconnected. In result the CSA output signal is

observed having passed through two unity gain buffers. In these modes, the clock does not need to be present, however if applied – discriminators are operating.

Mode	Description
Mode 0	Look at CSA output after average follower (with one memory cell in/out active)
Mode 1	Look directly at CSA buffer output
Mode 2	Sample, perform averaging and CDS, one value out
Mode 3	Sample and all out

Table 4.5 D^2R_1 readout modes.

The other two operating modes in Table 4.5 are sampling modes: the principal mode with MCDS processing and an additional test mode where the CDS amplifier is bypassed and all samples are read out. Consequently this offers an option to perform off-chip MCDS processing when necessary. The outcomes of these two operating modes have been illustrated in Figure 4.11 and Figure 4.12 (in the paragraph 4.2.1), through description of the sampling block. In case of any operating mode the analog voltage signal is available at the line buffer output upon read request. The in-pixel multiplexer (shown in Figure 4.3, in 4.2.1) decodes the operating mode to carry on the requested operation and to ensure that when the pixel is addressed for readout – the right signal is received by the line buffer.

The description of the operating modes concludes the D^2R_1 architecture description showing the desired functionality with the on-chip MCDS processing. With three more operating modes and options programmable with the Slow Control, additional functions are provided, which may be very useful in the circuit characterization. The above discussions in paragraphs 4.2.1 and 4.2.2 included detailed block level description of the circuit topology. However, in the design timescale, the layout involved a comparably large effort. Therefore I dedicate one more paragraph to the ASIC design to discuss the layout-related aspects.

4.2.3. Layout and technological issues

In D^2R_1 – the architecture and dimensioning of each block, at the transistor-level, had to be carefully considered to meet the required layout area. I have also identified possible risks of undesired interactions between nets or blocks. These had a great influence on the final layout of the ASIC. For example the fact of co-existence of two architectural domains: analog and digital imposed limitations in block placement. The considerations were extended from the pixel-level, through line signals arrangement up to the top level placement and routing.

4.2.3.1. Pixel layout

At the pixel level there were three major layout-related challenges:

- Fit the corresponding blocks into the pixel area.
- Deal with simultaneous presence of analog and digital circuits: how to place them to avoid digital noise.

- Placement compatible with the top level line arrangement with main impact on routing of: analog signals, digital signals and power network.

Below I describe the key methods and approaches applied to deal with these issues.

Meeting the layout area

The area for a readout channel in the D^2R_1 ASIC is limited to the pixel size of $300\ \mu m \times 300\ \mu m$. I have recognized early at the design stage that the main limiting factors to achieve this scale of integration are: the capacitances required by analog blocks and the signals and power routing. Especially the number of signals has been gradually growing as the architecture concept reached its maturity.

The chosen XFAB IC technology has certain options which were extremely valuable in the layout task. First of all, I have chosen the 5-metal process with one more additional level of top metal. The basic five metal layers were used at the pixel-level routing. This relatively large number of metal layers added flexibility in routing the numerous signals: several power supply nets, signal paths and inter-pixel and inter-block routing. Figure 4.22 illustrates the complete pixel layout of $300\ \mu m \times 300\ \mu m$.

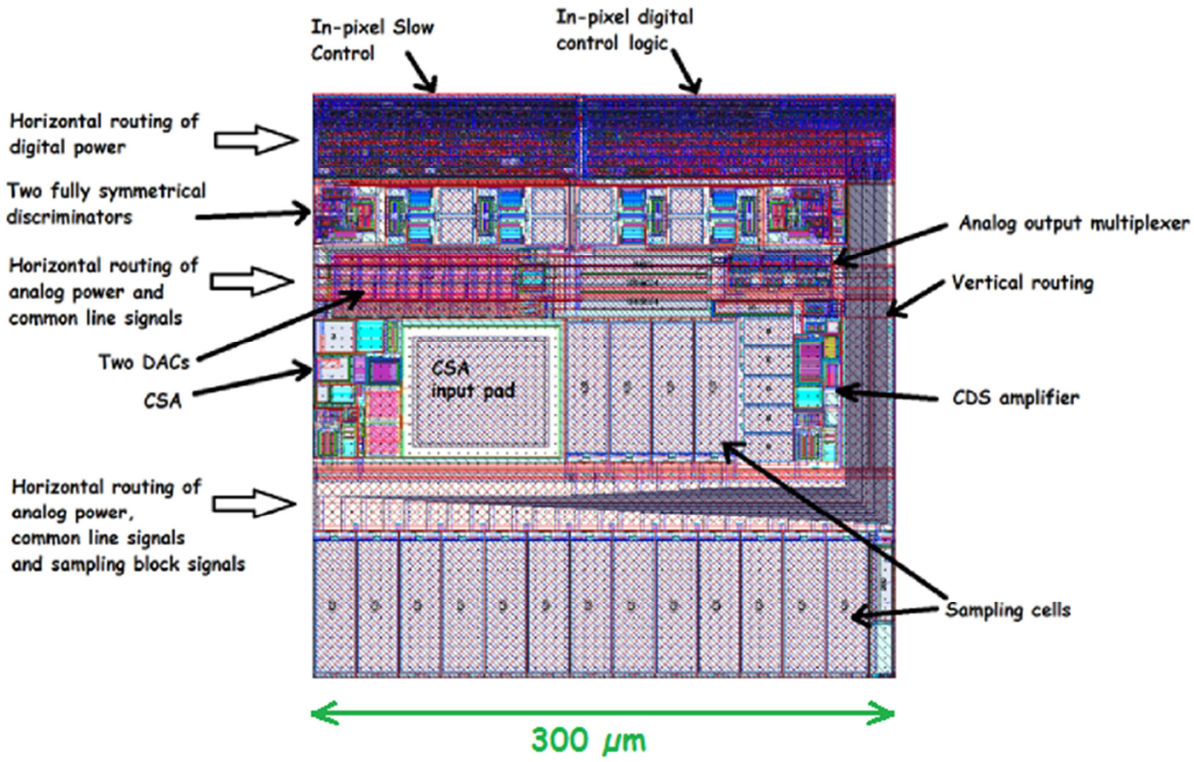


Figure 4.22 Layout of a complete readout channel with up to 16-folded MCDS in a square pixel of $300\ \mu m \times 300\ \mu m$.

Blocks that became a concern in terms of fulfilling the layout area are the two digital blocks: the Slow Control and the event managing control logic. In the course of design I have discovered that the complex digital control is much larger than initially expected. Despite the fact that these two blocks are almost independent – they have been placed next to each other. Their respective internal routing was done by the automatic Place & Route software. Several iterations in the software run were necessary to approach the problem limited in a tiny surface. Finally I have succeeded in fitting the

blocks in the desired area using only two metal layers. Consequently there were three remaining metal layers to include the digital signals and digital power routing right above these two blocks (in the horizontal orientation with respect to Figure 4.22). This arrangement has been especially meaningful in terms of the compatibility in the top-level assembly, the third of discussed pixel-level challenges.

Similar to the digital blocks – I have determined also few analog blocks, where routing could be performed above the active circuitry, namely: the two DACs and the analog output multiplexer. This selection was also strategic in placement. Routing above these particular circuits was not critical: the paths included analog power and the common line signals from the top-level Slow Control, which are essentially static during the signal acquisition and should not disturb operation of these circuits.

In the case of other analog blocks, I could not use the stacked routing approach for two reasons: being concerned about the design parameters accuracy in case of metal passing over the active circuitry and due to presence of structures (detector pad, capacitors) that block up the metal layers. This is a case in: discriminators, sampling cells, CDS amplifier and CSA, which are basically the remaining blocks.

Reducing impact of noisy control logic

The digital control logic inside the pixel is operating continuously throughout the signal acquisition. Therefore it imposes a significant risk of digital noise coupling to the sensitive circuit elements. The two paths through which this disturbance could affect the analog low noise performance are the power supply nets (that includes the substrate) and the parasitic coupling capacitances.

The digital circuits inside the pixel use the $1.8\,V$ supply. It was obvious that this power net as well as the ground power net should be separated from the analog $1.8\,V$ domain. Unluckily for the tight layout space limitations – the $3.3\,V$ power net also needed to be doubled. There is only the CDS block inside the pixel that uses the increased power supply, however its CDS reset switch as well as the output multiplexer switches need $3.3\,V$-supplied level shifters: to adapt the control signals from the digital control $1.8\,V$ domain. In addition, special guard rings have been integrated to reduce parasitic coupling by the substrate.

The second hazard in the mixed-signal readout channel design is the capacitive coupling from the digital signals to sensitive analog circuits and analog signal paths. The primary protections applied in the layout are the grounded shields around analog structures. For example the common output signal routed along the pixel to transmit the measured X-ray energy information is surrounded by metallization. The shield part below the signal of interest and on the sides, is connected to the substrate ground reference, and the part above it constitutes the functional analog power net. Any digital signals crossing this specific sensitive analog path are less likely to move the surrounding low impedance barrier.

Finally, the placement strategy had maybe the major contribution to prevent the unwanted digital noise. The specific arrangement can be recognized in the pixel layout shown in Figure 4.22. Between the digital control logic and the key low noise circuits: CSA, CDS and sampling cells – there is an active separation formed by the discriminators. However they are also likely to contribute noise due to their continuous switching between comparison phases. Therefore the two DACs, directly associated

with the discriminators, but static during signal acquisition, constitute the main space-barrier between the analog and the digital zones.

Placement compatible with top-level line arrangement

In the readout channel layout, shown in Figure 4.22, there is certain systematics that one can distinguish. The signal and power routings are organized in horizontal lines. With this arrangement I have anticipated the top level arrangement into lines of pixels. The common path used for readout of the analog output voltage is routed along the line to the line buffer. Thus the common net links the analog multiplexers of all pixels in a single line. With this planning it is purposeful to lead all the other shared signals and power nets in the same orientation. In result the occurrences of signals' crossings are rare, what is good for the layout simplicity and for saving the layout area. The only signals that are routed vertically are those common for the whole column, that is: the column trigger signal, the column readout address and the column Slow Control address. Let's see how it all fits together at the top level assembly.

4.2.3.2. ASIC top-level layout

The top level layout concerns were quite similar to those listed at the pixel level: mainly layout area and placement for the most appropriate output pads arrangement. In terms of layout area – the achievement of a compact pixel surface was the great part of the success. The 16 readout channels could be placed in one line next to each other without any gap in between them – with a pitch of exactly $300\ \mu m$. Each line has been terminated with an output buffer. In terms of placement the 16 line output buffers belong to the peripheral layout area surrounding the active core of the pixels array.

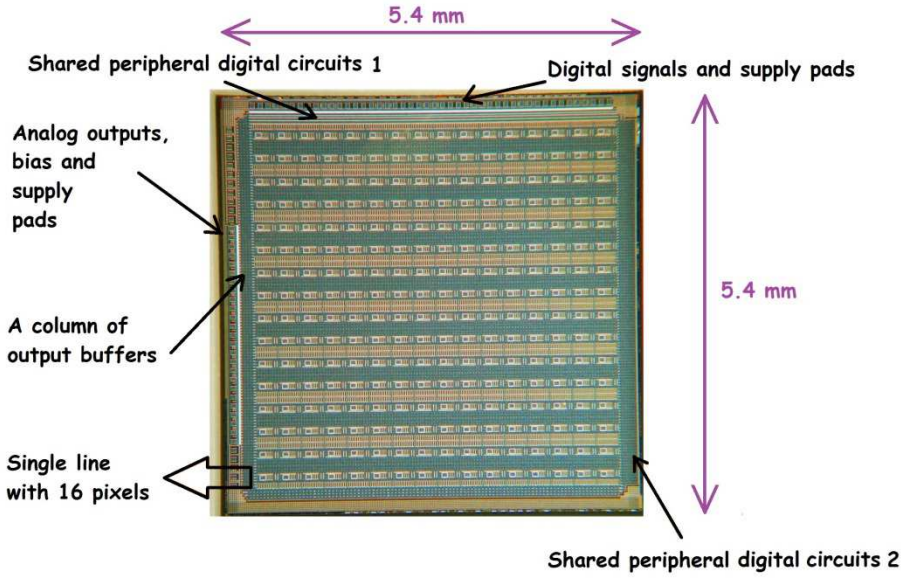


Figure 4.23 Photograph of the D^2R_1 ASIC die and indications of the principal blocks placement. The total active area of the 16×16 pixels array is $4.8\ mm \times 4.8\ mm$ large. There is a peripheral zone $300\ \mu m$ wide surrounding the matrix core, resulting in the ASIC dimensions of $5.4\ mm \times 5.4\ mm$.

To avoid false events related to coupling of digital signals to the detector, the top metal layer has not been used for signals and power routing, but was distributed with maximum possible coverage on the top of the active circuits as a shield. A special care has been taken to cover zones above the

digital blocks. The equipotential sixth metal layer has been supplied with a dedicated analog ground. This important distributed layout element is apparent on the ASIC photograph in Figure 4.23 since it is the top layer below the passivation.

The D^2R_1 ASIC is foreseen to be stacked with the target CdTe: with exact matching between the readout channels and the pixelated detector anodes pitch. According to the discussions in the section 1.2, where the CdTe detector is described – the matrix of electrodes is surrounded by the guard-ring structure to minimize the dark current. The additional dimensions required for guard-ring mean that the ASIC peripheral circuits would not become an unnecessary dead-zone in the final camera module. The most suitable guard-ring size has to be determined through simulations and experiments that are outside the frame of work presented here. However for reference I can refer to the three most recent camera modules developed in our team: Caliste 64 [6], Caliste 256 [7] and Caliste HD [41]. They are all based on pixelated CdTe detectors equipped with guard-rings of respective widths: $900\ \mu m$, $200\ \mu m$ and $20\ \mu m$, surrounding the pixel array. Having these high performance instruments as reference – the fact that I have accomplished the D^2R_1 layout with the peripheral zone of $300\ \mu m$ width seems satisfactory.

The most important in the peripheral circuits' placement was the pads arrangement. Because of their high number, highly increased with the presence of LVDS – they had to be arranged along two sides of the ASIC. The position of the output line buffers along the left hand side border – made it a natural choice to locate the analog output pads for energy readout in direct proximity. Consequently I placed along the same edge all the other pads related to the analog domain: analog power supplies, bias voltages and the CSA test voltage injection. The digital domain pads occupy the top border of the ASIC. Consistently all the digital peripheral cells, that is: Slow Control, drivers for internal signals, LVDS cells and hit registers with associated circuitry – are located within the top and the right zones of the peripheral ring.

The complete D^2R_1 ASIC layout is demonstrated in Figure 4.23. The multi-channel readout circuit with the initial functionality list from Table 4.1 (in paragraph 4.1.1) has been satisfied from the design point of view. Lots of attention was invested in the concept development, in the block-level design and in the physical layout – all to follow the desired performance. The experimental results, investigating the functionality and measurements done to inspect the performance, are the subject of the next section (4.3).

4.3. D^2R_1 experimental results

Throughout this work I have discussed the possible solutions to produce a high resolution circuit for readout of the pixelated CdTe detector. In Chapter II and Chapter III it was shown that each of the electronic stages has to be optimized: the detector geometry, CSA topology and dimensions as well as the filter type and parameters. In the presentation of the architecture concept for the final ASIC and its design in section 4.2 of this chapter, I have emphasized the tradeoffs that have been present throughout the development. In this section, the efforts are finalized with a demonstration of the achieved performance of the new readout ASIC D^2R_1. I start this paragraph showing the subject of interest in Figure 4.24 – an image of the fabricated D^2R_1 ASIC.

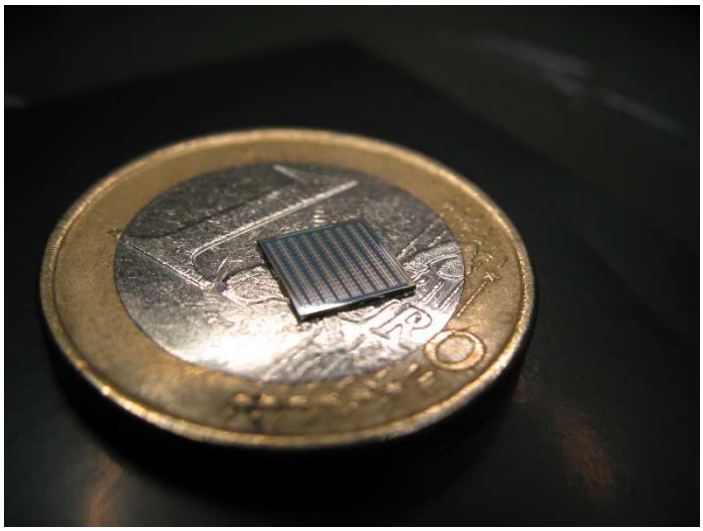


Figure 4.24 D^2R_1 ASIC die ($5.4\ mm \times 5.4\ mm$) and $1\ EURO$ coin.

4.3.1. Test environment description

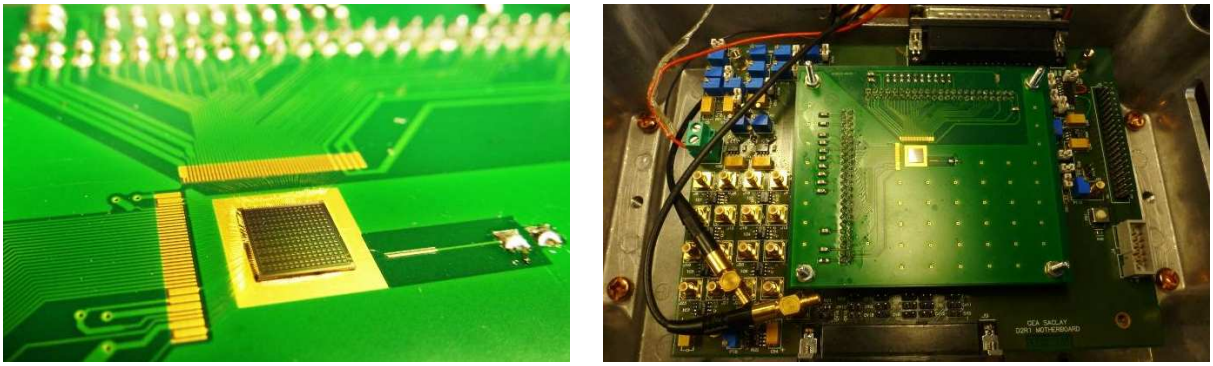
The ASIC D^2R_1 requires a dedicated measurement environment to perform a full characterization. I split this subject into two categories that are discussed below:

- The instrumental part including description of the physical test bench
- The definition of the setup that ensures the right conditions in the ASIC operation.

4.3.1.1. Measurement bench

The PCB used in the characterization was the most important part of the equipment – since it has to be customized to match D^2R_1. In fact it consists of two parts: the socket PCB where the bare-die ASIC is bonded and the main PCB which not only holds the structure but also contains dedicated circuitry with power supplies, analog bias adjustments, LVDS drivers and other discrete components indispensable in measurements. The main board, with the socket board on the top and the ASIC

ready for characterization are illustrated in Figure 4.25. I have developed these two boards during the D^2R_1 foundry.



A) B)

Figure 4.25 D^2R_1 measurement board. A) The ASIC bare-die bonded on the socket PCB. B) The socket PCB is mounted on the main PCB board containing adjustable analog bias control, power supplies, LVDS drivers and receivers, analog buffers and sockets for connecting with the external FPGA handling control, programing and readout.

One of the key elements for proceeding with the circuit measurements is the socket connecting the main board with external equipment, namely a board with an FPGA playing the role of the manager. It is responsible for: programming the ASIC setup of the internal Slow Control, transmission and reception of the control signals, as well as for readout of the ASIC discriminators and the measured analog outputs. The FPGA board is equipped with two 14-bit ADC, each one responsible for the digitization of analog signals coming from 8 lines of the D^2R_1 ASIC.

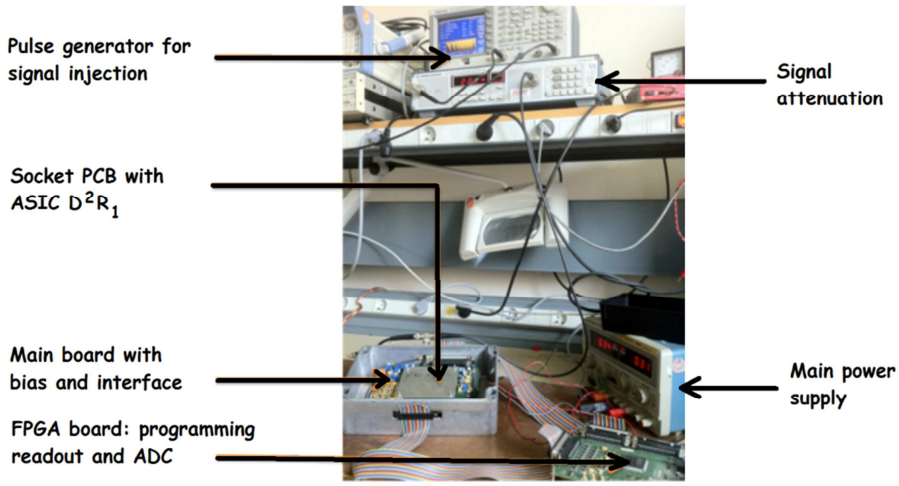


Figure 4.26 Photograph of the lab setup with the main PCB board including the ASIC D^2R_1 on the socket PCB, board with the control FPGA and the pulse generator for test signal injection to CSA at the absence of the detector.

In the D^2R_1 measurements presented in this work, it is only the electrical performance that is cross-checked. The circuit characterization is performed without detector connected to the ASIC inputs.

4.3.1.2. Measurement setup

In the test bench shown in Figure 4.26 there are three key elements that need adjustment to proceed with the ASIC characterization: the measurement board regulation, the input signal to which the ASIC responds and the on-chip Slow Control registers settings to define how the ASIC is desired to respond.

4.3. D^2R_1 experimental results

Typical measurement conditions

The main PCB dedicated to D^2R_1 measurements contains a set of power supplies, analog voltage adjustments and switches. The power supplies are set to nominal conditions, so are most of the bias currents and voltages. The main exception is the bias current for two unity gain buffers present in each channel, whose value is higher than the one used in simulations. This was necessary to modify in order to achieve the best ENC performance, but at the cost of power consumption. Among the analog bias conditions there is also the compensation current, which can add parallel noise at the channel input in the absence of the detector. In most measurements it has been set to the minimum value of $\sim 0\ pA$ resulting in negligible noise contribution. The particular ASIC functional settings are defined through the Slow Control registers. These that are the most essential in the measurements are: the CSA currents set to $I_{BIAS} = 10\ \mu A$ and $I_{OUT} = 800\ nA$, the operating mode set to 16-folded MCDS, CSA test input enabled in all pixels as well as all the pixels being active and all relying on the discriminator triggers. The DAC settings are identical in all channels and set to such value that no parasitic trigger on noise events could occur repeatedly in any of the channels. The CSA detection chain is sensitive to the typical anode readout polarity, with negative charge injected at the CSA input. Apart from these static adjustments there are also signals that must be sent to the ASIC to initiate its operation: the clock signal CLK and the CSA reset signal. Every time that the reset pulse occurs – it not only sets the CSA operating point, but it is also sent to digital blocks and restarts the in-pixel state machine to be ready for the event arrival. The CLK signal is set to $666\ kHz$, which means for the MCDS processing: CSA sampling with period of $1.5\ \mu s$. Finally there is the test signal at the CSA input that provokes the ASIC to trigger. With a variable amplitude of the injected charge, the performance of the discriminators and the MCDS processing can be examined.

CSA input signal

The input signal for the CSA in the electrical characterizations is applied on the test capacitance at the CSA input $TEST\ IN$, shown in Figure 4.4 (in 4.2.1). This input capacitance C_{INJ} for test injection has an identical value as the CSA feedback capacitance C_F: $25\ fF$. A negative input voltage step of amplitude A_{pulse} results in charge injection at the CSA input equal to: $A_{pulse} \cdot C_{INJ}$. In consequence an identical voltage step is obtained at the CSA output but with inversed polarity.

The form of the input signal is illustrated in Figure 4.27. It consists of ten negative pulses with increasing amplitudes. Their falling edge is sharp while the rising edge is a slow return slope. In the measurements it is the negative step that is of interest – it causes an instantaneous charge injection at the CSA input, therefore it is seen by the ASIC as an event: the discriminator triggers and the step amplitude is measured. After each of the input pulses the CSA reset is sent. The pulse amplitude seen by the CSA is attenuated with respect to the absolute value indicated in Figure 4.27. In typical measurements the attenuation is $22\ dB$, resulting in amplitude of the pulses ranging from $40\ mV$ to $400\ mV$ with a $40\ mV$ step between the ten pulses. This amplitude spread corresponds to the ASIC evaluation with the input charge dynamic range between $1\ fC$ and $10\ fC$. This corresponds to charge induced on CdTe electrodes in the input energy range of $28\ keV$ - $280\ keV$, what covers the upper dynamic range assumed as the D^2R_1 desired parameter.

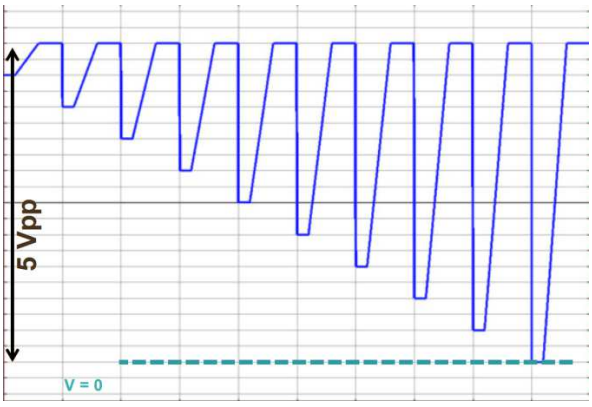


Figure 4.27 Voltage signal waveform programmed in the pulse generator, used in the D^2R_1 tests. It consists of ten negative pulses with sharp negative step, which is of interest since it causes an instantaneous charge injection at the CSA input, and with slow return rising slope. The waveform is attenuated before entering the CSA test input $TEST\ IN$, typically by $22\ dB$, resulting in amplitudes of the smallest and the highest pulses equal to $40\ mV$ and $400\ mV$.

Numerous repetitions of the input signal are required to collect enough statistics for reliable noise measurements. In order to approach the test conditions to the reality, where the pulse arrival is not synchronized with the ASIC control sequence – the frequency of the input waveform from Figure 4.27 has been modulated throughout the acquisition time between $1\ Hz$ and $14\ Hz$, not correlated with the D^2R_1 clock signal. In addition the CSA reset signal occurred not only after each pulse reception, but also independently of that: with a periodic occurrence. The described conditions of the three input signals: CLK, CSA reset and the test input signal resulted in a very wide range of possible circumstances of the pulse arrival reproduced in the electronic lab: without the detector and the radioactive source with random photon emission.

4.3.2. Performance

The measurements obtained with the D^2R_1 ASIC are divided into five categories:

- Functionality
- Dynamic range with gain and linearity
- ENC
- Detection threshold
- Power consumption

Initially the functionality of the circuit is demonstrated in different modes. The other tests are focused on the principal operation mode with in-channel MCDS processing. The readout chain characterization starts with examination of the dynamic range with special focus on gain and linearity. Then the ENC performance is studied at different conditions of the input parameters. The other subject in the detection chain also related to noise is the discriminator detection threshold. Finally I refer the obtained achievements to the corresponding power consumption measured on the ASIC.

4.3.2.1. Functionality

The readout circuit D^2R_1 has been equipped with four operating modes (listed in Table 4.5, in 4.2.2): the principal one where the full MCDS operation is performed and three test modes where either the CSA samples can be readout individually for off-chip analysis or the CSA output can be observed directly to inspect the analog signal. I present the functionality of the ASIC in the reversed order, gradually introducing the blocks in the processing chain from the CSA, through the sampling operation and ending up at the complete MCDS sequence involving discrimination and readout.

Analog CSA output

A dedicated test mode allowed direct observation of the CSA output voltage. The illustration in Figure 4.28 shows response of the CSA circuit to the input test signal. As expected – the negative input step results in a positive step of the same amplitude at the output. However the effect of the limited CSA bandwidth is also observed. The input signal fall time is in the range of $5\text{-}10\,ns$. Meanwhile the rise times of the two recorded waveforms at the CSA output, at two different output stage current I_{OUT} values, are in range of approximately $70\,ns$ to $200\,ns$. The result shows that modifying the adjustable bias current in the CSA output stage gives control over the CSA bandwidth. The feature has been implemented on purpose, since as I have demonstrated in the paragraph 2.3.5, the I_{OUT} parameter has influence on filtering capabilities of the MCDS shaper.

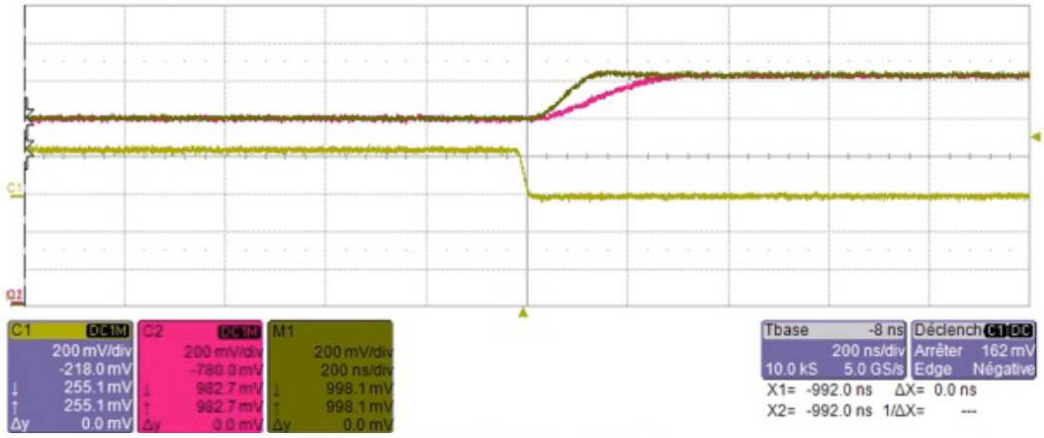


Figure 4.28 Two recorded CSA output waveforms (overlapping) in response to the negative voltage step at the D^2R_1 $TEST\ IN$ input, recorded at different values of the current I_{OUT} in the CSA output stage.

Sampled CSA output

The sampling block in each readout channel of the D^2R_1 circuit contains 17 sampling cells. In the ASIC I have implemented a dedicated test mode that enables verification of this processing stage. The CSA output (from Figure 4.28) is first sampled and then all the memorized discrete values are individually transmitted through the serial analog output. The readout can occur only once an event arrival has been detected. To reproduce the event the first 8 samples contain the baseline information while the remaining 9 samples store the response to input signal. This functionality of the sampling block has been described in 4.2.1. In Figure 4.29 the analog output in this operating mode is presented. In addition the clock signal CLK is shown, which indicates the event arrival at consecutive cycles.

4.3. D^2R_1 experimental results

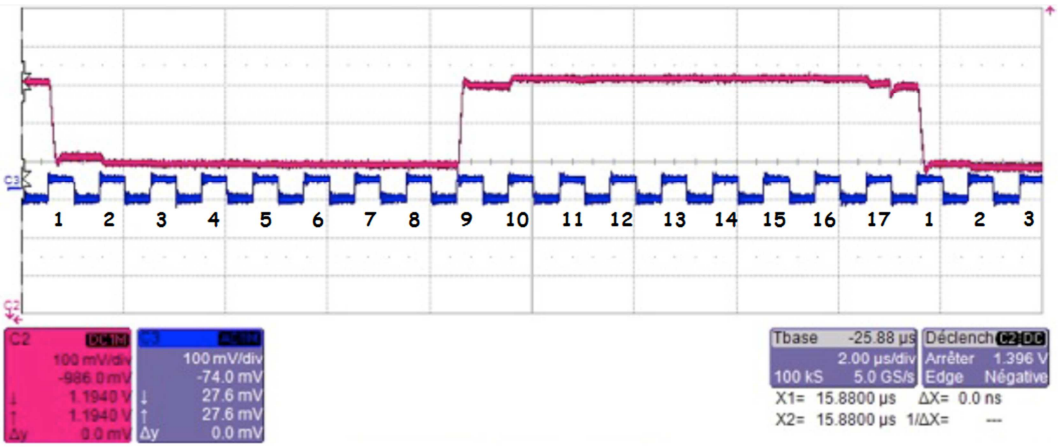


Figure 4.29 Illustration of D^2R_1 test mode where the sampling block is inspected. The sampled CSA output is shown together with the clock signal. With every cycle a new sample is read out. In the measurement – the maximum number of sampling cells has been activated, which involves all the 17 cells of the sampling block. Samples 1-8 contain the baseline information, samples 9-17 contain the pulse information. The last three samples are the CSA baseline samples of the neighboring pixel.

The first 8 samples illustrate the baseline level. The very first sample is systematically shifted with respect to the other samples, which is expected to be a parasitic effect related to the parasitic capacitance at the averaging node from Figure 4.10. It is the result of interconnections and the input buffer capacitances, which should be ideally negligible. This phenomenon should also explain why the first of the pulse samples, occurring 8 clock cycles later, is shifted to a lower value with respect to other pulse samples. This effect is expected to be k-times smaller in the ASIC operation mode with k-folded MCDS. Finally the 17^{th} sample is distorted by the address switching action when moving on to read out samples of the following pixel in the same line. Despite these non-idealities, this operating mode can be exploited to investigate the sampling noise and to perform the off-chip processing with up to 7-folded MCDS.

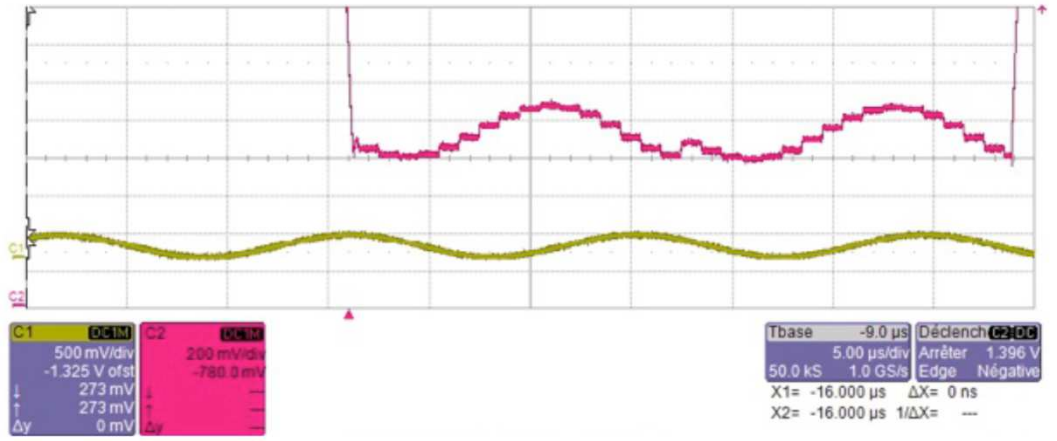


Figure 4.30 Verification of the ASIC performance by sampling of a sine-wave by the D^2R_1 sampling block.

The ASIC performance in this particular sampling mode has been explored beyond the principal functionality. We verified capability of the circuit to sample a continuous sine wave. In this test the ASIC was programmed to employ all 17 sampling cells inside the pixel. The results are shown in Figure 4.30, where the continuous readout of the acquired samples is successfully demonstrated.

MCDS mode

From the output analog waveform the MCDS operating mode is the least interesting one to observe on the oscilloscope: it is only a constant voltage that is read upon read request. Since measurement of this output voltage is the subject in the majority of measurement presented below, here I focus on the dynamic IO signals sequence that demonstrates the correct operation. The waveforms are illustrated in Figure 4.31. The first from the top is the analog test input voltage $1°$. Although this signal is routed to most channels, it is invisible to most of them since only few channels have been enabled in this measurement. The falling edge causes the ASIC to trigger, the discriminator pulse in the waveform $2°$ appears at the next clock edge (waveform $3°$) after the event. Once the FPGA receives this signal – it waits for a few cycles so that the sampling of the CSA signal pulse is completed (this takes between 1 and 8 clock cycles). Then it commands the hit registers scan clock $7°$ in the sequence of 16 cycles to read out the line hit register $5°$ and the column hit register $6°$. The hit registers' values read at each clock cycle inform whether the line/column with this specific number (between 0 and 15) has detected an event. According to waveforms from Figure 4.31 – the common test injection signal $1°$ caused all of the pixels in the lines 6 and 7 to trigger. The signal $4°$ is the analog output resulting from the readout request (readout request is not indicated in the plot).

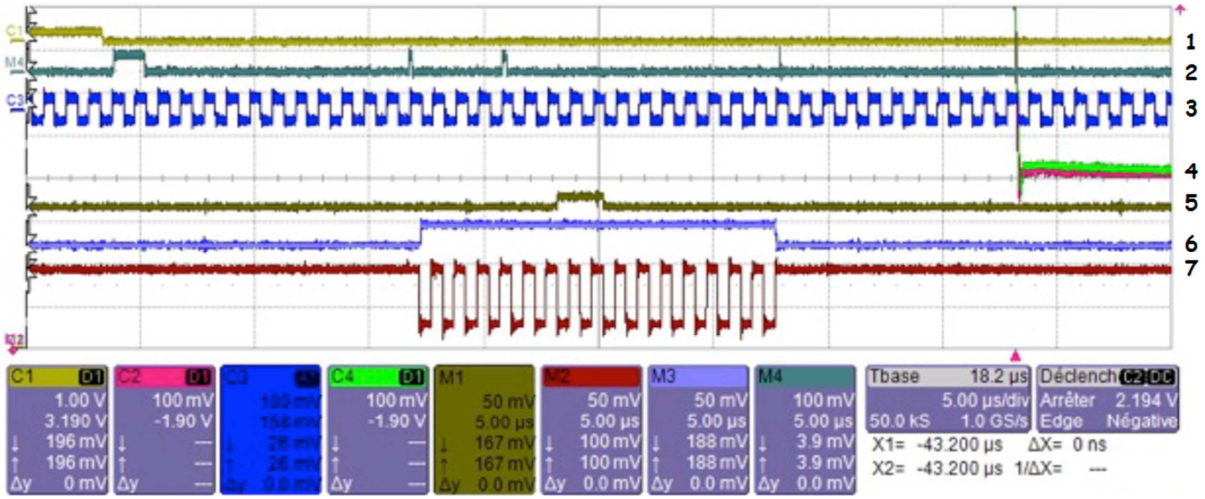


Figure 4.31 MCDS readout sequence. Signals from the top: 1° CSA analog test input, 2° Global OR, 3° CLK, 4° analog outputs, 5° readout line hit register, 6° readout column hit register, 7° hit register scan clock.

In the MCDS oscilloscope image two problems in the ASIC are apparent:

The first issue is that in fact only few pixels have been activated in the described test, not two complete lines, as one could understand from the waveforms ($5°$ and $6°$). Additional inspection has shown that the column register operates properly. However the readout from the column register always shows that: each column experienced an event, even when this is not correct. The reason is a mistake in the trigger logic circuit, which makes it vulnerable to any glitches on the trigger path. Despite this bug, the circuit is operational. Moreover the mistake can be easily fixed.

The second problem, related with the column hit register is the presence of glitches in the $Global\ OR$ signal $2°$. The longer pulse one-clock-cycle-long (in Figure 4.31) is the actual trigger from one of the discriminators, the shorter pulses are the parasitic glitches. Although the glitches might cause disturbance in the ASIC, they do not prevent signal acquisition and further characterization.

4.3.2.2. Gain, linearity and dynamic range

The characterization of the MCDS processing response as a function of the input pulses of different amplitudes is interesting for some reasons. With variable charge injection, the dynamic range can be established. Consequently the channel gain and the linearity can be determined – these are the key parameters to calibrate the energy spectrum measured with detector. Secondly, knowledge of the gain is important to calculate the channel input referred noise – that is the ENC, which is presented afterwards.

The signal illustrated in Figure 4.27 was applied at the ASIC input in multiple cycles. The resulting response is shown in Figure 4.32 showing the number of counted occurrences for each value measured by the ADC. In consequence there are 10 peaks. With the known input waveform – spacing between the peaks is used to calculate gain and linearity, while the peaks' shapes are analyzed to calculate the noise.

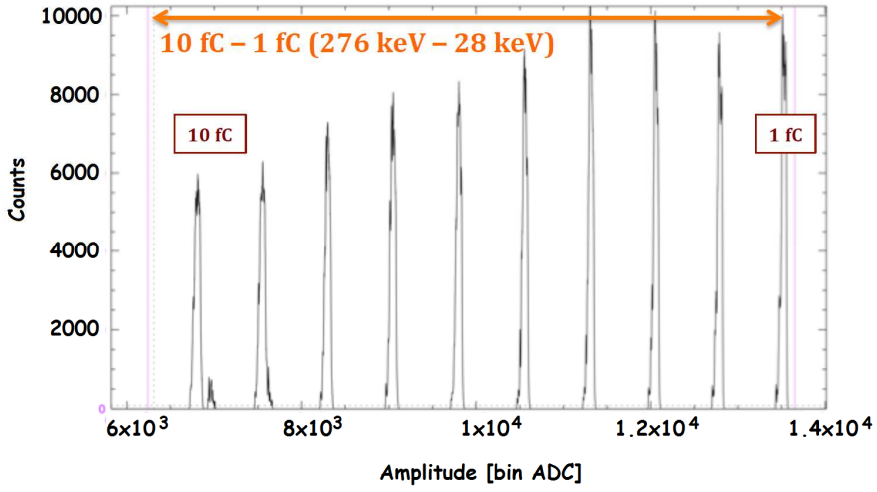


Figure 4.32 D^2R_1 response to the input signal from Figure 4.27 after the ADC conversion. Input voltage step of the highest amplitude corresponds to the left hand side peak. The plot is obtained on the whole matrix.

The same measurement has been performed on all pixels in the D^2R_1 array. In consequence gain and linearity have been obtained for each of the 256 readout channels in the ASIC. The results from gain calculations are shown in Figure 4.34, for the summed response of all 256 pixels. Measurements are very close to the simulated gain, resulting from the CSA capacitance setting the input stage gain to $1/C_F = 40\ mV/fC$ and the multiplication in the CDS stage by $\times 4$. Conclusion from this measurement is that the gain between pixels is very homogeneous. Also the corresponding DC offset of the analog output voltage is rather small, with the mean value equal to $5.4\ mV$. These outcomes have been obtained in the typical conditions listed at the beginning of this paragraph (4.3.1). In the plot Figure 4.32 of the output response in the CDS mode – one can distinguish a double peak corresponding to the highest input signal of $10\ fC$. The result has been obtained with responses from all pixels taken into account. Since gain of the first column is observed to saturate faster than in case of other pixels (what has not been yet fully explained) we observe the double peak. If we look on the same characteristic but with response limited to only one pixels, the double peak is replaced with a single one. This is illustrated in Figure 4.33.

4.3. D^2R_1 experimental results

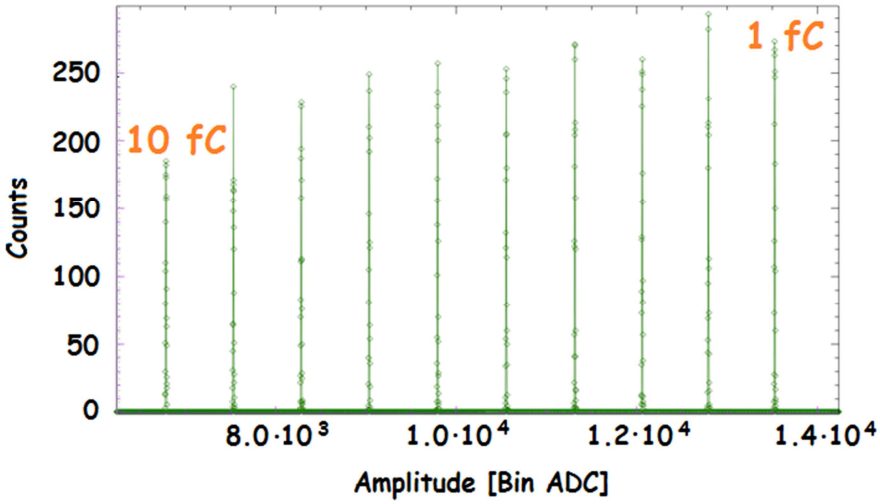


Figure 4.33 D^2R_1 response to the input signal from Figure 4.27 after the ADC conversion. Input voltage step of the highest amplitude corresponds to the left hand side peak. The plot is obtained for a single pixel.

Additional studies, results of which are not covered in this description, have shown, that the gain slightly changes with the operating conditions, like with: the number of MCDS samples, the CLK frequency, the CSA bias current I_{BIAS} and the CSA output current I_{OUT}. In consequence of the dispersion, each pixel requires calibration with respect to these settings.

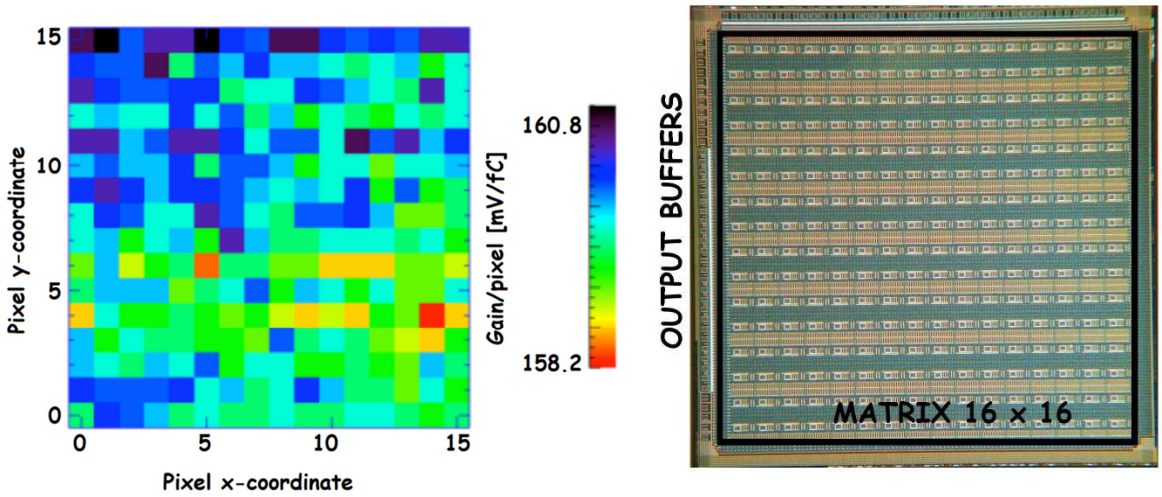
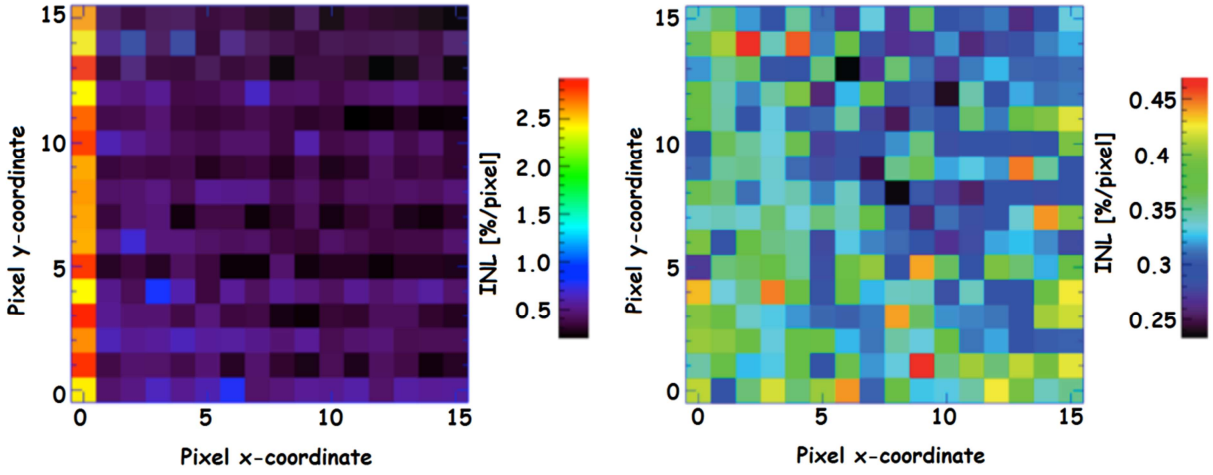


Figure 4.34 A) Gain map measured on the D^2R_1 ASIC measured for the input dynamic range from $1\ fC$ to $10\ fC$. B) The corresponding orientation of the ASIC, valid for all parameter maps presented in this chapter.

The integral non-linearity (INL) calculation results, the direct consequence of the gain map from Figure 4.34, are shown in Figure 4.35. The systematic increase of INL in the first column is observed in the case of Figure 4.35 A) where the whole input dynamic range is considered: $1\ fC$ to $10\ fC$. In the rest of the array of pixels INL is below $0.5\ \%$. Taking a closer look – the systematic offset disappears if the dynamic range is decreased down to $6\ fC$, as shown in Figure 4.35 B). The first column showing different behaviour is in the direct neighborhood with the output buffers and it is also the first one that is read out after each input event transmitted to all pixels. Why it acts differently has not been yet identified, the issue needs further investigations.



A) B)

Figure 4.35 D^2R_1 map of the integral non-linearity calculated in range: A) from $1\ fC$ to $10\ fC$, B) from $1\ fC$ to $6\ fC$.

4.3.2.3. Measured ENC

From the same measurements, from which the gain and linearity maps have been extracted (Figure 4.34 and Figure 4.35), also the ENC was calculated. The corresponding ENC map of the ASIC D^2R_1 is illustrated in Figure 4.36. The extreme values recorded over the whole readout circuits' array ranges between $25\ el\ rms$ and $50\ el\ rms$, with the mean calculated over all channels equal to $29\ el\ rms$. The assigned numbers of the "best" and the "worst" pixels identified in this particular ASIC are 113 and 109 respectively. Although the overall mean ENC dispersion is only slightly higher than in the reference pixel – the presented result is still over two times worse than expected with no additional capacitance or dark current at the CSA input.

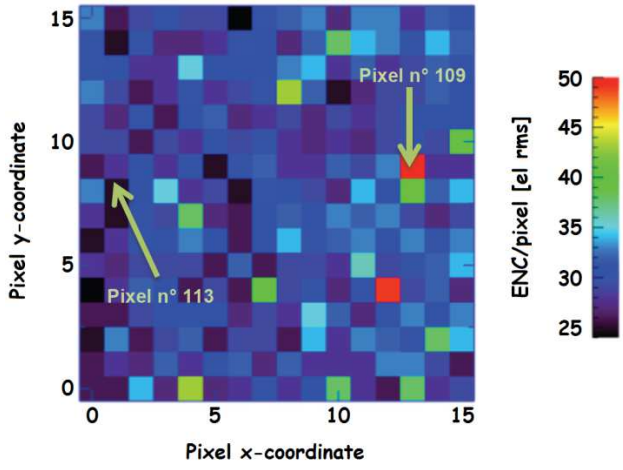


Figure 4.36 ENC map of D^2R_1 obtained in electrical characterization with no detector, no external input capacitance and with the compensation current set to zero. The presented values have been calculated for the input signal amplitude of $40\ mV$, corresponding to $1\ fC$ charge injected at the CSA input.

In pursuit for causes to the obtained ENC results, higher than expected, there are two things that I am going to analyze below:

- Measurements on a single "average" pixel of noise contribution due to individual blocks within the detection chain.

- Investigation of the operating conditions – how they influence ENC and how much the mean ENC value can be improved with different conditions.

Single channel ENC

First of all I have chosen one of the typical channels within the measured ASIC and returned one step back in the test mode, where the CSA output is directly observed. In fact according to Table 4.5 shown in 4.2.2 – there are two such test modes that permit this analog operation: CSA output after the first unity-gain buffer and CSA output after two unity-gain buffers (for architecture details please refer to Figure 4.3 from 4.2.1). I have used both of them in the inspection described below. The CSA implemented in the D^2R_1 ASIC is identical as in the testchip Caterpylar described in Chapter III. In the given test-modes it is possible to measure the CSA noise through the external semi-Gaussian shaper and to compare it with the corresponding results in D^2R_1.

In these measurements I have investigated the ENC in D^2R_1 with and without the clock signal CLK, as well as in the function of the observed output node: after the first or the second unity-gain buffer. Results of the comparison with the Caterpylar CSA are summarized in Table 4.6. From the obtained numbers I conclude that each buffer adds $8\,el\,rms$ contribution to the obtained result. Similar additional input-referred noise appears in the presence of the clock signal. In consequence, with all of these three noise sources present in the signal path, and a possible clock pick-up later in the sampling stage – the excessive ENC with the D^2R_1 MCDS processing chain shown in Figure 4.36 is mostly identified.

Measurement conditions*	Measured ENC $[el\,rms]$
Caterpylar ASIC	12.5
D^2R_1 ASIC no CLK signal, 1^{st} buffer output	14
D^2R_1 ASIC no CLK signal, 2^{nd} buffer output	16
D^2R_1 ASIC with CLK signal, 1^{st} buffer output	16.5
*Common conditions: CSA T10, $I_{BIAS} = 10\,\mu A$, external shaper CR-RC^2 with peaking time of $11\,\mu s$, input voltage signal 30 - $40\,mV$	

Table 4.6 Direct comparison of ENC obtained with the Caterpylar ASIC and with the D^2R_1 ASIC.

The next of the presented ENC measurements take into account the average obtained over all D^2R_1 pixels measurements at variable operating conditions. The CSA currents I_{BIAS} and I_{OUT} are varied at each set of acquisitions to study how much the average noise can be improved with respect to results from Figure 4.36. The possible improvement is studied also at different MCDS sampling periods $T_s = 1/f_s$ and with variable number of samples k in the k-folded MCDS processing.

ENC as a function of CSA bias current

Increase of the input transistor bias current reduces the thermal noise contribution in the CSA, therefore it is expected that the mean ENC in the D^2R_1 ASIC should decrease with increasing I_{BIAS}. The current in the CSA stage can be adjusted with four steps between $4\,\mu A$ and $20\,\mu A$. The summary from the corresponding ENC maps (like the one obtained for $10\,\mu A$ in Figure 4.36) is presented in Figure 4.37. The mean ENC, as well as the ENC of the pixel 113 (the best in the array) and the pixel 109 (the worst) are shown as a function of the CSA bias current. Indeed – the ENC improves with the bias current. However the major difference is observed between $4\,\mu A$ and $10\,\mu A$. Any further current increase does not bring significant ENC changes.

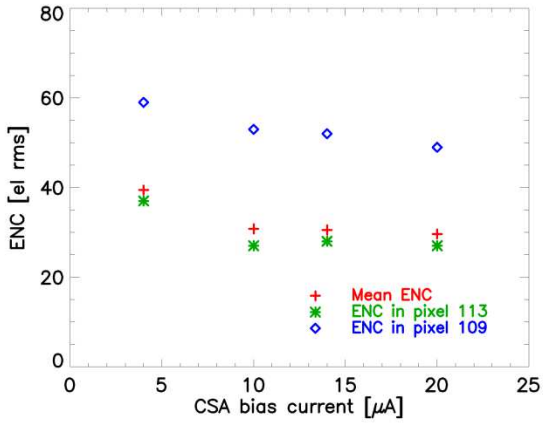


Figure 4.37 1 ENC as a function of the CSA bias current I_{BIAS} in the D^2R_1 ASIC: mean ENC over all pixels, ENC in the best pixel (113) and ENC in the worst pixel (109).

ENC as a function of the CSA output current

In the paragraph 2.3.5, I have demonstrated that the CSA bandwidth has an important influence on filtering of the thermal noise with the MCDS processing. With smaller bandwidth MCDS resembles more and more the triangular weighting function, whose thermal noise filtering properties are very good. In D^2R_1 the CSA bandwidth can be adjusted with the variable output stage current I_{OUT}, between $100\,nA$ and $800\,nA$. The previously presented ENC map from Figure 4.36 was obtained with the highest I_{OUT}, as its value decreases, also the bandwidth is reduced. The additional ENC maps have been produced with lower currents. The summary of the results is shown in Figure 4.38, with the mean ENC as well as the best and the worst pixels: 113 and 109. In the measurements outcome, there is almost no influence of the CSA output current on the ENC observed. The excessive noise dominates ENC and any improvement in the thermal noise filtering is of negligible significance.

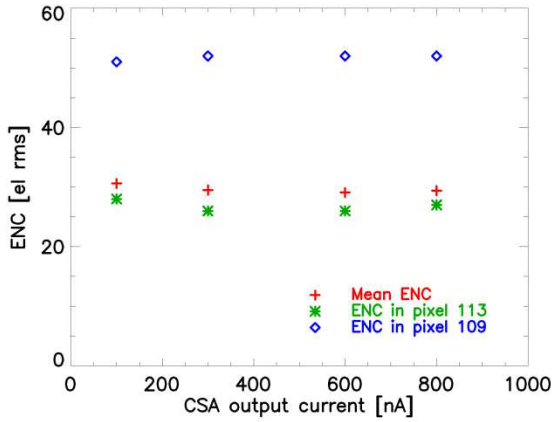


Figure 4.38 ENC as a function of the CSA output stage current I_{OUT} in the D^2R_1 ASIC: mean ENC over all pixels, ENC in the best pixel (113) and ENC in the worst pixel (109).

ENC at variable sampling period

The CLK frequency in the D^2R_1 ASIC directly sets the sampling period between the MCDS samples. However according to the theoretical results from 2.3.5 – it should have no influence on the thermal and flicker noise components in the total ENC. Only the ENC of the parallel noise component is

expected to change: it is expected to increase with increasing sampling period (due to worse correlation between samples). Measurements investigating this issue in the D^2R_1 ASIC have been performed at different clock frequencies. With the resulting sampling frequency T_s ranging from $1\ \mu s$ to $5\ \mu s$ – the mean ENC over the whole array of pixels has been calculated. The results are shown in Figure 4.39, again demonstrating that the resolution cannot be improved with respect to the first ENC map in Figure 4.36. Among the tiny variations with the sampling period – the lowest noise is achieved at T_s of $1.5\ \mu s$.

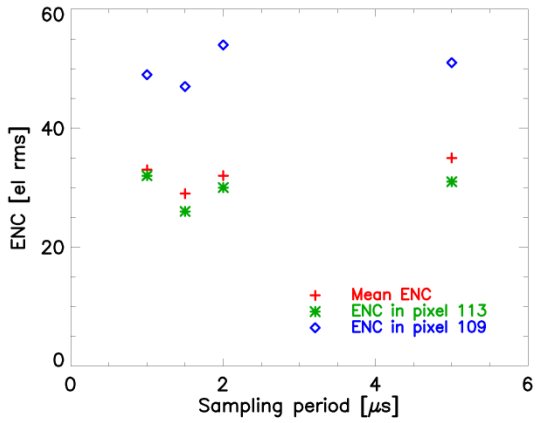


Figure 4.39 ENC as a function of the MCDS sampling period in the D^2R_1 ASIC: mean ENC over all pixels, ENC in the best pixel (113) and ENC in the worst pixel (109).

ENC at variable number of samples

The last parameter of high interest in the ENC evaluation is the number of samples k in the k-folded MCDS processing. Such measurements are possible in the D^2R_1 thanks to the logic that permits adjustment of the MCDS parameter k between: 1-folded (CDS) and 16-folded.

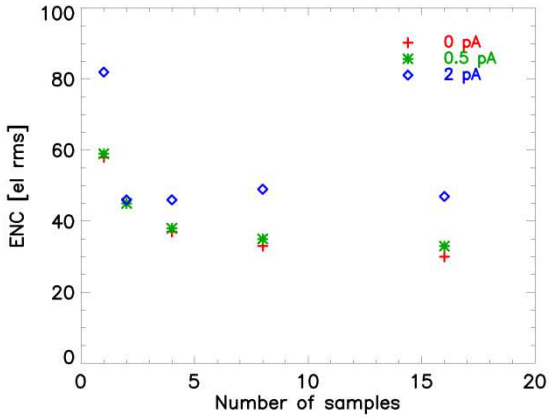


Figure 4.40 ENC as a function of the number of samples k in the k-folded MCDS in the D^2R_1 ASIC: at the compensation current I_{comp} set to $0\ pA$, $0.5\ pA$ and $2\ pA$. All $ENC(k, I_{comp})$ show mean ENC over all pixels.

The high number of samples is especially interesting for the thermal noise reduction. The confirmation of this statement is found in the experimental results shown in Figure 4.40. In the measured ENC it is also observed that there is not much improvement between the last two ENC values: at k set to 8 and 16.

In Figure 4.40, in addition to the general ENC characterization at variable number of MCDS samples – the impact of k is also measured with increasing parallel noise contribution. This has been realized through the adjustable input compensation current I_{comp}, whose noise characteristics highly resemble the shot-noise PSD. At the presence of this additional parallel input current source – it is observed that the optimal number of samples shifts to lower values. The observed effect is again in agreement with the MCDS theory described in the paragraph 2.3.5.

Expected energy resolution with CdTe detector

Studies of the D^2R_1 operating conditions influence on the ENC have been performed with respect to four parameters: CSA bias current, CSA output current, clock frequency and the number of MCDS samples. Despite all these efforts the best ENC resolution achieved with the circuit is close to the results shown in Figure 4.36 with the mean ENC of $29\ el\ rms$. This is much higher than results obtained with very similar CSA (input transistor length of $0.3\ \mu m$ instead of $0.45\ \mu m$ in D^2R_1) and with external MCDS filter, realized with the Caterpylar ASIC and presented in the paragraph 3.4.3. Those initial measurements reached down to $12\ el\ rms$, which is over twice lower than what has been achieved with D^2R_1. After inspection of D^2R_1's mean ENC as a function of the adjustable operating conditions, I have established that there must be other dominating sources of noise within the detection chain, additional to those identified in Chapter II: the thermal voltage noise and the flicker voltage noise (at the absence of I_{comp} the current noise is negligible). The investigations also demonstrated that this additional noise increases further only when the clock frequency becomes too low. Most likely the undesired disturbance is related to the mixed-signal nature of the circuit, where dynamic digital signals co-exist with the low noise signal path. In this case however – it is not expected that this noise component would increase in the presence of the detector.

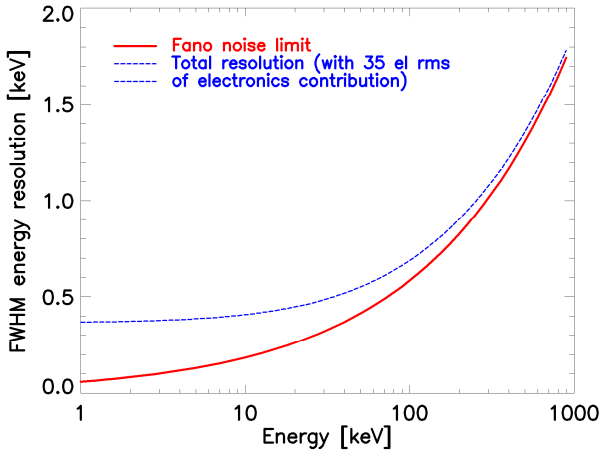


Figure 4.41 Estimated FWHM energy resolution of the detection system with pixelated CdTe (input capacitance of $500\ fF$ and dark current of $0.5\ pA$) and the D^2R_1 ASIC.

It can be estimated that the excessive noise mean contribution to the total ENC is $26\ el\ rms$ with calculations based on the difference between D^2R_1 characterization and the external MCDS measurements with the Caterpylar in 3.4.3 where the floor ENC of $12\ el\ rms$ has been obtained. Now, remembering the best theoretical MCDS estimations derived in 3.5.2 for the pixelated CdTe – the expected performance of D^2R_1 with the detector can be estimated. The ENC value obtained from the extracted the Caterpylar CSA noise PSD and the MCDS noise parameters indicate that at the

typical detector parameters (capacitance of $0.5\ pF$ and dark current of $0.5\ pA$) the ENC estimated to $24\ el\ rms$ (or $40\ el\ rms$ at the worst case of $1\ pF$ and $5\ pA$). Taking this typical condition – the ENC that should be fulfilled with the D^2R_1 ASIC connected to pixelated CdTe is estimated to $35\ el\ rms$. This value corresponds to $360\ eV$ FWHM resolution due to the electronic noise. The resulting achievable total FWHM resolution of the complete readout chain with the CdTe detector is illustrated in Figure 4.41, where the Fano statistics are also taken into account. Including all possible noise sources, the expected mean FWHM resolution of $600\ eV$ at $60\ keV$ (or $700\ eV$ at the worst-case detector capacitance and dark current) is still much lower than the values so far reported, with the Caliste HD [41] among the leading spectro-imaging instruments, reaching down to mean FWHM of $900\ eV$, calculated over all pixels.

4.3.2.4. Low energy detection threshold

In many ASICs used to measure the X-ray energy for astrophysics, the low detection threshold is strongly associated with the system ENC. This is because when the readout channel is realized as a time-invariant filter, e.g. with the analog semi-Gaussian shaper, then the event discriminator is placed after the shaper to profit from the reduced noise level. This is the case in the CdTe readout ASICs reported in [42] and [40]. Such solution saves power consumption and layout area, by using the same noise filter for two purposes: measurement and detection. In case of D^2R_1, however, the situation is different – the time-varying MCDS shaper must be informed of an event arrival to decide on the pulse processing. For this reason the detector constitutes an entirely different shaping stage, with their last common point at the CSA output (for the channel architecture details please refer to 4.2.1). The discriminator performs the CDS operation on the CSA output samples. However, except for the common control signal CLK, this block is independent from the main signal measurement path. Consequently I present the results studying the detection threshold separately from ENC.

I have used two approaches to estimate the limit of detection:

- By application of small input signals to observe how low they have to get to be ignored by the comparator. In this measurement the discriminator DAC references have been set to the lowest level V_{ref} that ensures that no noise events can occur.
- By setting the DAC references to a very low value where the continuously detected noise events are measurable – to calculate noise seen by the discriminators.

Detection of low input signals

In the first experiment the signal voltage at the ASIC output had the same shape as the waveform from Figure 4.27 in 4.3.1., however with much higher attenuation than in the ENC measurement. The voltage amplitude of the ten linear pulses has varied between $1\ mV$ and $10\ mV$, corresponding to input photon energies received with CdTe in range from $0.69\ keV$ to $6.9\ keV$. The analog output has been measured to evaluate D^2R_1 capability to detect such a low energies.

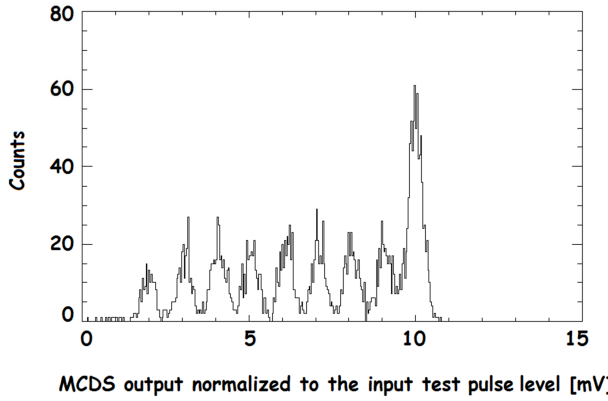


Figure 4.42 D^2R_1 response to input of 10 pulses of amplitude between 1 mV and 10 mV. The DAC references of the in-channel discriminators are set to a possibly low value, however with attention that detection of noise events would not occur.

Result of this multi-event acquisition is demonstrated in Figure 4.42. There are only 9 peaks – the lowest pulse is not present on the plot, which means its energy is too low for the discriminator to trigger at a given reference level. However if the reference had been set any lower the first peak would most probably disappear in a sequence of noise events. The amplitude of the first detected input signal is $2\ mV$, which corresponds to detection of signals below 312 electrons and to $1.38\ keV$ events detectable with CdTe.

Detection of noise events

The second experiment verifying the detection threshold was based on measurements of noise events. The measurement output directly translated to the equivalent energy received with CdTe (on the x-axis) is shown in Figure 4.43. It is a peak, that rises sharply at $0\ keV$ and decays back to zero at the equivalent detection threshold of $0.8\ keV$. The fact that the maximum number of counts does not occur at exactly at $0\ keV$ is mainly related to limited precision in the channel gain calibration. The maximum equivalent energy of the measured noise events corresponds to the equivalent noise charge of 180 electrons or the equivalent input voltage of $1.16\ mV$ with respect to results from Figure 4.42. Since the lowest amplitude of the input event in the first detection threshold experiment was set to $0.69\ mV$, knowing the measured input noise seen by the discriminator – it is understandable that the lowest peak could not be observed.

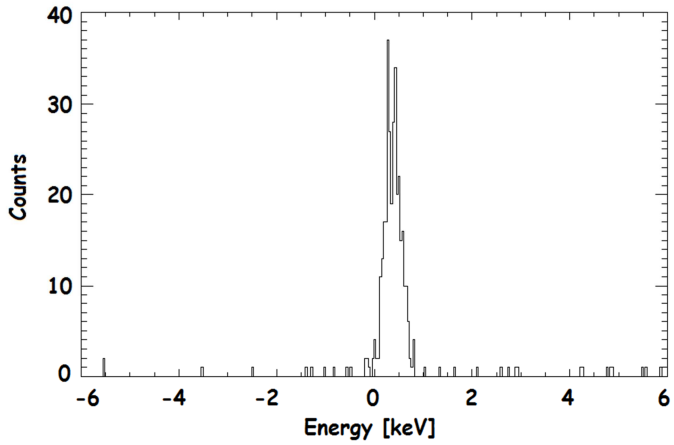


Figure 4.43 Response of D^2R_1 to noise events. The DAC references of the in-channel discriminators are set very low to be able to observe the ASIC detecting the noise events. The x-axis shows the noise amplitude in terms of equivalent input energy.

It must be noted that the two presented measurements (in Figure 4.42 and Figure 4.43), illustrating excellent performance of low detection threshold, were performed with no additional capacitance at the channel input and with negligible parallel noise. Once the detector will be connected at the CSA input the result is expected to be worse, however it is difficult to precise the exact detection threshold from these measurements.

4.3.2.5. Power consumption

The presented measurements of the D^2R_1 ASIC shown that it is a very low noise ASIC, although its resolution capabilities in the energy measurement are not as good as we could expected. Because of the high association between the noise, power consumption and the layout area, what I have presented throughout Chapter III and IV, the overall performance of the readout ASIC should not be judged before its power consumption is determined.

Considered domain	Power consumption per pixel $[\mu W/pixel]$	Power density $[mW/mm^2]$
$1.8\ V$ analog and digital	202.6	2.23
$3.3\ V$ analog (line buffers and CDS)	44.6	0.5
$1.3\ V$ for CSA input stage	10.7	0.63
$3.3\ V$ digital (mainly peripherals)	56.8	0.12
Total measured	**314.6**	**3.5**
Simulations – pixel	**117**	**1.3**
Simulations – pixel and peripherals	**181**	**0.2**

Table 4.7 Measured power consumption of D^2R_1 ASIC. For comparison – also simulation summary is shown. The power density calculations in the third column are pessimistic – they do not into account the significant peripheral area.

Consequently measurements of the current dissipated by each of the power domains on the main PCB board have been measured. The measured results divided by the number 256, corresponding to the number of channels, are summarized in Table 4.7. The average measured power consumption of $314.6\ \mu W/pixel$ is much higher than the one obtained in simulations, which is $181\ \mu W/pixel$ (accounting peripherals' power consumption). The results in the third column in Table 4.7 are recalculated and expressed in terms of power density, by taking into account area of a single channel of $300\ \mu m \times 300 \mu m$. According to the initially assumed specifications – this parameter should not exceed $2\ mW/mm^2$, meanwhile the density calculations from the PCB measurements indicate $3.5\ mW/mm^2$. This result however is pessimistic in the sense that the ASIC die area with the peripheral circuits has not been included. If the total measured ASIC power of $256 \cdot 314.6\ \mu W$ is divided by the total die area of $5.4\ mm \times 5.4\ mm$ the real power density of the D^2R_1 ASIC is obtained. It is $2.76\ mW/mm^2$. This true power consumption of D^2R_1 is higher by 38% than the desired value.

The most important reason of the increased power consumption is the excessive current in the $1.8\ V$ domain. It is dominated by the blocks inside the channel. Only a negligible share is related to the peripherals. From the first noise measurements it was clear that the current supplying the unity-gain buffers in the D^2R_1 processing channel must be significantly increased to arrive at the ENC level shown in the presented noise performance results. Without this increase – the power consumption would be very close to the simulated one, however with the mean ENC of $40\ el\ rms$ instead of the achieved mean value of $29\ el\ rms$. The noise-power trade-off has not been expected at the level of

this particular block, and has to be investigated, especially as according to Table 4.6 – it is still largely responsible for the too high ENC.

Through theoretical and experimental studies presented in the previous chapters, I have shown the possible directions in development of readout circuit for the pixelated CdTe. From the very beginning three principal criteria have been resolutely emphasized. The circuit realization should provide ultra-low noise of $20\ el\ rms$, minimized power consumption of $180\ \mu W/channel$ and fit in the highly restricted layout area of $300\ \mu m \times 300\ \mu m$ determined by the detector geometry.

Finally in this chapter, I have presented: the concept, design and measurements of the complete readout ASIC D^2R_1. The ASIC has 256 detection channels each with self-trigger capability at low threshold expected in the order of $2\ keV$ and with signal processing chain based on the 16-folded MCDS shaper, which once connected with CdTe should allow for energy measurement with the expected FWHM resolution of $600\ eV$ at $60\ keV$. The overall input dynamic range in combination with CdTe should permit measurement of X-ray energies up to $280\ keV$ or above.

These performances are predicted from the measurements without any detector connected at the channel input. At this condition of no additional capacitance and no additional dark current – the actual measured detection threshold is $0.8\ keV$ and the electronic noise is $29\ el\ rms$, which is the mean value over all channels. The results are achieved with a power consumption of $2.76\ mW/mm^2$.

Although in the presented ASIC certain aspects have been identified that need improvements, still the proposed concept is promising for application in the spectro-imaging X-ray camera based on the pixelated CdTe.

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FINAL CONCLUSIONS

… and perspectives

In this PhD thesis I have presented my approach to the development of a spectro-imaging instrument for modern X-ray astrophysics: a stacked hybrid module of the detector and its readout circuit. Followed by the justification for choosing a pixelated CdTe detector with an ASIC of matched geometry, I have identified the critical parameters at each stage of the readout process. Within the CdTe sensor, the Fano interaction statistics form a physical resolution limit in X-ray energy measurements. Furthermore the detector dark current and its input capacitance highly influence the electronic noise contribution. With the proposed pixel size of $300\ \mu m \times 300\ \mu m$ I have estimated the dark current to be below $5\ pA$ and the capacitance in range of $0.3\ pF$ - $1\ pF$. For these input parameters I have evaluated the readout chain capabilities to achieve the Fano resolution limit. The limited power consumption has been shown to be the main challenge.

In the first stage of the practical development I have realized the Caterpylar ASIC, which integrates 26 ultra-low power (typ. $14\ \mu W$) CSAs with different types and dimensions of the input MOS transistor. It has the highest contribution of the electronic noise and requires a fine optimization. Through noise analysis based on measurements with the CR-RC^2 shaper, whose noise filtering properties are accurately described with analytical equations, I have extracted the input-referred noise and the intrinsic input capacitance of each CSA. These results were sufficient to determine the ENC with any other shaper of known mathematical description and to reveal the resolution limits. I was especially interested to compare the semi-Gaussian (CR-RC^N) filter with the Multi Correlated Double Sampling (MCDS) as two possible on-chip implementations of the signal processing schemes. Consequently, I have performed a complete theoretical analysis of the MCDS noise filtering properties, calculating the specific filter parameters both in the time and in the frequency domains. I could then compare the MCDS capabilities with other shapers. The last task related to the Caterpylar ASIC was the determination of which CSA is the best suited for which filter and what are the respective ENC resolutions. In conclusion for the given pixelated CdTe detector the semi-Gaussian and the MCDS shapers are candidates with comparable performances.

After comparison of two proposed circuit topologies with the semi-Gaussian and the MCDS processing chains, I have finally chosen the second solution, motivated mainly by the power consumption advantages. I have designed a complete readout chain based on the MCDS processing that fits the restricted layout area of $300\ \mu m \times 300\ \mu m$. An array of 256 identical channels is the core of the new readout ASIC D^{2}R$_1$. Each channel has a self-trigger capability with the detection threshold of $180\ el$ and mean measurement resolution of $29\ el\ rms$, both were measured with no detector at the CSA input. The ASIC power density is $2.7\ mW/mm^2$, or $315\ \mu W/channel$. The obtained figures suggest promising results in spectro-imaging, with an expected resolution of $600\ eV$ FWHM at $60\ keV$ with CdTe, better than all reported results so far, and which can be lowered even more with certain proposed improvements for D^{2}R$_1$ regarding power consumption and noise.

5.1. D^2R_1 in the field

Despite the fact that measurements of D^2R_1 have not been yet performed with the dedicated detector, its measured electrical performance can be used to compare it with other existing solutions in the field of CdTe-based X-ray detection for astrophysics. In Table 5.1 is presented the summary of the most important parameters of D^2R_1 and corresponding values reported for four ASICs currently in use in the same domain.

	Hexitec [1][2][37][4]	[40]	Caltech [5][7]	[10]	D^2R_1****
Pixel pitch	$250\ \mu m$	$270\ \mu m$	$600\ \mu m$	$300\ \mu m$	$\mathbf{300\ \mu m}$
No. of channels	80×80	12×12	32×32*	32×32	$\mathbf{16 \times 16}$
Det. threshold	$4\ keV$	$4\ keV$	$5\ keV$	$7\ keV$	$\mathbf{\sim 2\ keV}$
Energy upper range	$200\ keV$	$300\ keV$	$100\ keV$	$53\ keV$	$\mathbf{> 280\ keV}$
FWHM at $59.5\ keV$	$1\ keV$	$0.9\ keV$	$0.9\ keV$	$equiv: 0.6\ keV$	$\mathbf{\sim 0.6\ keV}$
Power cons. per channel**	-	$0.33\ mW$	$0.05\ mW$	$0.54\ mW$	$\mathbf{0.32\ mW}$
Power density***	-	$1.67\ mW/mm^2$	$0.12\ mW/mm^2$	$1.86\ mW/mm^2$	$\mathbf{2.7\ mW/mm^2}$
Dead zone for detection	5 %	43 %	12 %	69 %	**21 %**
Processing	Semi-Gaussian	Semi-Gaussian	16 output samples for off-chip processing	Semi-Gaussian	**MCDS**

* It is the final CdTe module, there were previous prototypes with pitch of $498\ \mu m$ in 24×44 pixels array [38][39]
** Power cons. per channel is calculated for the ASIC only. In case of Caltech - ADC and processor are NOT included.
*** Power density includes the ASIC peripheral area (dead zone for detection)
**** Performance measurements without detector

Table 5.1 Comparison of D^2R_1 with other ASICs with pixelated channels arrangement dedicated for stacked assembly with CdTe detector and designed for application in X-ray spectro-imaging for astrophysics.

All of the circuits considered in Table 5.1 are designed for stacked assembly with CdTe detector. They have comparable pixel pitch, they are capable of self-trigger on event arrival and all of them provide a dynamic range compatible with the CdTe detector. D^2R_1 is the only one that proposes the on-chip processing using MCDS. In all the other cases, when the integrated shaper exists, this is a semi-Gaussian shaper. In terms of noise and detection threshold D^2R_1 is likely to be a competitive ASIC, however to confirm this measurements with a detector are indispensable. Finally, the power consumption is the parameter of great interest in the application dedicated for space-borne instruments. For the five ASICs considered, the comparison of the power density and of the power consumption per channel must also take into account the occupation of the peripheral area. In D^2R_1 this detection dead zone constitutes a small percentage of the total die area, especially considering that with 256 pixels it is one of the smallest arrays. Consequently, despite the currently achieved "poorer" power density when taken at face value, the new readout ASIC has a great potential to become a competitive actor in the X-ray astrophysics domain.

5.1. D^2R_1 in the field

As the initial phase of the ASIC electrical characterizations is nearly completed, let's look into the future steps. Bellow I summarize the next planned actions involving D^2R_1 as well as the possible perspectives for further improvements.

5.2. Vision of the X-ray camera module prototype

The ASIC D^2R_1 has been designed for readout of pixelated CdTe detector. The circuit layout geometry has been organized to match the CdTe detector with 16×16 anode electrodes in a stacked assembly. Figure 5.1 illustrates the view of the first prototype, with gold-stud bump connections between the ASIC and the detector and with bond-wire connections between the interface PCB and the ASIC.

5.2.1. Measurements with CdTe detector

Once the elementary prototype is finished, the complete characterization will be possible. Noise performance of the complete system will be evaluated through spectroscopic acquisition with a radioactive source.

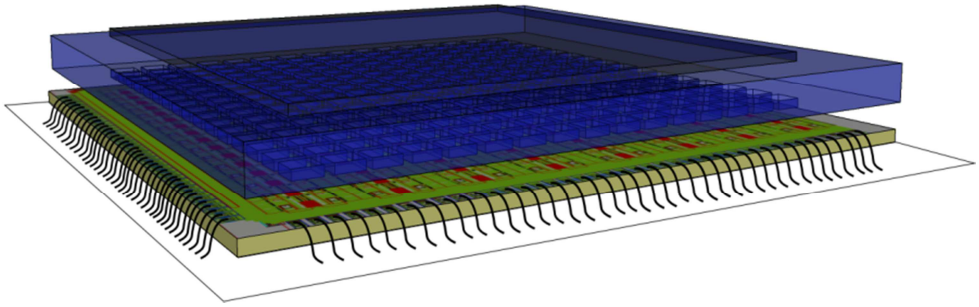

Figure 5.1 Image of the spectro-imaging camera prototype with D^2R_1 ASIC and pixelated CdTe detector on the top with 256 readout electrodes and pixel pitch of $300\ \mu m \times 300\ \mu m$.

5.2.2. Large detection surface

Because the bond pads in the ASIC are placed only along two edges, this first prototype can be used to construct detection focal planes of 32×32 pixels. Four identical 16×16 modules can be arranged in a mosaic with only $600\ \mu m$ space between the modules related to the peripheral area of the ASIC, which would be a dead zone for detection.

5.2.3. Scaling up the ASIC

All of the D^2R_1 processing channels are identical. Their architecture and readout topology enables the construction of a readout ASIC with any number of these pixel-size units. Consequently a readout array for detectors of any size can be produced, as long as the detector pixel pitch remains at $300\ \mu m$.

In practice one must pay attention to maintain the low impedance power supply nets. Therefore, if very large matrices are envisaged, an additional gap between the typical 16×16 units might be desired for additional routing of the power signals. Also in case of the analog output, the output signal speed has to be verified with the long and narrow metal path and the drive strength has to be ensured with the increasing capacitance of the signal routing.

There are three main reasons why increasing the ASIC dimensions, together with the corresponding detector size, would be interesting:

- To decrease the power density and the power consumption per channel
- To proportionally reduce the number of IO pins
- To have a detection dead zone smaller than in the case of a few-modules mosaic

The peripheral circuit in the current D^2R_1 ASIC would not need a significant modification with the ASIC scaling. Increasing the array from 16×16, to a four-times larger one 32×32 would require only 2 additional LVDS drivers and 16 additional output buffers. This would make the total of only 20 additional IO pins, $5.4\ mW$ of additional power consumption within the peripheral circuits (that constitutes only $30\ \%$ of D^2R_1 peripherals' consumption) and only 2-times larger peripheral area, assuming the $300\ \mu m$-wide peripheral ring. Simple calculations show that the total balance in each of the three criteria: power consumption, pin count and detection dead zone is better every time the readout ASIC size is doubled.

Finally if studies would confirm that 9-fold extension of the ASIC size is feasible from the routing impedance and drive-strength point of view an ASIC of identical architecture extended to 96×96 readout channels could be organized so that the IO pads are arranged only along a single edge, making the ASIC 3-sides buttable. This would be a great achievement in terms of construction possibilities with large detection surfaces.

5.2.4. Space qualifications

The hybrid module with stacked CdTe and D^2R_1 envisaged for space-borne application has a long path of additional qualifications. This is an integral part of the instrument development. First of all it includes mechanical tests involving the complete module, where, for example, the immunity against shock and vibrations are studied. The second set of tests must prove the readout electronics against the radiation exposure in the space environment. These qualifications include Total Ionizing Dose (TID) and Single Event Effects, like latch-up or up-set. Most of the radiation hardness tests can be carried out with the ASIC only, instead of employing the complete module. Therefore this issue does not need to await completion of the hybridization process. More importantly any eventual weakness should be detected as early as possible to leave time in the overall development for necessary fixes. D^2R_1 is based on experience with the Caterpylar ASIC, whose performance has been evaluated with TID of up to $1\ Mrad$, as presented in the paragraph 3.4.6. The new ASIC has good prospects for the TID qualification simply by because it uses identical CSA as in the Caterpylar testchip. More importantly the fact of using the same technology increases confidence in the space qualifications results.

5.2.5. Emerging alternative IC technologies

Together with colleagues from my project team we have already anticipated possible scenarios of outcomes from the space qualification tests. During development of the D^2R_1 ASIC, a new IC technology satisfying our choice criteria became accessible. The Caterpylar testchip has been exported with identical CSA electrical structures into new layout rules of AMS $0.18\ \mu m$. This second testchip is called Caterpylar AMS.

The options offered with this IC technology, including the number of metal layers and presence of MIM capacitors, make it a possible alternative to export the D^2R_1 ASIC, if this step would be ever indispensable.

Secondly the experimental measurements obtained with the AMS counterpart of the Caterpylar are equally satisfactory, as demonstrated in [11].

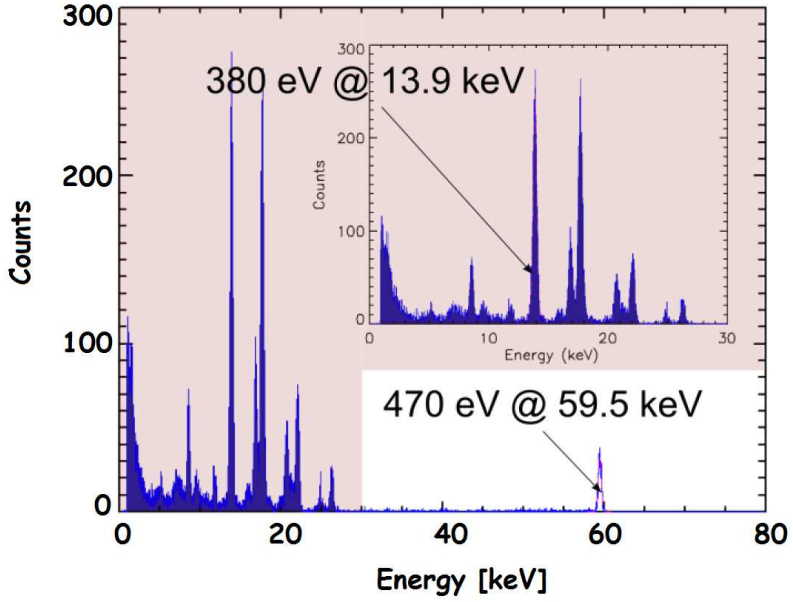

Figure 5.2 Spectrum of the ^{241}Am source obtained with $0.8 \times 0.8 \times 0.33\ mm^2$ Si diode and the ASIC Caterpylar AMS [11] – counterpart of the Caterpylar testchip however realized in a different technology, AMS $0.18\ \mu m$. Measurement conditions: 0 °C, detector bias voltage $65\ V$, on-chip CSA biased with $10\ \mu A$ resulting in power consumption of $14\ \mu W$, measurement with external CR-RC^2 shaper with peaking time set to $18\ \mu s$. The achieved FWHM resolutions are: $380\ eV$ at $13.94\ keV$ and $470\ eV$ at $59.54\ keV$.

In fact, in parallel with the XFAB Caterpylar spectroscopy tests with Si diode (presented in the paragraph 3.4.5), the same experiment was repeated with the Caterpylar AMS testchip. We have irradiated the ASIC with the most popular source of reference: ^{241}Am. Measurements performed at the temperature of 0 °C, higher than in the case of the previously presented results (from paragraph 3.4.5), gave a reason to lots of excitement. The result is presented in Figure 5.2 with an FWHM resolution of $470\ eV$ at $59.54\ keV$. Meanwhile a zoom to the low-energy band reveals the triple line emerging at $18\ keV$.

With this excellent result, that confirms the level of low noise/low power front-end expertise gained in our group in the last three years, I conclude this thesis.

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ANNEX I

Calculation of the ENC with the optimal filter: Cusp

The optimal filter with the two-step solution

The detection system, for which the optimal filter will be derived, is depicted in Figure 2.32. For simplicity of the derivation the flicker noise is assumed negligible and is not included. With the CSA output noise spectrum derived in the paragraph 2.2.6, the CSA output noise spectrum corresponding to the detection chain from Figure 2.32 is:

$$v_{nCSA}{}^2(\omega) = v_{nth}{}^2 \cdot \left(\frac{\omega C_{IN} + \omega C_{CSA} + \omega C_F}{\omega C_F}\right)^2 + \frac{i_{nIN}^2}{(\omega C_F)^2} \qquad \text{A1-1}$$

If the CSA output noise was white, the matched filter theory could be applied directly to conclude the transfer function of the optimal filter. However the equation shows that the noise spectrum at the CSA output is not flat. The issue of signal detection in the presence of colored noise is not uncommon in processing systems and there are methods to deal with that.

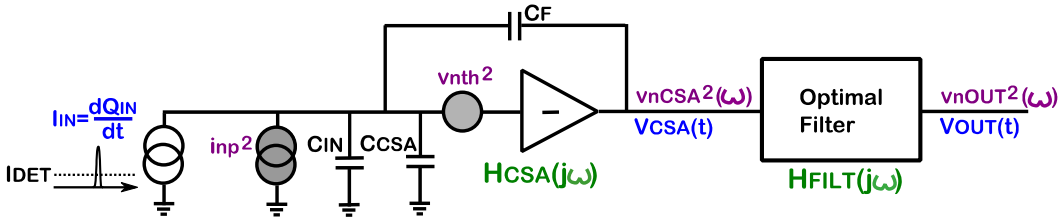

Figure A1.1 The schematic used for the optimal filter analysis.

The common solution to the optimal processing of a signal in the presence of a non-white noise is based on the two-step approach [51][52]. The "unknown" optimal filter is split into two parts, as illustrated in Figure A1.2: the noise whitening filter and the matched filter. The white noise assumption is fundamental for obtaining the matched impulse response. With the whitening filter the CSA output noise is transformed to a white distribution $v_{n\,white}{}^2$. The signal $V_{templ}(t)$ on the whitening filter output is surrounded by the white noise. It can be now processed in the conditions of the best signal to noise ratio, by direct application of the matched filter method.

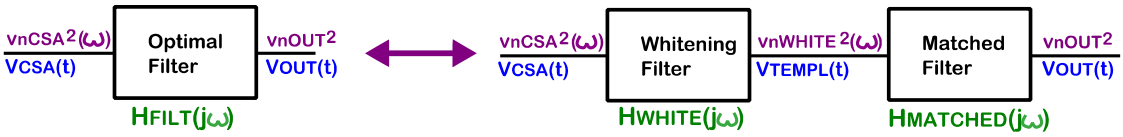

Figure A1.2 Illustration of the derivation method for the optimal filter in the radiation detection chain: non-white (colored) noise ${v_{nCSA}}^2$ is transformed to a white distribution ${v_{n\,white}}^2$ with signal output $V_{templ}(t)$ also distorted by the whitening filter. The step response of the whitening filter is the template for the impulse response of the matched filter $h_{matched}(t)$.

The noise whitening network requires knowledge of the input noise sources PSD, that is the CSA output noise: ${v_{nCSA}}^2(\omega)$. A filter with the following transfer function $H_{white}(\omega)$ transforms the noise spectrum from ${v_{nCSA}}^2(\omega)$ to an approximation of white spectrum ${v_{n\,white}}^2$:

$$H_{white}(j\omega) = \frac{C_F}{(C_{IN}+C_{CSA}+C_F)\sqrt{{v_{n\,th}}^2}} \cdot \frac{\omega(C_{IN}+C_{CSA}+C_F)\sqrt{{v_{n\,th}}^2/{i_{n\,p}}^2}}{1+\omega(C_{IN}+C_{CSA}+C_F)\sqrt{{v_{n\,th}}^2/{i_{n\,p}}^2}} \qquad \text{A1-2}$$

Consequently for the given CSA and the detector (Figure 2.32) the filter with the transfer function $H_{white}(j\omega)$ is the whitening filter. The white noise PSD at the output of the filter is: ${v_{n\,white}}^2 = 1$. The filter description corresponds to a high pass filter with the exponential step response, with the time constant τ_{white} equal to:

$$\tau_{white} = (C_{IN}+C_{CSA}+C_F)\sqrt{{v_{n\,th}}^2/{i_{n\,p}}^2} \qquad \text{A1-3}$$

Furthermore the transient response $V_{templ}(t)$ at the whitening filter output, resulting from the input charge Q_{IN} (at the CSA input) is:

$$V_{templ}(t) = \frac{Q_{IN}\cdot 1(t)}{C_F} \cdot \frac{C_F}{(C_{IN}+C_{CSA}+C_F)\cdot\sqrt{{v_{n\,th}}^2}} \cdot e^{-t/\tau_{white}} \qquad \text{A1-4}$$

In the last equation both the detector and the CSA are assumed ideal. The detector responds to an X-ray event with a Dirac current pulse, carrying charge Q_{IN}. In result, the unity step function $1(t)$ appears in the expression – related to response of the ideal CSA to the charge Q_{IN} arriving at the time instant $t = 0$. Any X-ray event in the detector results in an identical response of the whitening filter $V_{templ}(t)$, scaled with the Q_{IN} value. The output of the whitening filter $V_{templ}(t)$ is referred to as a template signal – it is the expected shape of the signal to be detected. It is plotted in Figure A1.3 (blue).

A1. Calculation of the ENC with the optimal filter: Cusp

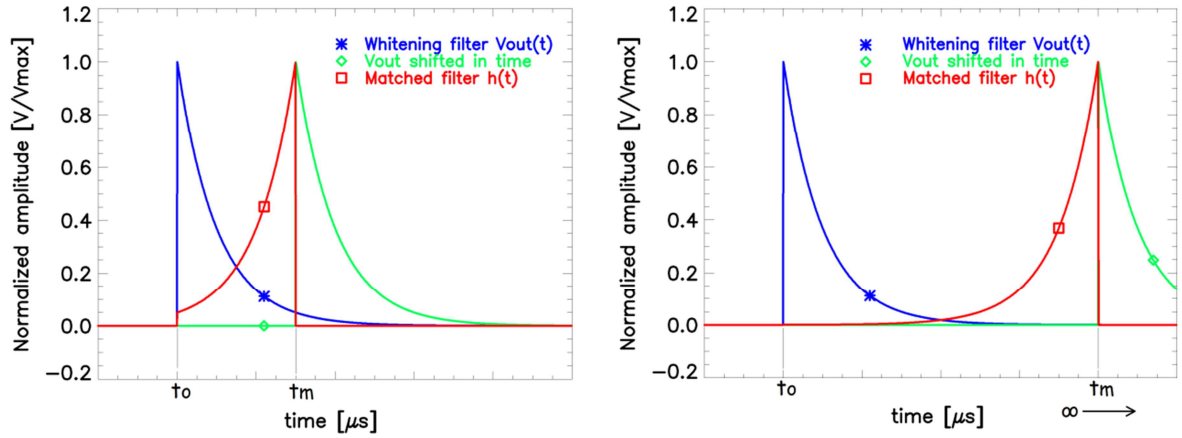

Figure A1.3 Illustration of the process of how the matched filter impulse response is created: the whitening filter output $V_{templ}(t)$ (blue) is shifted by t_m (green), then inversed in time results in the desired impulse response $h_{matched}(t)$ (red). Two examples of different measurement times are shown, the longer t_m the better matching between the matched filter and its input signal.

According to the matched filter theory the impulse response of the filter providing the best ENC is a mirror image of the template, scaled by a factor k, and shifted in time by t_m [52]. Thus the matched filter impulse response can be concluded:

$$h_{matched}(t) = 1(t) \cdot k \cdot V_{templ}(t_m - t) = 1(t) \cdot k_1 \cdot e^{(t-t_m)/\tau_{white}} \cdot 1(t_m - t) \qquad \text{A1-5}$$

The impulse response of the matched filter is illustrated in Figure A1.3 (red). The two illustrated examples are plotted for different measurement times t_m with respect to a fixed time of the event arrival and the instantaneous whitening filter response $V_{templ}(t)$ at $t_0 = 0$. The matched filter impulse response is not strictly the mirror image of the template waveform, but it is truncated at $t < t_0$. The response would be an exact time-inversed "matched" copy if t_m was in infinity, however this case is of course non-realizable.

Let's look on the filter output response $V_{out}(t)$ to the signal $V_{templ}(t)$. The output response of the detection system from Figure 2.32 with the CSA and the optimal filter (composed of the noise whitening and the matched filter) is obtained by convolution of the signal $V_{templ}(t)$ and the impulse response $h_{matched}(t)$:

$$V_{out}(t) = V_{templ}(t) * h_{matched}(t) = \frac{k_1 Q_{IN}}{\tau_{white}\sqrt{{i_n}_p^2}} \int_0^{\infty} 1(t-u) \cdot 1(t_m - t + u) \cdot e^{\frac{-t_m - 2u}{\tau_{white}}} du \qquad \text{A1-6}$$

The convolution is equivalent to cross-correlating the signal $V_{templ}(t)$ and the time-inversed impulse response $h_{matched}(-t)$. The cross-correlation reaches the maximum when the two functions are identical (scaled). This results in obtaining the possibly highest signal power present at the system output $V_{out}(t)$. This justifies the choice of the matched filter characteristics.

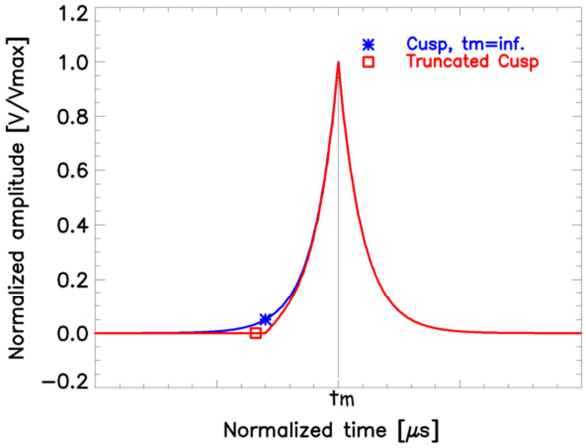

Figure A1.4 Response $V_{out}(t)$ of a radiation detection system with CSA and the optimal filter. Two cases of the measurement time are considered: with $t_m = \infty$ resulting in the Cusp-shaped output response (blue) and with a finite t_m resulting in the truncated Cusp output response (red).

The resulting output waveform $V_{out}(t)$ is demonstrated in Figure 2.33. Two scenarios of t_m are illustrated: the finite measurement time and with the measurement time approaching infinity. In the ideal case with $t_m = \infty$ the signal shape is called Cusp. This shape is expected to provide the lowest ENC. In the practical realization the measurement is performed within a finite interval after the event and the system response has form of a truncated Cusp, with loss of the measured signal power.

ENC of the readout chain with the optimal filter

With the known characteristics of the optimal filter – the Equivalent Noise Charge can be now calculated for the detection system from Figure 2.32. To perform the task, first of all two quantities have to be calculated: the maximum value of the output voltage $V_{out}(t)_{MAX}$ and the total integrated noise at the output $\overline{v_{n\,out}{}^2}$. The highest output voltage corresponds to the time instance t_m when its peak value is measured, which according to the equation *A1-6* yields:

$$V_{out}(t)_{MAX} = V_{out}(t_m) = \frac{Q_{IN} \cdot k_1}{2 \cdot \sqrt{i_{n\,p}{}^2}} \qquad \textit{A1-7}$$

The total integrated output noise is obtained from the known impulse response of the filter *A1-5*, by first applying the Parseval's theorem to the frequency domain expression:

$$\overline{v_{n\,out}{}^2} = \int_0^\infty v_{n\,white}{}^2 |H_{matched}(2\pi f)|^2 df = \frac{v_{n\,white}{}^2}{2} \int_{-\infty}^{\infty} |h_{matched}(t)|^2 dt = \frac{k_1{}^2 \tau_{white}}{4} \qquad \textit{A1-8}$$

Finally the ENC for the optimal detection system with the matched filter can be calculated with the following formula:

$$ENC^2 = \frac{\overline{v_{n\,out}{}^2}}{V_{out}(t)_{MAX}{}^2 / Q_{in}{}^2} \cdot \frac{1}{q^2} = (C_{IN} + C_{CSA} + C_F) \cdot \sqrt{v_{n\,th}{}^2 \cdot i_{n\,p}{}^2} \cdot \frac{1}{q^2} \qquad \textit{A1-9}$$

This is the lowest possible ENC achievable in a system with a given CSA and the detector, where the noise parameters ($v_{n\,th}{}^2$ and $i_{n\,p}{}^2$) as well as the capacitances (C_{IN}, C_{CSA} and C_F) are fixed. The

same result is obtained solving the lowest ENC problem in the frequency domain without separation of the intermediate whitening stage, for reference I recommend [47] and [4].

Final conclusions on the optimal filter

The best filter for the radiation detection in the presence of white noise sources has been presented. The flicker noise contribution has been neglected in the filter optimization this far, since it makes calculations significantly more complicated. An optimal filter that takes it into account is described in [5]. It requires some modifications of the transfer function. In the resulting response of the system the output signal shape $V_{out}(t)$ is found to be narrower in the middle and wider at the tail in comparison with the optimum filter for white noise sources only. Excluding this modification all the three noise parameters can be still calculated from the known filter characteristics.

Finally, from the system's output response to the instantaneous input charge Q_{IN} (in equation *A1-6*) – the weighting function of the detection chain with the optimal filter can be obtained. The weighting function is the inversed impulse response of the complete system shifted by the measurement time t_m, expressed as follows:

$$w(\tau) = \frac{k_1}{\tau_{white} \cdot \sqrt{{i_n}_p^2}} \cdot \int_0^{\infty} 1(t_m - \tau - u) \cdot 1(\tau + u) \cdot e^{(-\tau-2u)/\tau_{white}} du \qquad \textit{A1-10}$$

With the known weighting function and using the time domain expressions for the noise parameters I have calculated numerically the noise parameters: A_{th}, A_f and A_p. They are given in Table A1.1 for different values of the t_m/τ_{white} ratio. This ratio, of the measurement time to the whitening filter time constant (*A1-3*), defines the non-ideality of the truncated Cusp response.

Measurement time	A_{th}	A_f	A_p
$t_m = \tau_{white}$	0.75	1.97	0.4
$t_m = 2 \cdot \tau_{white}$	1.08	1.83	0.24
$t_m = 4 \cdot \tau_{white}$	1.92	1.65	0.13
$t_m = 8 \cdot \tau_{white}$	3.7	1.54	0.065

Table A1.1 Noise parameters of the Cusp filter for different values of the ratio t_m/τ_c (measurement time to the whitening filter time constant).

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A2. Noise in the folded cascode CSA

ANNEX II

Noise in the folded cascode CSA

Since the small signal models of the folded cascode and the unfolded cascode are the same, as well as the expressions describing the open loop gain – the following discussion is valid for both architectures.

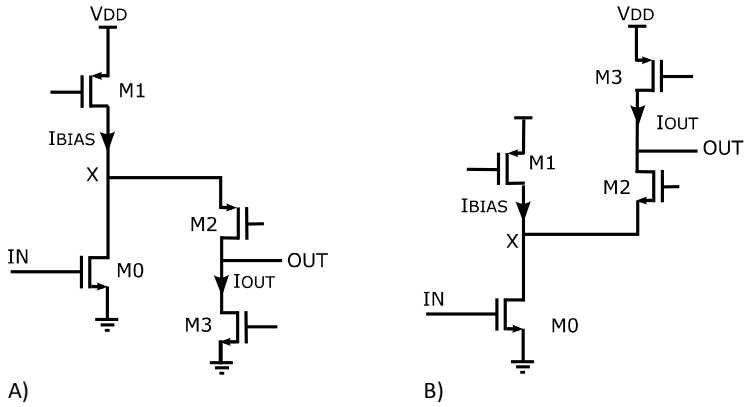

Figure A2.1 Topology of single-ended input amplifier: A) folded cascode, B) unfolded cascode

The basic structure of both amplifiers (Figure A2.1) is constructed with the four transistors:

- the input transistor $M0$
- the current source $M1$ for input transistor bias current I_{BIAS}
- the cascode transistor $M2$
- the current source $M3$ for the output stage with cascode I_{OUT}, typically $I_{OUT} \ll I_{BIAS}$

Each of the transistors $M0 \dots M3$ is characterized with an inherent electronic noise v_{n0}^2 .. v_{n3}^2, referred to its gate. Localization of the four noise sources is illustrated in Figure 3.7. The noise sources include both the thermal and the flicker component. In this paragraph individual equivalent input noise contributions referred to the CSA input v_{nIN0}^2 .. v_{nIN3}^2 are calculated for each transistor [55]. They all add up to the total CSA input referred voltage noise:

$$v_{nIN}^2 = v_{nIN0}^2 + v_{nIN1}^2 + v_{nIN2}^2 + v_{nIN3}^2 \qquad \text{A2-1}$$

The CSA input-referred voltage noise ${v_{nIN}}^2$ corresponds to the CSA serial noise analyzed in terms of the power distribution in the paragraph 2.2.6. Let's now have a look on each transistor noise contribution separately.

A2. Noise in the folded cascode CSA

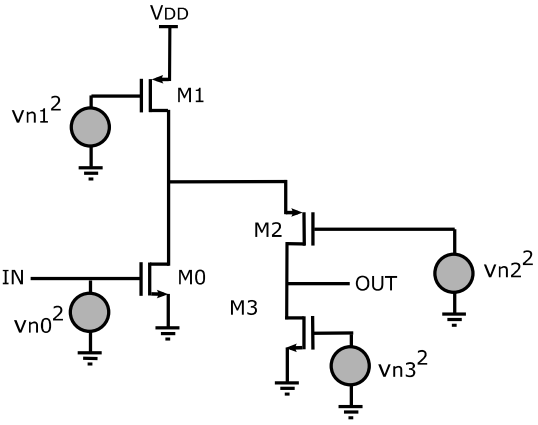

Figure A2.2 Transistor-level CSA: the NMOS-based folded cascode arrangement. Illustration of noise contributions from each transistors. Each noise is referred to the gate of a corresponding transistor.

Transistor $M0$

The input transistor gate is also the amplifier input. Therefore the contribution of $M0$ to the noise referred to the CSA input is equal to the voltage noise of $M0$ referred to its gate. This is simply written as: $v_{nIN0}^2 = v_{n0}^2$.

Transistor $M1$

The voltage noise coming from the transistor $M1$ is first calculated in reference to the output node V_{OUT}. This is done by multiplying the transistor input noise $v_{n1}^2$by the gain between the gate of $M1$ and the CSA output V_{OUT} and can be expressed as:

$$v_{nOUT1}^2 = v_{n1}^2 \cdot {g_{m1}}^2 \cdot \left(\frac{r_{o0} \cdot r_{o1} \cdot r_{o3} \cdot (1 + g_{m2} \cdot r_{o2})}{(r_{o0} + r_{o1}) \cdot (r_{o2} + r_{o3}) + r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2})} \right)^2 \quad \text{A2-2}$$

To refer the $M1$ noise to the CSA input V_{IN} the result is divided by the amplifier's open loop gain:

$$v_{nIN1}^2 = \frac{v_{nOUT1}^2}{A^2} = \frac{v_{n1}^2 \cdot {g_{m1}}^2}{{g_{m0}}^2} \quad \text{A2-3}$$

Transistor $M2$

The voltage noise v_{n2}^2 at the gate of $M2$ is multiplied by gain: from the $M2$ gate to the amplifier output. Thus the $M2$ noise contribution referred to the CSA output is obtained:

$$v_{nOUT2}^2 = v_{n2}^2 \cdot \left(\frac{g_{m2} \cdot r_{o2} \cdot r_{o3} \cdot (r_{o0} + r_{o1})}{(r_{o0} + r_{o1}) \cdot (r_{o2} + r_{o3}) + r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2})} \right)^2 \quad \text{A2-4}$$

Secondly the result is divided by the amplifier open loop gain to finally express the $M2$ noise contribution at the CSA input:

$$v_{nIN2}^2 = \frac{v_{nOUT2}^2}{A^2} = v_{n2}^2 \cdot \left(\frac{g_{m2} \cdot r_{o2} \cdot (r_{o0} + r_{o1})}{g_{m0} \cdot r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2})} \right)^2$$

It can be easily simplified to: *A2-5*

$$v_{nIN2}^2 = \frac{v_{nOUT2}^2}{A^2} = v_{n2}^2 \cdot \left(\frac{r_{o0} + r_{o1}}{g_{m0} \cdot r_{o0} \cdot r_{o1}} \right)^2$$

Transistor $M3$

Similarly like in case of $M2$, the voltage noise of $M3$ is first referred to the CSA output by multiplying it by the gain between the gate of $M3$ and the amplifier output:

$$v_{nOUT3}^2 = v_{n3}^2 \cdot \left(\frac{g_{m3} \cdot r_{o3} \cdot \left(r_{o2} \cdot (r_{o0} + r_{o1}) + r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2}) \right)}{(r_{o0} + r_{o1}) \cdot (r_{o2} + r_{o3}) + r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2})} \right)^2 \quad \textit{A2-6}$$

Consequently the result is divided by the amplifier gain to obtain the input-referred voltage noise due to $M3$:

$$v_{nIN3}^2 = \frac{v_{nOUT3}^2}{A^2} = v_{n3}^2 \cdot {g_{m3}}^2 \left(\frac{r_{o2} \cdot (r_{o0} + r_{o1}) + r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2})}{g_{m0} \cdot r_{o0} \cdot r_{o1} \cdot (1 + g_{m2} \cdot r_{o2})} \right)^2 \quad \textit{A2-7}$$

That can be simplified to:

$$v_{nIN3}^2 = \frac{v_{nOUT3}^2}{A^2} = v_{n3}^2 \cdot \frac{{g_{m3}}^2}{{g_{m0}}^2} \left(\frac{r_{o0} + r_{o1}}{g_{m2} \cdot r_{o0} \cdot r_{o1}} + 1 \right)^2$$

Substituting the formulas describing individual contributions to the input referred noise into *3-9* I obtain the complete expression describing the total CSA input voltage noise:

$$v_{nIN}^2 = v_{n0}^2 + \frac{v_{n1}^2 {g_{m1}}^2}{{g_{m0}}^2} + v_{n2}^2 \left(\frac{r_{o0} + r_{o1}}{g_{m0} \cdot r_{o0} \cdot r_{o1}} \right)^2 + v_{n3}^2 \frac{{g_{m3}}^2}{{g_{m0}}^2} \left(\frac{r_{o0} + r_{o1}}{g_{m2} \cdot r_{o0} \cdot r_{o1}} + 1 \right)^2 \quad \textit{A2-8}$$

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A3. Full-fit noise model to calculate ENC with any shaper

ANNEX III

Full-fit noise model to calculate ENC with any shaper

General description of the noise extraction

The ENC measurements (shown in Figure 3.32) performed with the Caterpylar ASIC and the CR-RC^2 shaper are used to extract precise noise information of each of the CSA from the ASIC. It will serve for more general system ENC calculations, with a wide range of the detector input parameters (capacitance and dark current). The parameters extraction is achieved by taking into account the whole measurement series $ENC(t_{peak}, C_{IN})$, e.g. all points from Figure 3.32 for the specific CSA.

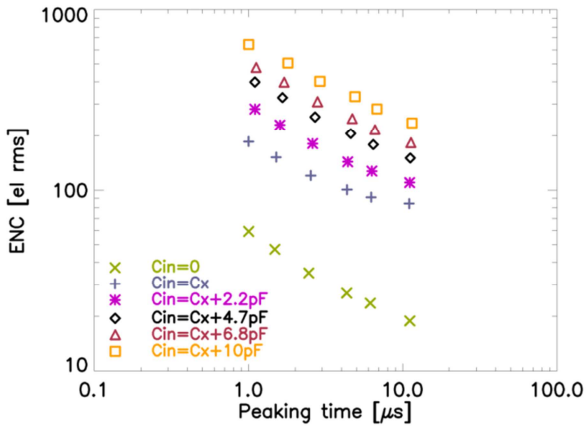

Figure A3.1 Example of CSA $ENC(t_{peak}, C_{add})$ characterization for extraction of the series noise parameters: ENC with CR-RC^2 shaper as a function of the measured peaking time for input capacitance C_{IN} ranging from $0\ pF$ to $C_x + 10\ pF$. CSA T6 with thin oxide PMOS $300\mu m/0.25\mu m$ input transistor, bias current set to $10\ \mu A$. The value of $C_x = 2.7\ pF$ is found in the parameter extractions described later in this chapter.

The set of measurements $ENC(t_{peak}, C_{IN})$ shown in Figure 3.32 characterizes the system with a specific CSA ($T6$ in this case) and with the CR-RC^2 shaper at different conditions of the peaking time and input capacitance. The characterization is done at a fixed CSA bias current. Each of the measurement points fulfills the already known equation:

$$ENC = \sqrt{{ENC_{th}}^2 + {ENC_f}^2} \qquad \text{A3-1}$$

Where the contribution of the parallel noise has been neglected because of the very low CSA input DC current $I_{comp} = 0.2\ pA$. The two remaining ENC contributions: thermal ENC_{th} and flicker ENC_f are equal to:

$${ENC_{th}}^2 = \frac{1}{q^2} \cdot \frac{1}{t_{peak}} \cdot v_{n\,th}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_{th} \qquad \text{A3-2}$$

$$ENC_f{}^2 = \frac{1}{q^2} \cdot v_{n\,f}^2 \cdot (C_F + C_{IN} + C_{CSA})^2 \cdot A_f \qquad \textit{A3-3}$$

where $C_{IN} = C_{add} + C_x$. In these equations the capacitance C_{IN} is split into the two parts distinguishable in the setup: C_x and C_{add}. The parameters A_{th} and A_f are related to the filter type. In these measurements with the CR-RC^2 they are equal to 0.85 and 3.41 respectively. Furthermore, the peaking time t_{peak}, the feedback capacitance C_F and the additional input capacitance C_{add}, are also known in the measurements. On the other hand there are four unknown parameters: $v_{n\,th}^2$, $v_{n\,f}^2$, C_{CSA} and C_x. By distinguishing the three types of measurements:

- with no bonding, $C_{IN} = 0$,
- with bonding but with no additional external capacitance, $C_{IN} = C_x$,
- with additional external capacitance, $C_{IN} = C_x + C_{add}$,

Proposed extraction strategy

I have proposed a strategy for extraction of these unknown parameters. First the initial conditions of the full-fit algorithm were determined. That is – the four unknowns parameters were pre-estimated as follows:

- Thermal noise $v_{n\,th}^2$ determined from the sensitivity $\Delta ENC/\Delta C_{add}$ at $t_{peak} = 1\ \mu s$ obtained in analytical calculations
- The capacitance C_{CSA} determined from the measurement point: $ENC(1\ \mu s, C_{CSA})$ using the previously obtained $v_{n\,th}^2$
- The flicker noise $v_{n\,f}^2$ determined from the measurement point: $ENC(11\ \mu s, C_{CSA})$ – again using the already obtained $v_{n\,th}^2$
- The capacitance C_x determined from the measurement point $ENC(1\ \mu s, C_{CSA} + C_x)$ using the above values of $v_{n\,th}^2$, C_{CSA} and $v_{n\,f}^2$

Then each of the unknown parameters was recursively adjusted, in a numerical loop, towards the direction that minimizes the total squared error (by increment or decrement). With every iteration the ENC was calculated and compared with the measurements – at the given C_{IN} and t_{peak} values. The total squared error is a quality factor that determines how close to measurements is the ENC model calculated with the four extracted parameters. The error E_r has been defined as follows:

$$E_r = \frac{100\%}{N_{points}} \sum_{t_{peak}} \left[\left(\frac{ENC_{meas} - ENC_{calc}}{ENC_{meas}} \right)^2_{at\ C_x=0} + \sum_{C_{add}} \left(\frac{ENC_{meas} - ENC_{calc}}{ENC_{meas}} \right)^2_{at\ C_x+C_{add}} \right] \qquad \textit{A3-4}$$

Each difference of the measurement-calculation pair: $\left[ENC_{meas}(t_{peak}, C_{IN}) - ENC_{calc}(t_{peak}, C_{IN})\right]$ in the error expression *A3-4* is weighted by its measured value ENC_{meas}. Thus all points have a fair contribution to the total error. It is analogous to the mean square percentage error. The number N_{points} equals to the total number of measurement points $ENC(t_{peak}, C_{IN})$ in the CSA data set. Typically it is 36, since each CSA has been characterized with six conditions of the input capacitance each at six values of the peaking time. However due to issues most likely related to faulty measurements – in some cases the lowest or the highest peaking times have been excluded or a series of a specific C_{add} value has been skipped. At the end, in the extraction process of each CSA, at

least four peaking times were included with input capacitance conditions C_{IN} of: zero, C_x and at least three values $C_x + C_{add}$. Because in the best case – all of the measured points take part in the algorithm, I have called the finally obtained model: the full-fit model.

Results of the noise parameters extraction

The parameters extraction procedure has been implemented in the IDL calculation environment. The output result of the procedure is a set of four parameters: $v_{n\,th}^2$, $v_{n\,f}^2$, C_{CSA} and C_x, which can be directly applied to the equations *A3-2* and *A3-3* to obtain the two ENC contributions.

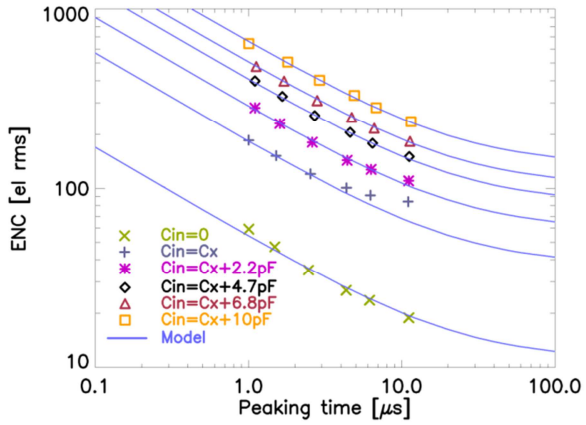

Figure A3.2 ENC measurements with the Caterpylar ASIC and the external CR-RC^2 shaper as a function of measured peaking time. The measurements are compared with the full-fit model based on the extracted parameters. The corresponding input capacitance and CSA T6 with $10\ \mu A$ are identical as in the measurements in Figure 3.32. Values of the extracted parameters in this specific case are: $C_x = 2.7\ pF$, $C_{CSAin} = 1.14\ pF$, $v_{n\,th} = 8.1\ nV/\sqrt{Hz}$, $v_{n\,f} = 0.84\ \mu V$. The total mean squared percentage error between the model and the measurements is 0.072%.

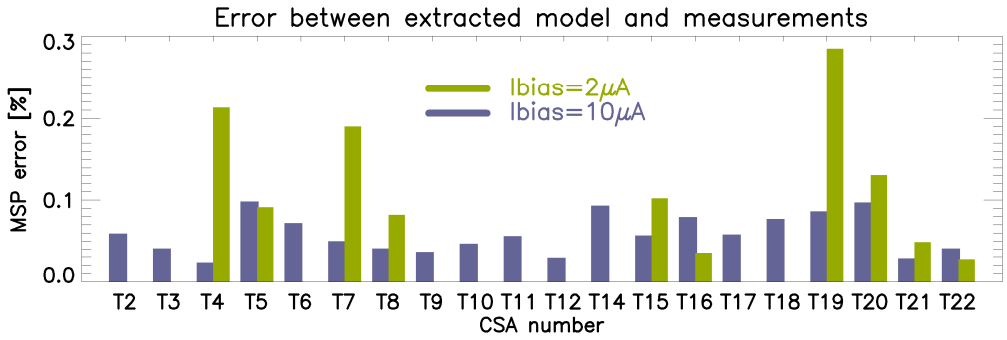

Figure A3.3 Mean square percentage error between the full-fit model with extracted parameters and the measurements. Values are shown for all characterized CSA with bias current set to $10\ \mu A$. For some CSA also the result at $I_{BIAS} = 2\ \mu A$ is shown.

The same measurement example as shown in Figure 3.32 is presented again in Figure A3.2, this time together with the extracted model. The resulting total error E_r between the measurements and the calculated model is 0.072% in this particular example of CSA T6 with I_{BIAS} set to $10\ \mu A$. The total error values for the complete extraction project for the Caterpylar ASIC are shown in Figure A3.3. The fit procedure for measurements with $10\ \mu A$ bias current results in: the maximum error not exceeding 0.1%. In case of characterization with $2\ \mu A$, however, the error is typically higher and reaches up to 0.3%. The main reason for the errors is the high noise present in measurements, related to the high

value of C_{IN} in this experiment, much higher than expected with the small pixel CdTe detector in the final application. This makes the measurements of the output amplitude more difficult and less precise. As already mentioned – some data of the full measurement set that have appeared faulty, have been removed for a better fit, but some remaining points are still corrupted with measurement errors.

ANNEX IV

Analysis of Caterpylar noise parameters obtained with the Full-fit model

Studies of the extracted noise parameters

A number of CSA circuits from the Caterpylar ASIC, each with different dimensions of the input transistor was analyzed with the Full-fit model (Annex III). It resulted in a set of noise parameters: C_{CSA}, $v_{n\,th}^2$, $v_{n\,f}^2$ and C_x obtained for each CSA. Their analysis is especially interesting in case of the extracted noise described theoretically with several mathematical models. It is not obvious which one fits the most the given application. More significantly, what was interesting for me in this exercise, is the confirmation – which of the simulation models corresponds better with the obtained measurements: BSIM3v3 or SPICE2. Both noise models are available in the simulation kit of the chosen technology XFAB $0.18\,\mu m$ and in the simulations they have demonstrated ENC values considerably far apart. The importance of the noise characterization is empowered by the fact that the MOS operates between the moderate and the weak inversion. This transition region with low drain current densities is rather difficult to model.

Among the obtained results on the top of the variety of physical dimensions, there are also measurements of CSA at two different values of the input transistor bias current. These bring additional conclusions. Table 3.8 provides a list of parameters that I took into account in the results analysis with indication: which design variables are relevant.

Parameter	I_{BIAS}	W	L	W/L	$W \cdot L$	$W \cdot L^2$
C_{CSA}					✓	
$v_{n\,th}^2$	✓	✓		✓		
$v_{n\,f}^2$	✓		✓		✓	✓

Table A4.1 Extracted CSA noise parameters: analysis of CSA design parameters with respect to mathematical models.

CSA capacitance

The CSA input node capacitance C_{CSA} has been extracted with the full-fit model both from the measurement and from the simulation data sets. The results are shown in Figure A4.1. It is observed that the simulation based capacitance is always slightly lower than the parameter obtained from the measured data. In case of PMOS transistors the difference in values is between 10 and 20%. For NMOS based CSA the discrepancy is larger, especially in case of the CSA T15 and T16, whose input transistors are the same as T21 and T22 and whose dimensions are the smallest of all NMOS-based CSA. I expect this is due to inaccuracy in the measurements, resulting in imprecise full-fit output results. All the other results are consistent with the proportional gate area.

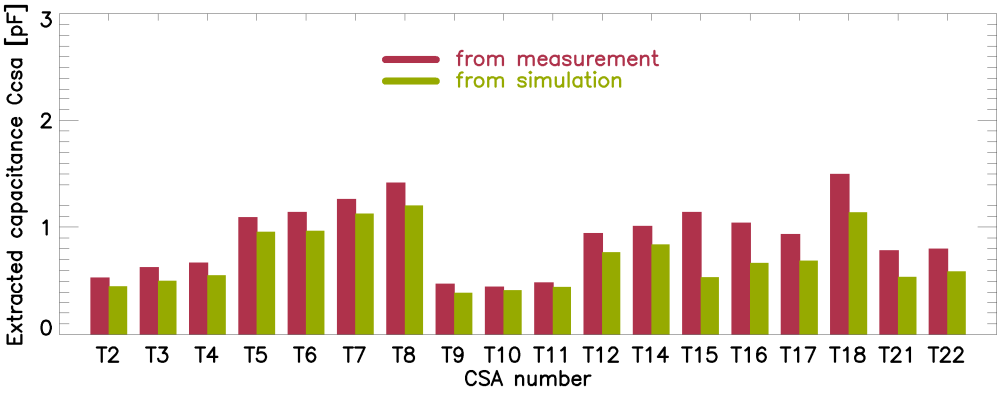

Figure A4.1 Capacitance C_{CSA} extracted with model fit from measurements and from simulations.

Thermal noise

The input series thermal noise is the second of the three parameters extracted for the CSA from the IDeF-X Caterpylar. Typically, models of the transistor thermal noise state that the voltage noise depends inversely proportionally on the transconductance [11][19][55]:

$$v_{n\,th}{}^2 = \frac{4 \cdot k \cdot T \cdot \gamma}{g_m} \qquad \text{A4-1}$$

While the coefficient γ has a value fixed with the operating region, the transconductance model strongly depends on the operating point [19]. Meanwhile the transconductance has a known dependency of the bias current and transistor dimensions. Understanding of the transconductance model is especially useful in the rough hand-calculations of thermal noise, useful in analog design. In strong inversion the transconductance fulfills the relation *3-48* whereas in the subthreshold it depends only on the bias current according to *3-49* [19]:

$$g_m \sim \sqrt{I_{BIAS} \cdot W/L} \qquad \text{A4-2}$$

$$g_m \sim I_{BIAS} \qquad \text{A4-3}$$

Of the entire CSA bias current range possible with the Caterpylar ASIC even the highest of $12\ \mu A$ locates the input transistor at the edge of the moderate and the weak inversion. My target was to find out which of the expressions *3-48* or *3-49* better describe the operating region and which of the thermal noise models: SPICE2 or BSIM3v3 reflect the measurements more accurately.

Figure A4.2 shows the absolute value of the thermal noise obtained for PMOS and NMOS CSA, as a function of the W/L ratio. In the case of the PMOS-based CSA the subthreshold region appears to be more relevant (with comparison to the relationship *3-49*): only small variations are observed in the thermal noise when the transistor dimensions ratio W/L increases by nearly a decade. On the contrary: the thermal noise of NMOS-based CSA significantly decreases with W/L increase by only a factor of two. Simple calculations show that the strong inversion model could be a better approximation to illustrate the effect of variable W/L in case of the CSA with NMOS as the input transistor.

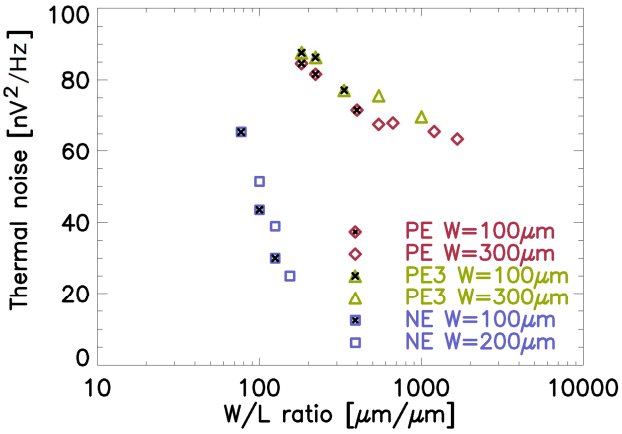

Figure A4.2 Thermal noise as a function of the input transistor W/L ratio. All data presented for CSA biased with $10\ \mu A$.

The noise characteristics in Figure A4.2 distinguish between two different widths of each input transistor type: the higher one of $300\ \mu m$ ($200\ \mu m$ in case of NMOS) and the lower one equal to $100\ \mu m$. A remarkable effect is observed with all CSA: at the same W/L ratio but different absolute dimensions – the thermal noise is systematically shifted: to a lower value with the greater width. The shift appears to be predictable: Figure 3.34 shows the thermal noise ratios of two CSA with the same length and different widths. The measurement-based values are nearly constant for all input transistor types. Simulations results show similar effect only when the SPICE2 model is used.

Meanwhile the theoretical ratio ${v_{n\,th\,300\mu m}}^2/{v_{n\,th\,100\mu m}}^2$ calculated for the saturation g_m model is:

- for PMOS CSA $\frac{{v_{n\,th1}}^2}{{v_{n\,th2}}^2} = \frac{g_{m2}}{g_{m1}} = \frac{\sqrt{100\ \mu m}}{\sqrt{300\ \mu m}} = 0.58$
- for NMOS CSA $\frac{{v_{n\,th1}}^2}{{v_{n\,th2}}^2} = \frac{g_{m2}}{g_{m1}} = \frac{\sqrt{100\ \mu m}}{\sqrt{200\ \mu m}} = 0.71$

In the subthreshold regime, the theoretical ratio would approach the value of 1 in both cases. The ratios obtained in reality from the measurements lie always in between the two results (Figure 3.34).

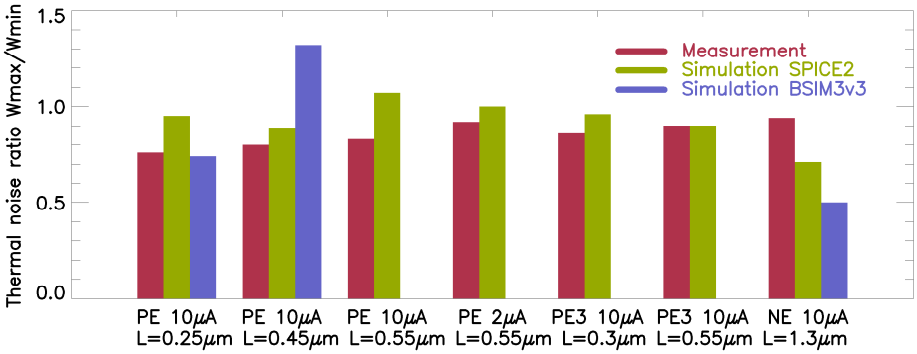

Figure A4.3 Ratio of thermal noise at $300\ \mu m$ and $100\ \mu m$ width ($200\ \mu m$ and $100\ \mu m$ for NMOS). Each ratio is calculated for two CSA of identical input transistor type and length, with a fixed bias current.

The additional results shown in Figure 3.35 give supplementary arguments towards the subthreshold g_m model. The chart shows thermal noise ratios, each obtained for the same CSA with different bias current. The theoretical values predicted from respective operating region models are:

- saturation model $\frac{{v_{n\,th1}}^2}{{v_{n\,th2}}^2} = \frac{g_{m2}}{g_{m1}} = \frac{\sqrt{2\ \mu A}}{\sqrt{10\ \mu A}} = 0.45$
- subthreshold model $\frac{{v_{n\,th1}}^2}{{v_{n\,th2}}^2} = \frac{g_{m2}}{g_{m1}} = \frac{2\ \mu A}{10\ \mu A} = 0.2$

Meanwhile the ratios obtained from the measurements oscillate between 0.2 and 0.25, resolutely following the weak inversion model. Meaningful is the fact that the SPICE2 model shows again results that are consistent with the measurements.

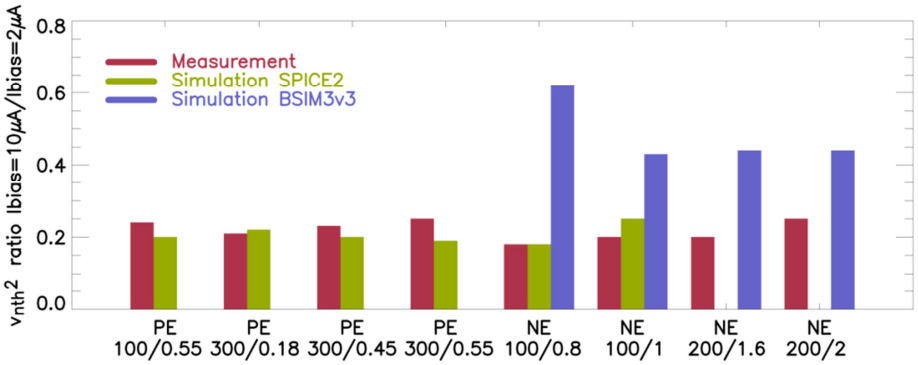

Figure A4.4 Ratio of thermal noise at two values of I_{BIAS}: $10\ \mu A$ and $2\ \mu A$ for a given CSA with fixed input transistor dimensions. Characterization of PMOS and NMOS CSA of various W and L dimensions.

The absolute value of the thermal noise extracted for the PMOS type CSA is higher in simulations than in measurements: up to 30% with the bias current of $10\ \mu A$ and up to 60% with I_{BIAS} set to $2\ \mu A$. Comparing the measurement results with the simulation results – the general trend is that the SPICE2 noise model is again much more accurate than the BSIM3v3 model.

In conclusion – the analyses of the thermal noise show that the overall CSA noise behaviour is too complex to characterize it with any of the simplified transconductance models (*3-48* and *3-49*). The important and extremely useful outcome of this analysis – is the consistency between the thermal noise obtained experimentally and the simulation results using the SPICE2 model. The indicated simulation model provides results of the squared noise ${v_{n\,th}}^2$ well within an order of magnitude. This conclusion has a key consequence in the future development of the complete readout ASIC, where the power consumption is set to be very low. In the final application with current densities expected to be very low – the selected noise model: SPICE2 is expected to ensure a good precision.

Flicker noise

The results of the flicker noise extraction from the Caterpylar measurements are presented in Figure A4.5. The parameter values are plotted as a function of the input transistor gate area. They are grouped with respect to CSA of the same width and bias current. In case of the PMOS-based CSA the extracted noise shows the following properties:

- Values are very similar for both oxide types: thin PE and thick PE3,
- Points extracted for two CSA of the similar gate area but with different widths show lower flicker noise at smaller W and higher L,
- Strong dependency of bias current is observed for the same PMOS CSA characterized at $2\ \mu A$ and at $10\ \mu A$.

In case of the NMOS-based CSA however the parameters are not consistent and the extrapolation of the individual points does not lead to an expected monotonic curve where noise decreases with gate area. Most likely the parameters extraction from measurements was not precise enough. I expect that the measurements were done at peaking times, where the thermal noise still has a dominating influence over the flicker noise. Extending the peaking time used in measurements to much higher values should increase the ${v_{nf}}^2$ extraction precision, if only the parallel noise contribution could be still neglected.

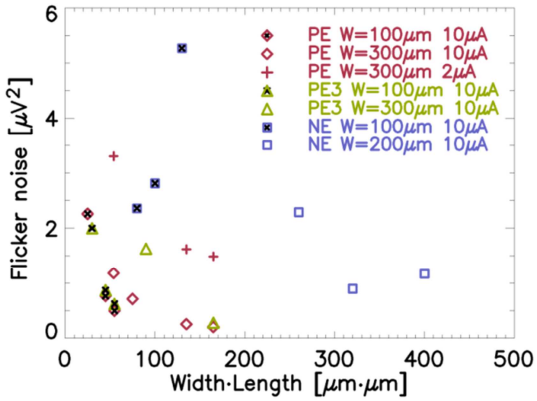

Figure A4.5 Flicker noise as a function of the input transistor gate area $W \cdot L$. Points are grouped with respect to CSA of identical transistor type with the same width and bias current.

In pursuit of the PMOS transistor flicker model I have studied its inverse proportions with respect to: L, WL or WL^2. The analysis with respect to gate dimensions would not indicate a specific noise model that follows the measurements. However the last proportion: WL^2, shows an interesting behaviour. It is demonstrated in Figure A4.6, where the axis $\langle x;\ y\rangle$ are chosen to the following coordinates:

$$\langle x;\ y\rangle = \langle W \cdot L^2;\ {v_{nf}}^2 \cdot W \cdot L^2\rangle \qquad \text{A4-4}$$

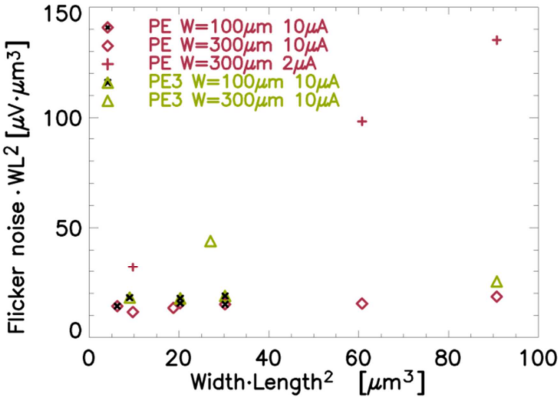

Figure A4.6 Analysis of flicker noise with respect to inverse proportionality to WL^2. x- axis shows the variable WL^2, y-axis is the flicker noise multiplied by the x-value. Results only shown for the CSA with the PMOS input transistor.

The plot in the given form should have a constant y-response for all points obtained for specific oxide thickness if the flicker noise model is correct:

$${v_{nf}}^2 \sim \frac{1}{C_{ox} \cdot W \cdot L^2} \qquad \text{A4-5}$$

Indeed Figure A4.6 shows trend towards a flat distribution, except for the measurements at the lowest bias current.

Meanwhile it should be remembered that the BSIM3v3 flicker noise model constitutes a sum of two terms: $A \cdot \frac{{I_{BIAS}}^2}{C_{ox} \cdot W \cdot L^2}$ and $B \cdot \frac{I_{BIAS}}{C_{ox} \cdot L^2}$, whereas the SPICE2 flicker model is only described by $C \cdot \frac{I_{BIAS}}{C_{ox} \cdot L^2}$ [11]. Because of the observations from Figure A4.6, where the width appears to be of high importance, not alike in the SPICE2 model – I have decided to compare the measurements only with the BSIM3v3 model simulations. Figure 3.36 shows flicker noise comparison: between the measured and the simulated values.

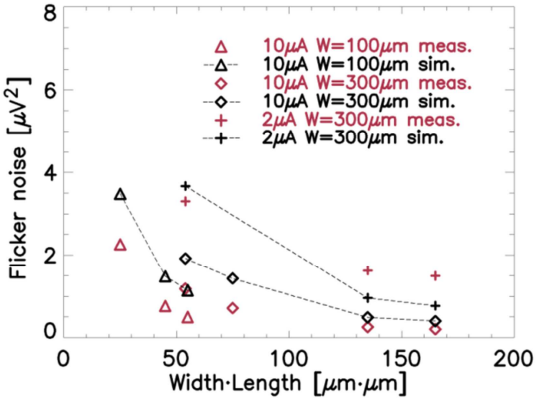

Figure A4.7 Comparison of flicker noise extracted from simulations and from measurements. Presented results for thin oxide PMOS input transistor at different width (100 μm and 300 μm) and bias current (2 μA and 10 μA). BSIM3v3 has been used as the noise model in simulations.

Systematically the absolute value is always slightly higher in simulations, yet the extrapolated profiles appear very similar in case of the measured and the simulated points. Only, as already pointed out in Figure 3.36, the curve obtained at $2\ \mu A$ current is not consistent with the trend. With the conclusion that the two points obtained at the highest lengths were not accurately extracted in the measurements (what is more likely at low bias currents with much higher ENC level) – the inconsistence in Figure A4.6 may be explained.

Parasitic capacitance C_x

Of all the parameters extracted from the Caterpylar measurements C_x is the only one not related to the CSA and ASIC. It represents an external parasitic capacitance characteristic to the measurement setup. Precisely it is mainly a stray capacitance between the ASIC and the additional capacitance C_{add} connected externally. The setup has been realized in the way that the external capacitance can be easily replaced with a different value. The simplicity came at the cost of the parasitic capacitance of the PCB path. Depending on which CSA is measured – a different PCB path is connected to the CSA input pad (out of the nine existing on the socket PCB. The absolute C_x value known from the parameter extraction ranges from 2 to $3\ pF$. It may slightly differ from one board to another, variations of up to 15% have been registered. However for a single CSA characterized at $2\ \mu A$ and at $10\ \mu A$ the value should be constant, even if other extracted parameters change. Figure A4.8 shows comparison of the parasitic capacitance C_x extracted from measurement sets with bias current of: $2\ \mu A$ and $10\ \mu A$. Except for the CSA T4, T15 and T16, where the difference is more significant, in all the other cases the C_x extracted twice for the same CSA remain within proximity of 7%. The results

confirm the previous conclusions: that the noise parameters extraction based on the full-fit model together with the proposed measurement setup is a reliable and reproducible method for the CSA characterization and ENC estimation.

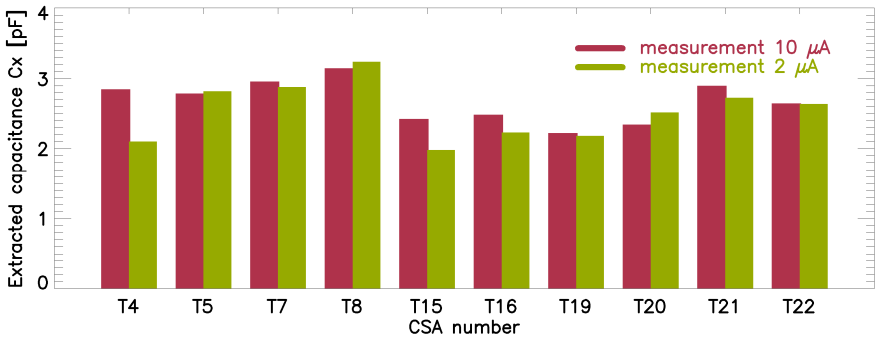

Figure A4.8 Extracted parasitic capacitance C_x related to the socket PCB used in the measurements. Values shown for CSA characterized with two values of the bias current: $10\ \mu A$ and $2\ \mu A$. Ideally the capacitance should be independent of the current.

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