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Development of a CdTe spectro-imaging for space application

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"Il n’y a que ceux qui ne font rien qui ne font jamais d’erreurs" *Un grand sage qui se reconnaitra*

"Le second, de diviser autant de parcelles qu’il se pourrait, et qu’il serait requis pour les mieux résoudre" *R, Descartes*

"Sans adversité, le courage s’amoindrit" *Sénèque*

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Abstract

Hard X-ray astronomy is a privilege witness of the most violent phenomena of our universe such as supernovae, black holes, neutron stars, active galactic nuclei for instance. Such phenomena are still largely unknown, and the systematic study and measurements of their signatures would enhance our understanding of the primal stages of our universe.

In this thesis, I focus on the study of thermonuclear supernovae, which requires highly sensitive telescopes in order to perform extra-galactic observation. Today's telescopes need improvement in their focusing optic as well as their central focal plane performing photo-detection.

Work on this topic has been performed for a long time by the CEA/IRFU (Institut de Recherche sur les loi Fondamentale de l'Univers) which succeeded in the development of X-Ray cameras for scientific missions such as Solar Orbiter or the Space Variable Object Monitor mission. These developments are based on the hybridization of a Cadmium Telluride (CdTe) semiconductor detector linked with an Application Specific Integrated Circuit (ASIC). The development of such integrated circuit is the main frame of this thesis which aims to improve two performances of the detection system: the smallest energy we can distinguish (spectral resolution) and the smallest unit we can distinguish (spatial resolution) through the whole measurement chain.

I will detail such a work in the different parts of this thesis, starting with an introduction on the specific needs and working principle of the Hard X-ray imaging spectroscopy consisting in being able to distinguish the position and energy of a celestial source. I will then detail the principle of low noise integrated circuits dedicated to the measure of such signals. In a third part I will focus on the demonstration of the different developments I have performed to increase the instrumental performances of such a system. Finally, I will detail my work on an integrated circuit able to perform imaging spectrometry at a very high density and fine pitch before concluding on the reached performances and perspectives.

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Glossary

1D 1-Dimension.

2D 2-Dimension.

3D 3-Dimension.

ADC Analog to Digital Converter.

AMS Austria MicroSystem. Micro-technology foundry.

ASIC Application Specific Integrated Circuit.

Auger electron When a vacancy in an atomic orbital of an atom is filled by another electron of the atom, the process can either be radiative, emitting a fluorescence photon, or non radiative, giving the energy difference to another electron of the atom, ejecting it from the atom itself. This ejected electron is an Auger electron.

BLH BaseLine Holder.

CCD Charge Coupled Device.

CDS Correlated Double Sampling.

CdTe Cadmium Telluride.

CR-RC Semi gaussian filter made of different stages of capacitors and resistors.

CSA Charge Sensitive Amplifier.

Cusp Optimal type of filter for radiation sensors. It refers to the shape of the output signal which is pointy.

DC Direct Current.

DDD Displacement Damage Dose.

ENC Equivalent Noise Charge. Corresponds to the output voltage noise refered to the input in the case of a charge measurement devince.

Fano Used in Fano noise, or Fano factor, it expresses the statistic ratio related to Poissonian process for a photoelectric interraction.

Fluorescence Ligth exitation provoked by electron exitation.

FPGA Field Programmable Gate Array.

FR4 Flame resistant 4. Dielectric material used in PCBs.

FWHM Full Width at Half Maximum. For a gaussian distribution, it equals 2.35 times the standard deviation.

GBW Gain to BandWidth product.

HEW Half Energy Width.

HXR Hard X-rays. Corresponds to the light energy spectrum between 1 and 100 keV (2 - 200 pm wavelength).

IC Integrated Circuit.

IDeF-X Imaging Detector Front-end for X-rays.

Leakage current It is the current flowing inside a medium when applying a voltage potential toward its electrodes. For semiconductor detector it is also referred as the dark current, as the current flowing inside the detector when no photon is detected.

Line sensitivity Expressed the minimum photon flux can measure at a given energy.

LVDS Low Voltage Differential Signal.

MCDS Multi Correlated Double Sampling.

METMID Process option to allow for an additional metal layer in the fabrication processing.

Miller effect Characterised by the influence of a voltage amplifier fed back by a capacitor. The Miller effect expresses the fact that in such schematic, equivalent system is the combination of an amplified capacitor at the input of the system and a following voltage amplifier.

MIM Metal Insulator Metal, is a type of integrated capacitance.

MOS Metal Oxide Semiconductor.

NSNS Non Stationary Noise Suppressor.

PCB Printed Circuit Board.

Peaking time Time for a filtered signal to go from 1% of the maximum value of the signal to the maximum value. Directly linked with the shaping time.

pnCCD CCD with pn junction.

PSF Point Spread Function. The response of point source by an optical system.

PZC Pole Zero Cancelation.

RHBD RadHard By Design.

S/R Signal to Noise Ratio. Can also be expressed SNR. It is the ability of a signal to discriminate a signal over its noise.

SEE Single Event Effect.

SEL Single Event Latchup.

SET Single Event Transient.

SEU Single Event Upset.

Shaping time Time constant of a filter.

SN 1a SuperNova type 1a or thermonuclear supernova.

SNR SuperNova Remnant. A fossile of a supernova explosion.

Spatial resolution Is the precision of position measurement. It is expressed in meters (more likely micrometers) but can also be expressed as an angle (in arcsec) for telescopes.

Spectral resolution Expresses the precision of an energy measurement, often expressed in FWHM at a given energy.

SPI Serial Peripheral Interface.

TAC Time to Amplitude Converter.

TDC Time to Digital Converter.

TID Total Ionizing Dose.

ToT Time over Threshold.

ULN Ultra Low Noise process mask.

WDoD Wirefree Die on Die.

Weighting field A geometric field, expressed by applying a voltage unit value to an elctrode and 0 v to the others.

X-FAB Micro-technology foundry.

XH018 XFAB high voltage 180 nm technology.

Chapter 1: Hard X-ray imaging spectroscopy

Hard X-ray (HXR) astronomy is a branch of astrophysics, aiming to witness the most violent phenomena of the Universe, often related to the latest stages of star evolution. Observation in HXR is essential to understand mysterious celestial objects such as black holes, neutron stars, supernovae remnant, or active galaxy nuclei for instance, which are deeply linked to fundamental physics and knowledge of the origins of the Universe.

The Earth atmosphere is opaque in HXR. Consequently, observation of the high energy sky, really started in late 60's with satellite development and space exploration. This intrinsic limitation of atmosphere opacity implies the development of space born telescopes, which makes this instrumentation field very special. Specific instrument design is required in order to cope with space constraints such as intuitive low power consumption, low mass, requirements and reliability, but also radiation hardness and ageing of instrument components as well as cosmic-ray induced background limiting the telescope sensitivity.

The development of HXR instruments is of a prime importance to increase the observational power of faint and transient sources. In this thesis I illustrate a challenging science case on the study of heavy atomic elements creation during a type Ia supernovae explosion.

In such particular case, instruments used nowadays in space telescopes *INTEGRAL* [1], *NUSTAR* [2], or *HITOMI* [3], are still lacking of sensitivity and full detection of such celestial events beyond our galaxy is helpful to support demanding instrument top level requirements. Not only focusing optics in HXR must constantly progress but HXR detectors in focus as well. Needs for wide field of views (~ 10 x 10 $arcmin^2$) and high angular resolution (~ 1 arcsec) will inevitably push the developments of pixelated and modular imaging spectrometer arrays depicted in this chapter. My work anticipates in priority the challenges at detector level where performance must be improved in terms of spatial and spectral resolution.

In the following, I will develop a demanding science case for the future and derive the required detectors properties to reach this goal. On purpose, I will describe the basics of signal generation and working principle of my detector.

I will conclude by suggesting new ASIC development trends, capable of reading out such a detector.

I. Main scientific challenge for hard X-ray

I.1. Thermonuclear supernovae

Stars end of life

Through its lifetime, a star consumes hydrogen, creating heat and heavier compounds through fusion reactions. As hydrogen starts to rarefy, fusion can no longer be sustained and the star leaves its main sequence.

In the case of a low mass star (< 4 times the mass of the Sun) the star expands under higher and higher internal radiation pressure. Star enters a red giant phase. At some point, nuclear fuel decreases, radiation pressure is no longer able to counter gravitational forces, the external layers give rise to a planetary nebula and the core collapses to a white dwarf.

In the particular case of a binary system, constituted of two stars, when the first star gives rise to a white dwarf, it captures the external layer of its companion. The matter is falling onto the white dwarf in an accretion process. The gravitational forces heat the accreted matter, leading the system to shine again. When the white dwarf mass is getting larger than the Chandrasekhar limit (1.4 solar mass), the compact object collapses and an explosion disperses heavy atomic compounds at high speed into the interstellar medium. Such a process is named thermonuclear supernova, or supernova type Ia (SN Ia).

Nickel Observation of SN Ia

This process generates a spread of radioactive ^{56}Ni which decay into ^{56}Co and then ^{56}Fe, emitting characteristics gamma-rays at 158 keV. At the same time, ^{57}Ni is spreadout as well and decays into ^{57}Co and then ^{57}Fe emitting characteristics gamma-rays at 122 keV.

The relation between the proportion of ^{56}Ni and ^{57}Ni is of a prime interest to understand the physical processes of the exploding white dwarf (density, metallicity) [4].

The half-life of both decays are respectively 6 and 270 days. On the other hand, the medium is opaque to photons during the ˜20 first days after the explosion [5]. Hence, direct observation of the ^{56}Ni and ^{57}Co lines is extremely challenging and has never been done before. In the case of ^{56}Ni, the time window to observe the line at 158 keV is only few days before the isotope has fully decayed. Regarding ^{57}Co, the decay is longer but the expected number of nuclei is much smaller. Extremely sensitive telescope with highest achievable energy resolution in HXR is a key to measure this phenomenon. Interestingly, such event is rare in our galaxy (about 1 event/mission life time); high sensitivity would enable routine observations in outer galaxies up to 25 to 50 MPc. On figure 1.1, the expected photon flux in ^{56}Ni and ^{57}Co lines after SN Ia explosion is shown as computed in [6].

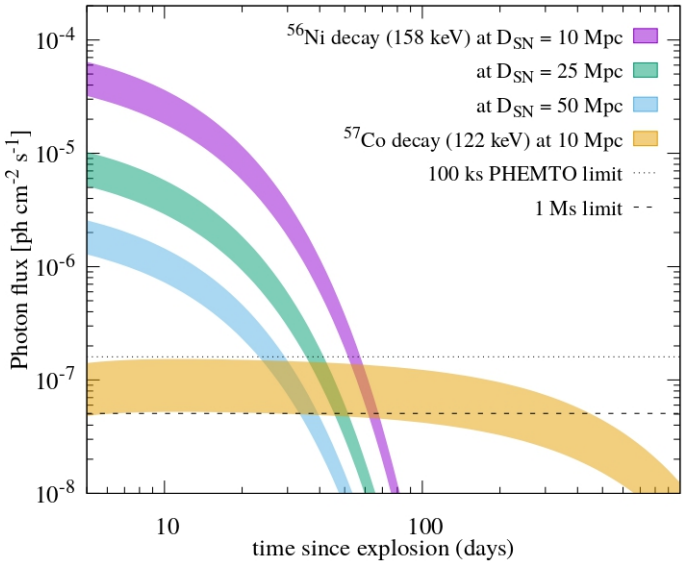

FIGURE 1.1 – *Photon Flux of $^{56}Ni- >^{56}$ Co decay and $^{57}Co- >^{57}$ Fe for various distances [6]. As a matter of fact, density of the supernovae explosion limits the observation of such hard X-ray lines at 20 days after explosion [5]. Hence the plot should be inspected for abscissa starting after 20 days.*

Thus, the requirements for direct observation of such heavy atomic compounds are tremendous and require a high line sensitivity of hard X-ray telescopes down to few $10^{-7} ph.cm^{-2}.s^{-1}$ for a 100 ks observation. At the time being, the sole space observatory able to operates as an imaging spectrometer at 122 keV and 158 keV is ISGRI, on board the ESA *INTEGRAL* satellite. Its line sensitivity is about 10^{-5} $ph.cm^{-2}.s^{-1}$ for a 100 ks observation, i.e. two orders of magnitudes away from the needs.

Titanium Observation of SN remnants

Thermonuclear supernovae (Type I) and core-collapse supernovae (Type II) are both able to produce ^{44}Ti with a different yield. ^{44}Ti is a radioisotope of particular interest due to its long decay time (˜ 854 years), enabling the observation and monitoring of the flux late after the explosion in SN Remnants (SNR). ^{44}Ti radiates gamma-rays at 67.8 and 78.4 keV, in the HXR band. Detection of ^{44}Ti in Cas-A SNR has been recently performed by *INTEGRAL*/ISGRI [7] and successfully imaged by *NUSTAR* [2] to compute the asymmetry of core collapse in this SNR [8].

Both observation of Nickel or Titanium yields in a supernova episode are of a great interest to perform physical analysis on the supernovae creation process. Despite interesting results on ^{44}Ti with Nustar, or even the observation on an upper limit ($7.1 \cdot 10^{-5} ph.s^{-1}.cm^{-2}$) to ^{56}Ni emission with *INTEGRAL* [9], state of the art detectors are lacking of sensitivity to discover events, routinely observe SN and SNR, and constrain SN explosion models with hard X-ray range observations. Breakthrough science is expected if telescope sensitivity could be increased by one to two orders of magnitudes in the next decades. This is the ambition of the PHEMTO proposal recently submitted to ESA Voyage 2050 call [6].

I.2. Sensitivity

The sensitivity of a telescope is expressed as its ability to detect a flux of photons above the background in a given energy range, for a given statistical significance, in a fixed observation time. From an instrument point of view, it can be expressed as the capability to detect celestial source photon flux within 3σ, hence three times the Signal to Noise Ratio (S/N).

The measurement of the signal is superimposed on the focal plane with the diffused signal of all other X-ray sources named Cosmological X-ray Background (CXB) and the signal generated internally by the instrumental background induced by cosmic rays and secondary particles. The source signal and CXB is focused by the optic whereas instrument internal background is not. Noise background and signal undergo a different effective area. Hence it can be expressed as:

$$S/N = \frac{T_{obs}}{\sqrt{T_{obs}}} \frac{N_s.A_{coll}.\epsilon_{det}.\frac{\Delta E}{E}.E}{\sqrt{(N_s.A_{coll} + N_{noise}.A_{det}).\epsilon_{det}.\frac{\Delta E}{E}.E}} \tag{1.1}$$

With [1]:
- T_{obs}, the observation time (in s)
- N_s and N_{noise}, the source and noise flux respectively (in $cts.s^{-1}.cm^{-2}.keV^{-1}$)
- ΔE, the energy range measurement (in eV)
- A_{det} and A_{coll}, the detector and collection area (in cm^2)
- ϵ_{det}, the detector efficiency (in %)

With a given emitted source flux, time, and telescope effective area, the ability to distinguish celestial source of a given flux with a good accuracy can be expressed for each energy, and is the figure of merit one wants to optimize in order to perform science on faint sources.

The broad band sensitivity is expressed in $cts.s^{-1}.cm^{-2}.keV^{-1}$ within an energy band ΔE taken as $\Delta E = \frac{E}{2}$ for each energies. The line sensitivity is expressed at a given energy with $\Delta E =$ energy resolution at E. The narrow line sensitivity is expressed in $cts.s^{-1}.cm^{-2}$ at E. The narrow line sensitivity is a parameter of interest to evaluate the ability of a telescope to detect radioisotopes lines in the science case above.

To illustrate this, let us consider state of the art instruments, and derive their narrow line sensitivity at different energies as shown in figure 1.2.

1. The units used here correspond to astrophysics community standard that differs from international system unit

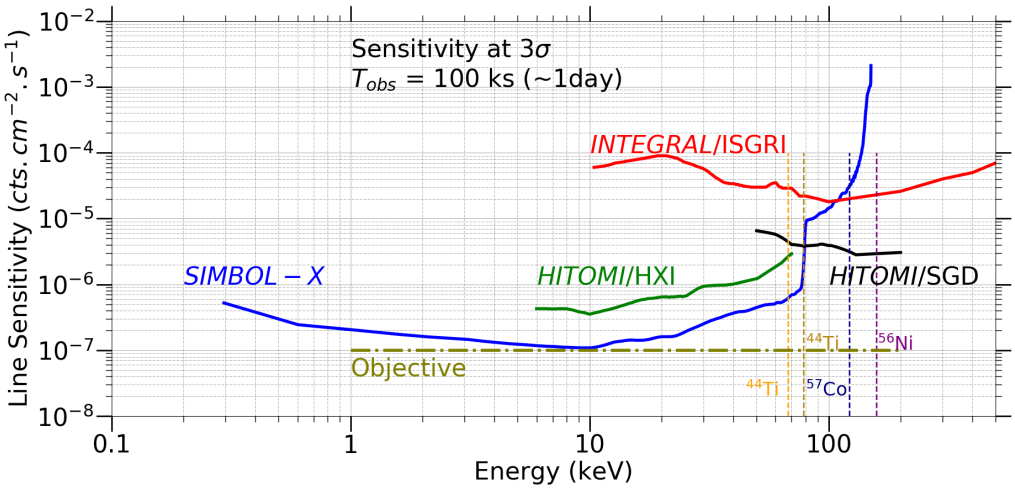

FIGURE 1.2 – *Narrow line sensitivity for different instruments, at different energies. Sensitivity is expressed for a 100 ks acquisition at 3σ signal to noise ratio. For SIMBOL-X data is taken on the behalf of P. Laurent and P. Ferrando (CEA/Dap). For INTEGRAL, data is taken from the 2007 low solar activity on flight calibration update and the observation manual [10]. For HITOMI/HXI and SGD, data was extracted from continuum sensitivity published in [11] and expressed in terms of line sensitivity considering the* $\frac{\Delta E}{E} = \frac{FWHM}{E}$ *instead of 0.5.*

Compared to the previous figure 1.1, it is clear that current instruments are lacking of sensitivity in order to perform the science case expressed before. The development of a novel instrument is hence of a great interest and its specificities can be derived from the analysis on S/N.

S/N is desired to be high enough in order to reduce the minimum sensitivity. As the signal is brought into focus (High S) in a small region of a detector (small N), instruments require a large collection area, a high detector efficiency, a high energy resolution, and a small detector area - The point spread function will be projected on limited number of small pixels where the internal background will be low -.

The collection area is directly linked to the optics defining the ratio between collecting area and detecting area. This optics has been tremendously improved in the last decades, with apparition of hard X-ray focusing optics by use of grazing incidence Wolter type mirrors as illustrated on figure 1.3.

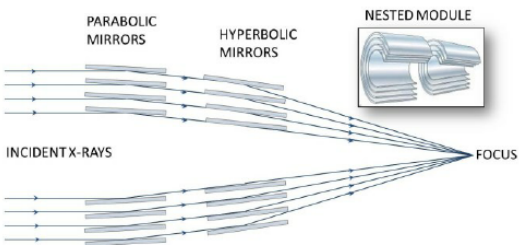

FIGURE 1.3

I.3. Needs for focusing optics

In order to improve sensitivity of instruments, optics is needed to focus light on a smaller detection area. On top of that, the position of celestial source and its shape in the case of an SNR can be determined by resolving the position of impinging photons.

The latter objective has been performed by the use of coded mask optics as it is the case in *INTEGRAL*. However, sensitivity is not affected as detection area is relatively close to the collection area. Hence, hard X-ray measurements have been limited to bright or near sources.

The apparition of Wolter I [12] hard X-ray mirrors, especially through the *NUSTAR* mission has tremendously opened the perspectives on the ability to focus faint sources with a high sensitivity, and reach extremely low flux measurements. Figure 1.4 shows the broad band sensitivity of recent space telescopes around 70 keV. It is clear that focusing telescopes improved the sensitivity by more than one order of magnitude.

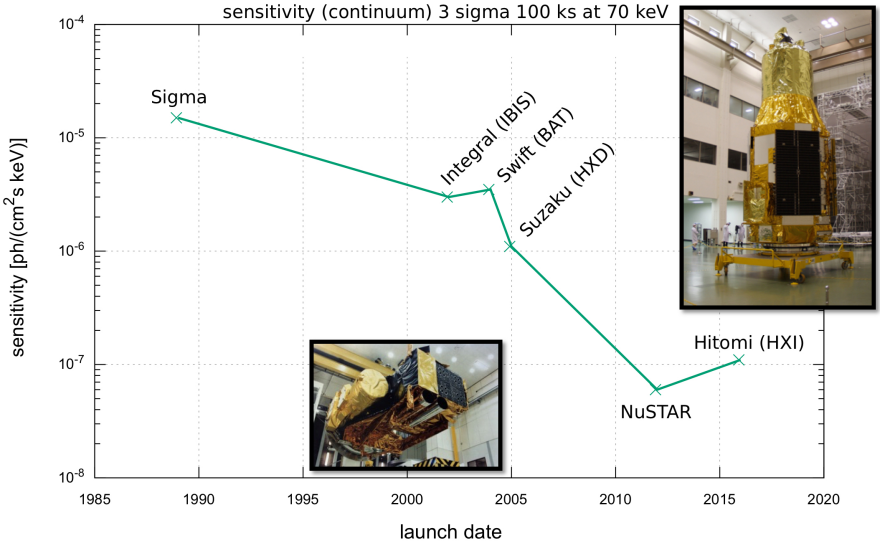

FIGURE 1.4 – *Sensitivity evolution of space mission. The last two telescopes are using grazing angle optics.*

These mirrors reflect X-rays by use of different incident coefficients coating implemented with W/Si or Pt/C and reflect X-rays up to 80 keV (Fig 1.5). Several experimental improvements were made recently to improve energy range with other coating (CoCr/C [13]) up to 120 keV or more. More efforts are needed to reach 200 keV at least.

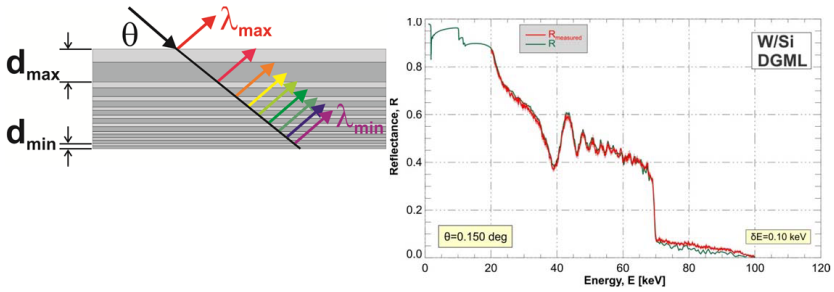

FIGURE 1.5 – *Non-periodic multilayer coating with different bilayer thicknesses in order to reflect X-rays of different wavelengths. Such multilayer coating takes advantage of coherent reflection in order to increase reflectance values for high energies (left). Reflectance response for the W/Si coating used in NUSTAR satellite (right).*

I.4. Building our telescope

The observation of faint sources at high energy X-ray pushes instruments toward their limits. In the scope of building an ideal telescope [6], let us asses the desired properties we dream of in the case of studying supernovae type Ia.

On top of studying the supernovae type Ia, the study of magnetic field along with pulsar and magnestars would require the measurement of polarimetry. Such polarimetry measurement is common for radio-telescopes, but still young and controversial in the hard X-ray energy band. Such a study leads to the following table:

TABLE 1.1 – *PHEMTO scientific requirements*

Parameter	Value	Unit
Energy band	1 - 200	keV
Continuum sensitivity	$6.24 \cdot 10^{-8}$ at 10 keV $6.24 \cdot 10^{-6}$ at 100 keV $1.9 \cdot 10^{-4}$ at 600 keV	$keV.cm^{-2}.s^{-1}$
Narrow Line sensitivity	$1.8 \cdot 10^{-7}$ at 158 keV	$cts.cm^{-2}.s^{-1}$
Minimum detectable polarization	1	%
Angular resolution (HEW)	1	"
Spectral resolution (FWHM)	1 at 100 keV	keV
Field of view	6 x 6	$arcmin^2$
Focal length	100	m

Requirements on the table above are given in the scope of the Voyage 2050 ESA science program. Hence, these are highly constraining and pushes for the development of highly dense and modular pixelated hard X-ray detectors

I.5. Need for highly modular pixelated detectors

A telescope of 100 m focal length and 1" angular resolution (HEW), requires pixels of less than 100 x 100 μm^2 in order to sample the optics Point Spread Function (PSF). For a field of view of 6 x 6 $arcmin^2$, this implies a 20 x 20 cm^2 detector plane area. This leads to a 4 Mpixels detector plane.

The fabrication processes of detector and readout circuit limit the scale of the maximum detector size that can be fabricated. Hence, the 4 Mpixels plane cannot be processed at a time but needs to be built from an assembly of smaller detection units.

This modular character is, required to build such a highly pixelated plane.

This strategy has been used in different previous hard X-ray missions and state of the art devices and parameters will be given later in this section. For now, I detail the process of detection inside such kind of detector, in order to find the correct material, appropriate for the mentioned requirements.

II. Hard X-ray detectors principle

II.1. Light matter interaction

As far as HXR is concerned, sensing medium of interest in this thesis is limited to semiconductors. According to the energy range, different crystals may be used (Si, CdTe, Ge, ...). The two main physical processes involved in the detection of photons are the photoelectric effect and Compton scattering. Both are described in the next two sections.

II.1.a. Photoelectric effect

At low energy, the dominant interaction is the photoelectric absorption. It is a photon-electron interaction of the photon with a bound electron. The photon transmits its entire energy to an electron which is ejected out of the atom. Its kinetic energy is then:

$$E_{photoelectron} = h\frac{c}{\lambda} - E_{boundshell} \tag{1.2}$$

Where h is the Planck constant, λ the photon wavelength, c the celerity and $E_{boundshell}$ the binding energy of the ejected electron to the atomic nucleus, more likely to be the K shell energy as the photon energy is higher to the binding energy.

This photoelectron ejection creates a vacancy that is quickly filled with another electron coming from the atom itself or from the medium. This process can re-emit X-ray photon of lower energy named fluorescence photon, or de-excite through the emission of an Auger electron.

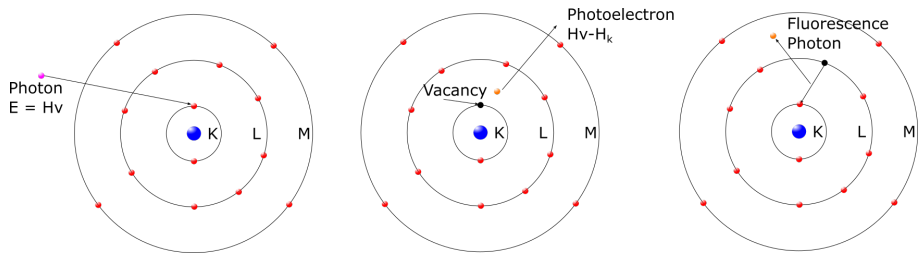

FIGURE 1.6 – *left picture depicts the arrival of a photon interacting with a K shell electron of a sensor. Middle picture shows the photoelectron emitted that interacts with Coulomb electrostatic forces to neighbour atoms. Right picture depicts the case when the vacancy is filled with an external bound shell atom that can emit X-ray fluorescence photons.*

If the pixel size is much larger than the photoelectron and the secondary fluorescence X-ray ranges, the full energy of the impinging photon can be recorded as a single event. This is a key advantage for spectroscopy because the noise is accounted only once in a readout channel. Consequently, the minimum size of a detector or pixel can be decided according to these ranges which typical order of magnitude is a hundred of micrometers at 100 keV in CdTe for instance.

II.1.b. Compton scattering

At higher energies, Compton scattering turns to be the dominant interaction process. Instead of giving all its energy to an atomic electron, the photon scatters and transmits a part of its energy to a recoil electron. The scattered photon energy and the scattering angle are related as described with equation 1.3.

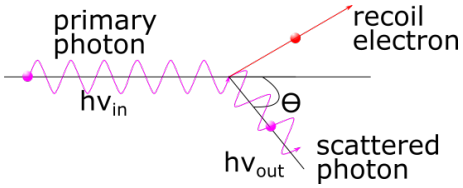

FIGURE 1.7 – *Compton scattering schematic.*

$$h\nu_{out} = \frac{h\nu_{in}}{1 + \frac{h\nu_{in}}{m_e c^2}(1 - cos(\theta))} \tag{1.3}$$

Where $h\nu_{out}$ and $h\nu_{in}$ are the energies of scattered and incoming photons respectively. θ is the scattering angle and $m_e c^2$ is the rest mass energy of electron (0.511 MeV).

The recoil electron interacts through Coulomb forces to give its energy, whereas scattered photon may scatter again, stop by photoelectric effect further away, or escape the detection unit. In that last case, the exact impinging photon energy is not fully detected. The Fig 1.8 illustrates the two interactions of a Compton scattering in a gaseous detector: the principle is the same as in a semiconductor detector but the mean free path of electron is bigger which makes possible to distinguish the two charge deposits.

This process is the basis of imaging detectors for high energy gamma-rays, like those used in nuclear safety gamma cameras.

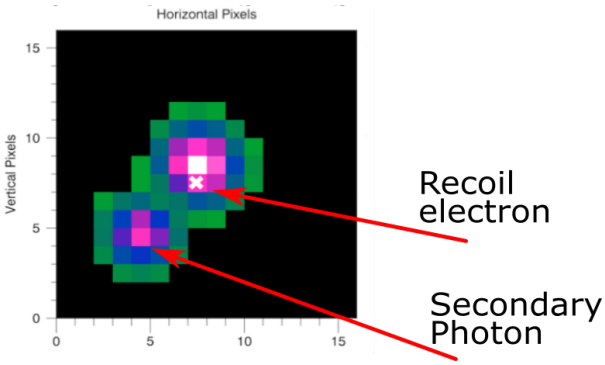

FIGURE 1.8 – *Picture of Compton interaction occurring in pixelated gaseous detector Caliste MM [14]. Colours shows the amount of charge deposit (white is the higher charge, green the smaller).*

II.2. CdTe vs other semiconductors

The choice of the detector to perform hard X-ray imaging spectrometry depends on the requirement on sensitivity expressed before in a given energy band. In order to increase sensitivity, the detector requires to have a high probability to absorb photons up to 160 keV, as the line of ^{56}Ni. This is expressed in the equation 1.1 by the ϵ value.

This probability is linked to the material atomic number, density, and volume.

This leads us to the choice of a high Z atom in order to interact with a high photoelectric absorption probability. CdTe is well suited with a mean Z of 50 (48 and 52 for Cd and Te respectively). Si would not be efficient enough in the HXR while Ge is hardly used when a large detection surface has to be covered due to cryogenic systems requirements. Other specific reasons are explained on the following sections.

Fig 1.9 shows the efficiency of the photoelectric effect at different energies depending on the thickness of a CdTe absorber [15] and compared to other sensing media.

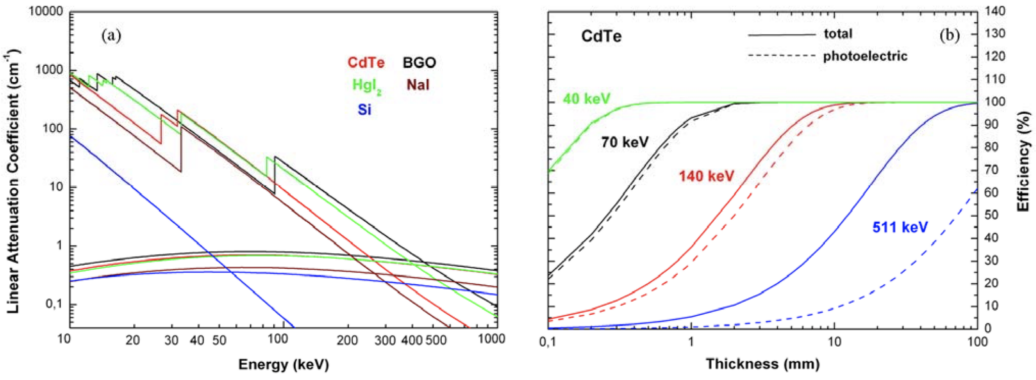

FIGURE 1.9 – *Linear attenuation coefficient function of energy for several semiconductors (left) and efficiency versus thickness for CdTe (right)*

II.3. Principle of detection

II.3.a. Ionization energy

After a photoelectric absorption occurs, a photoelectron is emitted with an energy close to the one of the incoming photons. Its energy is deposited along its path in the medium through Coulomb inelastic interaction, generating electron-hole pairs, which number depends on the chemical composition and structure of the sensing crystal. It is mainly linked to the bandgap of the material. The electrons and holes can be separated and directed towards the detector electrodes by means of a high electric field (~ 100V/mm). This motion creates a transient current related to the energy of the incoming photon.

The ionizing energy corresponds to the mean energy necessary to create one electron-hole pair. Its value is typically three times larger than the bandgap of the semiconductor as a part of the energy is lost in lattice excitation for instance.

In table 1.2, CdTe appears to be a good compromise combining a high Z and density for stopping power and large bandgap for room temperature operations at the expense of quite high ionizing energy.

TABLE 1.2 – *Comparative table between semiconductors*

Material	C (Diamond)	Si	Ge	GaAs	CdTe	Cd(Zn)Te
Atomic Number	6	14	32	31/33	48/52	30/48/52
Density	3.51	2.33	5.32	5.32	5.85	5.81
Bandgap (eV)	5.47 [16]	1.14 [17]	0.67 [17]	1.43 [17]	1.48 [18]	1.52 [18]
Ionization energy (eV/$e^{-}h^{+}$ pair)	15.5 [19]	3.6 [19]	2.4 [19]	4.5 [19]	4.42 [19]	4.6 [19]

Thus, the photoelectric gain of a semiconductor is computed as:

$$N_{pair} = \frac{E_{\phi}}{w} \tag{1.4}$$

Where w is the ionization energy depicted in Table 1.2.

II.3.b. Current generation

A detector can be schematically described as shown in Fig 1.10. It is based on a crystal composed of our semiconductor, with a high electric field ϵ between its two electrodes. Electrons are attracted toward the anode, with the highest potential, whereas holes are attracted towards the cathode, lowest potential. The drift of the charge carriers creates a current as long as they do not reach their respective electrodes or are trapped or recombined by crystal imperfections.

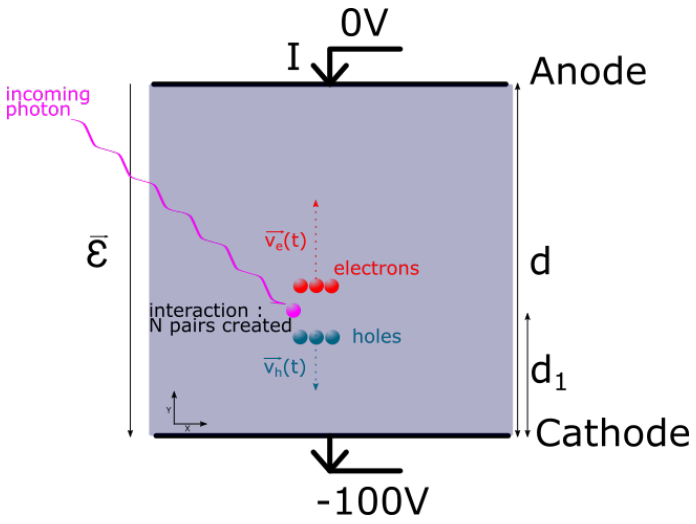

FIGURE 1.10 – *Schematic of a one-pixel planar detector.*

According to the Shockley-Ramo theorem, the current created by N elementary charges through the detector can be expressed as:

$$i(t) = N.q.\vec{v(t)}.\vec{\epsilon}_w \tag{1.5}$$

Where:
- $\vec{\epsilon}_w$ corresponds to the Weighting field (field when $\Delta V = 1$)
- q is the elementary electron charge $1.6 \cdot 10^{-19} C$

$$\vec{v(t)} = \mu.\vec{\epsilon}_d \tag{1.6}$$

- μ is the mobility of electrons or holes in the material
- $\vec{\epsilon}_d$ corresponds to the drift electric field

This general equation can be easily solved in the case of a planar electrode with one pixel and requires a lot more work for a pixelated detector as drift field and weighting field began to differ [20].

TABLE 1.3 – *Comparative table between semiconductors charge carriers mobilities at room temperature [21], [22], [23]*

Material	C (Diamond)	Si	Ge	GaAs	CdTe	Cd(Zn)Te
Electron Mobility $(cm^2.V^{-1}.s^{-1})$	2150	1400	3900	8500	950	1000
Hole Mobility $(cm^2.V^{-1}.s^{-1})$	1700	600	1900	400	80	100

The total detector output current is the sum of the hole induced current and the electron induced current. These currents can be very different especially in CdTe considering the significant difference between electron and holes mobilities (see table 1.3). Assuming a uniform mobility through the entire detector, and N electron-hole pairs created, the output current is constant and expressed as:

$$i(t) = N.q.(\mu_e + \mu_h).\frac{\Delta V}{d^2} \tag{1.7}$$

The time before collection or recombination of the charges depends on the bias voltage and the interaction depth. Assuming the interaction occurring at a distance d_1 from the cathode, collection times are:

$$\begin{aligned} t_e &= \frac{d.(d-d_1)}{\mu_e.\Delta V} \\ t_h &= \frac{d_1.d}{\mu_h.\Delta V} \end{aligned} \tag{1.8}$$

The resulting currents are shown in Fig 1.11.

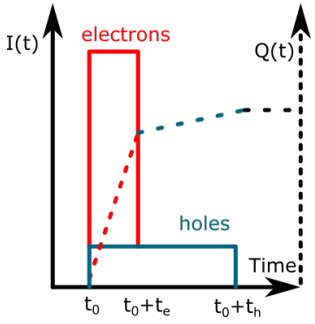

FIGURE 1.11 – *Temporal evolution of electron and hole charge and transient current signal*

For high resolution spectroscopy, the aim is to be able to collect the whole charge. This implies either a long integration time, or to limit the transit time for holes (slow carriers). At low energy X-rays, exposing cathode to the X-rays privileges photons to interact close to the cathode. In this case, most of the signal is due to electron transport while holes only travel a short distance to the cathode. In case of deep interactions, an optimal solution is to get rid of the hole signal, using the detector in a single carrier mode which is doable using the "small pixel effect" described later.

II.3.c. Charge trapping

Depending on the drift path length and detector impurities, charges can be trapped deteriorating the total measured charge on both electrodes, named charge loss. The

mean drift path of a charge carrier can be expressed as follow:

$$s = \mu.\tau.\frac{V}{d} \tag{1.9}$$

Where μ is the mobility, τ the lifetime, V the bias voltage and d the thickness of detector.

A usual metric to compare the quality of a detector is the $\mu\tau$ product. The higher this product is, the longer a charge carrier can drift without getting trapped. Table 1.4 shows carrier lifetimes and mobilities for CdTe semiconductor. It is relevant to note a poor $\mu\tau$ product of holes compared to electrons. Thus, privileging electron charge transport improves signal quality.

TABLE 1.4 – *Mobility lifetime product for CdTe [22]*

Carrier	Mobility ($cm^2.V^{-1}.s^{-1}$)	Lifetime (μs)	$\mu\tau$ product ($cm^2.V^{-1}$)
Electron	950	1.6	$1.5.10^{-3}$
Hole	80	1.9	$1.5.10^{-4}$

Speeding up the charges by means of a high electric field helps reducing the charge trapping. As expressed in equation 1.10, the charge loss will be negligible when the mean drift path is at least ten times higher than the detector thickness.

$$d < \sqrt{\frac{\mu_e \tau_e V_{bias}}{10}} \tag{1.10}$$

However, this will inevitably increase the leakage current (see page 29). Again, getting rid of the slow carrier contribution, specifically subject to trapping, will help optimizing the signal formation in CdTe.

II.3.d. Small pixel effect:

Applying the Shockley-Ramo theorem [24] to a pixelated detector, the weighting field appears to have a non-linear behaviour. In fact, when the detector thickness is relatively high with respect to the pixel size (typically in a ratio of 1 to 4), the weighting field is no longer linear and appears to have large values close to the pixelated electrodes (see figure 1.12). Considering the equation 1.7, the current is mainly driven by one carrier: electrons. This effect is named "small pixel effect" and helps running the detector in a quasi-single carrier sensor.

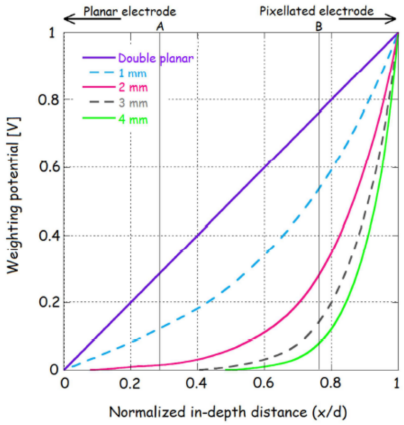

FIGURE 1.12 – *Weighting field comparison between different detector thicknesses and pixelated or planar detector. Pixels have x= 500 µm.*

II.4. Key parameters for highly pixelated spectrometers

In this section, I describe the critical parameters to consider in the architecture of my detector for an imaging spectrometer use.

II.4.a. Segmentation and charge sharing

Collecting the charges after a photon has interacted into the detector allows to build a spectrometer. An imaging spectrometer must be equipped with pixels to determine the location of the interaction in two dimensions. Single crystals placed next to next are a way to proceed but restrict the spatial resolution in the millimeter range. Sub-millimeter range requires the collecting electrodes to be segmented, i.e. patterned with pixels or double-sided strips.

Strips and pixels: Segmentation can be implemented either by Double-sided Strips Detectors (DSD) [25] or by a pixelated detector [26] (see Fig 1.13). DSDs have the advantage of minimizing the number of readout channels ($2n$ channel for DSD, n^2 for pixels). Double-sided strips detectors appear to have a larger capacitance for each channel compared to a pixel pattern with the same pitch. In chapter 2, I explain that such capacitance adds noise to the measurement of the incoming charge, hence degrades the energy resolution. In the scope of this thesis, the development aims at the readout of a pixelated detector.

As mentioned before, the goal is to reach a sub-mm pitch. I chose to design a 250 x 250 μm^2 pixel size detector as an intermediate development toward 100 x 100 μm^2 for PHEMTO. With 250 μm, the small pixel effect is already strong when the detector is at least 1 mm thick. In this configuration, my detector is considered as a single carrier device.

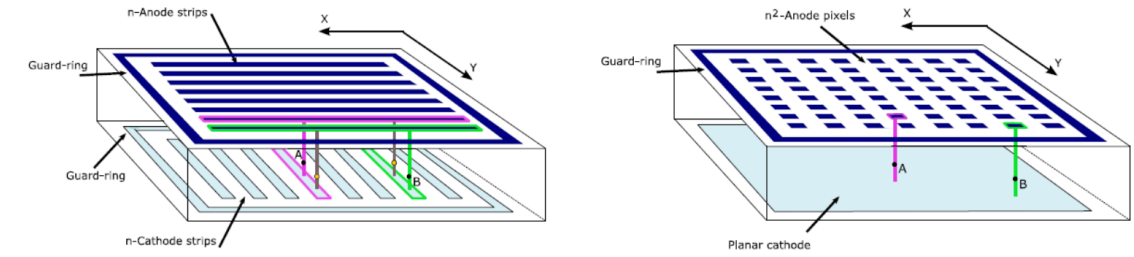

FIGURE 1.13 – *Double sided strip architecture (left) vs pixelated design (right) [27]*

Charge sharing: When a photon interacts in the detector, it creates a first charge cloud made of electron-hole pairs with a spatial distribution dependent on its energy. These pairs diffuse in the detector medium, influenced by electrostatic repulsion. While drifting to the corresponding electrode the charge cloud expands by diffusion mechanisms. If this cloud is large enough or the interaction occurs between two pixels, then the total deposited charge is shared between the neighbour pixels.

This charge sharing effect [28], [29] is not desirable for imaging spectroscopy. Image reconstruction computation is necessary to compute the exact location of a pixel interaction when two pixels have been hit. Furthermore, energy is measured with more than one channel. When for instance two channels are fired, the noise is increased by a factor $\sqrt{2}$ compared to a single-pixel energy readout.

Considering a detector of thickness d and applying a potential of V between its electrodes, charge cloud radius due to diffusion is computed as:

$$r = 1.15d\sqrt{\frac{2kT}{qV}} \tag{1.11}$$

Where k is the Boltzmann constant, T the temperature and q the elementary electron charge.

Such equation is a key to optimize a detector design. Having a relatively thick detector would increase the charge sharing effect when biased to a moderate voltage.

Compromising the detector efficiency in the range of 100-200 keV, the pixel pitch, the charge sharing effect, and the small pixel effect brings me to a detector thickness ranging from 0.75 to 2 mm. the lowest will optimize the spectroscopy by limiting the charge loss with a low applied voltage while the thickest will optimize the photopeak efficiency, the small pixel effect and the pixel stray capacitance. My system will be compatible with this thickness range.

II.4.b. Energy resolution

The mean number N of electron-hole pairs is proportional to the energy deposit E of the impinging photons. E is the full energy in case of photoelectric interaction considered hereafter. The true number of electron-hole pairs is subject to statistical fluctuations based on a random Poissonian process. The expected variance of electron

hole pair creation is N where N is the number of pairs created and expressed in equation 1.4. In practice it has been shown [30] that each electron-hole pair creation is not a sequence of independent processes but dependent processes, showing that the process is not strictly Poissonian.

The ratio between the variation of a Poissonian process and the electron-hole pair creation process has been extensively measured for each semiconductor and is named the Fano factor F, leading to the following expression of the energy standard deviation.

$$\begin{aligned} \sigma &= w.\sqrt{F.N} = w.\sqrt{F.\frac{E}{w}} \\ FWHM_{Fano} &= 2ln(2)\sigma = 2.35.\sqrt{F.E.w} \end{aligned} \tag{1.12}$$

This expression shows that by increasing energy of the impinging photon, the statistical behaviour of the photoelectric process leads to a degradation of the energy resolution. A perfect spectroscopic system can be defined as the one whose contribution to the energy resolution is negligible compared to the statistical behaviour of the standalone detector.

TABLE 1.5 – *Fano factor for different semiconductor at room temperature*

Semiconductor	Fano Factor
C (Diamond)	0.08 [31]
Si	0.125 [32]
Ge	0.13 [31]
GaAs	0.12 [33]
CdTe	0.15 [22]
CdZnTe	0.089 [34]

Since the measurement system measures a charge, the usual expression on its noise is expressed in terms of Equivalent Noise Charge (ENC). Thus, the measurement unit exhibits a noise that can be expressed as:

$$FWHM_{measurementunit} = 2.35 \cdot w \cdot ENC \tag{1.13}$$

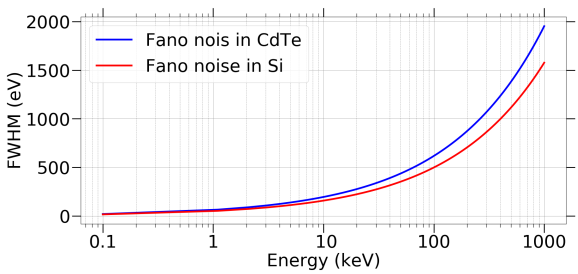

FIGURE 1.14 – *Fano resolution versus Energy*

The total energy resolution equals to:

$$FWHM = \sqrt{FWHM_{Fano}^2 + FWHM_{measurement_{unit}}^2} \tag{1.14}$$

This thesis aims at the design of a so-called Fano limited detection system, i.e with $FWHM_{measurement_{unit}} << FWHM_{Fano}$. This is valid at a given energy as shown on figure 1.14. The usual reference energy for this type of detectors is set to 60 keV (^{241}Am gamma-ray line). The Fano limit is expected to be 469 eV FWHM at 60 keV in CdTe. A Fano limited CdTe detector requires an ENC down to 15 ˜ 20 electrons rms, an extremely demanding requirement for a fine pitch design.

II.4.c. Capacitance

Capacitance influences the thermal and flicker noise of the charge readout electronics (see Chapter 2). To develop an ultra-low noise charge readout, i.e. high spectral resolution, capacitance needs to be computed in order to optimize and match the measurement chain. From the detector point of view, 3 different capacitances are identified, and an analytical model for each one can be found [35].

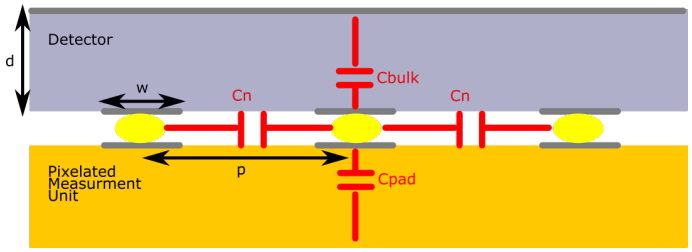

FIGURE 1.15 – *Cross section view of capacitances in a pixelated detector*

•**Bulk Capacitance (C_{Bulk})**: It is the capacitance between pixel and the detector opposite electrode. CdTe acts as a dielectric of high value ($\epsilon_R = 10.3$), thus a capacitance between cathode and anode is dependent on the detector geometry: thickness, width and pitch of pixels. It has been shown [36] that if the ratio between detector thickness and pixel size is significantly larger than 1, the bulk capacitance is larger than a typical planar electrode configuration expressed as:

$$C_{Bulk} = \epsilon_0.\epsilon_{Semicond}.\frac{w^2}{d} \tag{1.15}$$

With w the pixel width and d, detector thickness

A 3D computational analysis of this capacitance with respect to the interpixel pitch and pixel size ratio has shown a dependency between bulk capacitance and pixel size [20]. Such difference needs to be considered for accurate estimation.

•**Neighbour Capacitance (C_n)**: Each pixel can be seen as virtual ground from its neighbour. When interpixel gap is small with respect to the pixel pad itself, the neighbour capacitance is dominant over the bulk capacitance [36].
•**Pad Capacitance (C_{pad})**: Measuring charges implies to use a system that needs to be interconnected to the detector. Such measurement unit has its own capacitance to the ground that is depicted here as C_{Pad}.

Total input capacitance can be estimated:

$$C_{in} = C_{Bulk} + x.C_n + C_{Pad} \tag{1.16}$$

Where x is the number of neighbours (x=4 for pixelated architecture and x=2 for strip architecture).

II.4.d. Leakage current

In solid state physics, electrons can occupy different energy bands, and the probability to have one electron promoted to a given energy band is expressed by the Fermi-Dirac statistics:

$$f(E) = \frac{1}{1 + exp(\frac{E-E_f}{kT})} \tag{1.17}$$

Where E is the band energy, E_f: the Fermi level.

In the case of a semiconductor crystal, two energy bands are of interest, the valence and conduction bands. If an electron belongs to the conduction band, current can flow through the crystal. The more electrons are in the conduction band, the more current can flow. Such quantity is depicted as the charge density. Similar reasoning applies to the valence band for holes.

Knowing the density of charge carriers in the valence (hole) or conduction band (electrons) at a given temperature leads to compute the conductivity of our detector:

$$\sigma = q.n.\mu_e + q.p.\mu_h \tag{1.18}$$

With n and p the electron and hole densities, q the elementary charge and μ_e, μ_h electron and hole mobility.

Such a conductivity leads to a constant current flowing into the detector under the influence of its electric field. This current creates fluctuations on the number of charge carriers in the detector contributing to noise. Measurements have been performed to characterize the leakage current of different detectors in order to choose the most appropriate one [37].

It is possible to express leakage as the following equation:

$$J = J_0 exp(\frac{-\delta E_a}{kT}) \tag{1.19}$$

With J_0 the current density at a given electric field for 0 K, and δE_a the activation energy.

Such an equation allows us to calculate the value of leakage currents in the detector we mentioned earlier at different detector temperatures. These values are reported in Tab 1.6.

TABLE 1.6 – *Leakage current for electrical field of 200V/mm and a pixel size of 250 x 250 μm^2*

Detector	J_0 ($\mu A/mm^2$)	δE_a	Leakage current per pixel (pA) at 300K	Leakage current per pixel (pA) at 253K
CdTe/Pt	23342	0.39	412	25
CdTe/In (Schottky)	3908	0.44	10	0.4
CdTe/Al-Ti-Au (Schottky)	82011	0.55	3	0.4

For the so-called Schottky detectors, the metal used to perform the electrical contact to the semiconductor creates a Schottky barrier, an energy band differential potential, that in practice decreases the leakage current. This Schottky barrier can influence the behaviour of a detector by the polarization effect [38]. Polarization effect reduces efficiency and energy resolution after several weeks of measurements in the case of a CdTe Schottky detector biased at -250V at -20^{o}C. Resetting bias voltage for few minutes permit a new set of measurements.

Surface leakage current can also appear, and is usually assessed by the use of a guard ring surrounding the cathode. At the end, an extremely low dark current can be expected in the desired detector, chosen as the Al-CdTe Schottky, typically less than 400 fA at -20^{o}C for a pixel of 250 x 250 μm^2 at -250V and up to hundreds of pA at room temperature.

II.5. Key parameters related to space environment

As mentioned before, the Earth atmosphere is opaque to HXR. Telescopes and detectors must be brought to space for observations, creating specific constraints in the detector system development. For instance, short duration sounding rockets experiments (Foxsi [39]) can be used to escape the dense atmosphere, to 40 km in altitude to observe bright sources. Balloon borne telescopes (HEFT [40]) fly approximately the same altitude on longer duration up to 100 days. Both have the drawback of flying at a too low altitude to detect X-rays which still limit their sensitivity, especially at low energies (< 100 keV).

Launching satellite-based telescopes is the ultimate solution approach to escape the atmosphere for long duration flights. However, satellites add many specific extra requirements which impact the development of a detector.

• **Temperature:** Depending on the orientation of the satellite with respect to the Sun, Low Earth Orbiting (LEO) satellites' temperature can vary down to 100 K up to 300 K. For Sun observation missions, such as Solar Orbiter (ESA) [41], temperature can even go up to 800 K which implies the use of thermal shields. Furthermore, heat cannot exchange via convection in vacuum. This imposes a careful design for temperature monitoring and a need to be able to exchange their produced heat by radiation and conduction.

• **Vibrations:** During lift-off, payloads and sensors may endure harsh vibrations, and qualification is needed to assure each sensor can be able to survive the lift-off and rocket stage separations.

• **Power:** Space born systems relies only on photovoltaic panel energy. The power dedicated to scientific instruments is usually as low as possible not only due to limited available power on board, but also due to demanding temperature control at sensor level, as they often operate in very stable conditions.

• **Mass:** Sending a payload to space requires launchers that are specified for a maximum payload mass. For instance, Ariane 5 can lift-off 10 000 kg up to geostationary orbit and 6 000 kg up to Sun Earth Lagrangian orbit.

• **Radiation:** Through the entire life of a satellite high energy cosmic rays, such as protons are likely to cause radiation damages. Such damages can create a malfunction or can decrease the instruments performances. In space mission, these damages need to be qualified, in order to develop sensors able to have a good ability to measure through the entire mission duration (typically 10 years).

II.6. State of the Art

State of the art parameters for fine pitch pixelated detectors can be compared through the above-mentioned key parameters. Usually associated with their readout, I compare them through generic metric more linked with the science case. Table 1.7 reports such comparison.

TABLE 1.7 – *State of the Art detector and parameters*

Name / Satellite	Sensor	Segmentation	Size (μm^2)	Spectral resolution (keV FWHM at 60 keV)	Energy range	Number of channel	butability
Nustar	CdZnTe	Pixels	600 x 600	0.9	5 - 100 keV	32 x 32	2 sides
Hitomi HXI	CdTe	Strips	250 x 250	1.5	5 - 80 keV	128 x 128	No
Caliste HD	CdTe	Pixels	625 x 625	0.77	5 - 100 keV	16 x 16	4 sides
Hexitec (Super-HERO)	CdTe	Pixels	250 x 250	0.78	1 - 200 keV	80 x 80	Tile or 4 sides
Timepix 3	CdTe	Pixels	55 x 55	4.4	1 - 1300 keV	256 x 256 Or abutable strategy	2 sides
Aimed values	CdTe or CdZnTe	Pixels	100 x 100	0.5	1 - 200 keV	2000 x 2000 Or abutable strategy	4 side

Compared to the desired values for the study of SN Ia, state of the art technologies are mostly limited in pixel size and energy range.

III. Trends for future highly pixelated large surface CdTe base hard X-ray imaging spectrometer

Thanks to optimized new detectors at the focal plane of new HXR grazing incidence mirrors, unprecedented high sensitivity, high angular resolution and high effective area space telescopes ranging up to 200 keV or beyond may emerge in the era of 2050. New developments of large and modular, highly pixelated CdTe imaging spectrometer must be anticipated to populate the telescope focal planes. Dreaming of a 100 m focal length with 1 arcsec angular resolution in a 6 x 6 arcmin FoV results in a ˜100 μm pitch array over 20 x 20 cm^2, with a Fano limited spectral response. This will inevitably call for entirely new concepts of modular and 4-side buttable space qualified HXR detectors.

My work intends to pave the way toward this goal, bringing an advanced design of a low pitch, high spectral resolution, and modular spectro-imaging device. The spectro-imaging device would be composed of a detector, chosen as a CdTe crystal with fine pitch pixelated anodes, an Application Specified Integrated Circuit (ASIC) able to readout a CdTe pixelated detector and an Analogue to Digital Converter (ADC) able to sort digital data out. Such a device aims modularity, by the mean of three dimensions interconnections between detector, ASIC, and ADC. The subject of this thesis here, is the deep study and development of the ASIC part.

Such integrated circuit is strongly linked with the detector characteristics and objectives in terms of performance and functionalities. Thus, it is of a prime interest to fix the first constraints before the ASIC development by selecting the proper detector. Considering the objectives of the PHEMTO prospect, I have selected a proper detector as expressed in Table 1.8

TABLE 1.8 – *Characteristics of the chosen detector*

Characteristic	Value
Semiconductor	CdTe
Contact	Schottky (Al)
Working Temperature	253 K
Exposition Side	Cathode
Thickness	750 μm
Bias Voltage	-250 V
Pixel size (pitch)	250 x 250 μm^2
Capacitance	200 fF
Leakage Current	400 fA

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Chapter 2: Acquisition channel for imaging spectroscopy

The energy of a photon interacting in the semiconductor detector creates a number of electron-hole pairs proportional to the photon energy deposit. These N electron-hole pairs are drifted to electrodes by an applied electric field. Charge carriers drift induces a current during a limited time, until charge carriers reach their respective electrodes. The integral of this current, i.e. the charge, is directly proportional to the energy deposited by the photon in the detector. The charge has to be measured in order to get information on the photon energy

Hence, a measurement circuit is needed, in order to convert such charge into a usable value (as a voltage for instance). Later, the voltage can be processed (filtered, digitized...). The acquisition channel needs to cope with the detector size and segmentation. In the case of a pixelated matrix detector, the circuit needs to process each pixel of the matrix.

As interconnection capacitance limits spectroscopic performances, it has to be minimized to few hundreds of femtofarad. Hence, the channel performing charge integration is required to be connected as close as possible to the detector. In this chapter, I explain why such capacitance is required to be minimized, and show more broadly the necessity to adapt the channel circuitry to the detector properties.

This justifies the development of specific circuit which allows the measurement unit to have the same size as a detector pixel. With pixels as small as 250 x 250 μm^2, such circuit cannot be developed with discrete electronic components, pushing for the development of integrated circuits specified for the detector applications, or more often called Application Specified Integrated Circuit (ASIC).

I. Charge measurement chain description

A widely used acquisition architecture [1] is depicted on Fig 2.1. Architecture of different blocks may vary but the global picture is almost the same for every ASIC measuring charge for Hard X-Ray imaging spectrometers.

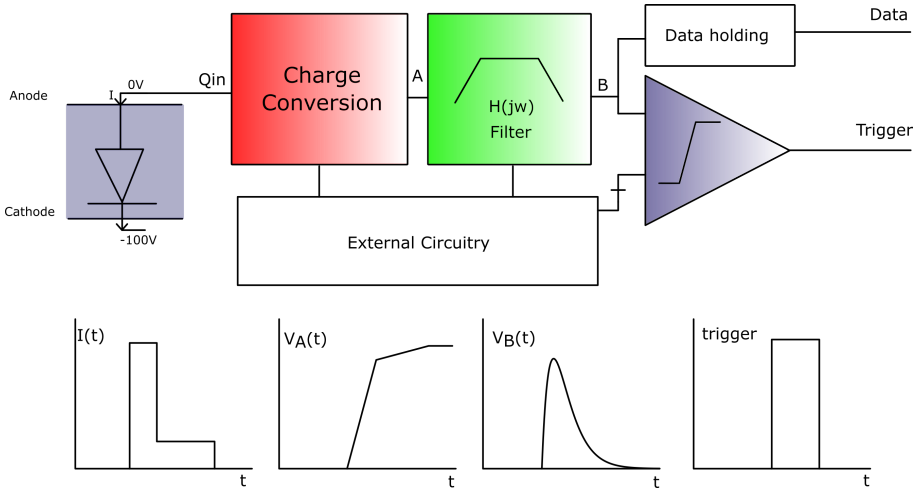

Figure 2.1 – *Typical Charge detection chain schematic (top) and signals (bottom)*

The first stage acts as a charge to voltage converter. This block can be expressed as an equivalent integration capacitor converting the charge into a voltage through the equation:

$$V_A(t) = \frac{Q_{in}}{C}(t) \tag{2.1}$$

A second stage processes the signal to increase the signal to noise ratio. Its behaviour is represented by its frequency transfer function:

$$V_B(j\omega) = H_{Filter}(j\omega).V_A(j\omega) \tag{2.2}$$

Depending on the application, either the signal shape is needed or only its maximum. Thus, the next block can be either an ADC [2], an analogue memory [3], a peak detector [4], or a time-over-threshold circuit [5].

Trigger block allows to know when an X-Ray photon has been detected. This function is necessary for a photon-counting system. It can save power by allowing selective readout of the signal and self-trigger capability. However, generally speaking, this block is not mandatory for spectroscopic channel in a frame readout mode such as in Charge Coupled Devices (CCDs).

Finally a set of digital or analogue auxiliary blocks are required to bias or to interface the core of the circuit with the outer world as digital link, buffers, references...

II. Charge Conversion

The first stage of the channel is a charge converter. It converts the charge into a value (voltage or current) that can be measured by an electronic circuit. Several possible architectures can perform such a conversion.

The simplest way to convert a charge is to consider the detector capacitance as a converter. With small pixel sizes, detector exhibits a low capacitor (200 fF for the described detector in chapter 1). The converter output voltage is $V_{out} = \frac{Q}{C_{det}}$ and can be measured. If the gain of such device is too low, it is possible to add a voltage amplifier to increase the total gain value. In this case, the input capacitance of the measurement circuit also contributes in the integration having $V_{out} = \frac{A_0.Q}{C_{det}+C_{amp}}$. Interconnection stray capacitances need also to be considered into such converters. Such architecture exhibits the best signal to noise performance as electronic noise is minimized. However, gain is highly dependant on detector and hybridization capacitance. It can vary from pixel to pixel, possibly leading to poor spectroscopic performances, as well as no adaptability to different detector sizes. On top of that, integrating charge into the detector capacitance creates voltage variation on one side of the capacitance. Such effect leads to a polarization that can vary as charges are integrated, that decreases the energy resolution especially for high charges.

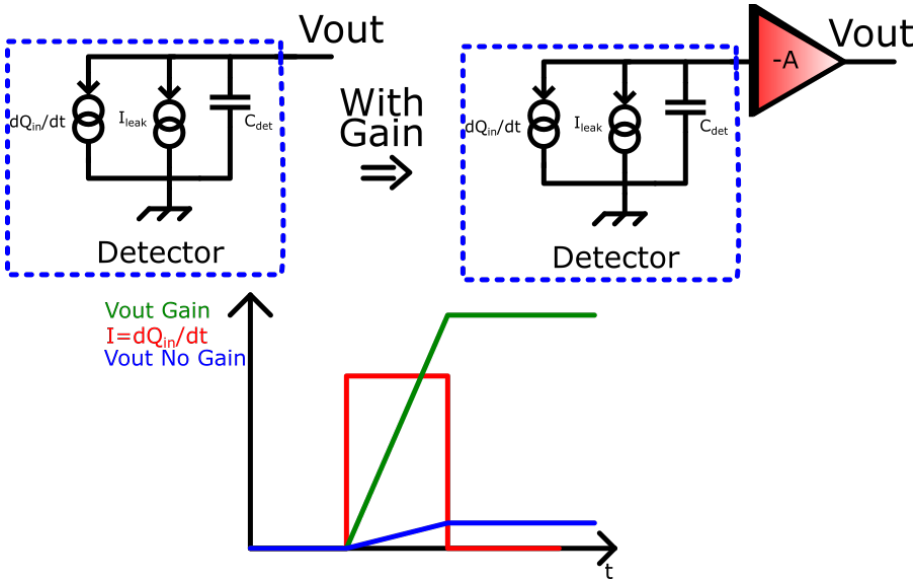

Figure 2.2 – *Conversion made by detector capacitance (left) and amplified by a voltage amplifier (right)*

Another way to process the charge is to amplify the current produced by the charge carrier before integration or sampling. A transimpedance amplifier can be used. It is generally based on an amplifier fed back by a resistor. It produces an output voltage of $V_{out} = R_f I_{in}$ where I_{in} is the derivative of our charge in time. Such architecture has the advantage of having a low input impedance and therefore produces an output voltage independent on input capacitance variation, hence reducing the previously mentioned drawback of detector capacitance converters. However, signal needs to be quickly amplified, needing for a fast amplifier and potentially high-power consumption. Furthermore, feedback resistors need to have a high value to exhibit a sufficient gain and low noise which leads to a large area occupation.

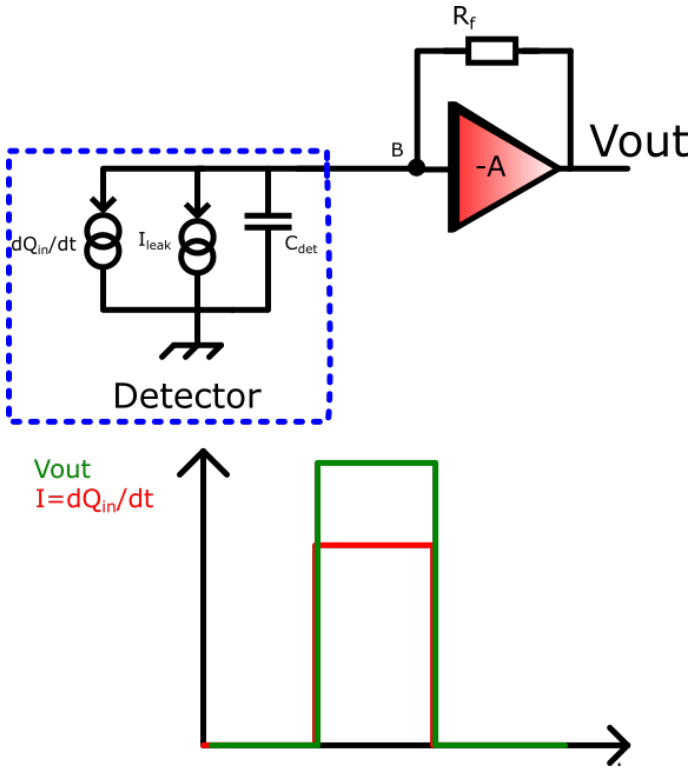

FIGURE 2.3 – *Transimpedance amplifier. Current is converted into voltage through feedback resistance.*

A particular case of the transimpedance amplifier lies in taking advantage of the Miller effect occurring in an amplifier fed back by a capacitor. Such circuits are named Charge Sensitive Amplifier (CSA) and combine the advantages of having a gain independent on the detector capacitance as well as a possible limited bandwidth that can be used to contribute to filtering. Advantages of such configuration has been introduced in [6] and are the subject of the following development.

II.1. Charge Sensitive Amplifier

Charge Sensitive Amplifier and the Miller effect are illustrated on Fig 2.4.

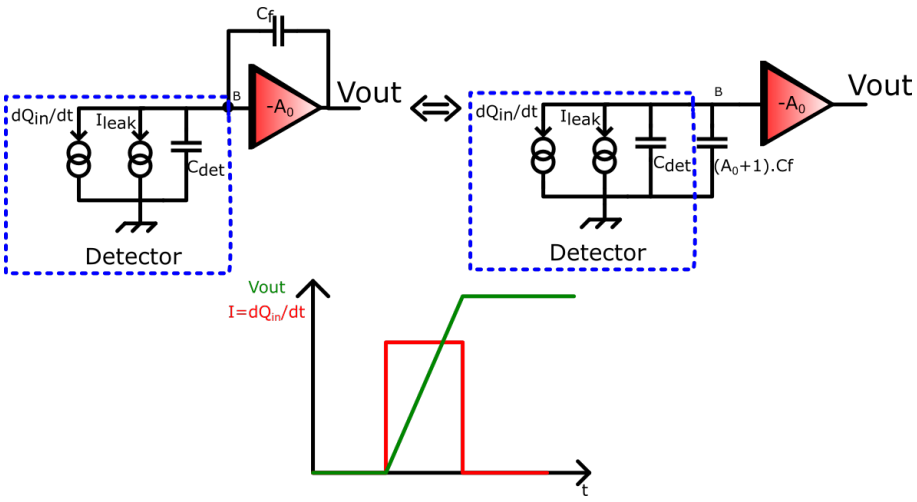

FIGURE 2.4 – *Illustration on the miller effect for Charge Sensitive Amplifier*

Assuming an ideal amplifier of Gain "$-A_0$", and assuming a charge step, we can compute its transient response by inverse Laplace transform:

$$\begin{aligned} H_{Csa}(j\omega) &= \frac{V_{out_{Csa}}}{Q_{in}} = \frac{A_0}{(A_0 C_f + C_{in})} \\ H_{Csa}(j\omega) &\simeq \frac{1}{C_f} \\ V_{out_{Csa}}(t) &= \frac{Q_{in}}{(C_f + \frac{C_{in}}{A_0})}\theta(t) \simeq \frac{Q_{in}}{C_f}\theta(t) \end{aligned} \tag{2.3}$$

Where $\theta(t)$ is the the Heaviside step function and C_{in} represents the total input capacitance (composed of detector capacitance, interconnection capacitance and CSA input capacitance).

It shows that the product $C_f A_0$ needs to be larger than C_{in} in order to keep a large gain value insensitive to change with detector capacitance.

II.1.a. Effect of Finite Bandwidth

Practically, bandwidth depends on the power budget allocated to the amplifier, its design, and the input capacitor. One can assume its behaviour, as a first order gain amplifier with frequency transfer function as below:

$$A = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{A_0}{1 + \tau j\omega} \tag{2.4}$$

Where A_0 is the open loop gain and τ the amplifier time constant.

Considering this transfer function, the response of the charge sensitive amplifier becomes [7]:

$$\begin{aligned} &\text{Assuming } A_0.C_f >> (C_f + C_{in}) \\ &V_{out_{Csa}}(t) = \frac{Q_{in}}{C_f}.[1 - \exp(\frac{-C_f.A_0.t}{\tau.(C_f + C_{in})})] \end{aligned} \tag{2.5}$$

In practice, a 750 μm thick detector with 250 V differential potential would allow a total signal collection time of approximately 25 ns. If the amplifier is faster than 25 ns, the signal development due to electron and hole collection can be tracked. This is used in reference [8] where collection time and signal shape are used to correct double event signals correlation by taking advantage of knowing the drift time, hence the position inside a 3 dimension cube.

If the amplifier is slower than 25 ns, the integration will still fully take place, but collection waveform cannot be tracked.

The expression of CSA time constant is the rising time, expressed as the time for signal to go from 10% to 90% of its maximal value. Its expression in our case of first order amplifier is:

$$T_{rise} = \frac{\tau.(C_f + C_{in})}{C_f.A_0}.\ln(\frac{0.9}{0.1}) \tag{2.6}$$

Where τ depends on the characteristics of my amplifier. A typical value could be $\tau = 2$ μs giving a rise-time of 15 ns for $C_{in} = 300$ fF, $C_f = 25$ fF, and $A_0 = 8000$. Such values allow monitoring of the collection time and having a gain almost independent of the detector and interconnection capacitance.

II.1.b. Resetting the CSA

Following the previous models, once a charge has been integrated, the voltage output of the CSA remains at a constant level. If one integrates several charges, one after another, the system tends to saturate, and the CSA is no longer properly working. On top of that, we stated in the Chapter 1 that my detector has a leakage current in the range of pA. In a compact pixelated hybridized detection system, where there is no room for external components, this current must be delivered or sunk by the ASIC for each pixel. Thus, the integrated circuit is preferably DC coupled to the detector.

In this case, two configurations exist. The first one presented in [9] uses a bias circuitry for leakage current while having the signal AC coupled to the integration circuitry. It has the advantage of having the possibility to bias the first stage independently of the detector. But It requires a large capacitor to AC couple the whole circuitry without filtering fast signals.

AC coupling capacitance can be avoided by integrating a block providing the required current to the detector. This block which can also be used to control the discharge of the CSA feedback capacitance is called "reset" block.

Different kinds of reset architectures exist. A detailed comparison on different reset circuits can be found in [10], and [11], I only mention the working principle here. The following plot shows how a reset circuitry prevents saturation:

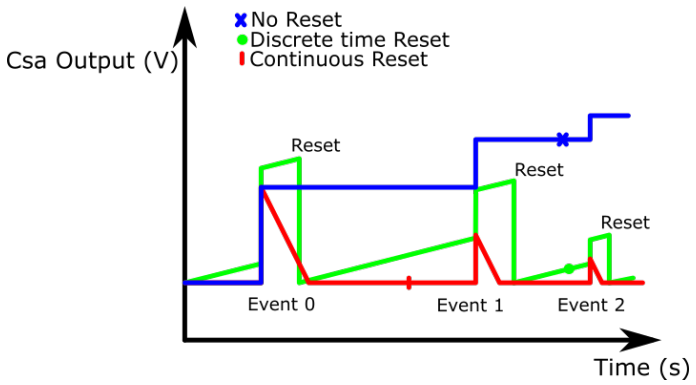

FIGURE 2.5 – *Plot of resets schemes. The first curve (blue) expresses the problematic of no reset, the signal tends to saturate after several integrations. Discrete time reset is expressed in green; we can witness here the problem of constant current integration developed later in this section. Finally, red curve expresses solutions with continuous reset.*

As shown on Fig 2.5, accumulation of charges by CSA without reset leads to saturation. This is avoided either by continuous or discrete time reset.

Discrete time reset:

A discrete time reset takes advantage of a signal (for instance a clock) occurring periodically. At each of these periods, the feedback capacitance is fed back with a low value equivalent resistor in order to be discharged.

This can be achieved using a MOS switch between input and output of the CSA [12]: When transistor is "Off", the current is integrated as well as signal charge. When transistor is "On", the reset occurs, allowing a path for the capacitor to reset and signal at the amplifier output to return to its baseline.

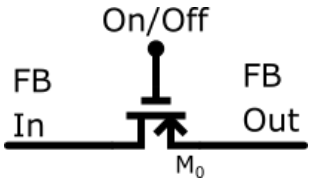

FIGURE 2.6 – *Schematic of synchronous reset MOS*

This kind of reset has the advantage of being dense and fast with a small power dissipation and a low complexity. However, it suffers from two main disadvantages. The first one is related to the non-existing DC path that tends signal to increase due to leakage current integration as shown in the green curve Fig 2.5. The other drawback is related to the period. As reset is periodic, it may occur during the integration of a signal leading to corrupted data.

Continuous reset:

Signal is constantly discharged through a resistive path that can be implemented in different ways.

•**Resistor [13]:** Such a resistive path can be implemented directly using a resistor. Such resistor needs to have a high value in order to define a time constant together with the feedback capacitor lower than the one corresponding to the charge integration time. A high value is also necessary for noise consideration.

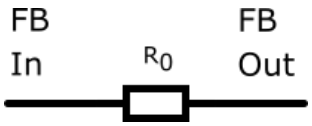

FIGURE 2.7 – *Schematic of resistor feedback reset. For high gain feedback capacitance is in tens of femtoFarads. This implies a resistor value close to the GigaOhm range, hard to provide in Integrated Circuit (IC) technologies*

The resistor feedback has the advantage of being completely passive, linear and is able to drive the leakage current. However, the necessary GigaOhm value for such resistor is a major drawback incompatible with high density integration.

•**Transistor [14]:** It is possible to overcome such density limit by using MOS transistor showing a higher equivalent resistance value for the same area.

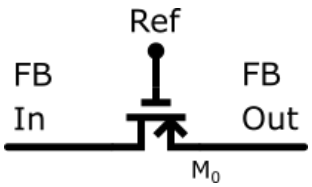

FIGURE 2.8 – *Schematic of transistor acting like a resistor. It is biased using a fixed reference.*

According to its low bias current (I_{leak}), one can assume a behaviour in the subthreshold saturation region where its transconductance is equal to:

$$R = \frac{1}{g_m} = \frac{nkT}{qI_{leak}} \tag{2.7}$$

Where: n is the technology dependant subtrheshold factor

R in GigaOhm can be reach with an area of several μm^2

MOS transistor based continuous reset, is able to drive the detector leakage current passively, is relatively dense even for high equivalent resistor values when biased with such low current, and is relatively simple to implement in a microelectronic circuit. However, its behaviour is highly non-linear and fall-time depends on the detector leakage current. Such a drawback can be overcome by using a proper pole zero cancellation discussed in chapter 3.

•**Krummenacher reset [11]:** The idea behind Krummenacher architecture is to use both a transistor acting like a resistor feedback as well as a circuitry acting as an inductor. Thus, the equivalent circuit is both a resistor and an inductor connected in parallel to the feedback capacitance. Such system privileges the leakage current to pass through the equivalent inductor, allowing high value of leakage current without perturbing the reset time, fixed by the resistor.

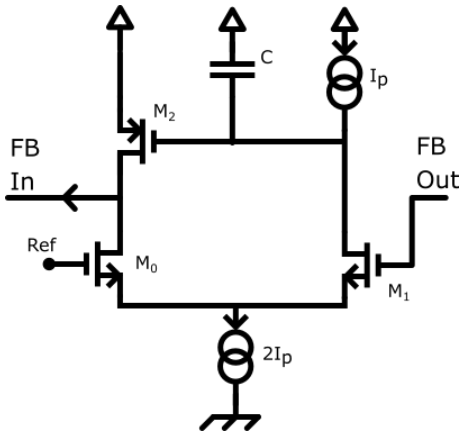

FIGURE 2.9 – *Schematic of Krummenacher Reset. M2 and C act together as an inductance, and the MOS pair. M0/M1 are here to bias and send output csa voltage to capacitance C.*

This type of reset is relatively dense, linear and can drive large amount of detector leakage current. However, its complexity and relatively poor noise behaviour (due to two noisy resistive path) makes it not competitive for very low noise applications.

•**Current Conveyor [15] [16]:** The idea lies in scaling down a referred current proportional to the output signal of the CSA. Such current is scaled down and fed to the input stage (hence the detector). It allows fast processing and supports a high leakage current.

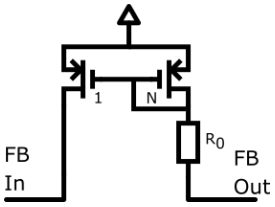

FIGURE 2.10 – *Simplified schematic of Current Conveyor Reset*

Such circuit is relatively dense, linear and can drive high leakage current values. However, the low current division performed by the current mirror is an issue for very low noise applications when a filter is used after the CSA.

•**Current mirror [17]:** Instead of using a fixed value MOS reset transistor with a non-constant fall-time, the idea is to create a current mirror source in the CSA's feedback to allow constant current to flow in the capacitance. Such constant fall-time is an advantage for time-over-threshold measurement, detailed later in this chapter.

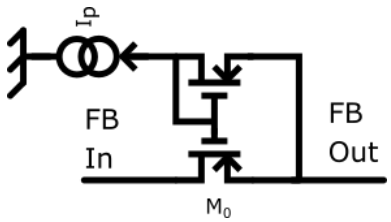

FIGURE 2.11 – *Schematic of Current Mirror Reset.*

Its advantages and drawbacks are the same as discussed for single MOS configuration, with the benefit of being more linear. However, it adds a significant amount of noise due to the bias current used for the mirror transistor.

Choice of reset

In order to choose the right reset architecture needs to consider several designs aspects:
•**Area:** First of all, with a pixel size equal to 250 x 250 μm^2, reset area is desired to be as low as possible.
•**Noise:** reset must add negligible noise to the system.
•**Leakage current:** This reset circuitry needs to provide a path for detector leakage current. A certain immunity to leakage current variation is important in order to be able to feed high level and variable leakage currents. With my detector, leakage current is relatively small (tens of pA at room temperature), hence requirement on leakage current immunity is relatively low.
•**Linearity:** Finally, the association with following stages has to be considered, in order to optimize the linearity requirements of the system. This requirement has to cope with the desired complexity of the calibration system and is in our case desired to be lower than few percent.

Each of the above-mentioned circuits show advantages or drawbacks, with respect to area, noise, leakage current and linearity key parameters. Hence, the optimal choice depends on the application. In the scope of this thesis, the architecture has to be low power, small, linear, and low noise. Immunity to leakage current fluctuations is not considered as a priority. At that stage, considering these input parameters and mainly for the low noise constraints, I chose the MOS architecture and the continuous time reset.

II.1.c. Fall-time

Considering a MOS reset continuous architecture, the reset transistor acts as a resistor of value $\frac{1}{gm_0}$ where gm_0 is its transconductance. Considering this, and an ideal amplifier (infinite gain and bandwidth), the transient response becomes:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \exp(\frac{-gm_0}{Cf} t) \tag{2.8}$$

The fall-time of this signal is defined as the CSA's output decay from 80% to 20% of its maximum value. For the reset MOS configuration it is expressed as:

$$T_{Fall} = \frac{C_f}{gm_0} \ln(\frac{0.8}{0.2}) \simeq 1.4 \frac{nkTC_f}{qI_{leak}} \tag{2.9}$$

Generally speaking, a short fall-time value is generally needed in particle accelerators where high flux is expected, and less critical in most of the HXR astrophysics missions where count rate in a channel tends to be lower (kHz max per channel).

Summary

I presented several properties of a non-ideal charge sensitive amplifier. Characteristic parameters of the CSA such as rise-time, fall-time and closed loop gain have been introduced as well as its working principle. Figure 2.12 illustrates the comparison of ideal, limited gain, and limited gain and bandwidth CSA.

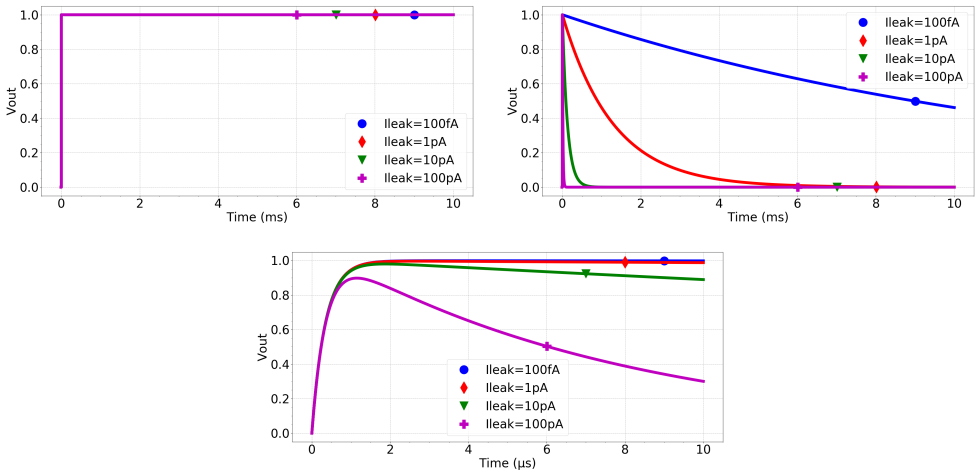

FIGURE 2.12 – *Different CSA models. First is the ideal non reset CSA 2.5, second is ideal CSA with MOS reset 2.8. Third is the bandwidth limited CSA with MOS reset.*

II.1.d. Amplifier design

The amplifier is the most critical element of the CSA. It has to fulfil several characteristics, to match the system requirements:
• **Open loop gain:** As expressed in equation 2.3, the open loop gain "A_0" expresses the permanence of overall gain with input capacitance. The higher ratio between detector's capacitance and feedback capacitance is, the higher the open loop gain needs to be. Its value can vary from 100 V/V (40dB) to more than 10000 V/V (80 dB).
• **Output swing:** The output swing expresses the maximum output difference voltage that an amplifier can handle at its output. For a given feedback capacitance it defines the energy range of the CSA, hence is desired to be as large as possible. Value are very dependant on technology, for modern circuit technologies, where power supplies tend to decrease down to 1.8V, 1.2V or even 1V, its typical value is around 800 mV.
• **Stability:** When high open loop gain is made by the use of several amplifying stages, instability can begin to be an issue and proper compensation circuits needs to be implemented.
• **Power consumption:** In the case of a highly dense measurement system, with a large amount of readout channels, power consumption must be low to limit heating, in order to be able to cool down the system for detection performances. For a pixel size lower than 500 x 500 μm^2 with a detector operating at 0^oC (Schottky contact CdTe detector), the power consumption has to remain lower than several hundreds of μW to reach a noise level lower than hundreds of electrons.
• **Bandwidth:** When collection time information is needed, the bandwidth must be high for a given open loop gain. For our application, assuming a typical open loop gain of 8000 V/V leads to a bandwidth in the hundreds of kHz range.

Various amplifier architectures can be found in literature [18] [19] [20]. Two types of architecture need to be distinguished, the single ended and the differential ones. For single ended architecture only one input signal is amplified while with differential architectures, the difference between two inputs is amplified. The later has the advantage to set the input voltage easily. It has a major drawback of experiencing the same noise for twice the power consumption. I detail here only single ended architectures. The most simple and naive architecture consists in the one stage common source amplifier design depicted inf figure 2.13:

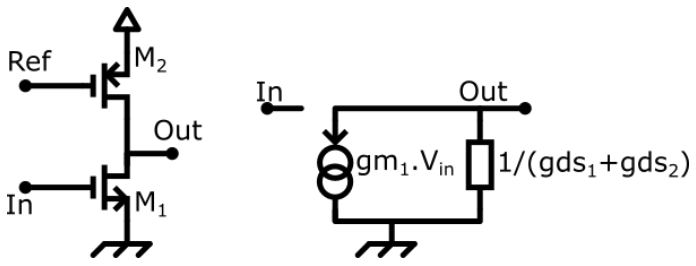

FIGURE 2.13 – *Common source amplifier (left) with small signal schematic (right)*

Examining the small signal equivalent scheme in Fig 2.13, such amplifier uses one transistor acting as a transconductance, in parallel with a resistor (that can be a MOS transistor as well). Thus, the gain is directly proportional to the resistor transconduc-

tance product, which is, for suitable amount of power, typically 10. According to our previous analysis, the detector capacitance is around 300 fF. In chapter 3, I determine a suitable feedback capacitance value of 25 fF. The product AC_f: 10x25=250 fF is not larger than $C_{det} = 300$ fF. Using a common source amplifier would add uncertainty and dispersion in the CSA gain that clearly becomes linked to the detector capacitance and to the open loop gain of the amplifier.

Consequently, more elaborated architectures are required to reach higher gain. They differ from application to application. For instance, when focusing for application with highly capacitive detector with fast response, the amplifier needs to have an important gain-bandwidth product. The regulated cascode architecture (see Figure 2.14) is one of the possible architectures to reach gain up to 170 dB as detailed in [21]. The drawback of these architectures is that the power consumption is not optimized for noise reduction, part of the power is mainly used for open loop gain increase.

For high density pixelated detectors, as with imaging devices, capacitance is typically lower than 1 pF, and focus is made on power consumption and bandwidth. In these architectures [22] [23], amplifier is made out of a simple telescopic cascode or common source, as it only amplifies voltage and is not fed back by a feedback capacitance (integration is made by the detector capacitance).

Finally, for "in between" architectures, where medium gain, low power consumption and relatively high speed are needed, one of the most common architecture is the folded cascode architecture like the ones used in [24] [25]. Compared to the telescopic cascode, folded cascode architecture allows for input (gm) and output (gds) transistors to be biased with different currents, allowing for increasing the gain.

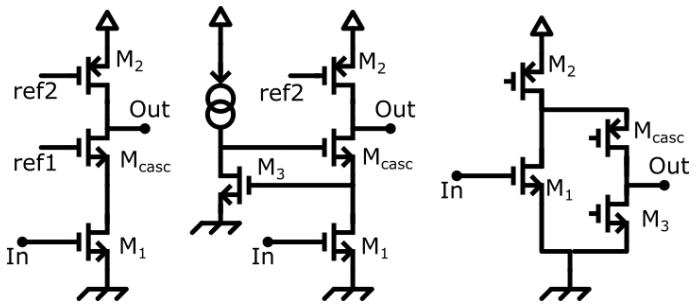

FIGURE 2.14 – *Different amplifier architectures (telescopic cascode, regulated cascode, folded cascode)*

II.2. Noise

All above mentioned electronics devices add their own noise to the signal. Each time amplification occurs, following signal is less sensitive to noise. For that reason, the dominant part of the whole noise of a well-designed circuit often comes from the earliest stages.

The usual way of representing noise in circuits for X-Ray detectors is to convert the output voltage noise into the input referred noise expressed in charge. This input noise is called Equivalent Noise Charge (ENC). A way of computing this value is to integrate the total output noise and divide it by the transfer function (charge to voltage) of the channel:

$$ENC = Q_{in} \frac{\sqrt{\frac{1}{\pi} \int_0^\infty v_{noise_{Out}}(j\omega)^2 \, \mathrm{d}\omega}}{V_{Out_{Max}}} \tag{2.10}$$

Where $V_{Out_{Max}}$ represents the output maximum voltage to a given charge Q_{in}.

For spectroscopic performance noise needs to be reduced, hence a correct knowledge on the different noise sources is essential.

II.2.a. Noise Analysis

Charge sensitive amplifiers add some noise to the measurement due to different noise sources present in MOS transistors. Each of these noise sources are present in each transistor but contribute differently to the output depending on their location, and frequency behaviour. The noise at the output of the charge sensitive amplifier can be expressed as follows:

$$v^2_{noise_{Out}} = [Q^2_{noise_{det}} + \frac{i^2_{p_i}}{\omega^2} + \frac{v^2_s}{\omega^2 Z^2_{in}}] \mid H_{Csa} \mid^2 \tag{2.11}$$

The terms $\frac{v^2_s}{Z^2_{in}}$ and $\frac{i^2_p}{\omega^2}$ can be considered as the input referred noise coming from the charge sensitive amplifier. This input referred noise can be separated into two categories:

• **The Parallel noise i_{p_i}:** contribution of input noise considered as a current (example: the reset noise)

• **The series noise v_s:** contribution of input noise considered as a voltage noise (example: the thermal noise of input transistor).

Such point is illustrated in Fig 2.15 where two input referred noise sources are considered.

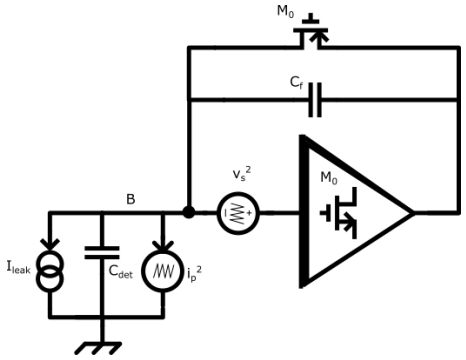

FIGURE 2.15 – *Charge sensitive amplifier with noise sources*

The input noise impedance, is expressed as the impedance seen by the series noise voltage input. It is expressed as $\frac{Vin}{Iin})_{V_{out}=0}$ and equals to:

$$Z_{in}^2 = \frac{1}{(C_f + C_{in})^2 \omega^2} \tag{2.12}$$

Thanks to this expression, the equivalent noise charge can be computed by expressing each noise sources present in the system in terms of parallel or series noise source and injected to the equation 2.11. A variety of noise sources can be expressed. I report below a non-exhaustive list of the source terms referred to the input.

II.2.b. Noise sources

Shot noise [26]:
Current consists of a flow of discrete carriers. The process of discrete carriers flowing inside a medium is driven by Poisson statistics that stipulates a variation on the total amount of such flow (i.e. current). This variation from the mean amount of current is seen as a noise for the charge measurement circuit. Such a fluctuation of a DC current is named detector shot noise and its spectral density is expressed as

$$Q_{noise_{det}}^2 = \frac{2qI_{leak}}{\omega^2} \tag{2.13}$$

Where I_{leak} corresponds in our case to the leakage current of our detector and q the elementary charge ($1.6 \cdot 10^{-19} C$).

Such current is "seen" directly at the input of my readout ASIC. We will see later that its contribution can be minimized by reducing the filter shaping time. However, it has to be as low as possible in order to avoid having excessively short peaking time, where other noise sources such as thermal noise will dominate. This is the reason why I detailed the use of low leakage current detector in chapter 1 by the means of CdTe Schottky diodes operated at low temperature. The shot noise is a white noise.

Thermal Noise

The thermal noise (or Johnson noise or Nyquist noise) corresponds to the charge carrier agitation inside a conductor at a given temperature. Such agitation generates fluctuation on the current. In resistors, the spectral density of the thermal noise is expressed as:

$$v^2_{thermal_R} = 4kTR \tag{2.14}$$

In MOS transistors, the spectral density is expressed as:

$$v^2_{thermal_{MOS}} = \frac{4kT\gamma}{g_m} \tag{2.15}$$

k is the Boltzmann Constant, T the temperature, g_m is the MOS transconductance. γ is a technological bias dependant parameter (usually equals to 2/3 in strong inversion).

In figure 2.15, the two main thermal noise contributors are the amplifier's input transistor and the reset transistor. The first one exhibits its noise in term of a series noise expressed as:

$$v^2_{s_{M1_{th}}} = \frac{4kT\gamma}{gm_{M1}} \tag{2.16}$$

For the reset transistor, its noise appears at the CSA input as a parallel noise expressed as:

$$i^2_{p_{M0}} = \frac{4q\gamma I_{leak}}{n} \tag{2.17}$$

Flicker Noise
Flicker noise is directly linked to the fabrication process defaults and impurities on MOS transistors. There is no single fundamental physical mechanism that explains this noise and it is mostly the sum of different mechanisms such as electron-hole recombination due to impurities, crystal damages or other sources [27]. These sources can vary differently in the whole spectra but a common assumption is to consider that the resulting total noise has a spectral density that varies with a factor $\frac{1}{f^{EF}}$. Different models exist for its behaviour, one of them (SPICE2 [28]) expresses the flicker noise spectral density as:

$$\begin{aligned} v_{1/f}^2 &= \frac{2\pi K_F I^{AF}}{C_{ox} L^2 gm^2} \frac{1}{f^{EF}} \\ i_{1/f}^2 &= \frac{2\pi K_F I^{AF}}{C_{ox} L^2} \frac{1}{f^{EF}} \end{aligned} \tag{2.18}$$

Where K_F, AF, EF are technological parameters, C_{ox} is the transistor oxide area capacitance and L, the transistor length.

The spectral density of flicker noise is not flat. In the majority of cases, EF is close to 1. Such a noise becomes a $\frac{1}{f}$ noise and is usually called "pink noise".

It can be demonstrated [29] that the main contributor of flicker noise is the input transistor (M_1 fo Fig 2.14). Such noise is seen as a series noise:

$$v_{s_{M1}1/f}^2 = \frac{K_F I_{bias}}{C_{ox} L_{M1}^2 gm_{M1}^2} . \frac{1}{\omega} \tag{2.19}$$

Dielectric Noise
When a capacitor is fed with a varying electric field (voltage), charges tend to move to both capacitor electrodes due to the fluctuation of the electric field [30]. When charges move in both directions, they tend to lose a part of their energy by collision and transform it into heat. This loss can be modelled by considering a complex permittivity. The higher the imaginary part is, the higher is the loss. Moreover, collisions tend to appear more often when the frequency is high. We can summarize this by considering a dielectric noise for each capacitance as an input parallel noise:

$$i_{p_\epsilon}^2 = \frac{1}{2\pi} 4kT \tan(\delta) \omega C_d \tag{2.20}$$

With C_d the capacitance and δ the tangent loss, that depends on the dielectric material.

Dielectric noise is experienced by the detector capacitance, but also by the ASIC input pad capacitance (Dielectric: SiO2). For both, the loss is relatively low due to the material tangent loss (around 5.10^{-4} for $CdTe$ [31] and 2.10^{-4} for SiO_2 [32]). Conversely, for Printed Circuit Board (FR4), the dielectric loss tends to be 2.10^{-3} which is no longer negligible. Hence, if the application needs a PCB extender to interconnect the detector to the ASIC inputs, this noise component has to be carefully studied.

Total noise
The total noise at the CSA output can be expressed as:

$$v^2_{noise_{Out}} = [Q^2_{noise_{det}} + \frac{i^2_{p_\epsilon} + i^2_{p_{M0}}}{\omega^2} + (v^2_{s_{M1_{th}}} + v^2_{s_{M1_f}})(C_f + C_{in})^2] \mid H_{Csa} \mid^2 \tag{2.21}$$

This expression can be simplified into:

$$v^2_{noise_{Out}} = [\frac{i^2_p}{\omega^2} + (v^2_{th} + v^2_f).(C_f + C_{in})^2] \mid H_{Csa} \mid^2 \tag{2.22}$$

The detector shot noise has been expressed inside the parallel noise component i_p and Fano noise has been neglected.

As mentioned before, the expression of noise is usually referred as the input noise charge also named Equivalent Noise Charge (ENC). Its formula is expressed in equation 2.10. The expression of the total noise in equation 2.21 is integrated through the whole spectrum, divided by the total gain (in our case $Gain = \frac{1}{C_f}$ if we consider an ideal amplifier) giving the expression of the equivalent noise charge.

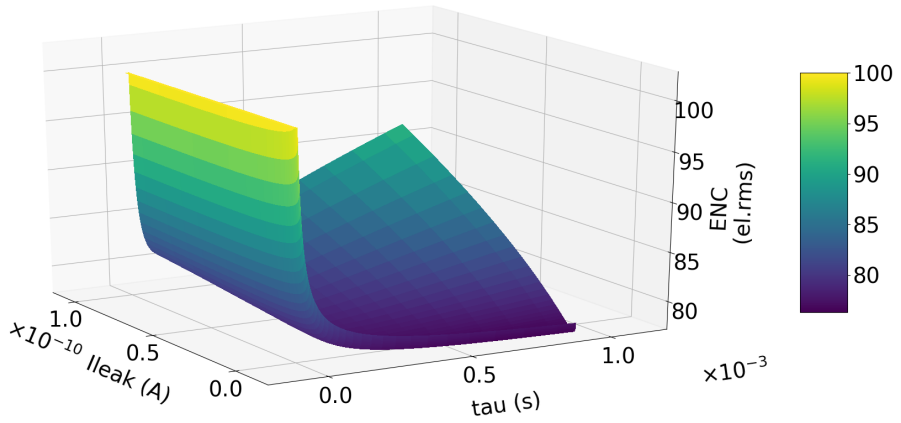

FIGURE 2.16 – *3D plot of equivalent noise charge with no filter considering a detector capacitance of 300 fF. The plotted axis are the following: ENC (el.rms), tau: time constant of the CSA (s), Ileak: the leakage current (A). First order model leads to 80 el.rms minimum for noise assuming only thermal, flicker and parallel noise (no dielectric).*

If we consider only a Charge Sensitive Amplifier, at the input, Equivalent Noise Charge has a complex behaviour dependant on the CSA bandpass, that acts as a first order filter. Thermal input noise is proportional to the input transconductance, as well as the bandwidth of the amplifier which leads to an optimum value for the input transistor transconductance. Using equation describing noise and CSA transfer function, I found this optimum to be numerically around 80 el.rms (see fig 2.16) for 150 μW of power consumption in the AMS 0.35 μm technology, a too high value for our foreseen HXR application. Thus, a filter is needed to decrease the noise by cutting the bandpass of the CSA.

III. Filtering

In order to reduce the equivalent noise charge, a filter must follow the charge sensitive amplifier. In the next parts, I detail the purpose of such a filter, its ideal behaviour, and some classical implementations. The filter will be considered to be noiseless, which is in practice normally the case if the input stage has a sufficient gain. The schematic of the whole circuit CSA+filter becomes:

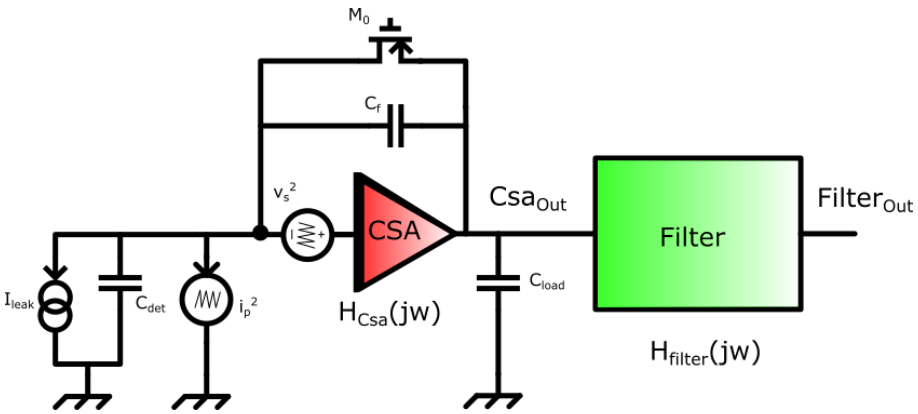

Figure 2.17 – *Schematic of a Charge Sensitive Amplifier followed by its filter used for noise analysis*

In the case of a filter the equation 2.22 becomes:

$$v^2_{noise_{Out}} = [\frac{i_p^2}{\omega^2} + (v_{th}^2 + v_f^2).(C_f + C_{in})^2] \mid H_{Csa} \mid^2 \mid H_{Filter} \mid^2 \tag{2.23}$$

Such equation expresses the noise as a function of filter transfer function and is the basis of the following study.

III.1. Ideal Filter

In order to reduce the electronic and detector noise and to maximize the signal to noise ratio, bandwidth of the whole chain has to be adapted. This task is performed by the filter.

III.1.a. Introduction on Matched filter theory

Matched filter theory has been originally introduced in [33] for radar measurements. This theory can be applied for any application to reduce a signal to noise ratio. The principle lies in the schematic 2.18.

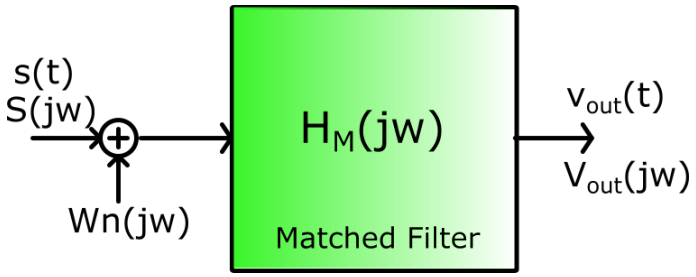

FIGURE 2.18 – *Schematic of the matched filter theory, applied for a white noise input source.*

We consider a noiseless signal $S(j\omega)$ to which we add a white noise $W_n(j\omega)$. The matched filter here expressed as $H_M(j\omega)$ is considered linear. Assuming a signal occurring at time t=0, one measures the output signal at time t_m. Computing the signal to noise ratio at the output of the filter at time t_m, a minimum of such a ratio can be found by applying the Cauchy Schwartz inequation. Such a study is detailed in [33] and leads to the following result:

$$H_M(j\omega) = k\frac{\overline{S(j\omega)}}{W_n(j\omega)}e^{-j\omega t_m} \tag{2.24}$$

$H_M(j\omega)$ is the transfer function of the matched filter that maximize the signal to noise ratio.

If we assume a white noise, then $W_n(j\omega) = k$ (k is a constant value) and results in expressing the optimum filter as the complex conjugate of the signal at time t_m. Such study can be applied for radiation sensor applications as detailed in [34]. The results of this study will be expressed in the next part.

III.1.b. Application to thermal and parallel noise

The noise at the output of Charge Sensitive Amplifier is not purely white but composed of different sources as detailed in equation 2.21. Hence, the direct expression found in matched filter theory needs to be adapted. Figure 2.19 details this adaptation consisting in whitening the CSA output noise and deriving the previously mentioned theory. Such a study is made here for thermal and parallel noise, omitting flicker noise

for simplification reasons. A fully detailed study can be found in [35] with flicker noise taken into account. Results of this study are very close to the optimization for parallel and thermal noise only.

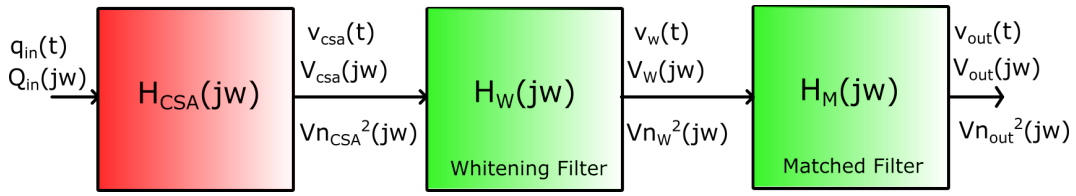

FIGURE 2.19 – *Schematic of the matched filter theory, applied for radiation sensors application*

Assuming the schematic Figure 2.19, expression of the noise at the output of CSA can be derived from equation 2.23 assuming a zero-flicker noise contribution. At this point the expression of noise is composed of a thermal white noise and a parallel noise. To comply with the study of a matched filter, this noise is converted into a white noise by passing through $H_W(j\omega)$. At the end of $H_W(j\omega)$, noise component of signal $V_W(j\omega)$ is white and matched filter theory can be applied on $V_W(j\omega)$. Such a study has been performed in the case of a radiation sensor measurement in [35] and leads to a matched filter transfer function expressed as:

$$H_M(j\omega) = k\frac{Q_{in}}{\sqrt{i_p^2}}\frac{1}{(1-\tau_w j\omega)}e^{-j\omega t_m} \tag{2.25}$$

With $\tau_w = C_{in}\sqrt{\frac{v_s^2}{i_p^2}}$

If we assume a charge step occurring at time t=0, whitening filter output can be expressed in time domain by inverse Fourier transform. In the case of the whitening filter, its temporal behaviour is expressed by assuming a Dirac impulse at its input and inverse Fourier transform. This leads to the two plots of the figure 2.20. On the right, the output signal of the whole circuitry is expressed. It details the optimized signal occurring at the output, named cusp filter. This whole circuitry expression of filter corresponds to the convolution of both, the signal at the output of the whitening filter, and its time decay complex conjugate corresponding to the match filter response to a Dirac pulse.

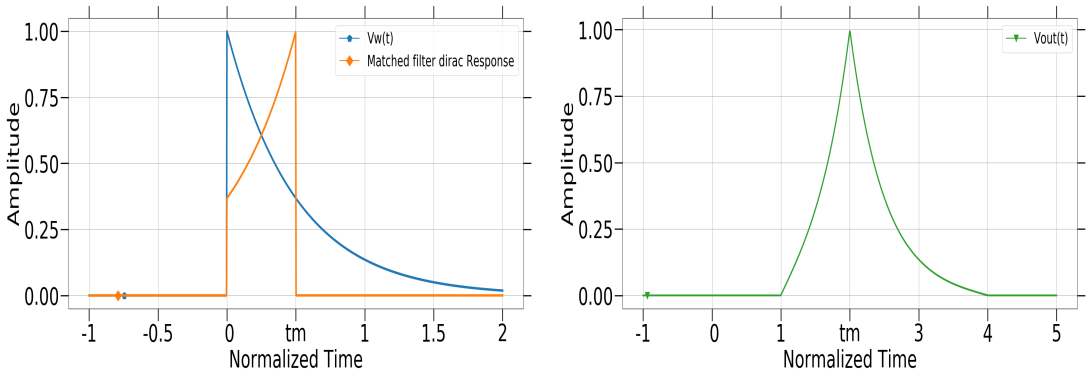

FIGURE 2.20 – *Whitening filter output is depicted in blue and response of matched filter to a Dirac impulse is depicted in orange. Note that at negative time, both signals are equals to 0, leading to an edge in the matched filter response. The right curve (green) expresses the output voltage of the whole chain to a charge step.*

III.1.c. Noise parameters

We discussed the optimal filtering theory and calculated the proper theoretical transfer function that minimized the thermal and parallel noise contributions. The reference [35] expresses in the same way an optimal filter which considers flicker noise. Such has a wider shape (in time) with respect to the cusp.

In order to compare filter, the equivalent noise charge can be computed as the output noise value integrated over the whole frequency and divided by the output voltage gain. In the particular case of a matched filter, this expression can be expressed as follow:

$$ENC^2 = A_{th}\frac{\alpha_{th}^2(C_f + C_d)^2}{T_{peak}} + A_f\alpha_{1/f}^2(C_f + C_{in})^2 + A_{//}T_{peak}\alpha_{//}^2 \tag{2.26}$$

Expressing the filter as the cusp filter, coefficient can be expressed as: $A_{th} = 0.5$, $A_f = 2.01$, $A_{//} = 0.5$, and $T_{peak} = \tau_w$.

III.1.d. Discussion

I described the optimal acquisition chain that maximizes the signal to noise ratio, for negligible flicker noise. Such study leads us to the definition of a theoretical filter named cusp and the calculation of the ENC expression.

I took the assumption of a fixed measurement time named t_m. Looking closely at the figure 2.20, it appears that the filter shape shows an asymmetric behaviour, the slope is more linear on the left part than on the right part. This is due to the finite value of t_m. When measurement time is considered to be finite, we use only a fraction of the data at the output of the whitening filter. This finite time cusp filter is truncated and signal to noise ratio is impacted by a factor $\sqrt{1 - e^{-2\frac{t_m}{\tau_w}}}$. The detailed study on the

impact of finite time measurement and with flicker noise taken into account can be found in [36].

The matched filter theory gives the best theoritical achievable ENC. It is obtained for an infinite measurement time and is thus not realizable. At the end, the filter has to be integrated into an ASIC. Hence new parameters that make the implementation of the filter achievable have to be taken into account: density, complexity, power, speed, linearity.... Different types of filter exist in the literature, all of them trying more or less to mimic a cusp shape. They can be classified into two categories: time variant and time invariant filters. Depending on application, and ASIC architecture strategies, both filters are implemented in literature and detailed below.

III.2. Semi-gaussian filter

III.2.a. Description

One practical approximation of a cusp filter is the semi-gaussian filter. It is a time invariant filter, which can be implemented by means of active filters (Rauch, Sallen Key), or just by means of passive elements such as resistors and capacitors. Such a filter is composed of a high pass filter followed by low pass filters:

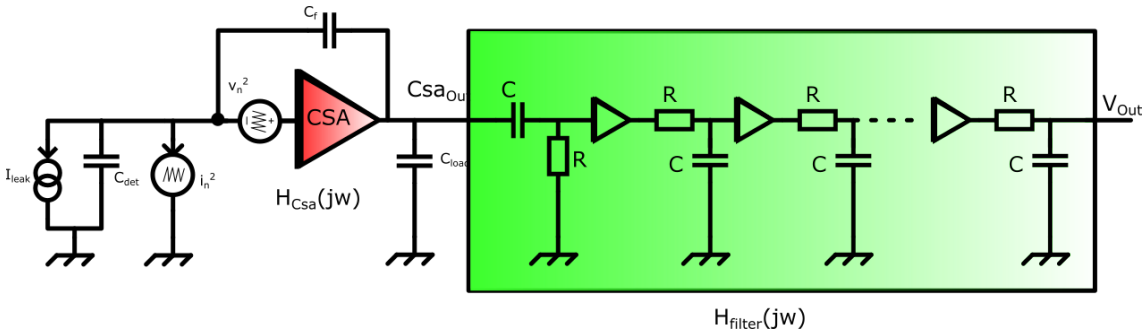

FIGURE 2.21 – *$CR - RC^n$ Filter, ideal implementation: one CR filter followed by n RC filters.*

III.2.b. Transfer function

Considering a number n of identical cascaded low pass filters as shown in Fig 2.21, the expression of its transfer function is:

$$H_{filter}(j\omega) = \frac{V_{Filter_{out}}}{V_{Csa_{out}}} = \frac{RCj\omega}{(1+RCj\omega)^{n+1}} \tag{2.27}$$

Considering the response an ideal charge amplifier with no reset (equation 2.3) the total transfer function becomes:

$$H_{tot}(j\omega) = H_{Csa}(j\omega).H_{filter}(j\omega) = \frac{1}{C_f}.\frac{\tau j\omega}{(1+\tau j\omega)^{n+1}} \tag{2.28}$$

$RC = \tau$ is called the shaping time constant of the filter.

III.2.c. Temporal expression

Considering a step charge $\frac{Q_{in}}{j\omega}$, at the input of the CSA, the output transient response of the filter is:

$$V_{out}(t) = \frac{Q_{in}(t)}{C_f \tau^n} \frac{t^n e^{\frac{-t}{\tau}}}{n!} \tag{2.29}$$

When the order of the filter n increases, its transient response is getting more and more symmetrical and tends to a Gaussian shape (see figure 2.22). The fall-time decreases, allowing the chain to recover faster from a charge deposit. Furthermore, next sections demonstrate that depending on the order, different types of noise are differently filtered.

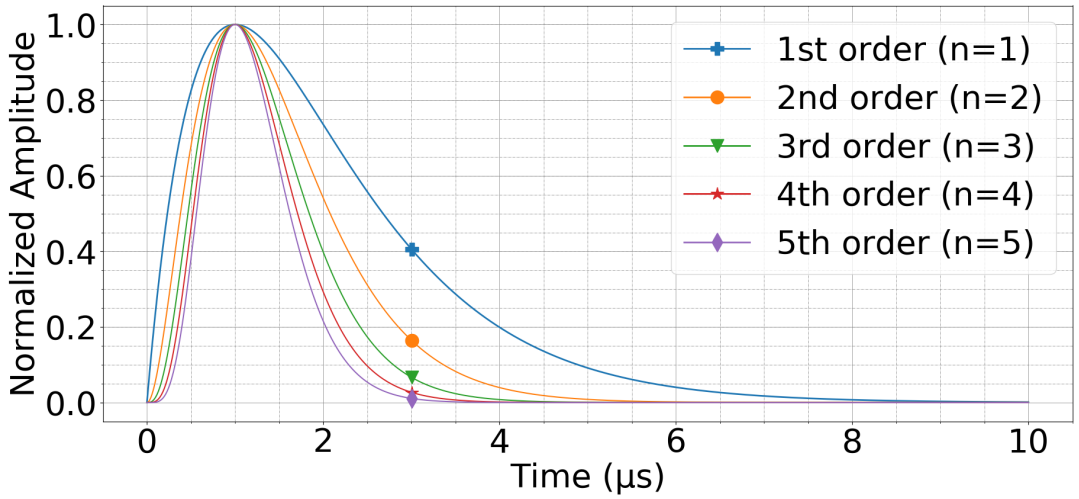

FIGURE 2.22 – *$CR - RC^n$ Temporal output signal normalized in amplitude and $T_{peak} = nRC = 1\mu s$ for n =1 to 5.*

III.2.d. Peaking Time

The time at which the signal is maximum is called the peaking time. It is expressed by solving $\frac{dV_{out}}{dt} = 0$ giving:

$$T_{peak} = n\tau \tag{2.30}$$

III.2.e. Maximum Value

When $t = T_{peak}$ the maximum value is expressed as:

$$V_{out_{max}} = \frac{Q_{in}(n)^n}{C_f n!} e^{-n} \tag{2.31}$$

III.2.f. Noise parameters

Considering equation 2.10 and equation 2.23, the Equivalent Noise Charge (ENC) of a CSA followed by a semi-gaussian filter can be expressed as:

$$ENC^2 = \frac{Q_{in}^2}{V_{out_{max}}^2 \pi} \int_0^\infty [\frac{i_p^2}{\omega^2} + (v_{th}^2 + v1/f^2).(C_f + C_{in})^2] \mid H_{Csa} \mid^2 \mid H_{Filter} \mid^2 \mathrm{d}\omega \quad (2.32)$$

In a same way as for the cusp expression, ENC, can be separated into three terms: thermal, parallel and flicker noise that undergo different frequency behaviours. The noise parameters, often correlated with design choices and technology are taken out of the integration part, becoming only coefficients. The equivalent noise charge is thus expressed as:

$$ENC = \sqrt{\frac{1}{q^2}(\frac{A_{th}\alpha_{th}^2}{T_{peak}} + A_f\alpha_{1/f}^2)(C_f + C_{in})^2 + \frac{1}{q^2}A_{//}\alpha_{//}^2 T_{peak}} \quad (2.33)$$

With: α_{th}^2, $\alpha_{//}^2$, and $\alpha_{1/f}^2$ the different noise source coefficients. And filter noise parameters expressed as below [29]:

$$\begin{aligned} A_{//} &= \frac{n!e^{2n}}{4n^{2n+1}\sqrt{\pi}}\Gamma(n+\frac{1}{2}) \\ A_{th} &= \frac{n!e^{2n}}{8n^{2n-1}\sqrt{\pi}}\Gamma(n-\frac{1}{2}) \\ A_f &= \frac{n!^2e^{2n}}{2n^{2n+1}} \end{aligned} \quad (2.34)$$

Where $\Gamma()$ is the Gamma function expressed as $\Gamma(z) = \int_0^\infty x^{z-1}e^{-x}\mathrm{d}x$.

Equation 2.33 is essential to understand noise processing inside an high energy resolution X-Ray detection system. From this expression, we demonstrate that noise increase with the detector, as stated earlier. The ENC can be plotted versus peaking time to highlight the evolution of main noise terms, the influence of detector parameters, and to localize the minimum of the function.

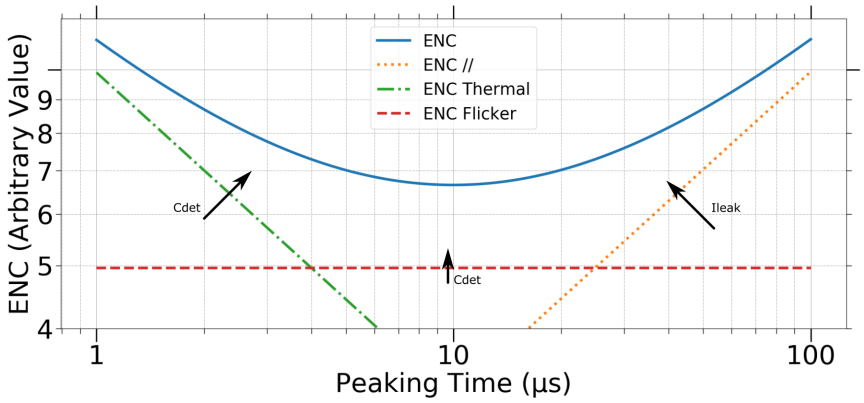

FIGURE 2.23 – *Equivalent Noise Charge function of peaking time, arbitrary values. ENC is expressed as* $\sqrt{ENC_{//}^2 + ENC_{1/f}^2 + ENC_{thermal}^2}$. *Variation of each part of the equivalent noise charge in front of leakage current or capacitance shift the noise behaviour to the peaking time of filters.*

III.3. Other filters

A large variety of filters exists in literature, each one showing advantages and drawbacks. Hereafter, I describe some of the usual filters in the scope of X-Ray imaging spectroscopy.

III.3.a. Delay line pulse shaping

One filtering method is to sum the value of the CSA signal with its inverted and delayed signal. This way, the low frequency noise is attenuated, and shaping is relatively fast. This type of filter is essentially used for scintillation detectors at higher energies than hard X-rays. It suffers from a poor resolution because the thermal noise is not filtered. It is used when speed is the limitation [37]. It is one of ancestor of time variant filters detailed below.

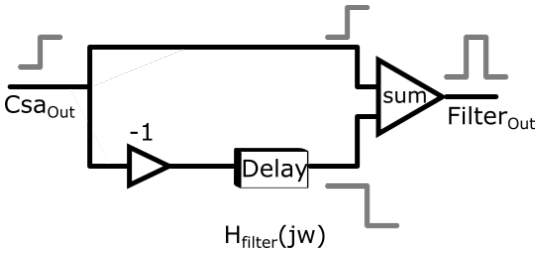

FIGURE 2.24 – *Schematic of a typical delay line shaping. On the bottom part, the inverted delayed signal is summed with an amplifier to the non-modified signal out of the CSA. This way a small pulse is created, result of a very simple and fast filtering.*

III.3.b. Time variant filters

Some implementation can be done by sampling data at different points and performing subtraction, averaging or other type of arithmetical operations with the sampled data. The fact of sampling the signal at a certain point in time implies a variation of the filtering with this same time. A filter which transfer function varies in time is called a time variant filter. The most popular ones are triangular, trapezoidal, Correlated Double Sampled (CDS) filters [22], [23], [12]. Contrary to the previous analysis on semi-gaussian filter, no frequency transfer function can be set up due to the equivalent infinite response frequency when the signal is sampled. Still, an equivalent to the transfer function in time domain can be used to perform analytical analysis of such filters, named weighting function [38].

The weighting function is the response of a system at a measured time t_m for a charge step input (or current Dirac pulse) occurring at a time τ. Each noise contribution can be computed the same way as with time invariant shaping, with integral in time instead of frequency and the use of Campbell theorem. For example, parallel noise would be expressed as [39]:

$$ENC_{//}^2 = \frac{1}{2}\alpha_{//}^2 \frac{\int_{-\infty}^{\infty}[w_N(\tau)]^2 d\tau^2}{q} \tag{2.35}$$

With w_N, the normalized weighting function equivalent to the transfer function divided by output maximum.

Following the previous explanation, diversity of filter can arise from sampled output. Such filters can be used for long time constant filtering without the use of large passive components. One can cite the use of trapezoidal shape filter, which is a robust approximation to cusp ideal filter, with VERITAS [23] ASIC. Correlated Sampling or Multi Correlated Double Sampling (MCDS) implementation of time variant filter is common in literature with for instance CAMEX [22] ASIC or D2R1 [40] ASIC.

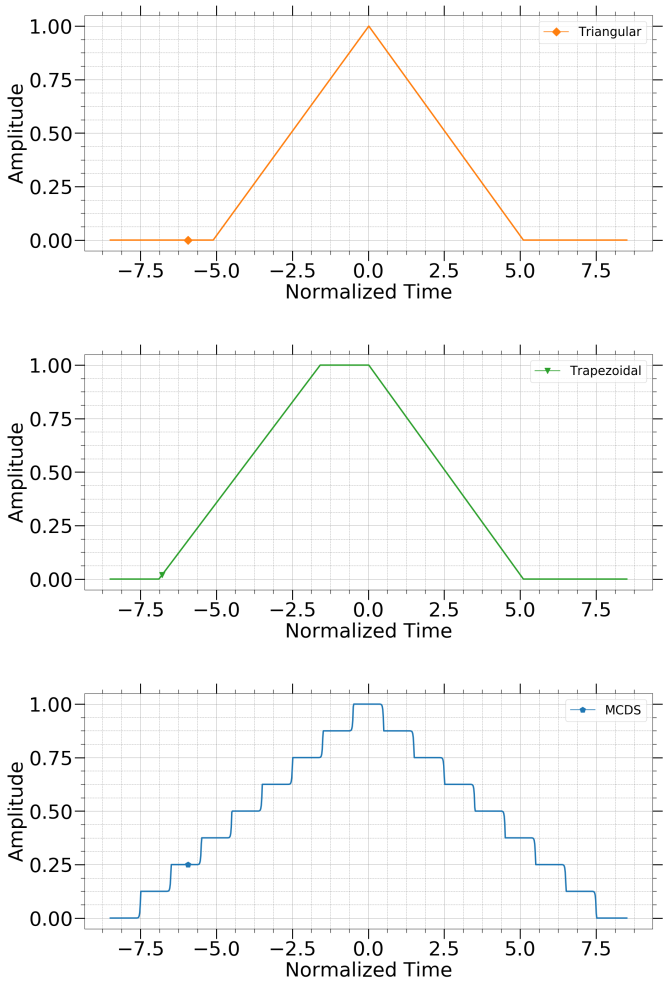

FIGURE 2.25 – *Weighting function of different time variant filters: a trapezoidal filter, a MCDS filter with low number of samples, a MCDS filter with high number of samples*

Relatively good resolution can be reached with both type of filters (semi-gaussian or time variant filters). The advantages of MCDS for instance, rely in the relatively small area occupied by the sampling and averaging part which is only limited by kt/C noise of the sampling. Semi-Gaussian, takes advantage of having a continuous shaping, that does not need any clocking circuitry. Clocking during acquisition might generate pickup noise on surrounding circuit or on the detector itself. This is particularly risky when the detector is just on top of the ASIC, as specified in the scope of this thesis.

Both types of filters can be compared computing their $A_{//}$, A_f, A_{th} coefficients:

TABLE 2.1 – *Comparative table of filters.*

Filter	$\mathbf{T_{peak}}$	$\mathbf{A_{//}}$	$\mathbf{A_f}$	$\mathbf{A_{th}}$	$\sqrt{\mathbf{A_{//}A_{th}}}$
Cusp	τ	0.5	2.01	1	0.5
Triangular	t_m*	0.33	2.77	1	0.57
Trapezoidal	$T_{Flat} = t_m$*	0.83	4.33	1	0.92
$CR - RC^1$	RC	0.92	3.69	0.92	0.92
$CR - RC^2$	2RC	0.64	3.41	0.85	0.74
$CR - RC^3$	3RC	0.52	3.32	0.93	0.70
$CR - RC^5$	5RC	0.40	3.25	1.11	0.67
$CR - RC^9$	9RC	0.30	3.20	1.41	0.65
MCDS	k=4** f=0.8MHz	0.34	2.9	3.15	1.03
MCDS	k=16** f=1.6MHz	0.33	2.62	1.71	0.75

*: t_m is the time to peak for triangular and trapzeoidal filters
**: CSA time constant equals $\frac{1}{2\pi B_w}$ with $B_w = 0.8$ MHz

The most valuable data to compare filters is the last column of the table 2.1 where one can see the better filtering for a fixed peaking time in absence of flicker noise. For all of the above coefficients, it appears that values are relatively close to each other.

III.4. CSA Optimization

For any type of filter, equivalent noise charge can be expressed using the coefficient expressed in table 2.1 as the combination of flicker parallel and thermal noises:

$$\begin{aligned} ENC^2 &= ENC_{//}^2 + ENC_{th}^2 + ENC_{1/f}^2 \\ ENC^2 &= \frac{1}{q^2}\left(\frac{A_{th}\alpha_{th}^2}{T_{peak}} + A_f\alpha_{1/f}^2\right)(C_f + C_{det} + C_{Csa})^2 + A_{//}\alpha_{//}^2 T_{peak} \end{aligned} \tag{2.36}$$

Compared to equation 2.33, we expressed $C_{in} = C_{Csa} + C_{det}$. Input MOS transistor has its own capacitance which influences the noise the same way as a detector capacitance does. With a fixed current, input transistor size modifies its transconductance as well as its input capacitance C_{Csa}. For a fixed length, increasing area of input transistor reduces the noise factors α_{th} and $\alpha_{1/f}$ but increases C_{Csa}. Thus, an optimal dimension of the input transistor that minimizes the thermal noise or the flicker noise can be calculated. Such optimization is detailed in Appendix A, which leads to different optimal points for flicker or thermal noise.

III.4.a. Flicker Noise Optimum

The optimal point for flicker noise is found when:

$$C_{Csa} = C_{det} \tag{2.37}$$

III.4.b. Thermal Noise Optimum

The optimal point for thermal noise is found when:

$$C_{Csa} = \frac{C_{det}}{3} \tag{2.38}$$

III.4.c. Optimum

Since the dimension of the input transistor has no effect on parallel noise, the optimum transistor capacitor stands between these values. For a given ASIC technology, development and optimization of the chain is directly linked to the knowledge of detector metrics such as capacitance and leakage current. Both parameters shift the optimum, hence require a different CSA scaling and filter time constant. In other words, for each detector parameters pair (C_{det}, I_{leak}), one can find an optimal electronic parameters pair (W, T_{peak}) that minimizes the ENC of the whole system.

In terms of noise, the optimal point of the chain is the minimum point of the ENC curve (as shown in Fig 2.23) and it is reached when the parallel noise equals the thermal noise at:

$$T_{peak_{opt}} = \sqrt{\frac{A_{th}}{A_{//}}} \frac{\alpha_{th}(C_{Csa} + C_{det} + C_f)}{\alpha_{//}\sqrt{I_{leak}}}$$

Giving:

$$ENC_{opt} = \frac{1}{q}\sqrt{\begin{array}{l} 2\sqrt{A_{//}A_{th}}\alpha_{th}\alpha_{//}\sqrt{I_{leak}}(C_{Csa} + C_{det} + C_f) \\ + A_f\alpha_f^2(C_{Csa} + C_{det} + C_f)^2 \end{array}} \tag{2.39}$$

For instance, if the leakage current is relatively large, following equation 2.39 leads to a reduction of peaking time to reduce impact of leakage current noise contribution. The ASIC has to cope with this, and has to minimize the thermal noise. For this reason, NMOS input transistor is preferred because it has a better transconductance over area ratio than PMOS.

For AMS 0.35 μm technology, we can estimate the different parameters for α_x. For instance, with $\alpha_{th} = 2.10^{-9}C.s^{\frac{1}{2}}.F^{-1}$, $\alpha_f = 5.5.10^{-7}C.F^{-1}$, $\alpha_{//} = 6.10^{-10}C.s^{\frac{1}{2}}A^{\frac{-1}{2}}$, with a detector of 200 fF capacitance and leakage current around 1 pA, optimizing for thermal noise, minimum noise is expected to be 6 el.rms at 1 μs.

IV. Holding data and discrimination

Referring to Figure 2.1, once signal has been filtered, the desired information needs to be memorized. This function is performed by the above-mentioned data block which can vary in many ways. Moreover, some triggering circuitry can be used to inform of the arrival of a charge above a predefined threshold. In this case, the circuit is read only when something has to be read out. Such function is not always necessary as it can be assessed by reading out pixel constantly (see next part on readout strategies). I will detail the possible implementations of such circuitry which is largely used in imaging spectroscopy.

IV.1. Holding data

IV.1.a. Sample and hold

The easiest way to memorize the charge is to sample the output of the filter at its maximum value. It can be made by the use of a switch and a capacitance combined together. The switch can be activated at the appropriate time, copying signal to the capacitance that holds the signal until another signal allows to read the stored value.

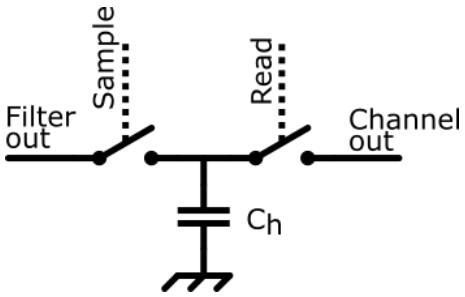

Figure 2.26 – *Sample and hold ideal schematic*

Two points can be emphasized for sample and hold system:

Firstly, the sample signal has to arrive at the exact maximum of the filter's output or at least at a constant time delay. The general use of sample and hold circuitry is directly inside the filter with MCDS filtering schemes or combined together to have a full view of the signal shape as with the analogue memories [15], [3].

Secondly, sampling is subject to errors due to injection of charges created by the coupling capacitors and switches when sampling the signal. This tends to use relatively large sampling capacitance in order to minimize such effects. The later is also a good way to reduce $\frac{kt}{C}$ noise sampling.

IV.1.b. Analogue Memories

As mentioned before, tracking the signal shape can be done by means of an array of sampling and hold circuitry connected together. Such architecture is called an analogue memory. Such circuitry is relevant when the signal shape is needed. This type of circuitry occupies a large area in a silicon device due to the large amount of capacitance needed.

However, such a design allows for good performance and can be useful when signal track is needed as it could be the case with gaseous detectors [3].

IV.1.c. Peak and hold

Introduced by [4], [41],and [42], the peak and hold circuitry takes advantage of a non-linear circuit (such as a diode) connected with a capacitance and an operational amplifier to charge the capacitance until signal has reached its maximum.

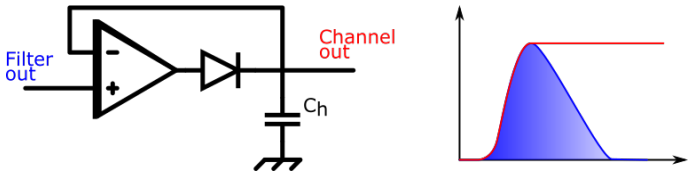

FIGURE 2.27 – *Peak and hold ideal schematic*

When the signal has reached its maximum, the output amplifier amplifies difference between the maximum value of the signal and the falling shaper signal. This results in the output of the amplifier to be lower than the diode biasing voltage and results in keeping the voltage at the maximum experienced value.

A proper circuitry is then needed to reset the capacitance and restart the peak and hold. Moreover, if another higher value signal occurs before reading out the value, the peak and hold circuitry memorized its value instead of the first one.

I detail more thoroughly the design of a peak and hold circuit in chapter 4.

IV.1.d. Time over threshold (TOT) and counting

Another way to obtain a digital output linked with input amplitude is to make use of a time over threshold measurement.

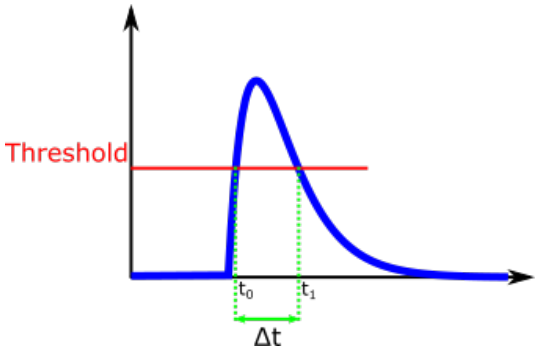

FIGURE 2.28 – *Time over Threshold*

In a typical time over threshold architecture [43], either a Time to Digital Converter (TDC) or a Time to Amplitude Converter (TAC) is used in order to measure time difference between t_0 and t_1, the two thresholds crossing detector times. With a TDC, the time information that depends on the energy is a digital value. Discrepancies due to signal jitter (noise in time) as well as highly non-linear behaviour requiring tedious calibration does not allow time over threshold to be used for high resolution spectroscopy applications. However, it is often a useful function to allow charge measurement beyond the linear and even in the saturation range of the circuit.

IV.1.e. Direct digitization

In all above mentioned methods except TOT+TDC, the information is memorized in analogue manner. Values are usually digitized downstream by an external (or internal) Analogue to Digital Converter (ADC). Such circuitry could be directly used to sample the signal into the chip. In such a design, the ADC needs to have a good resolution, and to be fast enough. Such prerequisites generally require a power consumption which is usually not desirable. However, with new microelectronic technologies and increasing ADC performances, it is a more and more feasible option, as it has been demonstrated in several ASICs in [2], [13].

IV.2. Discrimination

It is often suitable to give information to the external controller that a charge has been detected in the device and is ready to be read out. This trigger signal can be used to initialize an external ADC to sample the data, or can be used to measure the counting rate of the experiment. Such information is provided by a discrimination stage detailed below.

IV.2.a. Basic circuit description

Introduction

Discrimination consists in comparing the filter output to a fixed reference. When the filter output is higher than the reference, discriminator output sends a digital signal named trigger, to inform of the arrival of a photon whose energy is higher that the fixed reference.

We can sum up its behaviour with the Figure 2.29. An amplifier amplifies the difference between the signal and the reference with a gain A_1. The output $V_{discri} = A_1.(V_{filter} - V_{ref})$ is sent to a logic circuitry to provide a proper digital signal: here inverters.

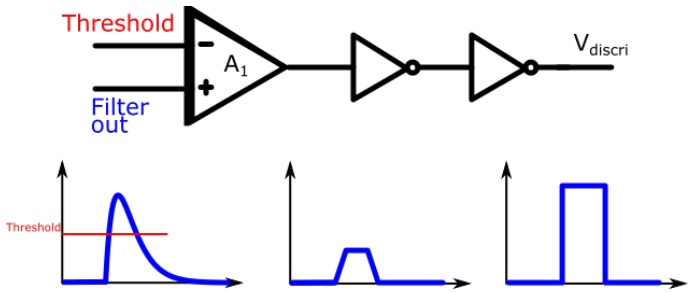

FIGURE 2.29 – *Discriminator functional schematic*

Speed

Discrimination speed is a function of the bandwidth. When designing an amplifier, for a fixed power, it is only possible to have a fixed gain to bandwidth product (GBW). Assuming a series of first order amplifier, it can be proven [44] that an optimum exists in the number of stages for a fixed open loop gain. Such optimum is expressed to be $n = 2ln(A_{tot})$. However, this optimum leads to a large number of stages which also lead to a larger area and power consumption.

Hence common architectures do not reach this optimum. As usual, a compromise has to be found between power consumption, area and speed that greatly depends on the application.

Noise

Such discrimination system aims at detecting the smallest possible charge, triggering the circuitry. However, if threshold is too close to the filter's baseline, auto triggering in presence of noise might occur. This behaviour is not desirable. A mathematical model is expressed in reference [45] which details the rate of noisy triggers in presence of a CR-RC filter with a white noise output.

Time walk

From the beginning of the discussion on discrimination circuitry, we assumed the filter signal to rise as a step. In practice, this is not true as rising time is defined by the peaking time of the filtering circuitry. This leads to different triggering times with respect to real event arrival time, when amplitude is varying. Figure 2.30 details such behaviour.

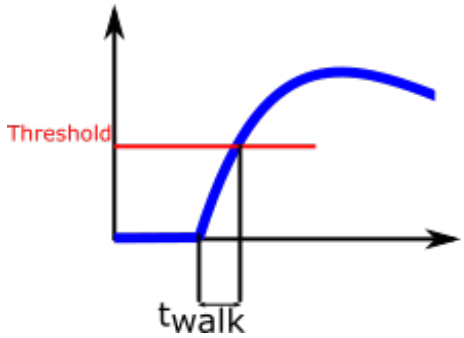

FIGURE 2.30 – *Time walk description*

This effect is named time walk and contributes to degrade the timing resolution. Time walk can be compensated after charge measurement. However, discrepancies between channel in baselines, and peaking times can lead such a compensation to be resources consuming. Setting a really low value threshold is a good point for reducing the time walk. Low noise architectures are naturally more immune to time walk. Moreover, different compensating techniques and architectures exist in literature in order to compensate for such time walk such as leading edge, zero crossing or constant fraction discriminators.

V. ASICs FOR X-RAY IMAGING SPECTROSCOPY

In the scope of X-Ray imaging spectroscopy, many ASICs have been developed through years for different applications, with different needs. The purpose of this paragraph is to introduce the relatively recent ASICs, performing Hard X-Ray spectroscopy and compare performances between ASICs and emphasize the different strategies used to develop such readout circuits. The list is not exhaustive, and specialized for relatively hard X-Ray ranging from hundreds of eV to several hundreds of keV.

Table 2.2 – *ASIC for X-Ray Imaging Spectroscopy*

Name / Technology	Layout	Pixel Size	Pixel Number	ENC floor (el.rms)	Power (W/cm^2)	Energy Range (kel)	Ref
HEXITEC / AMS 0.35	2D	250 x 250 μm^2	80 x 80	20	NA	0.9 - 45	[46] [24]
Timepix3 / TSMC 0.13	2D	**55 x 55 μm^2**	**256 x 256**	60 (ToT)	1	0.3 - 30	[5]
CAMEX / IMS Duisburg 5V	1D pnCCD	75 μm	128	2.5	0.32	0.09 - 7	[22]
D2R1 / XFAB 0.18	2D	300 x 300 μm^2	16 x 16	29	0.3	0.5 - 56	[40]
IDeF-X HD / AMS 0.35	1D	150 μm	32	33	0.13	0.45 - 223	[47]
AGIPD IBM 0.13	2D	200 x 200 μm^2	64 x 64	322	NA	0.8 - 5	[12]
H02 TSMC 0.25	2D	200 x 200 μm^2	32 x 32	300	0.28	2.3 - 20	[48]
VEGA / AMS 0.35	1D	200 x 500 μm^2	32	12	0.42	0.05 - 16.7	[25]
VATA451 / NA 0.35	1D	NA	64	30	NA	-10 - 10	Ideas
XRS Asic / TSMC 0.25	1D	350 x 2000 μm^2	16	**7**	**0.015**	0.04 - 2.8	[49]
NuASIC / Orbit 1.2	2D	600 x 600 μm^2	32 x 32	50	0.13	0.2 - 30	[50] [51] [52]
DANA-3 / XFAB 0.18	2D	500 x 500 μm^2	16 x 16	200	0.08	2 - 340	[53]
VIP-PIX / TSMC 0.25	2D	700 x 800 μm^2	10 x 10	98	0.04	**-438 - 438**	[54]

V.1. Hybridization strategies

For hybridization, I distinguished 3 types of architectures [55] that are depicted in Table 2.2, expressed as 1D, 1D pnCCD, or 2D. Figure 2.31 shows a schematic view of such hybridization architectures.

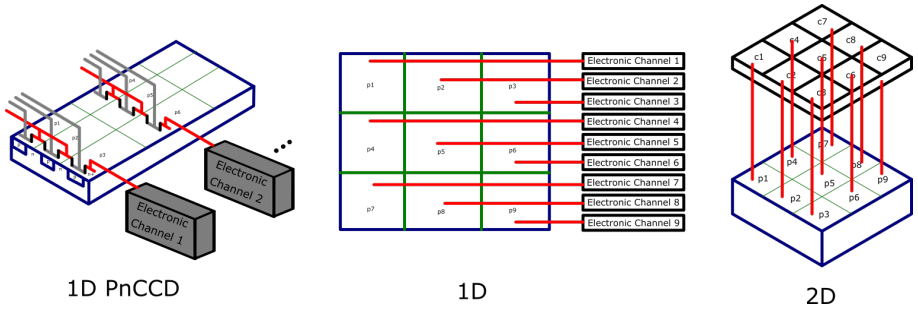

FIGURE 2.31 – *1D PnCCD, 1D, and 2D architecture schematic.*

The 1D architecture has the advantage of having a fixed channel width but not a fixed length. This freedom allows designer to reach better spectral resolution as the capacitance is not increased if the channel increases due to improved filtering. The main drawback is the limitation on the pixel density. In case of a pixelated detector, 1D ASIC must either be implemented on top of the detector as with XRS ASIC, leading to several black spot, or above the detector as it is the case with IDeF-X ASIC and Caliste technology [56]. The later takes advantage of the possibility of 3D interconnection between vertical ASICs and horizontal detector. 1D architecture can also be used with silicon drift detectors (as with VEGA [25]) to perform imaging reconstruction, without having a proper pixelated detector.

The 1D pnCCD architecture is based on the insertion of some transistors directly inside the detector. Clocking each transistor allows for passing the charge of one pixel to another, in a train-like configuration. Hence, 1D ASICs are able to read the pixelated detector, frame by frame. The main advantage of such configuration is the immunity to noise as input JFET (main source of electronic noise) is directly inside the detector minimizing input capacitance, hence electronic noise. Unfortunately, for hard X-ray, Silicium has a relatively low efficiency forcing the use of denser detector (such as CdTe) which can not be produced with input JFET transistors for now.

The 2D architecture is the architecture depicted and explained in the Chapter 1. An ASIC with a pitch equals to the detector's pitch is bump bonded to the detector. Considering this, a relatively high density can be achieved (impressive examples lies with the Timepix3 ASIC [5]). The direct connection has the main advantage of reducing input stray capacitance, which allow achieving very good energy resolution by reducing flicker and thermal noise.

V.2. Readout Strategies

Mainly two types of readout can be distinguished. The self-triggered (photon counting mode) architecture and the frame readout.

V.2.a. Triggered readout:

Triggered readout is based on two steps. The first step consists in waiting for a photon of sufficient energy to be detected, and integrated. Once it has been integrated, a triggering circuit inside the ASIC informs the controller (FPGA) that a photon of sufficient energy has been detected. Performing a "OR" logic operation between channels, one may know if any pixel has encountered a sufficient energy. Once such information is acknowledged, the second step starts by freezing the chip to acquire other data and send pixel data.

The time for reading out every data is considered as a dead time (since no charge integration is authorized) which can be fixed or depends on the number of pixels to read. This constant dead time allows for time stamping event with a good accuracy but usually suffers from lower counting rate than continuous readout.

However, one of the main advantages is the power consumption of such circuitry which does endure a digital consumption only for a small-time during data acquisition. It also allows for fewer spurious event created by readout sequence cross talking to the detector.

We can cite [47], [48] as references for such architectures.

V.2.b. Continuous readout:

Continuous readout circuits do not use any triggering system and follows a single step operation. Each pixel acquires data while being read one by one at a fixed time period. The time of arrival of photon is unknown but framed in the readout period. However, the complexity is reduced and speed is allowed to be relatively high.

Some events can be corrupted if pixel acquisition occurs during integration. To avoid such misbehaviour, one can cite [24] and its sampling system allowing for sampling signal if it has not been fully integrated during previous acquisition.

A majority of ASIC mentionned in Table 2.2 are using a continuous readout as for example [5], [53], [12], [22]. It lies in the simplicity of such readout combine with high count rate necessity.

VI. Conclusion

I have introduced the basic functions essential in a charge readout channel. I explained the necessity to use an Application Specified Integrated Circuit that has to cope with the detector parameters in order to optimize the whole detection system in terms of noise.

The chain composed of a charge sensitive amplifier, a filter, discrimination, and data analysis blocks has been detailed and leads to a variety of architectures in the literature.

I also detailed the working principle of filters, and described the optimum filtering spectroscopic chain based on cusp. The impossibility to reach infinite time measurement led us to detail the practical existing filters, allowing for a relatively close to optimum filtering.

Great progresses have been made in the last decade, following the affordability of small size integrated circuit technologies. Such technologies have to cope with space harsh environment as detailed in Chapter 1.

Now that these concepts have been introduced, especially the basis of noise analysis, I can start to detail the developments and measurement performed during my thesis. Such developments aim to develop a high density, low noise integrated circuit for space based Hard X-Ray imaging.

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Chapter 3: First steps in the design with prototype results

In the firsts chapter, we demonstrated the need of a new detection system for hard X-ray space-borne astrophysics made of a pixelated CdTe detector coupled to a specific low noise integrated circuit. In order to optimize the design of such an ASIC, one needs to fix several parameters. The choice of microelectronic technology (node and manufacturer), the feasibility and performances of hybridization to the CdTe detector, and the architecture choices.

The choice of the technology node has been made before my thesis. It is a compromise between radiation performances, price, and density. The node is 180 nm. In this aspect two prototypes named "Caterpillar chips" from two different manufactures AMS and XFAB have been developed and tested in a previous thesis and have shown almost similar behaviours. I have performed Total Ionizing Dose measurements on these chips in order to discriminate both manufacturers and make a choice. I have chosen the XFAB 0.18 μm technology as detailed on the first part of this chapter.

In order to evaluate the detector to ASIC hybridization process, a chip named D2R1 has been produced in the XFAB 0.18 μm technology and hybridized to a CdTe detector prior to my thesis. I have performed measurements with X-Ray sources in order to test the noise performances of the hybridization process for high resolution spectroscopy. Details are given on the second section of this chapter.

Finally, I have developed and tested a new ASIC in the AMS 0.35 μm technology named IDeF-X HDBD in order to get familiar with low noise design for radiation detectors and validate particular circuit architectures before integration in the final circuit. The technology choice has been driven by the advantages of previous developments on this technology in the laboratory in order to decrease the design time. The last part of this chapter details this circuit in details.

The ASIC, named IDeF-X D^2R_2, resulting in the choices expressed above is detailed in chapter 4.

I. Caterpillar Test chip: radiation measurements

As mentioned in Chapter 1.II.5 page 31, integrated circuits in space endure harsh conditions. These conditions can lead to failures in the circuit and have to be considered during the design phases. High temperatures variations, vibrations or radiation damages can be one of the origins of these failures. For temperature, in order to maintain the detector performances (essentially leakage current), the system is maintained at a regulated temperature. Hence, no extreme temperature variation is expected in the electronics. For vibration, the critical point in the system made of a detector on top of the ASIC is the interconnection part. Hence, tests should be performed with both systems and do not especially require vibration tests at the ASIC level. For radiation, damages can occur in the detector but also inside the ASIC.

When an object is sent outside the atmosphere, it becomes exposed to cosmic rays coming from the outer space [1]. These cosmic rays interacting with atmosphere and magnetosphere create environments in upper atmosphere and space with various particles as neutron, protons... Integrated circuits are subject to different kinds of damages due to these fluxes [2]. In this part, I detail the different radiation effects, the mitigation techniques and the results of total ionizing dose sensitivity performed with a prototype chip.

I.1. Radiation damages on integrated circuits

Radiation damages can create different defaults depending on the location of the interaction of particles within the integrated circuit:

- **Cumulative effects**
  - Total Ionizing Dose (TID)
  - Displacement Damages Dose (DDD)
- **Single Event Upsets (SEU)**
- **Single Event Latchup (SEL)**

I.1.a. Total Ionizing Dose

Charged particles interact with an integrated circuit by ionizing the medium (here mostly silicon or silicon oxide). Depending on their inner energy, the interaction is mostly probable to take place at different depths. For relatively small energies (around keV), interaction is mostly at the surface of the device creating no default, whereas for higher energies, the particles tend to modify transistors behaviour. The main effect that causes degradation of transistor performances is when a high energy photon, a proton or an electron interacts with the silicon dioxide under the gate. The charged particle deposits an amount of energy through the dioxide creating electron-hole pairs. If an electric field exists between both electrodes (i.e. between Gate and Drain or Gain and Source), electrons are collected whereas holes stay inside the oxide due to their poor mobility. This creates positive charges under the gate that either decrease/increase the threshold voltage (NMOS/PMOS) or create leakage current on transistors edges [3]. If the ASIC is not powered, consequences tends to be limited as no hole is trapped in the oxide. This means that the circuit has to be biased during TID tests.

As mentioned before, holes have a poor mobility, however, after a large amount of time, holes recombine and the ASIC return to its initial state. This effect named annealing can be sped up by increasing the temperature.

For a space mission, the dose rate can be computed by simulation knowing the orbit, the shielding, the interaction with silicon. Dose is computed as the received energy per mass :

$$Dose = \frac{1}{\rho}\frac{\mathrm{d}E}{\mathrm{d}V} \tag{3.1}$$

Where ρ is the true density.

The received energy is the result of a complex calculation of interaction that depends on the source spectrum (nature and energy of the incident particles) and geometrical data (angle). We cannot fix a universal dose value for every missions but a typical value at the end of a mission is in the range of 100-3000 Gy (10 - 300 krad) according to some future missions like ATHENA [4], JUICE [5], or ESA specifications [6].

Different solutions can be experienced in order to mitigate dose effects:
- Enclosed Transistor Layout (ELT) [7] which reduces the geometrical border effects. Preventing charged particle to create a path inside isolation between gate border and drain.
- Increase transistor size (especially its length) to reduce border effect.
- Reduce the gate thickness, allowing a lower probability of interaction within the sub gate dioxide layer. This means that reducing technological node generally reduces the TID sensitivity of a circuit.

The later one is the main reason why we decided to test two 0.18 μm node technologies appearing to be a good compromise between technology availability (price) and TID hardness.

I.1.b. Displacement Damages Dose

Un-charged particles (such as neutrons) do not deposit electron/hole pairs under the gate like charge particles would do. Hence, they do not affect any intrinsic part of a CMOS. Instead, it creates displacement damages in the Silicon lattice. Displacement damages correspond to the interaction of a neutron directly with the atoms, displacing one of them, creating default in the structural lattice of the circuit. These defects change the energy gap of the concerned region, that in practice, results in a shift of electrical parameters (conductivity, thresholds...). Annealing can correct defaults created by neutron damages, allowing thermal movement of the lattice that tends to return to its equilibrium state.

I.1.c. Single Event Effects

Charges created in a circuit by ionizing particles may be collected at the node of an active circuit (such as a flip-flop cell), modifying its behaviour. These charges can flip the value of a digital circuit at this node. The amount of deposited charge can be expressed by:

$$
\begin{aligned}
&Q_{particle} = \frac{LET.\epsilon.\rho.q}{X} \\
&Where : LET = \frac{1}{\rho}\frac{\mathrm{d}E}{\mathrm{d}x} \text{ is silicon the linear energy transfer} \\
&\epsilon \text{ is the digital device thickness} \\
&\text{q is the elementary charge} \\
&\rho \text{ is the silicon density} \\
&\text{X is the silicon energy gap : 3.6 eV}
\end{aligned}
\tag{3.2}
$$

When this charge is larger than the charge stored on the digital node, a bit flip happens in the digital circuitry that can modify its behaviour. These kinds of effect can happen in a combinatory circuitry (Single Event Transient) or in sequential circuitry (Single Event Upset). This can lead to misinterpretation of data, that can modify the whole behaviour of the chip. Several mitigation techniques exist:
- One can just increase the critical charge of its digital circuitry by increasing circuit size [8]:

$$Q_{critical} = \frac{\epsilon_0.W.L.\Delta V_{Flip}}{q} \tag{3.3}$$

Where: W,L are the transistor sizes
ϵ_0 is the oxide permitivity
ΔV_{Flip} is the voltage needed to flip the state (around $\frac{V_{dd}}{2}$)

This solution has the inconvenient of increasing size and delay of digital circuitry without being sure of suppressing the effect.

- Another way of preventing damage is to multiply the number of flip flop. For instance, duplicating the sequential part allow to alert when a fault has been detected. Triplication even allows to automatically correct such error by use of majority voters. Triplicating and splitting the 3 cells with an appropriate distance [9] in combination with majority voters reduces the amount of SEE's by a larger factor. Still, these solutions introduce larger delays, and increase the circuit size.

A comparison of solutions for RadHard By Design (RHBD) can be found in [10].

I.1.d. Single Event Latchups

When a PMOS and an NMOS transistor are close to each other, they can constitute a parasitic thyristor as depicted in Fig 3.1. In order to increase density of logic functions, in CMOS technologies, PMOS and NMOS transistors are closer and closer to each other and can make parasitic thyristor more and more sensitive. The impact of a high energy particles can generate a charge that can activate the thyristor. Once activated, current is free to pass between power supplies creating a short circuit. This ends up increasing temperature due to Joule's effect until it destroys the structure [11].

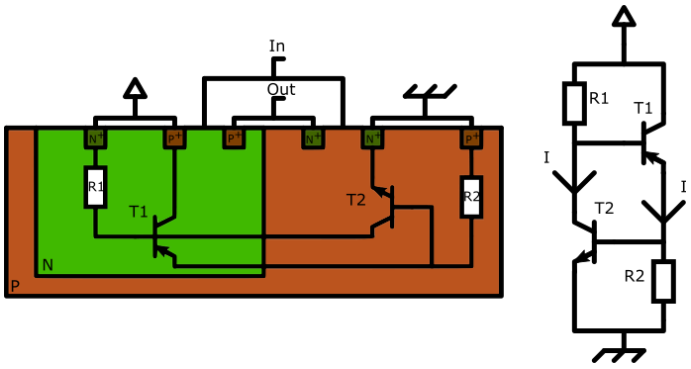

FIGURE 3.1 – *Parasitic thyristor of an inverter. The I current is potentially destructive.*

To prevent this to happen, the most robust mitigation technique consists in creating a whole set of digital cells with a larger distance between P and N tubs and add substrate contacts between these tubes to the ground. By doing so, one modifies the critical electronic parameters of the thyristor (access resistors, bipolar gains) and one at least reduces the sensitivity of the circuit to latchups. But this solution suffers from major inconvenience: it reduces the speed of the circuitry and decreases its density.

To conclude, a proper design takes into account all these potential damages from radiation and try to mitigate them by choosing the proper technique, in balance with the desired performances in term of speed, size, and technological choice and with the foreseen environment. For TID mitigation, we demonstrated that a modern technology with small oxide thickness was mandatory. In contrast, modern technologies are more sensitive to SEU because of their small critical charge due to low power supplies and low charge capacitors. For our design we decided to work on a 0.18 μm technology. This decision was made in order to reduce TID induced damages as well as increasing chips density. In the next section I describe the tests we have made to choose between two different technologies of this node: AMS and X-FAB.

I.2. Caterpillar chips description

Caterpillar test chips include a set of different sizes and different input transistor types Charge Sensitive Amplifiers (CSA) in order to optimize CSA noise behaviour on both technologies (AMS 0.18 μm and X-FAB 0.18 μm technology). Both ASICs results can be found in literature [12] [13].

I performed the TID test on the AMS 0.18 technology only. Descriptions of such chips, and test results are given in the following part.

I.2.a. Basic cell description

For both ASICs, the basic cell is a Charge Sensitive Amplifier composed of a folded cascode architecture amplifier, a feedback capacitor, and a reset transistor as depicted in Fig 3.2.

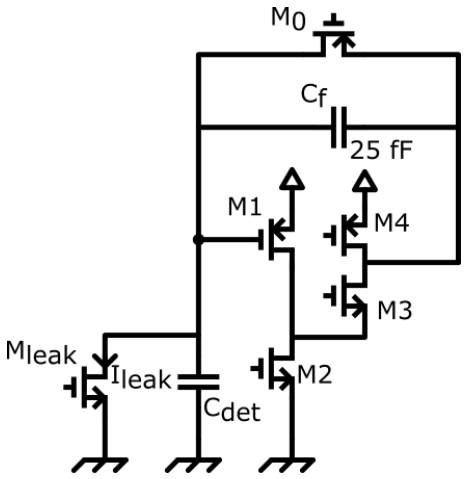

FIGURE 3.2 – *Charge sensitive amplifier with PMOS folded architecture*

In the scope of my thesis, input capacitance and leakage current were smaller than in [14], so a new optimization has been made. I detail this optimization in Chapter 4 and do not detail the one made for Caterpillars chip that can be found in [12]. For comparison purpose I chose one charge sensitive amplifier, similar on both ASICs and compatible with the dimensional study presented in Chapter 4. I compared both CSA sensitivity to radiations after measurements. Table 3.1 details the important values of these transistors.

TABLE 3.1 – *Caterpillar transistor sizes and type for X-FAB and AMS 0.18µm technologies*

M1	M0	M1 Size (W:μm,L:μm)
P thin oxide	P thin oxide	100/0.25

First of all, we need to define, for both technologies, the different parameters of our charge sensitive amplifier on which we want to measure influence of radiation. Then

a very simple and classical modelling of our charge sensitive amplifier enables us to extract some intrinsic electronic parameters from our measured parameters.

I.2.b. Measured parameters

We will focus the analysis on a folded cascode amplifier fed back with a capacitor and a transistor.

Output Amplitude By considering an ideal amplifier of gain -A_0, we can express the transfer function and the output amplitude of a charge sensitive amplifier as expressed in equation 2.3.

Considering the small signal schematic of a PMOS folded cascode amplifier (see Fig 3.3) we can consider its gain (A_0) as:

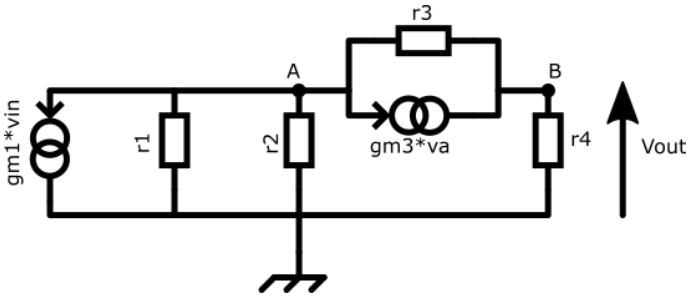

FIGURE 3.3 – *Small signal PMOS folded cascode*

$$\begin{aligned} A_0 &= \frac{gm_1.r_4}{1+\frac{(r_3+r_4)}{r_1.r_2.(1+gm_3.r_3)}} \\ A_0 &\simeq gm_1.r_4 \end{aligned} \tag{3.4}$$

On a first order we can then consider $A_0.C_f >> C_f$ which will give:

$$\Delta V_{out} = \frac{Q_{in}}{C_f + \frac{C_{det}}{gm_1.r_4}} \tag{3.5}$$

Baseline In this architecture, the output baseline is fixed by the reset transistor through the relation:

$$V_{baseline} = V_{Gate} + V_{th_0} + \frac{nkT}{q} ln(\frac{I_{leak}}{I_0}) \tag{3.6}$$

Where V_{Gate} is the applied reset transistor gate voltage equals to: 0.8 V
And I_0 the current when $V_{gs} = V_{th}$.

Thus, if we find a way to extract the evolution of leakage current, we can get information on the shift of M0 threshold voltage with TID. However, we do not expect

such information to be directly usable with measurements. In practice, the chip has been designed to test several transistors to optimize noise parameters. Hence an output buffer allows for choosing the transistor and drive output capacitance. This buffer is composed of a PMOS common drain buffer and one Miller amplifier with adjustable gain. Both have been made with 5V transistors. Thus, baseline is not directly the value of CSA's baseline.

Fall time Fall time of this circuitry is directly linked with the transconductance of transistor M0 which acts as a resistor of high value. The transistor is directly biased by the detector leakage current as described in Chapter 2 with DC coupled reset. The transistor is in the weak inversion since its current is in the pico ampere region whereas length and width are only around few μm. We can then express its transconductance as follow and derive the fall time:

$$\begin{aligned} gm_0 &= \frac{q.I_{leak}}{n.k_B.T} \\ T_{fall} &= \frac{C_f}{gm_0} \ln \frac{0.8}{0.2} = 1.39 \cdot \frac{nk_bTC_f}{qI_{leak}} \end{aligned} \tag{3.7}$$

With n is the subthreshold factor equal to: 2.2 for X-FAB and 1.4 for AMS

Rise Time Rise time is directly linked with output impedance and gain of the amplifier. In measurement, we considered the time the signal takes to get from 10% to 90% of its maximum value. Considering no effect of output cascode stage, its simplified relation can be expressed as:

$$t_{rise} = 2.2\frac{(C_f + C_{det})^2}{C_f.gm_1} \tag{3.8}$$

Thus, by measuring rise time as a function of TID, we can extract the evolution of the transconductance with TID. It gives us a relation between transconductance of the input transistor and Total Ionizing Dose. thanks to this extraction, we can then take information from amplitude shift measurement to extract the output resistance as a function of TID.

Equivalent Noise Charge With previous model we are able to get some important parameters from our transistors. The main goal here is also to quantify noise variation with TID in terms of equivalent noise charge. I remind its equation detailed in Chapter 2:

$$ENC^2 = (C_f + C_{det} + C_0)^2.(\frac{\alpha_{th}^2}{T_{peak}} + \alpha_{1/f}^2) + \alpha_{//}^2.I_{leak}.T_{peak} \tag{3.9}$$

With:
•C_{det}: the detector capacitance
•C_0: the M1 input capacitance and interconnection parasitics
•T_{peak}: the peaking time of out filter used for measurements
•α_{th} , $\alpha_{1/f}$, $\alpha_{//}$ noise parameters related to amplifier and filter

A deep analysis of these parameters has been made for both technologies during a previous thesis [14]. This study has been made for different known input currents, and capacitances. Thus, noise parameters have been extracted from fits measurements and models. We can summarize results in Table 3.2.

TABLE 3.2 – *Caterpillar transistor sizes and type for X-FAB (top) and AMS (bottom)*

Technology:	X-FAB 0.18 μm
α_{th}^2:	$3.2.10^{21}\ s.el^2/F^2$
$\alpha_{1/f}^2$:	$6.2.10^{25}\ el^2/F^2$
$\alpha_{//}^2$:	$1.6.10^{19}\ el^2/s$
Technology:	AMS 0.18 μm
α_{th}^2:	$2.9.10^{21}\ s.el^2/F^2$
$\alpha_{1/f}^2$:	$3.29.10^{26}\ el^2/F^2$
$\alpha_{//}^2$:	$1.6.10^{19}\ el^2/s$

I.3. Results

Measurements for both technologies come from different radiation campaigns. The same setup has been used as well as the same radioactive source.

I.3.a. Test setup

Caterpillar chips are wire bonded to a daughter board composed of passive elements and connectors. This daughter board is connected directly to a mother board containing bias circuit, and slow control link for the change of parameters such as input/output current. This board is then connected to a computer for parameter control. The output of the chip is connected to a CR-RC^2 shaper using BNC cables. The filter output is then sent to an oscilloscope for data analysis and measurement. An internal integrated capacitor allows to inject a charge in the CSA input to monitor functionality during irradiation. For radiation measurements, data has been taken for several Charge Sensitive Amplifiers but will be analysed here only for CSAs expressed in Table 3.1. Fig 3.4 shows pictures of the setup. Equivalent Noise Charge is calculated thanks to signal standard deviation measurement on the baseline and gain measured with charge injection. During irradiation, the whole setup powered on. At several period of time, the setup was taken back to laboratory to perform the different tests and then moved back to irradiator.

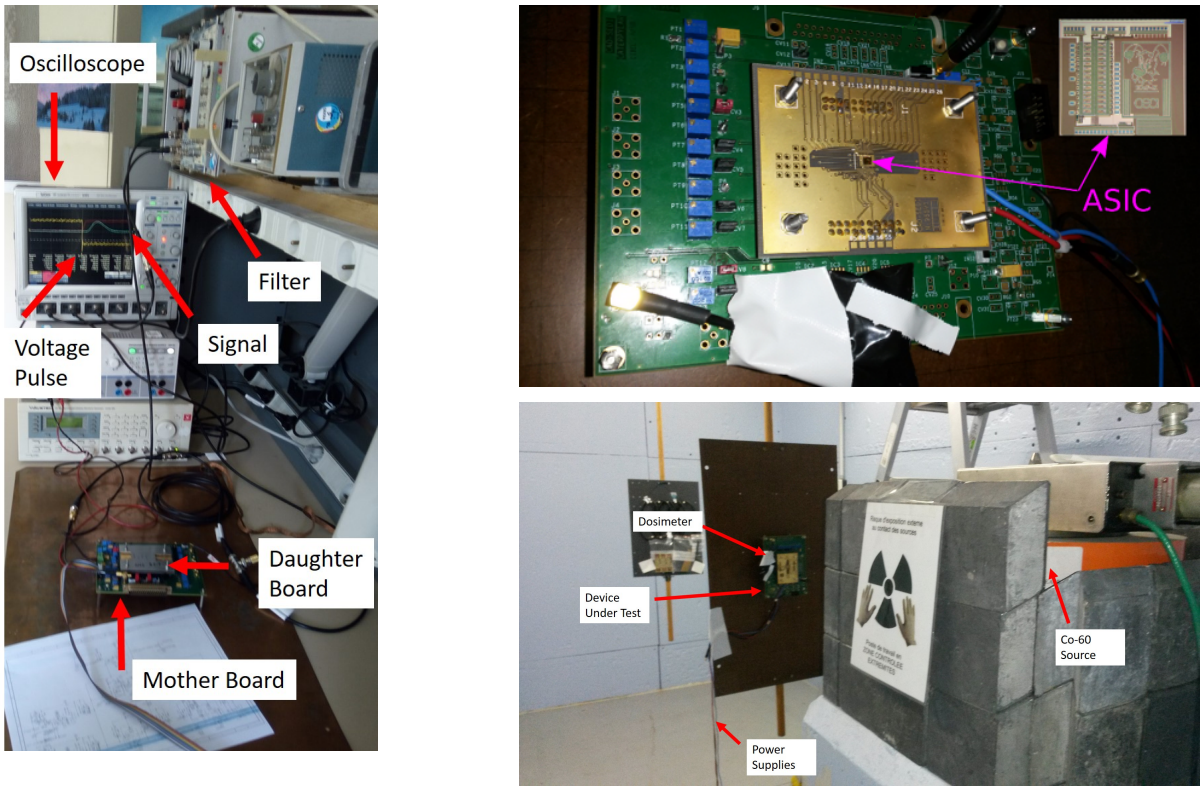

FIGURE 3.4 – *Test setup for signal measurements(left) and irradiation setup (right)*

The whole system has been irradiated at two different periods by using the same ^{60}Co gamma-ray source of 60 GBq that emulates the interaction of space cosmic rays. The source emits 1.17 MeV and 1.33 MeV gamma-rays, high enough to penetrate and damage the electronic system as a cosmic ray would do. During irradiation, dose was measured by a dosimeter taped very close to the ASIC (see figure 3.4). For both irradiation campaigns, the test procedure was almost the same: between each irradiation, setup were taken off the irradiation facility for a small period of 4 hours in order to perform measurements. In caterpillar AMS, Device Under Test (DUT) was always 12.7 cm from source whereas 3 distances (33 cm, 17.5 cm, 11cm) has been used for caterpillar X-FAB. Thus, both measurements did not experience the same dose rate and integrated dose. In the following plot, one can find the total dose for both measurement campaign compared to the time.

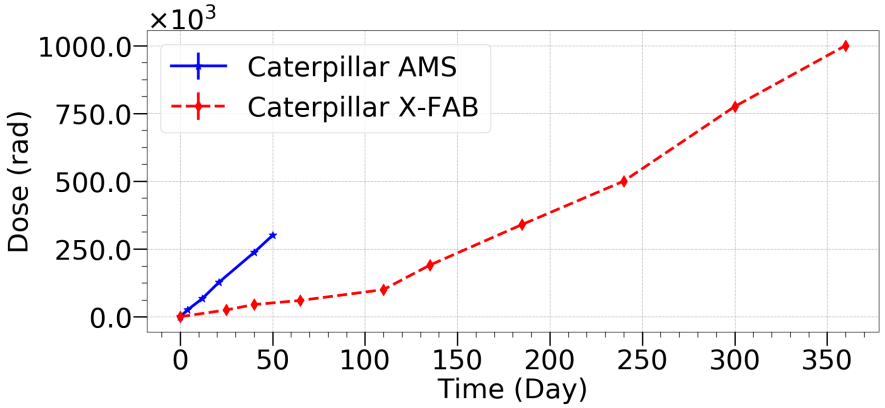

FIGURE 3.5 – *Caterpillar chips accumulated dose*

In Caterpillar AMS, a detailed study has been made to deeply understand radiation damages on the circuit. Equivalent noise charge was measured using an external CR-RC^2 filter with adjustable peaking times. We also measured the output amplitude for a given input pulse, the output DC baseline, the fall time, and the rise time. For X-FAB technology, I quickly present the ENC variation with radiations, letting the reader to look for more information in the published data in [14]. Then, a direct comparison is made in order to compare both technologies, looking for the best radiation tolerant technology in an affordable node.

I.3.b. Results for Caterpillar AMS

Rise time

As mentioned in equation 3.8, the rise time is a good marker of variation on transconductance of our input transistor. Thus, we measured variations on this parameter with radiations. These results can be found in Fig 3.6.

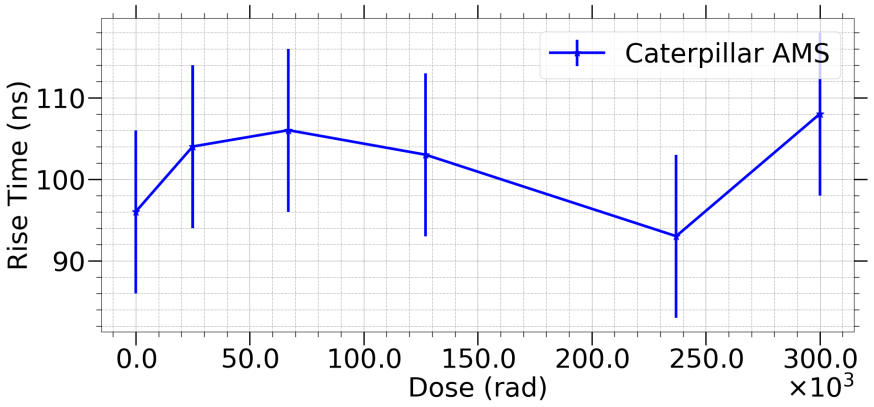

FIGURE 3.6 – *Rise time variation to Total ionizing radiation. Definition of rise time we used is the time for the signal to go from 10% of the maximum value to 90 %*

Even if we noticed some variations, these are far lower than our error bars. These measurements were taken with a small amount of statistics as it had to take only a small amount of test time in order to reduce recombination and thermal annealing during the test in between irradiation periods. We can conclude on this part that the transconductance of our input transistor has not experienced larger modification than 15 % of its original value. Thus, transconductance can be assumed to be almost constant up to 300 krad.

Fall Time

Fall time enables us to have information on the evolution of the input leakage current with the total ionizing dose. Such current corresponds to a current generation inside the ASIC, necessary to bias the reset transistor in a proper region. It emulates the detector leakage current.

During irradiation campaign, I measured the variation on the fall time expressed from 80% to 20% of the signal maximum value. Results are given in Figure 3.7.

The leakage current is mainly expected to increase due to the leakage current generator composed of a NMOS transistor with a fixed gate voltage (see Fig 3.2). Applying model equation 3.7, the computed leakage current has been plotted in the same figure.

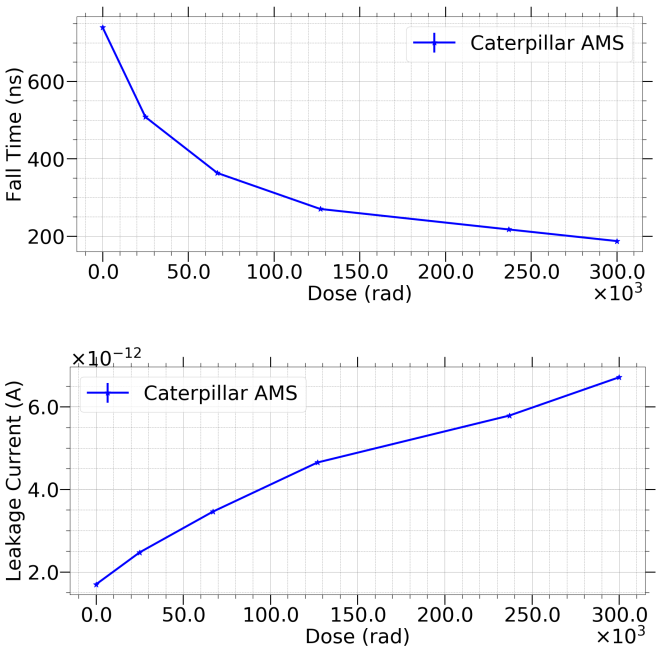

FIGURE 3.7 – *Fall time variation with total ionizing dose (top) and ileak extraction (bottom)*

Leakage current variation, in the range of pico-amperes, is high enough to quantitatively change the equivalent noise charge of our system.

Considering the design Figure 3.2 this increase can originate either from M_{leak}, from M_0 or a combination of both. Giving the data I have measured ; I have no mean to discriminate which is the main contributor to this increase of 4 pA at 300 krad. I personally suspect transistor M_{leak} to be the main contributor, considering the value of gate induced leakage currents for this technology given in the literature [15], [16].

Leakage current increase would be one of the major reasons of the spectral performances degradation with time due to electronics in a space mission. However, considering a semiconductor detector, radiations damages also decrease detector performance. For instance, for Silicon in the scope of a space mission, proton induced damaged increases the leakage current of the detector by a factor of 10 [17]. Moreover, for CdTe detectors, charge transport efficiency and spectroscopic capability is supposedly worsened by neutron damages as reported in [18]. Hence, we can expect a TID induced spectroscopic degradation primarily due to detector degradation and to a lesser extent to the electronics degradation.

On top of that, if the leakage current increase is due to the M_{leak} transistor, as supposed, such transistor can be cutoff when electronic is linked to a detector, as no external leakage current is needed to bias the circuitry.

Baseline

During the whole irradiation campaign, baseline has been monitored in order to have information on the threshold voltage shift of the PMOS reset transistor. In this chip, baseline is not directly the value of the output CSA value but a shift through two buffers. Variation may be due to the reset transistor but also to the voltage buffers. This is the reason why we expressed on Fig 3.8 the threshold variation instead of direct value.

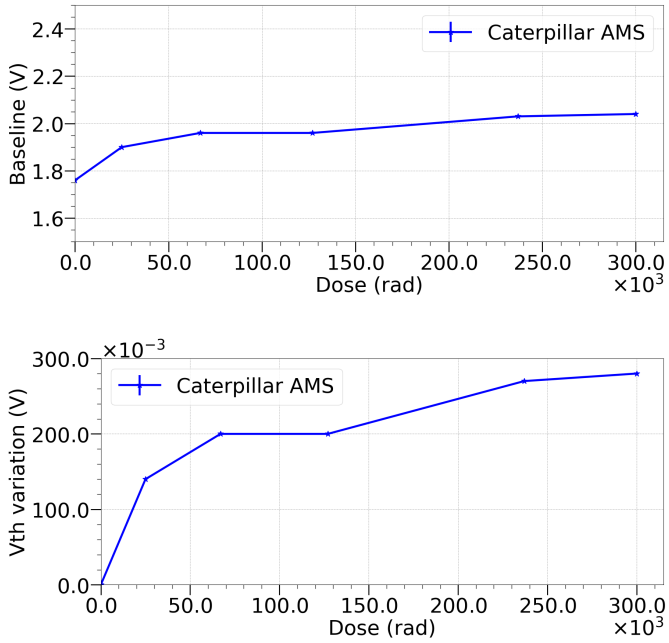

FIGURE 3.8 – *Baseline variation with total ionizing dose (top) and threshold variation extraction (bottom)*

We experience a maximum shift of 300 mV for 300 krad. This shift appears to be significantly larger than expected in the case of a 1.8 V PMOS. As explained before, this shift is mostly due to the 5V common drain amplifier used as an output buffer. Hence no useful information on the intrinsic part of the circuit can be extracted from this measurement.

Equivalent Noise Charge

We studied the variation of ENC of the pre-amplifier connected to an external shaper at different peaking times with ionizing dose. We then tried to fit each curve with leakage current variation as shown in Fig 3.9.

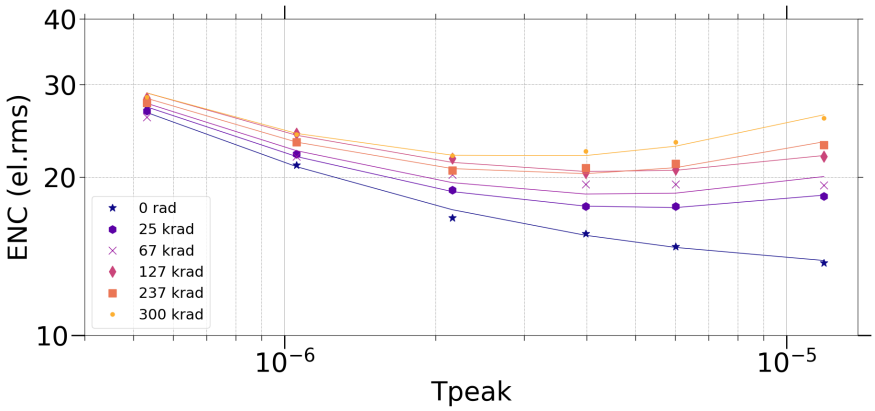

FIGURE 3.9 – *Equivalent noise charge variation with total ionizing radiations. Measurements were taken with a CR-RC^2 external shaper with variable peaking times. Point expresses the data while fitted analytical model is expressed with lines.*

We measured an increase of 86% of noise, at high peaking time in correlation with the assumption of having an increasing leakage producing parallel noise. Values vary from 13.74 el.rms to 25.6 el.rms at the highest peaking time. From the fitted parameters, pre-irradiation, leakage current is close to zero and ranges up to 2.5 pA at 300 krad. This is not in accordance with the leakage current extracted from fall time. Such difference is due to the charge injected of 2.5 fC, high enough to generate a CSA output voltage which, by increasing M_0 source voltage, increases its transconductance, hence the fall time. This non-linear effect can affect the leakage current extracted parameters, leading to extract higher leakage current than the ones that the ASIC experienced. Hence, we can stipulate that the worst-case leakage current variation is expected to be 4 pA and the nominal increase is closer to 2.5 pA.

I.3.c. Results for Caterpillar X-FAB

The same way as previously mentioned, equivalent noise charge has been measured with X-FAB 0.18 μm technology in front of an external shaper peaking time. Results are depicted in figure 3.10.

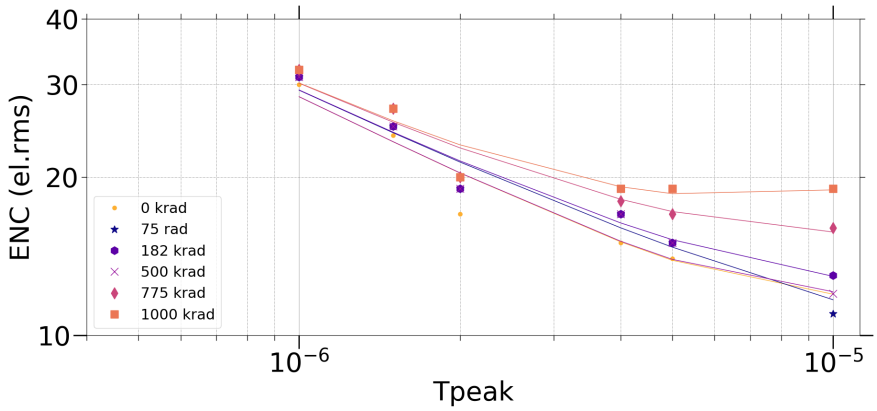

FIGURE 3.10 – *Equivalent noise charge variation with total ionizing radiations. Measurements were taken with a CR-RC^2 external shaper with variable peaking times.*

Measures show an increase in parallel noise same as with the AMS technology. At the highest peaking time, value varies from 11 el.rms up to 19 el.rms. The increase of 72% for 1 Mrad seems reasonable, since at this dose, noise will be dominated by the increase of the shot noise of the detector.

I.3.d. Comparison

We have shown two measurement sets with X-FAB 0.18μm and AMS 0.18μm CMOS technologies. Both show a reasonable behaviour after irradiation campaign. It is significant that for almost the same amount of dose for both technologies, i.e. 300 krad, AMS depicted an increase of 82% where X-FAB experienced an increase of only 20%.

However, this increase in both cases seems to be due to leakage current variation (hence shot noise) that may appear in the reset transistor as well as in compensation current transistor. The later transistor is more likely to leak with the AMS technology which has lower level of threshold voltage.

Choice on technology does not only lies in the inner parameters of transistors. We have described both technology behaviour and shown that the main differences in performances for the case of a space mission are due to the design more than the technology differences. Other parameters have to be taken into account. In our case, the price is important when aiming for a relatively large chip, as well as the location of the fabrication unit as it may be better for space missions to have a European based technology. On top of that, knowledge on interconnection to the detector is a valuable information that contributes to the choice of technology. I have detailed the main parameters that can influence the technology choice, in table 3.3.

TABLE 3.3 – *Technology choice comparison*

Parameter	XFAB	AMS
Thermal	$3.2 \cdot 10^{21} s.el^2/F^2$	$2.9 \cdot 10^{21} s.el^2/F^2$
Flicker	$6.2 \cdot 10^{25} el^2/F^2$	$3.29 \cdot 10^{26} el^2/F^2$
ENC increase at 300 krad	20%	86%
Price (MPW)	$1605€/mm^2$	$1200€/mm^2$
Low noise transistor	Yes	No
Location	Kuching (Malaysia)	Graz (Austria)
Interconnection possible	Yes	Not tested

From the mentioned arguments, I chose to work on the X-FAB 0.18 μm technology, due to the already proven interconnection (to be seen in the next part), the addition of a low flicker noise NMOS transistor in their library (I detail this point in next chapter), and the relatively good tolerance of the device to radiation damages.

II. D^2R_1: A MATRIX CONCEPT FOR DETECTOR CONNECTION

A test prototype chip has been designed in X-FAB 0.18 μm technology in order to test the interconnection and spectroscopic performances of such an assembly. A complete thesis describes this chip and can be found in [14]. The cadmium telluride detector interconnected with this ASIC has been studied and several generations of such a device has been studied in the lab and can be found in [19], [20], [21].

II.1. D^2R_1 chip description

D^2R_1 is a matrix ASIC with 16 x 16 pixels designed in the X-FAB CMOS 0.18 μm technology. Each of these pixels of 300 x 300 μm includes a full spectroscopic chain as described in Fig 3.11. The ASIC exhibits a power consumption of 81 mW (315 μW/pixel).

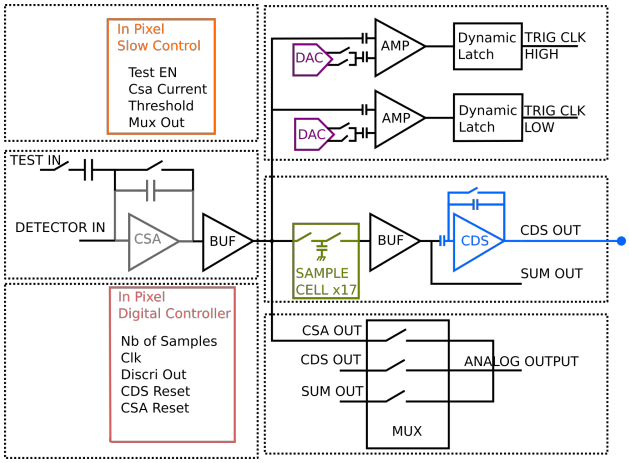

FIGURE 3.11 – *Schematic of a pixel, including a full spectroscopic chain.*

II.1.a. Pixel Description

Charge Sensitive Amplifier

A charge sensitive amplifier converts the incoming charge (ranging to 10 fC) into a readable voltage with a conversion factor corresponding to $Gain = \frac{q}{C_f} = 40\ mV/fC = 6.4\ \mu V/el$. This CSA is composed of a PMOS input folded cascode architecture amplifier, as in Caterpillar with an input transistor of size W/L = 100 μm/0.45 μm. One can tune the amount of current going through the input (M1/M2) or the output (M3/M4) (see 3.2 by an internal register programmable by the slow control link mentioned above). Contrary to the Caterpillar chips, discrete time reset (see Chapter 2 Page 44) in this ASIC is pulsed every ms, reducing "shot" noise value. In addition to that, an internal capacitance has been implemented for each CSA. This injection capacitance (of 25 fF) allows to test each pixel by Slow Control, activating the Test In signal and sending a voltage pulse on a common line.

Filter

Filtering is made by the use of a Multi Correlated Double Sampling filter (MCDS) [22] which maximizes the signal-to-noise ratio. The description of this filter expresses with its weighting function [23] is fully described in [24]. Moreover, a detailed study and comparison with previously mentioned CR-RC filters is expressed in [25].

Trigger

Each pixel has its own latched trigger. This trigger is composed of 2 interleaved Correlated Double Sampling (CDS) blocks with a dynamic latch. The signal at the CSA output is sent to a CDS block which will, during a first phase, create the baseline value. Then, during a second phase, a programmable threshold is subtracted giving a positive value if the signal is above threshold and a negative one otherwise. This value is sent to a latch that stores the information when the signal has been larger than the programmed threshold. Two blocks are controlled either by the positive and negative edge clock in order to have triggering information on both edges. This signal is then sent to an output line and column register for further treatment.

Digital Circuitry

As filtering stage has to be controlled, an internal digital circuitry unit sends the commands to the Multi CDS (MCDS) stage. It uses a continuous clock at the input and some signal coming from the triggering stage. Sampled signals are sent at the externally fixed frequency. Once a channel is fired, a counter begins to count, sampling continue and analog averaging on the k previous sampled cells is performed. Once the counter has reached k, another averaging is performed. Digital circuitry is thus always performing computation.

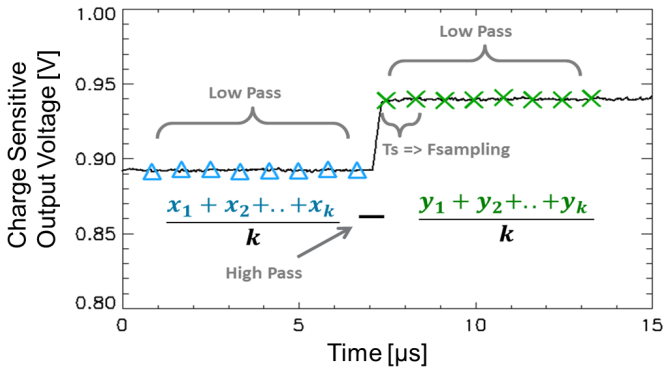

FIGURE 3.12 – *Multicorrelated double sampling implementation in D^2R_1 schematic (top) and sampling curve (bottom)*

Output

In each pixel, user can choose which signal she/he wants to look at. A multiplexing circuitry permits to read either the filtered signal (difference between first k samples and last k samples) that corresponds to CDS OUT, or the sum of each averaged signal independently on SUM OUT. It is also possible to look at each individual signals (SUM OUT) or directly to the CSA OUT signal.

II.1.b. Readout circuitry

We have seen how a pixel behaves in D^2R_1. When a pixel has detected a charge above its threshold, it triggers its line and its column. Simultaneously, an OR logic operation is performed between each column and line registers. This ends up setting a high logic level to the external pad of the ASIC each time a charge has been seen in any pixel. When the external control circuitry receives information, controller inside each pixel stops sampling the signal. This readout strategy allows a fixed dead time depending on the sampling frequency. This dead time is typically 12.5μs/event. This allows for time tagging events in the case of low flux (around 10 000 photons.s^{-1}.cm^{-2}).

II.2. Measurements without detector

The ASIC has been extensively tested without detector prior to my thesis. These values will be used and compared to the results I performed with the ASIC connected to the detector.

Without detector, each measurement has been performed using charge injection capacitance detailed in Part II.1. A set of voltages steps chosen to correctly match the ASIC input range is sent to the line VTEST which is distributed to all pixels. We then addressed pixels one by one in order to perform the different measurements.

For each pixel, an Analog to Digital Converter converts the output signal and data are analysed off-line. Results are taken for each pixel as a distribution of Gaussian like shape for each injected charge.

For each pixel, Gaussian fit has been performed. The mean value of each Gaussian gives information usable to extract the linearity and standard deviation give information about noise. We experienced some non-linearities for charges larger than 6 fC that affect noise distribution. Thus, in order to compare results with and without detector, we focused the results only on charges below 6 fC (37500 el / 165 750 eV (eq CdTe)).

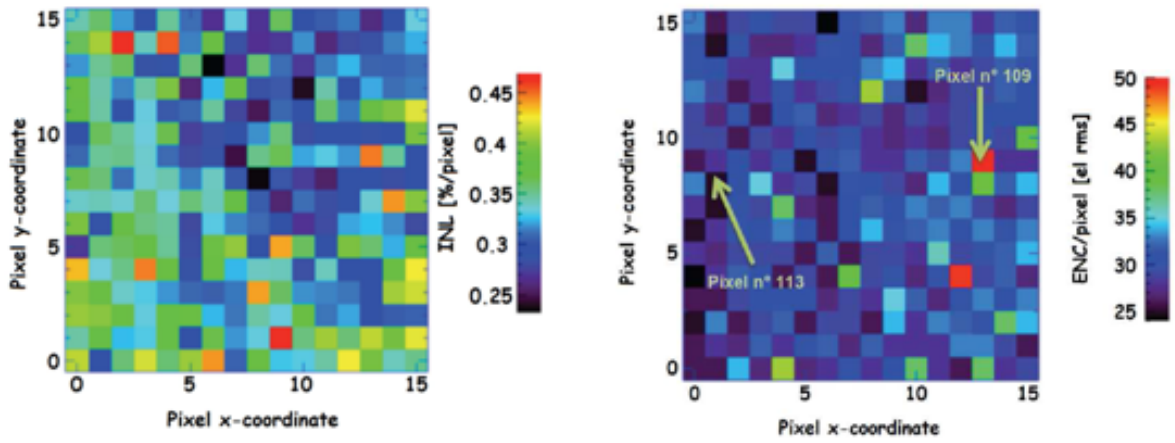

FIGURE 3.13 – *Linearity map (left) and Equivalent Noise Charge Map(right) for charges from 1 fC to 6 fC*

Fig 3.13 summarizes the results of these measurements. The maximum Integral Non-Linearity (INL) is 0.45%, and noise vary from 25 el.rms to 50 el.rms with a mean value at 29 el.rms. This is without any additional capacitance or leakage current. Considering our model for noise with charge explained in [14]:

$$\begin{aligned} ENC &= \sqrt{(C_0 + C_{det})^2.(\frac{\alpha_{th}^2}{T_{peak}} + \alpha_{1/f}^2) + \alpha_{//}^2.I_{leak}.T_{peak} + 26^2} \\ With: \quad & \alpha_{th}^2 = 4.38 \cdot 10^{21} \quad \alpha_{1/f}^2 = 7.22 \cdot 10^{25} \\ & \alpha_{//} = 0.41 \cdot 10^{19} \quad C_0 = 0.55\,pF \quad I_{leak} = 0\,fA \end{aligned} \tag{3.10}$$

We can thus estimate the noise with a detector of 0.5 pF with a 0.5 pA leakage current (that means a detector cooled down at 0^oC). We expect an ENC of 35 el.rms. This value is quite high comparing to the objective of the Caterpillar test chip, and mainly due to the mixed signal nature of the filtering. In fact, we experience an increase on the noise of 26 el.rms (squared) when using MCDS directly inside the chip. This can be due to different parasitic signals due to different clocks and digital signal close to the analog input.
To conclude on this, we expect with connection to a detector an Equivalent Noise Charge of 35 el.rms at 0^oC. This would lead to a **FWHM = 594 eV** for the 60 keV peak in a ^{241}Am source and **FWHM = 760 eV** for the 120 keV peak with a ^{57}Co source.

II.3. Detector interconnection and results

A detector has been interconnected to the D^2R_1ASIC and measurements have been performed with X-ray sources such as ^{241}Am and ^{57}Co. The detector is a 750 μm thick Shottky pixelated CdTe detector. Illuminated electrode has been chosen to be the cathode side in order to take advantage of the electron mobility, and the small pixel effect. This detector has been interconnected thanks to the JAXA/HMI indium gold stud bump bonding technology [26]. A gold stud (diameter: 25 μm and height: 200 μm) is placed on the ASIC pads and a thin layer of indium is printed on the top of the stud to improve connectivity. Then, the ASIC and the pixelated CdTe diode are pressed together with 20 g of compression with no filler in the space in between ASIC and CdTe diode allowing air to be the dielectric between pads (reducing crosstalk). Fig 3.14 shows the circuit with detector while Fig 3.15 shows the test bench used for measurement at low temperature.

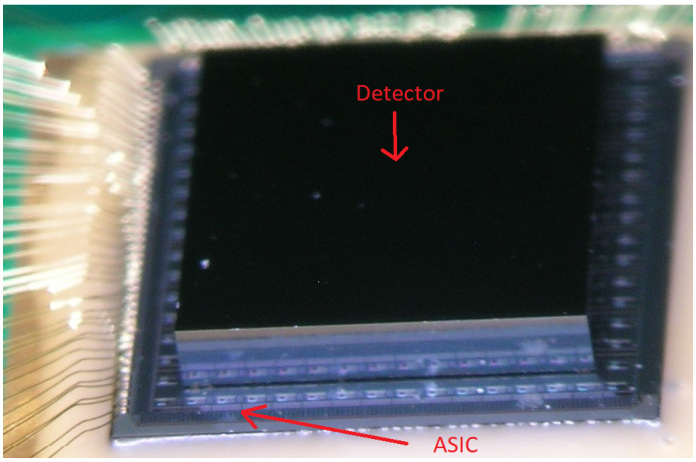

FIGURE 3.14 – *Picture of D^2R_1 ASIC (bottom) and its Schottky CdTe diode detector (top)*

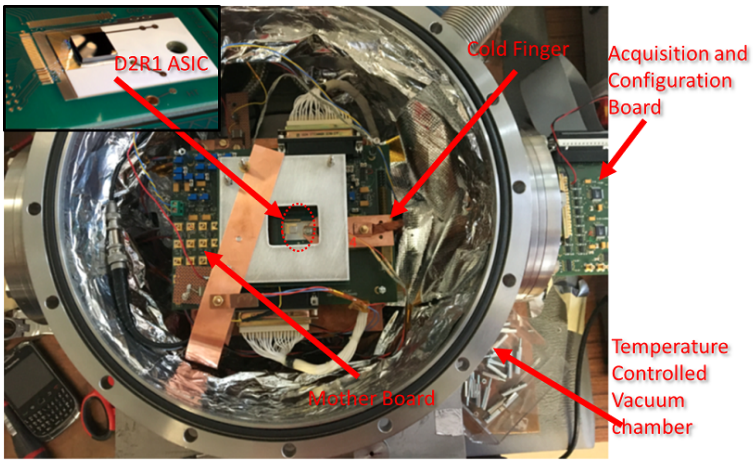

FIGURE 3.15 – *Test bench for measurement of ASIC + Detector*

The setup was configured to perform spectral analysis of radioactive source. We decided to test the ASIC with ^{241}Am and ^{57}Co corresponding to our desired energy

range. Data have been taken for 1 night (for each source) with a mean count rate of 34 cts/s. Thus having a relatively high statistics to perform gaussian fit to our spectra. Results are shown in Fig 3.16.

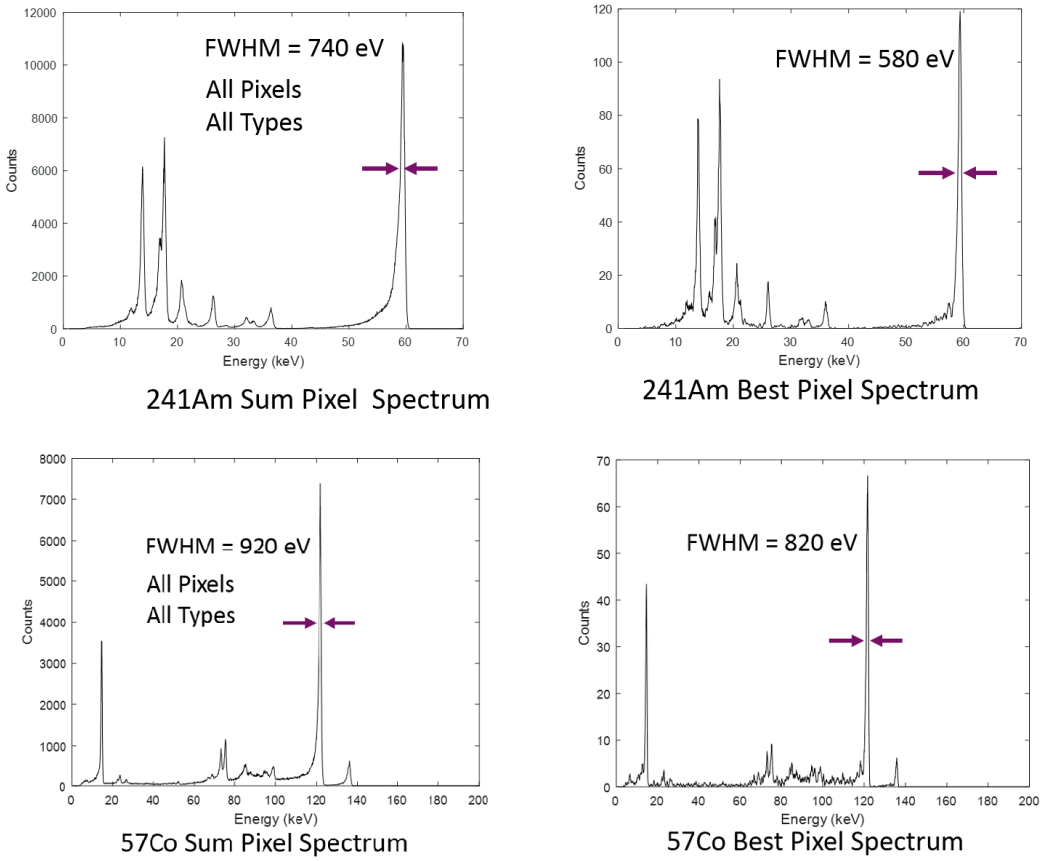

FIGURE 3.16 – *Spectrum of ^{241}Am source (top) and ^{57}Co source (bot) performed at -6°C. Left plots show the sum spectra with all types of interaction (meaning event with double events, triple or quadruple are considered) whereas right plots show the best spectrum with only one pixel and one event per trigger*

The best spectrum pixel shows an energy resolution of 580 eV FWHM at 60 keV, corresponding to the estimated value shown before. The energy resolution of the sum spectrum measured on all pixels is 740 eV FWHM, substantially higher (ENC = 55 el.rms) mainly due to the significant part of photons interacting between pixels, sharing noise together.

II.4. Conclusions

We managed to interconnect a highly dense and default free detector to the D^2R_1 integrated circuit. This enables us to test this 16 x 16 matrix of 300 μm x 300 μm pixels full spectroscopic chain. Tests are encouraging showing best results down to 580 eV at 60 keV of FWHM. We thus managed to prove the feasibility to get excellent energy resolution with an assembly of fine pitch CdTe pixelated detector and an integrated circuit fabricated in the X-FAB 0.18μm technology.

Still, without detector, the ASIC showed different performances than expected especially from the spectroscopic point of view. Added 26 el.rms of noise due to suspected pickup noise forces us rethink of the idea of a MCDS filter. This lead us to find an alternate architecture in order to consider to increase the spectral resolution of the system.

For this reason, I decided to discard the MCDS architecture and more generally architectures requiring permanent clocks for the design of my D^2R_2 chip. Thus, I decided to focus the work on the typical continuous reset architecture scheme [27] that has the advantage of being a full analogue chain with no digital circuitry involved during charge integration.

In order to evaluate the suitability and the limit of such an architecture to low noise, system, I developed an ASIC, based on an existing previous one, in the AMS 0.35 μm technology.

III. IDeF-X HDBD: Low noise ASIC with bidirectional capabilities

IDeF-X HDBD is a 32-channel charge sensitive integrated circuit based on a previous version IDeF-X HD [28]. I developed this ASIC in order to try to reduce total noise by a factor of 2 as well as allowing bidirectional input (cathode or anode readout) to make it compatible with more types of detector and especially with silicon detectors. This ASIC has been developed in the CMOS AMS 0.35 μm technology in order to take advantage of already designed bloc of the IDeF-X HD and to take advantage of the lab expertise on this technology. In addition, this design was an opportunity to familiarize myself with ultra-low noise continuous time filtering design and to develop new circuits that would be used later in the D^2R_2 chip.

III.1. Channel Description

IDeF-X HDBD is based on a continuous reset and continuous shaping self-triggered architecture [27]. Fig 3.17 shows the channel architecture. Both PMOS and NMOS based reset are depicted in the architecture. One can select the reset current to flow out of the ASIC to the detector (anode mode) or out of the detector to the ASIC (cathode mode), enabling bidirectional readout for different kinds of detector.

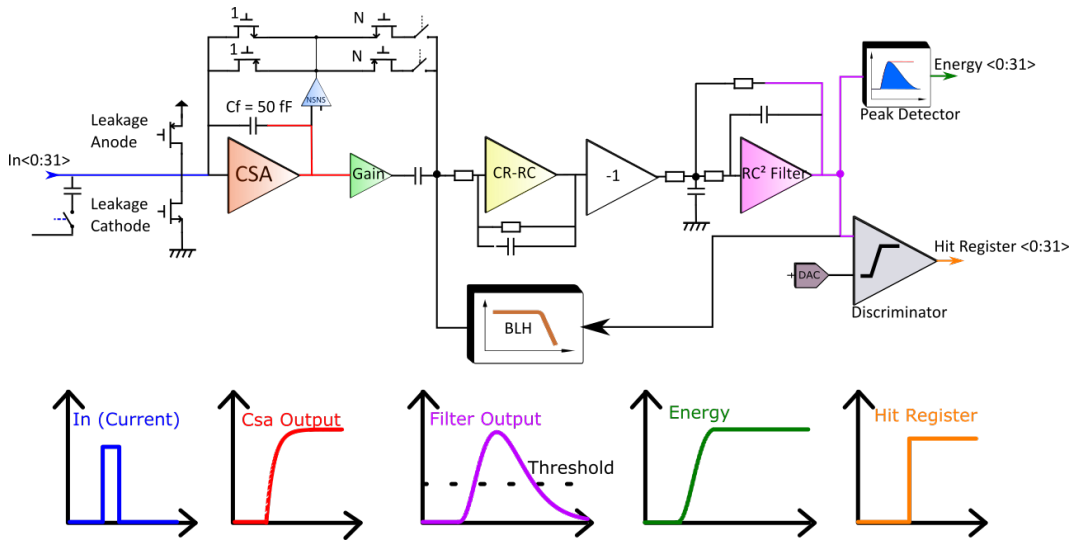

Figure 3.17 – *IDeF-X HDBD channel architecture*

In its nominal operation, the input of a channel is DC-coupled to a detector. The Charge Sensitive Amplifier (CSA) converts the incoming charge into a voltage. The CSA includes a so-called Non Stationary-Noise Suppressor (NSNS) that reduces reset noise for high charges. For test purpose, a compensating current source at the input of the CSA creates a small leakage current that is tunable between 0 pA to 100 pA and selectable for both polarities.

In order to inject calibrated charge, an injection capacitance has been integrated in each channel, linked to a common line allowing tests with a voltage step.

The CR-RC network is made by the use of N reset transistors in order to have a perfect copy of the non-linear feedback resistor of the CSA. Thus, a zero is created and

compensated by a pole made by the RC circuitry. An inverter is enabled in case of a cathode-mode signal and a second order Rauch filter allows low pass filtering.

This whole chain is fed back by a low pass filter named BLH to stabilize the baseline with respect to temperature and leakage current variations. At the end of this chain, the maximum of the shaped signal is stored in a peak detector and stretcher and multiplexed sequentially for each channel. And at the same time, the output of the shaper is compared to a programmable threshold in order to trigger the readout sequence once a charge has been detected.

I detail each of these blocs more thoroughly in the next part starting by the charge sensitive amplifier.

III.1.a. Charge Sensitive Amplifier

The charge sensitive amplifier uses a CMOS voltage amplifier as shown in Fig 3.18. This novel architecture is based on a CMOS input. The main idea of this architecture is to take benefit in the same CSA from the low flicker noise of PMOS transistor and low thermal noise of NMOS transistor. In Appendix B, I demonstrate that using two transistors instead of one increases the total transconductance without increasing the total area and the total input capacitor for both weak and strong inversion.

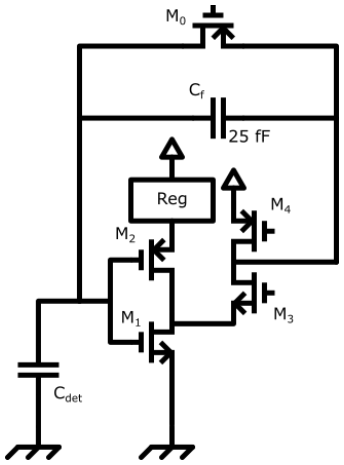

FIGURE 3.18 – *CMOS Charge Sensitive Amplifier*

Such a new architecture brings a real benefit if ultra-low noise or high speed is required. In the table below I resume the analytical conclusion of Appendix B by comparing the optimum noise for an NMOS input CSA, a PMOS and a CMOS in the strong inversion region.

TABLE 3.4 – *Comparison of three architecture (NMOS input, PMOS input, CMOS input) for AMS 0.35 µm technology with Ibias=10 µA*

ENC ratio	NMOS	PMOS	CMOS
Flicker	1.1	1	0.95
Thermal	1	1.3	0.93

Table 3.4 expresses the gain on noise for a strong inversion region. Such comparison is the worst case of such an architecture where the maximum benefit arises in weak inversion. For instance, having a NMOS input architecture with the same thermal noise than the CMOS one represents an increase of 34% on current consumption.

III.1.b. Non Stationary Noise Suppressor

As mentioned before, the equivalent noise charge can be expressed by equation 3.9. Where $\alpha_{1/f}$ and α_{th} are directly derived from the input transistor characteristics. For $\alpha_{//}$, this noise is the combination of the detector shot noise and the reset transistor thermal noise. Thus, we can express its value as:

$$\alpha_{//} = A_{//}.(2q + \frac{8q}{3n}) \tag{3.11}$$

Where $A_{//}$ is the filter coefficient and n a weak inversion coefficient

Considering this equation, M0 acts as a shot noise source. Note in this situation that the source voltage of the reset circuitry is directly the output voltage of the CSA. Thus, for high charges, high voltage swing is seen by the source of M0. As the gate voltage is set to a fix voltage, this changes the transistor bias potentially to the strong inversion region during the CSA integration. In consequence, it increases highly the transconductance. In the equation 3.11, this can be modelled as a decrease of the value "n", and so as an increase of parallel noise, dependant on the signal amplitude and finally on the particle energy.

In order to mitigate this effect, we inserted a very low pass filter "H" (with frequency down to 10's of mHz) between reset transistor and CSA output as shown in Fig 3.19.

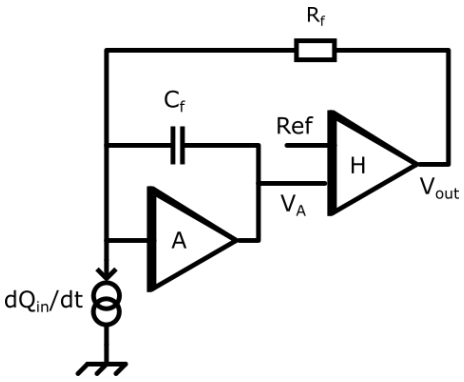

FIGURE 3.19 – *CSA with Non-Stationary Noise Suppressor feedback. The NSNS is expressed as a transfer function H. I detail the particularities of such function in Chapter 4 and can be summarized here as a low frequency low pass filter.*

Noise reduction has been measured with IDeF-X HDBD in comparison with the IDeF-X SX0 [29] that has the same CSA but no NSNS. Results can be seen on Fig 3.20.

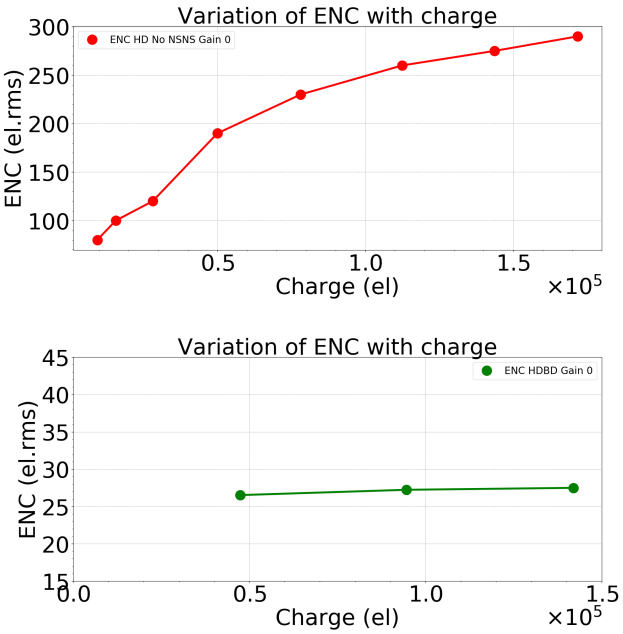

FIGURE 3.20 – *Non stationary noise variation (top: IDeF-X SX0, with no NSNS scheme, bottom: IDeF-X HDBD with NSNS scheme). Note that both noise floors are different even for small charges, due to differences in the design. Only relative variations have to be compared.*

III.1.c. Filtering Stage

In order to reduce noise, filtering CSA's output is necessary. This involves to use a bandpass filter that rejects both low and high frequencies. This filter is implemented at the CSA's output where signal can be expressed by:

$$V_{out_{csa}}(j\omega) = Q_{in}\frac{\frac{j\omega}{Hgm_0}}{1 + j\omega.\frac{C_f}{Hgm_0}} \tag{3.12}$$

Where gm_0 represents the reset transistor transconductance
And H the NSNS gain

Thus, pole on the equation 3.12 has to be rejected in order to create a proper CR-RC^n filter. In this aspect, one has to note that gm_0 and thus the dominant pole of the transfer function depends on the leakage current. In order to compensate for potentially non-linear behaviour, pole zero cancellation stage has to be perfectly matched to the reset transistor and also change with leakage current.

This problem has been solved by G. De Geronimo in [30], by using the same type of transistors to generate a zero that has the same dependence on leakage current.

Fig 3.21 describes the schematic of such a circuitry when the zero is made by N similar transistors in parallel. This pole cancellation stage differs from the literature by the addition of a resistor named "Rc". This resistor has been inserted in the design in order to create an additional pole with the advantage of using the already existing "C_c" capacitance, thus having a more compact and low power design.

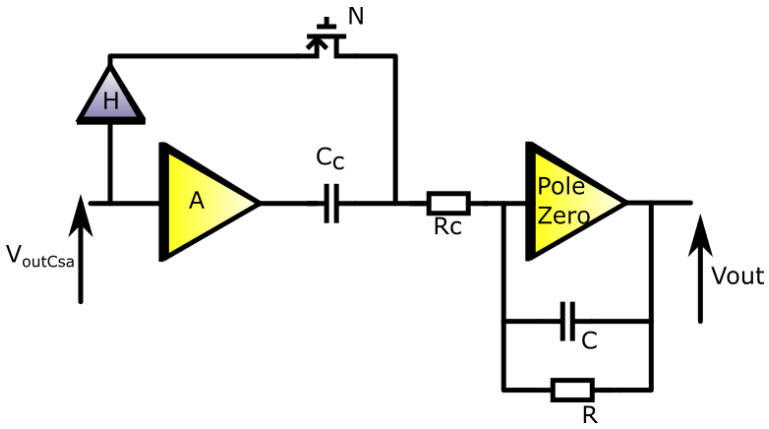

FIGURE 3.21 – *IDeF-X HDBD Pole zero cancellation stage*

The behaviour of such a circuitry can be computed, as described in equation 3.13.

$$V_{out_{pz}}(j\omega) = -R.H.gm_0.N\frac{1+j\omega.\frac{A.C_c}{N.H.gm_0}}{(1+RCj\omega)(1+gm_0R_cN+R_cC_cj\omega)}.V_{out_{Csa}}(j\omega) \tag{3.13}$$

Considering equation 3.13 and 3.12, fixing $N = \frac{A.C_c}{C_f}$ and $\tau = R.C$ we have:

$$V_{out_{pz}}(j\omega) = -\frac{A.\tau.C_c}{C_f.C}.\frac{1}{(1+\tau j\omega)(1+gm_0R_cN+R_cC_cj\omega)}Q_{in}.j\omega \tag{3.14}$$

Now depending on the additional resistor value it leads to two cases:
• Case 1: $R_c = 0$

$$\boxed{V_{out_{pz}}(j\omega) = -\frac{A.\tau.C_c}{C.C_f}.\frac{1}{(1+\tau j\omega)}Q_{in}.j\omega} \tag{3.15}$$

• Case 1: $R_c = \frac{\tau}{C_c}$ and provided the fact that: $R_c.N.gm_0 << 1$

$$\boxed{V_{out_{pz}}(j\omega) = -\frac{A.\tau.C_c}{C.C_f}.\frac{1}{(1+\tau j\omega)^2}Q_{in}.j\omega} \tag{3.16}$$

With this simple idea, the order of the pole zero cancellation stage can be increased by one without additional active device and with only a small increase in the silicon area.

After the pole zero cancellation stage, an inverter can be set up (or bypassed) in order to have positive voltage for both input signal polarities. Following the inverter, a proper second order filter with two real identical poles at $\tau = RC$ has been implemented following the Rauch architecture as shown in Fig 3.22.

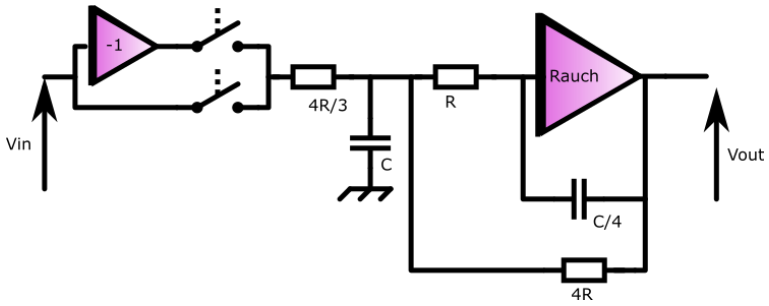

FIGURE 3.22 – *IDeF-X HDBD 2 order filter stage*

The whole circuit is equivalent to a CSA followed by a CR-RC^3 filter and is expressed in equation 3.17.

$$V_{out}(j\omega) = Q_{in}.\frac{\frac{3\tau.N}{C}j\omega}{(1+\tau j\omega)^4} \tag{3.17}$$

And the transient response to an input charge step is:

$$V_{out}(t) = \frac{Q_{in}.N}{2.C.\tau^3}t^3e^{\frac{-t}{\tau}} \tag{3.18}$$

In my design, the peaking time ($T_{peak} = 3\tau$) and the gain value (A) are tunable. As mentioned in equation 3.18, the output voltage can be expressed as a function of a capacitance C and a factor N. The N/C value is fixed for each peaking time to $6.8.10^{13}$, when the peaking time is modified (hence C), N changes as well. the factor A corresponds to the amplifier stage (see figure 3.21) equals to 1, 2, 3, or 4 depending on the slow control register. Thus the total gain of our circuit can be computed by finding the maximum value of the equation 3.18 occuring at $t = T_{peak}$ and ranges from 46 mV/fC (7.3 $\mu V/el$) to 181 mV/fC (29 $\mu V/el$).

III.1.d. Noise computation

As shown in Chapter 2, equivalent noise charge is composed of 3 contributions varying differently with peaking time (Tpeak). In the case of IDeF-X HDBD, the filter is a semi-gaussian $CR - RC^3$ filter. Filtering constant parameters for this kind of filter can be found in Table 2.1 of Chapter 2:

$$\begin{aligned} A_{th} &= 0.93 \\ A_f &= 3.32 \\ A_{//} &= 0.52 \end{aligned} \tag{3.19}$$

The equivalent noise charge can be expressed as:

$$ENC^2 = ENC_f + ENC_{th} + ENC_{para}$$

$$ENC^2 = (C_{det} + C_f + C_{CSA})^2.(A_f\alpha_{1/f}^2 + A_{th}\frac{\alpha_{th}^2}{T_{peak}}) + A_{//}\alpha_{//}^2 T_{peak} I_{leak}$$

With:

- α_{th} : The series thermal noise component (input transistor thermal noise)
- $\alpha_{1/f}$: The series flicker noise component (input transistor flicker noise)
- $\alpha_{//}$: The parallel noise component (shot noise and reset thermal noise)

(3.20)

The minimal ENC value is reached for an optimal peaking time where $ENC_{para} = ENC_{th}$. This optimum has already been calculated in chapter 2. By using equation 2.39, with the parameters extracted from measurements on IDeF-X HD shown in table 3.5 together with an estimate value of the input capacitance of IDeF-X HDBD (1.9 pF instead of 2.9 pF), we can estimate the optimal value of the noise for IDeF-X HDBD. Considering a Silicon Drift Detector with a leakage current of 500 fA and a capacitance of 100 fF (see next part), the optimal point appears at **Tpeak=10.5 μs** for an equivalent noise charge of **17.4 el.rms** as shown on Figure 3.23.

TABLE 3.5 – *Model parameters for IDeF-X HD (naked die)*

Parameter	Value	Unit
$A_{th}.\alpha_{th}^2$	$2.56.10^{20}$	$el^2.s.F^{-2}$
$A_f.\alpha_{1/f}^2$	$9.68.10^{24}$	$el^2.F^{-2}$
$A_{//}\alpha_{//}^2$	$3.2.10^{19}$	$el^2.s^{-1}.A^{-1}$
C_{csa}	$3.9.10^{-12}$	F

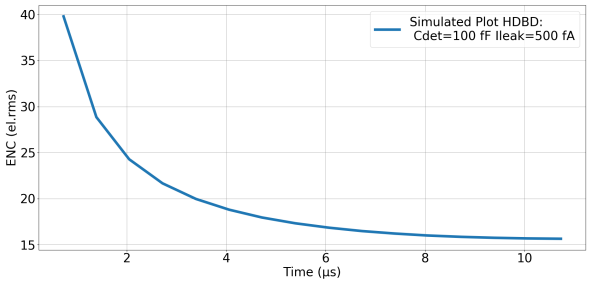

FIGURE 3.23 – *Simulation of IDeF-X HDBD Equivalent noise charge for $I_{leak} = 500fA$ and $C_{det} = 100fF$*

III.1.e. Bidirectionality

IDeF-X HDBD has been designed to perform both anode or cathode readout. We described in Chapter 1 the signal creation in the case of an anode connected to the ASIC. In this aspect, leakage and signal current are flowing out of the ASIC .

In the case of a cathode readout, signal and leakage current are flowing into the ASIC. Following our architecture depicted in Fig 3.17, a switch allows the user to select NMOS transistor network instead of PMOS network to permit leakage current to flow in the opposite direction.

In this cathode connected mode, the output voltage of the Pole Zero cancellation stage is increasing during charge integration instead of decreasing. Thus, I inserted and analogue inverter with gain close to -1 than can be switched on, allowing the following part of the system to behave the same way as with anode connected mode.

III.1.f. Discrimination Stage and low Energy threshold

In IDeF-X HDBD, the shaper is used for the energy path and for the discrimination path. Using a slow shaper for discrimination allows the ASIC to exhibit a low threshold, at the expense of a relatively large time between a particle arrival and the trigger. For each channel, a single discriminator has been implemented, as well as a 6-bits Digital to Analogue Converter (DAC).

This DAC controls the threshold value and can be addressed channel per channel in order to compensate for process variations. It is also a useful system to prevent the whole setup to be dominated by the worst pixel.

Such system allows for low threshold discrimination, which allows for low energies to trigger the circuitry.

III.1.g. Noise reduction for small capacitance

The IDeF-X HDBD is derived from IDeF-X HD. In order to optimize the chip to match small detector with small capacitances, I suppressed the protection pad at the input of the charge sensitive amplifier.

Following extraction parameters from layout design, I designed a new pad with no protection and composed only of a top metal. Thus, the capacitance of the pad itself has been reduced from 2 pF to 83 fF (according to the extraction model. Extracted using Assura).

III.1.h. Peak detection and pileup rejection

IDeF-X HDBD performs spectro-imaging. In order to have access to the spectral information, the value of the integrated charge must be measured. In order to do this, the maximum value of the shaped signal is memorized by a circuit named peak detector in each channel.

It is based on an architecture described in [31], [32]. A simplified sketch is given in Fig 3.24.

Before acquiring any charge, the hold capacitance named C_h is set to a reference level lower than the baseline of our analogue chain. This is the reset sequence. After reset, the loop is closed, the circuit amplifies the difference between the *Filter output* value and the *Peak Detector Output* value. This causes V_p to decrease and M1 to allow current to flow and charge the hold capacitance. When the voltage difference is as low as V_{th}/A_0 (where V_{th} is the PMOS threshold and A_0 the open loop gain of the amplifier), M1 starts to stop providing current to C_h and the output voltage equals the input voltage. When a charge is integrated, the same happens, as soon as $Filter\ output > Peak\ Detector\ Output$, hold capacitance is allowed to charge until $Filter\ output = Peak\ Detector\ Output$. When the shaped signal begins to decrease, $Filter\ output < Peak\ Detector\ Output$, M1 is in the cut-off region, thus no current is allowed to charge the holding capacitance. The maximum value of *Filter output* is memorized on C_h.

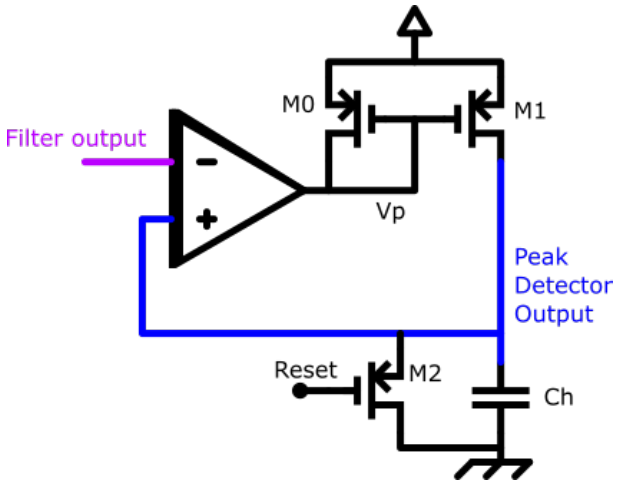

FIGURE 3.24 – *Typical Peak detector architecture*

In addition to the previous architecture, in IDeF-X HDBD, some additional blocs were integrated especially for reducing the pile-up effect. This effect occurs when two charges are close one to another. Both are integrated such as the first one cannot be uncorrelated from the second one. The measured energy corresponds to the sum of both charges.

Pile-up effects can produce very different signal shapes, depending of the time between the two charges, their values, their peaking time. I illustrate the different kinds of signal one has to treat to solve the pile-up issue in Fig 3.25.

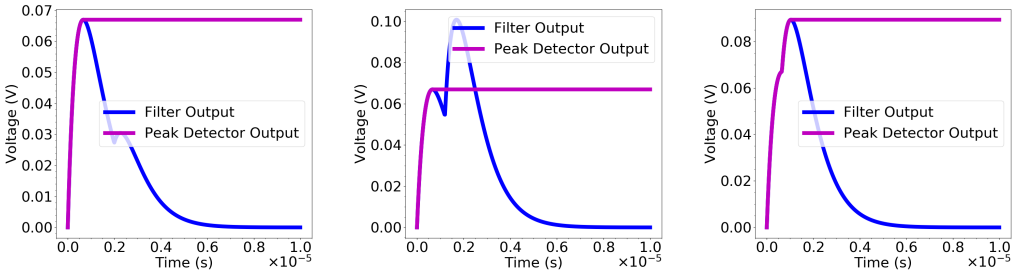

FIGURE 3.25 – *Different kinds of pileup signal. First plot shows a case when the second charge is lower than the first one and appears after the integration time. Second plot shows a case when the second charge is higher and close to the first one (it also expresses the case when the second is lower but is so close that the first one did not retrieve its baseline). The last plot shows the case in which pile-up occurs so close one to another that the difference between both charges cannot be detected.*

Fig 3.26 illustrates the solution that I implemented in the ASIC to mitigate pile-ups. One of the main constraints to perform such a mitigation was to perform this without a controlling digital circuitry during readout (in order to reduce cross talks).

The idea is to compare the Vp signal to a reference that can be changed by slow control before an acquisition. Vp signal can be seen as the derivative value of the input voltage signal. The comparator compares if the signal has detected a summit (increase of the slope, then decrease). If a summit has been detected, this information ('0' or '1')

is stored in a register for each channel, that can be read during the readout phase later. At the same time, a switch uses the output of the comparator to block M1 transistor, preventing the output signal to increase. Such strategy, easily asses case two described in Fig 3.25. The second event is lost but the first one can be recorded in the case second event appears after first charge integration, otherwise event should be discarded. Case one is assessed automatically by a standard peak detector, however, information of having two charges is lost.

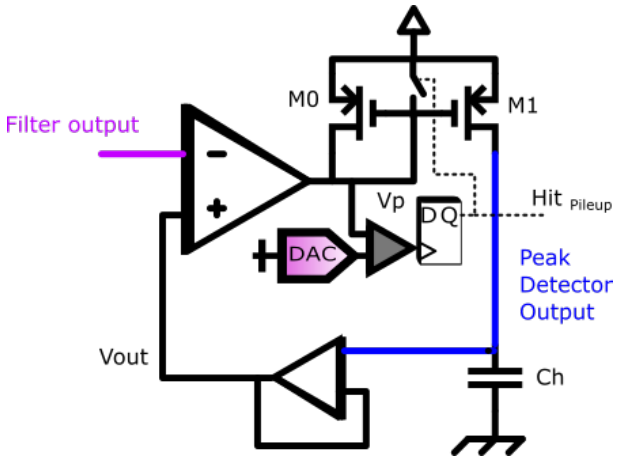

FIGURE 3.26 – *Implemented Peak detector circuitry with pile-up mitigation*

Case three is the limit case when a pile-up occurs during the increasing slope of our signal (meaning during the peaking time). In order to tackle this, I took advantages of the previous IDeF-X HD readout architecture. Once a trigger has been detected, the peak detector signal is hold externally after a time ΔT. In IDeF-X HDBD, hold signal can be both automatically internally generated or external, with priority on the external controller. By setting ΔT really close to T_{peak}, and reading the summit register, one may have information about having the correct amplitude (if summit equals to '1') or a pile-up (summit equals to '0'). Unfortunately, this assumption only works for high charges, that has a negligible time walk (time between incoming charge and trigger).

Despite suffering of such an inconvenient, the system can still be effective for relatively high energy and high flux application (such as in medical imaging applications).

Typical simulated curves in Fig 3.27 show the working principle of such circuitry along with some more dedicated performance results.

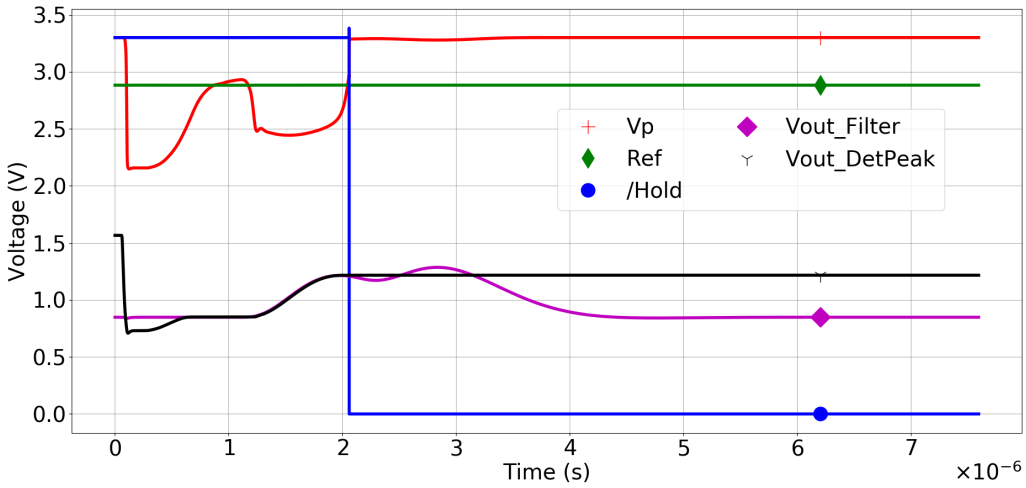

FIGURE 3.27 – *Simulated result for pile-up rejection circuitry. First curve shows typical event along with the Vp signal and automatic holding.*

III.1.i. Readout

The whole simplified structure of IDeF-X HDBD can be illustrated by Fig 3.28. When a charge appears in one or several channels, it is integrated, filtered, and compared to a fixed threshold. If the threshold has been crossed in at least one channel, a trigger signal is sent outside of the ASIC (trig signal).

On the same time, for each channel, if the threshold has been crossed, information is stored in a register named "hit register". The same way, if a summit has been detected the information is stored in another register named "summit register". In order to make the schematic understandable, I did not represented registers.

Once a trigger has been sent, the external controller waits for a fixed time with a value close to the peaking time in order to let the charge being integrated. Then, a Hold signal is sent together with a Read signal. The hold signal freezes the peak detectors of every channel, whereas read signal enables the internal digital circuitry to set-up.

Then, the 32-bits hit pattern (digital frame identifying the hit channels) is serially sent by the chip, sequenced by the input strobe signal. During these 32 strobes, one can use the "Din" signal to select the readout mode of the chip (all channels, hit only channel or programmable set).

As details are beyond the scope of this chapter, I just focus on the nominal mode where only the hit channels are read. After the hit-pattern frame has been send, each next falling edge of the strobe signal multiplexes the peak detector value of each channel one by one starting with the first hit channel. Once every channel has been multiplexed (i.e. read), the external controller sets the read and hold signal to '0' and sends a reset signal to reset the peak detector and to the hit register.

Prior to the acquisition, one can also decide by slow control, to multiplex on the shaper output signal instead of the peak detector. In the next sections reporting on the ASIC, most of the measured performances where made using the shaper output.

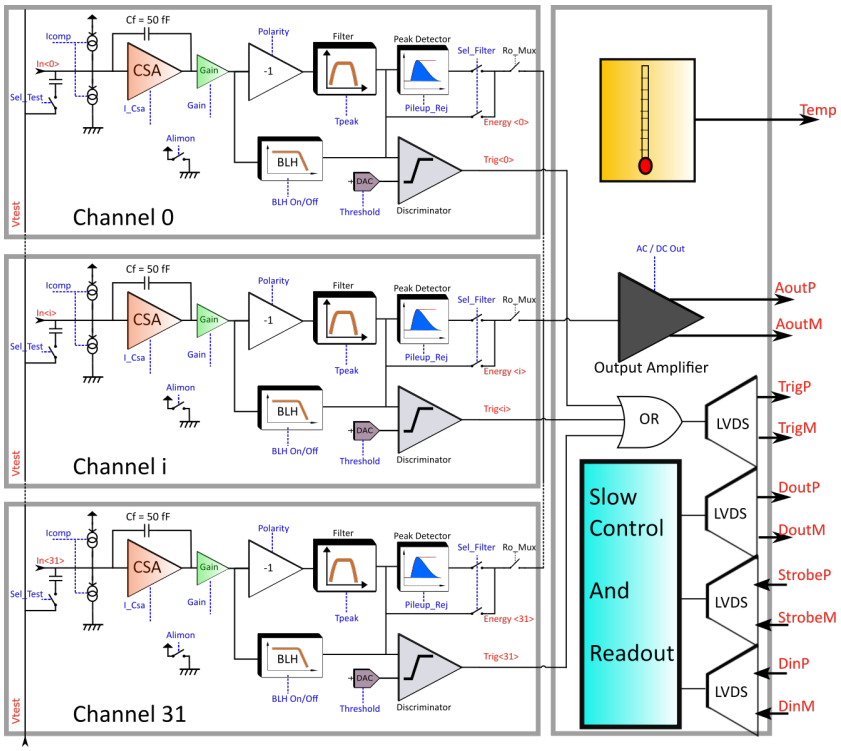

FIGURE 3.28 – *Schematic of IDeF-X HDBD*

III.2. Test Results

IDeF-X HDBD has been received on August 2018, I developed a daughter board dedicated to this ASIC and implemented the setup on a previous version of the main control board developed for IDeF-X HD. Thus, all the possible modes have not been extensively tested. For example, the pileup mode, that needed an update in the firmware, will be tested in a near future. Main following results have been performed by the use of the internal injection system and a voltage pulser. Another board has been populated with IDeF-X HDBD and linked to a Silicon Drift Detector. In this part, I detail electrical characteristics of the ASIC before describing the whole setup measurements with a radioactive source.

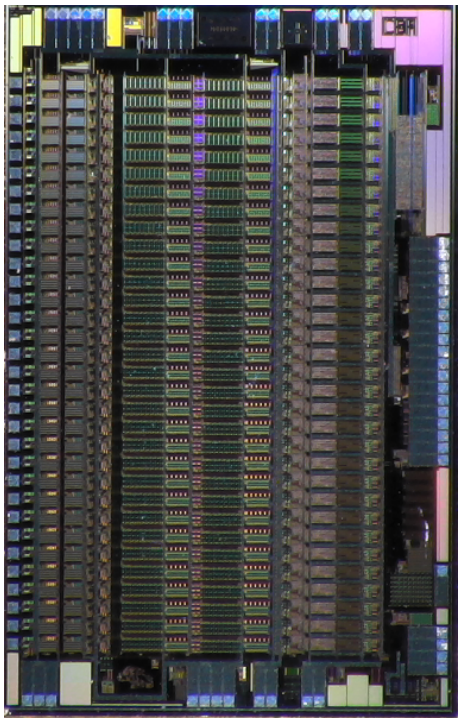

FIGURE 3.29 – *Picture of IDeF-X HDBD*

III.2.a. Electrical Tests

Tests have been performed at ambient temperature by injecting voltage steps to the ASIC. These steps were sent to the injection capacitance of each channel one by one. Each voltage step consisted of injecting a different charge in order to scan the whole ASIC input range (i.e. from - 40 fC (-250 000el) to 70 fC (460 000 el)) for two gain configurations. These inputs are shown in Fig 3.30.

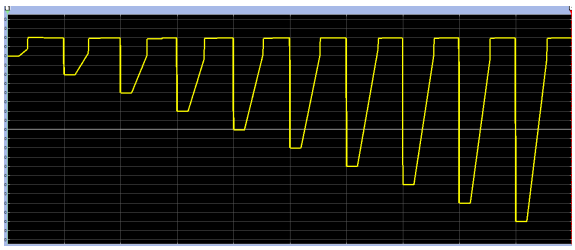

FIGURE 3.30 – *Input steps are sent to each channel individually. These steps were used to perform anode measurements, same steps with positive polarity were used for cathode measurements. The maximum voltage value corresponds to 460 000 el = -1.4 V. The very specific shape of these signals was used in order to prevent false triggers by injecting a negative charge on the circuitry.*

The rate of the injection was relatively low (around 100 Hz). For the first measurements, we used a test mode allowing the access to the shaper output of each channel (one by one) and use and external ADC (14 bits, 2.5V range) for data extraction. Such signals can be seen in Fig 3.31

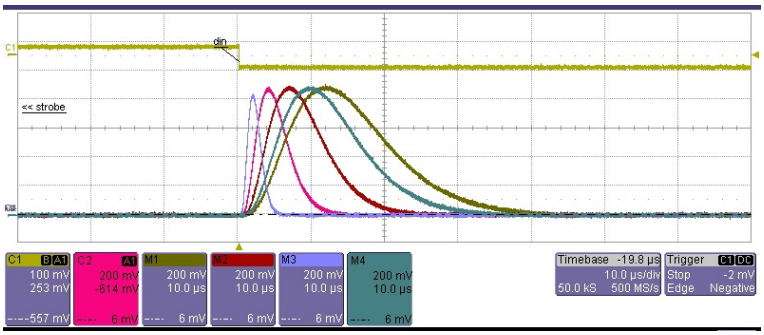

FIGURE 3.31 – *Shaper signal at the output of the ASIC for varying peaking times (from 1µs to 11µs). Yellow curve is the injection step voltage.*

Several parameters have been extracted from traces of Fig 3.31. For each input charge, 1000 events were used to perform statistical analysis.

Transfer function and non-linearity Figure 3.32 shows the measurements for one typical channel (channel number 15) to varying input voltage steps.

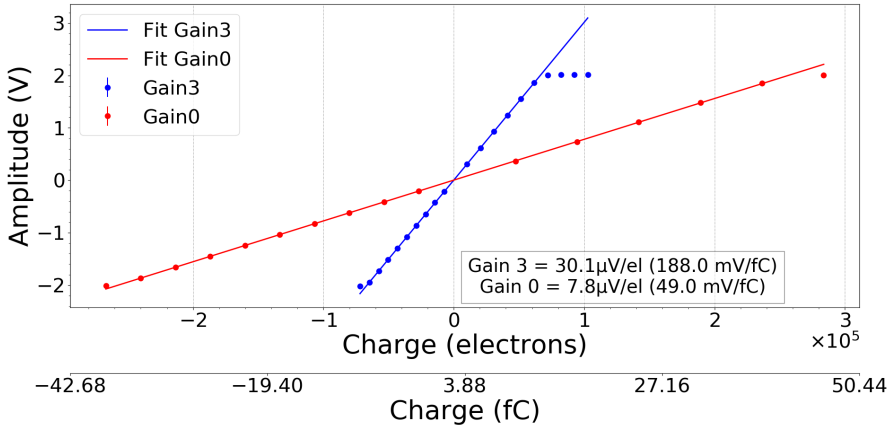

FIGURE 3.32 – *Amplitude variation for gain 0 and gain 4 in both mode anode and cathode. Data corresponds to 2 acquisitions benches, one for the cathode, the other for the anode of 10 000 samples each*

The measured gain of 49 mV/fC (Gain 0) and 188 mV/fC (Gain 3) are similar to the one expected by simulation (46 mV/fC and 181 mV/fC). The junction between anode and cathode mode without major difference in gain was expected in simulation and shows a proper design in the inverter.

The measurements also confirm that the maximum measurement ranges are respectively -40 fC to +40 fC for gain 0 and -10 fC to +10 fC for gain 3. Considering a semiconductor detector, such as CdTe, the energy range would go up to 1.2 MeV, large enough for Compton interactions spectro-imaging.

For both Cathode and Anode mode, Integral Non Linearity (INL) has been extracted separately from the amplitude measurement and is shown on Fig 3.33

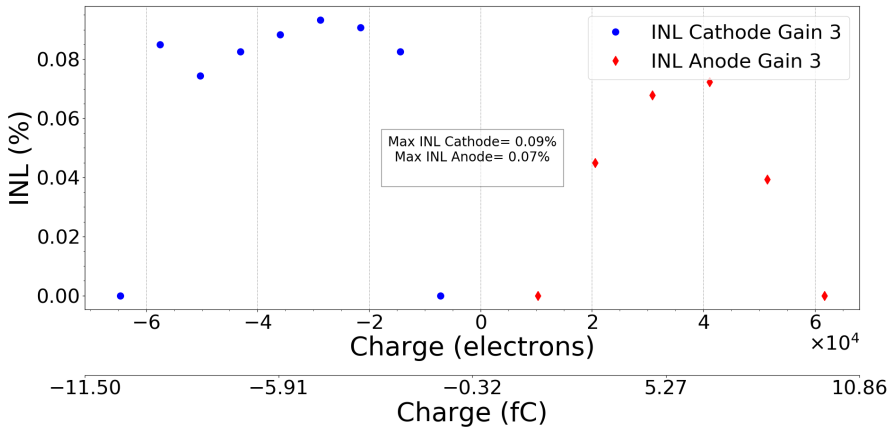

FIGURE 3.33 – *IDeF-X HDBD Integral Non Linearity. The INL is expressed as* $\frac{|Val(x)-Fit(x)|}{Range}$. *The range is the expressed range of 10 fC and the Fit is the line curve passing from the first point to the last point of the gain curve.*

Maximum INL has been found for the cathode mode with 0.09% of maximum integral non linearity. This result, slightly larger than for the anode was expected and corresponds to the addition of an inverter in the charge integration chain.

By looking at this result, performing a simple calibration with two points at a low charge and a high charge would lead to an error of less than 0.09% of the maximum range, resulting in a 56 electrons error. Such result does not take into account the peak detector which could also add non linearity. To conclude, such a result is satisfactory as small errors would be made in the case of a simple calibration. However, for precise spectroscopy over the whole spectral range, precaution has to be made on the calibration process.

Channel to channel variations have been measured for anode mode by taking the mean value of the overall channels gain and calculating their spread around this value. This measurement is expressed in Fig 3.34, resulting a mean variation of 0.2% for a maximal variation on channel 31 to 22%. Such a difference was expected as channel 31 is slightly different from other channels, allowing different test modes. Note also that channel 0 has a relatively different gain refereed to other channels. The reason lies in the fact that a large capacitance is set at its input, resulting in a variation on the closed loop gain as expressed in the Chapter 2.

Variations, channel to channel, seem reasonable but would need for a proper calibration for multichannel high spectroscopic resolution.

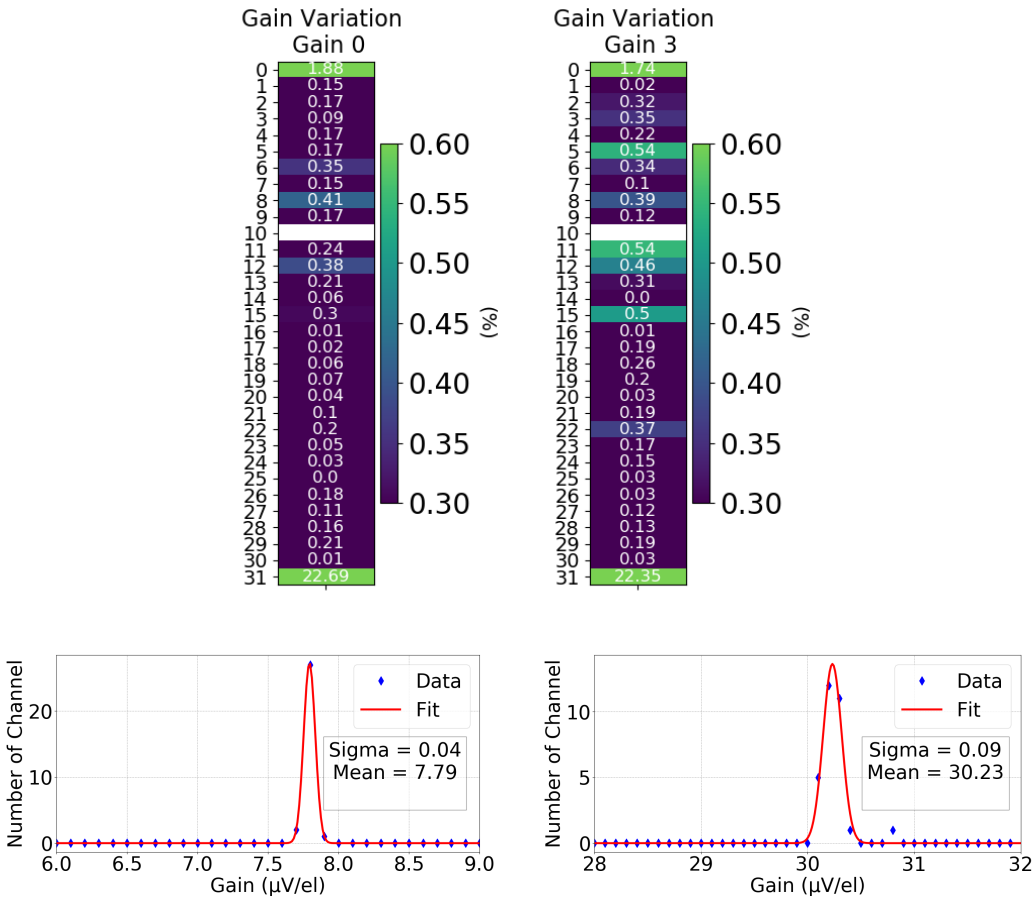

FIGURE 3.34 – *Channel to channel gain variation in anode mode. Channel 10 is broken on the tested ASIC.*

Noise Equivalent noise charge has been computed with the same set of values shown before, considering the standard deviation of the maximum value for the shaper output. These measurements have been made for every channel in anode mode.

Cathode mode has not been thoroughly tested due to leakage noise issue: By default, residual leakage current flow from CSA's input to the ground allowing for anode mode to be correctly biased but not cathode mode. To correctly bias the chip in cathode mode, one has to compensate for this residual current. The 20 pA step of compensating current circuit does not allow testing the circuit for such low noise as 20 pA adds up to 50 el.rms of parallel noise at high peaking time. However for one channel (channel number 15) tests has been performed by using an external voltage to force a small amount of current in the right direction, showing no significant difference than anode mode.

Results on floor noise for each channel are depicted in Fig 3.35. Mean value is 17.3 el.rms with a standard deviation of 1.6 el.rms. Channel 0 has a higher noise and has been taken out of the statistical extrapolation. Its noise is higher since its input is wire bonded to the board and its input capacitance is consequently much higher than the ones seen by other channels.

Compared to the theory expressed before in this chapter and the expected value of 17 el.rms, the results seem to fit clearly with the expected values. No geometrical effect is experienced, validating the proper layout of the circuitry.

Test measurements were also performed with different input capacitances and are shown on Fig 3.36 and Fig 3.37. These tests allowed us to fit the data to the ENC model expressed in equation 3.9.

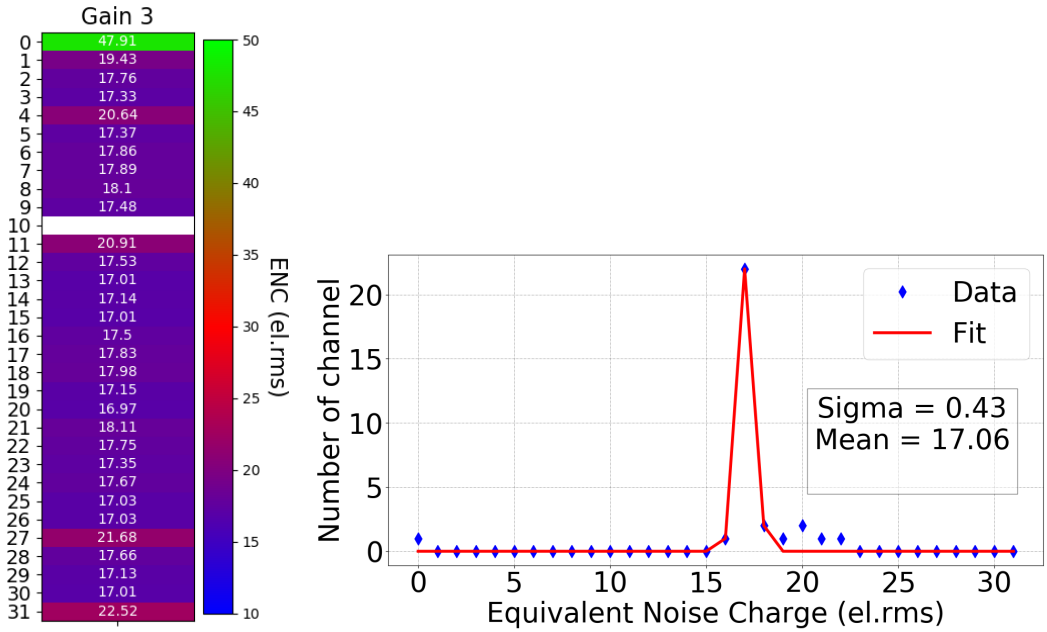

FIGURE 3.35 – *Channel equivalent noise charge floor per channel (left) and its distribution (right)*

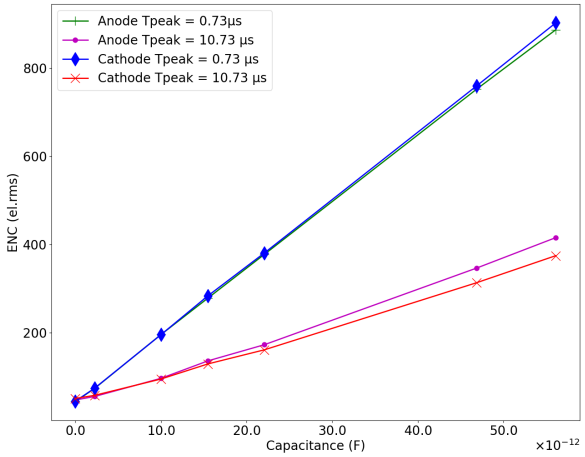

FIGURE 3.36 – *Equivalent noise charge as a function of additional capacitance with varying peaking time. Tests were performed on channel 31.*

The parameters extraction has been made considering firstly the lowest peaking time. I neglected the leakage current noise and flicker noise coefficients and started to extract the α_{th} and C_0 parameters. Then the highest peaking time measurements have been used to extract the $\alpha_{1/f}$ coefficient considering the same $\alpha_{//}$ as in IDeF-X HD (as no design modifications has been made that would modify this value). Finally, the set of value with all the peaking time expressed in Fig 3.37 has been used to refine the α_{th}, $\alpha_{1/f}$ and $\alpha_{//}$ values.

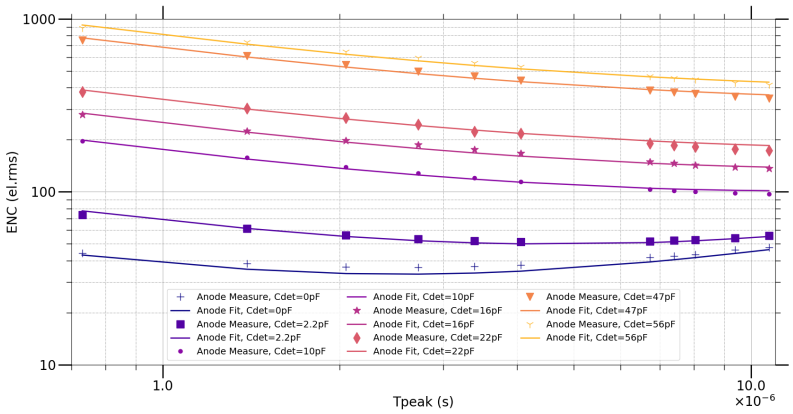

FIGURE 3.37 – *Equivalent noise charge as a function of additional capacitance with varying peaking time. Tests were performed on channel 31.*

Following the equation 3.21, the different parameters are expressed in table 3.6.

$$ENC = \sqrt{(C_f + C_{det} + C_0)^2.(\frac{\alpha_{th}^2}{T_{peak}} + \alpha_{1/f}^2) + \alpha_{//}^2 I_{leak} T_{peak}} \tag{3.21}$$

TABLE 3.6 – *Model parameters for IDeF-X HDBD considering C_0 as the CSA input capacitance and interconnection stray capacitance of wire bonding.*

Parameter	Value	Unit
α_{th}^2	$1.51.10^{20}$	$el^2.s.F^{-2}$
$\alpha_{1/f}^2$	$3.9.10^{25}$	$el^2.F^{-2}$
$\alpha_{//}^2$	$8.2.10^{18}$	$el^2.s^{-1}.A^{-1}$
C_0	$2.6.10^{-12}$	F

As I did not make any measurement with varying input leakage current, the model expressed below fit with measurement only in the case of a relatively high leakage current (20 pA used in measurements).

Discussion the ASIC has been validated through its major functionalities. However, pile up rejection circuitry has not been characterized yet. This is mainly due to test bench particularity that does not allow for the readout of summit register.

III.3. Spectroscopy results

Thanks to the INAF/INFN Roma, two of the ASIC boards have been populated with a Silicon Drift Detector as shown in Fig 3.39. A silicon drift detector is a type of semiconductor detector that allows the readout of a large area with a small anode [33] and thus a small capacitance. A drift is created between anode and cathode (as for nominal semiconductor detectors described in chapter 1) to allow the drift of electron-hole pairs. Moreover a second drift is also created on different anode rings horizontally, creating a path for electron-hole pairs to drift toward a small area collecting anode with a very small capacitance (see Fig 3.38).

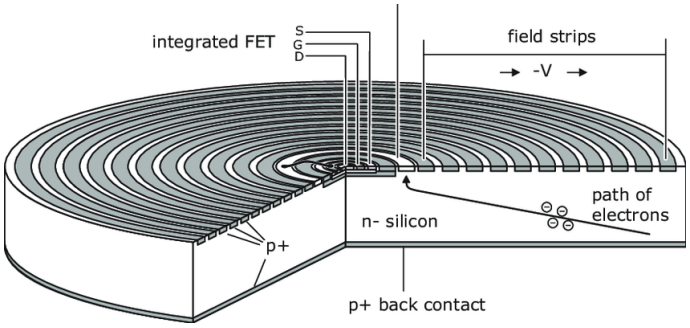

FIGURE 3.38 – *Silicon Drift Detector schematic [34]. The advantage of such architecture is also its ability to integrate directly a JFET to the sensor, thus reducing noise. In our case the SDD had no integrated JFET.*

One pixel has been wire bonded to the ASIC's input. Tests have been performed with a ^{241}Am source in order to fit with the ASIC and detector input range. Calibration and gaussian extrapolation have been performed on the 14 keV ray.

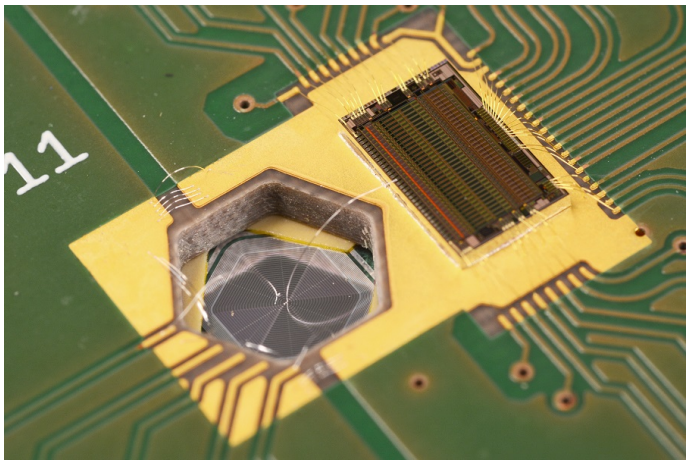

FIGURE 3.39 – *Picture of IDeF-X HDBD (right) connected to a Silicon Drift Detector (SDD) (left). The detector is composed of one 11 mm^2 pixel with 450µ thickness and is biased with 110 V.*

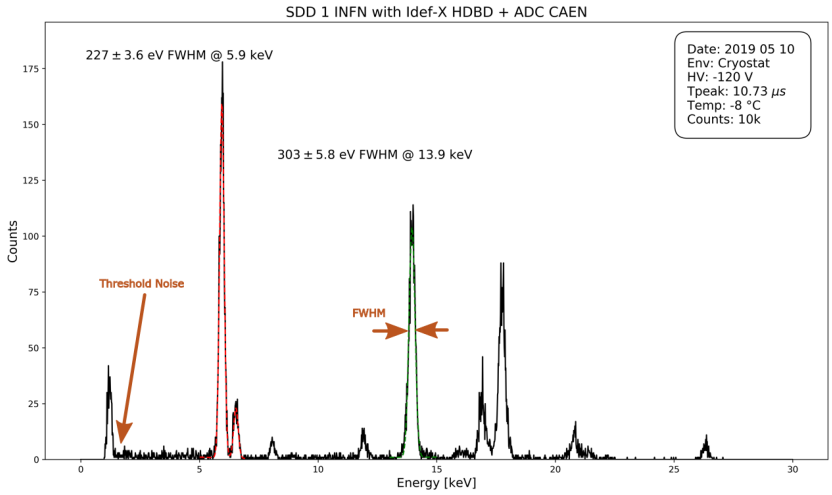

FIGURE 3.40 – *^{241}Am and ^{55}Fe superimposed source spectra on one pixel with a cool down system around (-8 ^{o}C). The red fit corresponds to the two distinguishable ^{55}Fe 5.9 and 6.4 keV K_α and K_β rays, and the green fit corresponds to the ^{241}Am 13.9 keV L_α ray.*

Results gave us a spectral resolution of 303 eV at 14 keV as shown in Fig 3.40. This, by suppressing Fano noise of the detector leads us to an equivalent noise charge of 28 el.rms. The peaking time corresponding to the minimum noise is 10.73 μs, which shows that leakage current noise is no longer dominant at -8^oC for this detector. We performed measurements for different peaking times, allowing to fit ENC with our model expressed in equation 3.21. We therefore estimate the detector to have a leakage current of 1.5 pA and the input capacitance constituted of the stray bonding capacitance and the detector capacitance of 500 fF. Such values are close to the one given by the INFN except for the input capacitance that appears larger due to the long bonding wire.

IV. Conclusion

The first part of this chapter concerning the radiation test of two technologies shows us the impact of radiations and especially total ionizing dose on the noise characteristics. For a typical space mission, TID does not reach more than 500 krad. We characterised both AMS 0.18 μm and X-FAB 0.18 μm technologies to such level of radiations. Both indicates that the major change in the circuit would be its increase of noise and of baseline, due especially to an increase in the MOS leakage current and threshold voltage. Such an assumption allows us to choose the best technology linked to the less amount of noise increase with radiation. Such a technology would be in our case the X-FAB 0.18 μm technology.

A second point then has been the test of a circuit previously developed in the X-FAB 0.18 μm technology named D^2R_1. This chip, allowed the feasibility test of the interconnection between a CdTe sensor, highly pixelated with small pixel size of 300 x 300 μm^2. The interconnection in practice has been successfully performed after mote than 1 year development thanks to the work of the Japan Aerospace eXploration Agency (JAXA) on the behalf of Takahashi san. The proof of such a highly dense interconnection and compatibility with low noise spectroscopy moved us to continue the development of a new version of such ASIC in the same technology. As mentioned in this chapter, we suspected that having high speed (MHz range) and high voltage signals (from 0 to 1.8V) in such a dense circuitry may be a source of additional noise due to charge cross talk between inputs and outputs. Thus, we decided to move to a fully analogue readout with continuous filtering.

Finally, the development and tests of the ASIC IDeF-X HDBD has demonstrated the feasibility of a really low noise ASIC with the previously mentioned fully continuous analogue shaping and part of the architecture of this chip, even if designed in a different technology, can be re-used for the design of the final chip.

Provided the assumption above, I started the development of a fully analogue shaping ASIC, with a low pitch of 250 μm in a matrix assembly and 1024 channels. This chip, and its development will be the subject of the next chapter.

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Chapter 4: D^2R_2: Design of a high spatial and spectral resolution integrated circuit

The previous chapters emphasized the development of different ASIC prototypes to read out charges at very low noise levels. I detailed the different challenges for the main performance optimizations of such a device (radiation hardening, low noise, interconnections,...).

In Chapter 1, I have shown the need of a highly segmented CdTe based detector with 250 x 250 μm^2 pixels and its corresponding readout chip, able to read charges with an accuracy better than 20 el.rms. During my thesis work, I have developed a 2-dimensional readout ASIC named *IDeF-X* D^2R_2 standing for Imaging Detector Front-end in X-rays Dimension 2 Revision 2. The circuit consists in a matrix of 32 x 32 pixels designed in the X-FAB 0.18 μm technology, optimized for the readout of a 32 x 32 CdTe pixel detector for high spatial and high spectral resolution imaging spectroscopy in space.

D^2R_2 is the successor of D^2R_1 with four times more pixels, higher spatial resolution but with a totally different architecture to fit into the tiny pixel area. The global architecture of the pixel is very similar to the channel of IDeF-X HDBD but the whole circuitry including pixels pads is compressed in the 250 x 250 μm^2 pixel area and in addition, it includes many new features developed in this chapter. As explained in the previous chapter, I chose to design the D^2R_2 ASIC in the CMOS 0.18 μm X-FAB technology essentially because we successfully proved the technology to be compatible with the hybridization process of CdTe pixel detectors by means of indium gold stud bump bonding without scarifying the spectral response.

In the following, I will detail the design and models of D^2R_2 ASIC and I will report on the performance results I obtained. So far, promising performance have been reached.

I. Introduction

First of all, let us summarize the detector and front end ASIC requirements in terms of performance, as shown in table 4.1.

The detector is a full custom 32 x 32 pixels CdTe detector. The pixelated anode is made of aluminium Schottky contacts. The pixels are surrounded with a Schottky guard ring to drive the detector side leakage current out of the pixel region. This way, the typical leakage current into the pixels will be uniform across the array and smaller than 400 fA per pixel at -20^oC. The cathode is a full surface platinum ohmic contact where the high voltage will be applied, typically -250 V for a 750 μm thick crystal. The small pixels of 250 x 250 μm^2 have a low input capacitance, smaller than 200 fF including the neighbour pixels and interconnection capacitances.

In these conditions, the charge development duration is expected to be shorter than 20 ns for electrons. Holes travel 10 times slower but are mostly screen due to the small pixel effect. The energy range should be in adequation with science requirements, being able to read ^{56}Ni gamma-ray line at 156 keV where CdTe detector with a thickness of 1 mm has 50 % of efficiency. Keeping in mind that the detector has to be Fano limited at 60 keV, the noise of the circuit must be optimized to be lower than 18 el.rms, as a goal. However, it is convenient to design the chip so that the gain can be adjusted to a larger dynamic range for applications beyond 156 keV, at the price a slightly degraded noise.

Table 4.1 – *Aimed Performances of D^2R_2*

Metric	Value	Unit
Pixel Number	1024 (32x32)	
Pixel Size	250 x 250	μm^2
Pixel Current	400	fA (at -20^oC)
Pixel Capacitance	200	fF
Energy Range High Gain Energy Range Low Gain	160 450	keV
Floor Noise High Gain Floor Noise Low Gain	12 35	el.rms
Power Consumption	2 125	mW/mm^2 $\mu W/pixel$

The ASIC has been processed in the XFAB XH018 technology with MIM / ULN / METMID process options. I received three 200 mm wafers with 280 chips for each of them. One of them has been sawed for testing. Two fully functional prototypes have been mounted on a dedicated daughter board. The latter is connected to a test bench for power, communications and control. Due to the complexity of the circuit and necessary precautions in the implementation for high density bonding and low noise operation, I designed the daughter board myself, managed the circuit bonding and prepared FPGA firmware and control software as well.

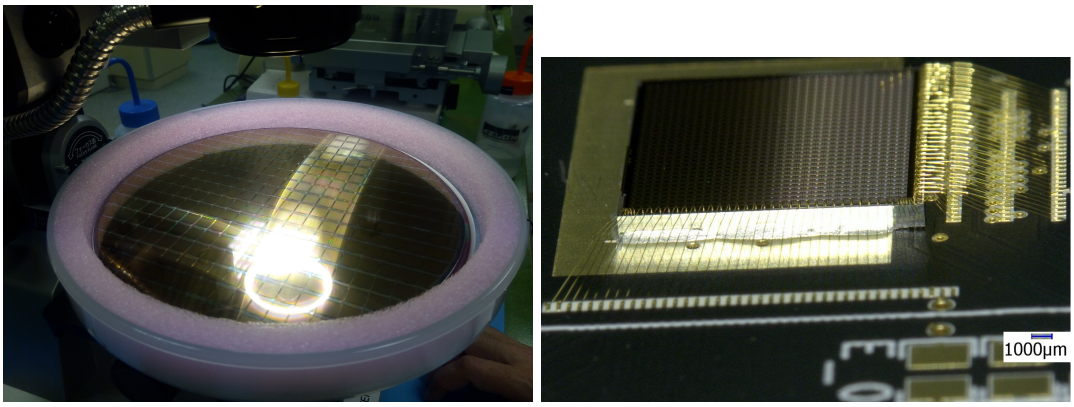

FIGURE 4.1 – *Picture of the complete D^2R_2wafer (left), and close up view of one chip bonded to its daughter board(right).*

II. GLOBAL VIEW OF ASIC AND TEST SETUP

II.1. General Architecture

The general picture of the ASIC is illustrated in the sketch below.

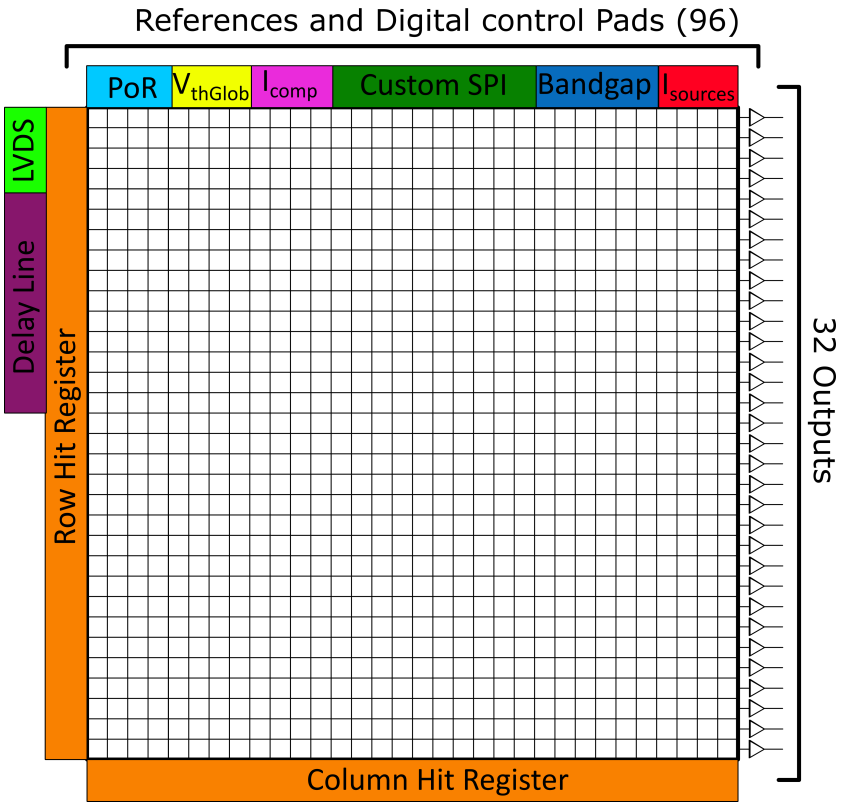

FIGURE 4.2 – *General view of the D^2R_2 matrix. Each pixel shares the same schematic depicted in Fig 4.3. Different global blocks create biases and references for the ASIC. A slow control state machine allows to digitally control several configuration registers in the ASIC. When an event occurs, D^2R_2 sends its analogue data column by column by means of 32 row buffers.*

The architecture of each individual pixel is based on a fully continuous reset system as it has been developed in the scope of this thesis for IDeF-X HDBD described in chapter 3.

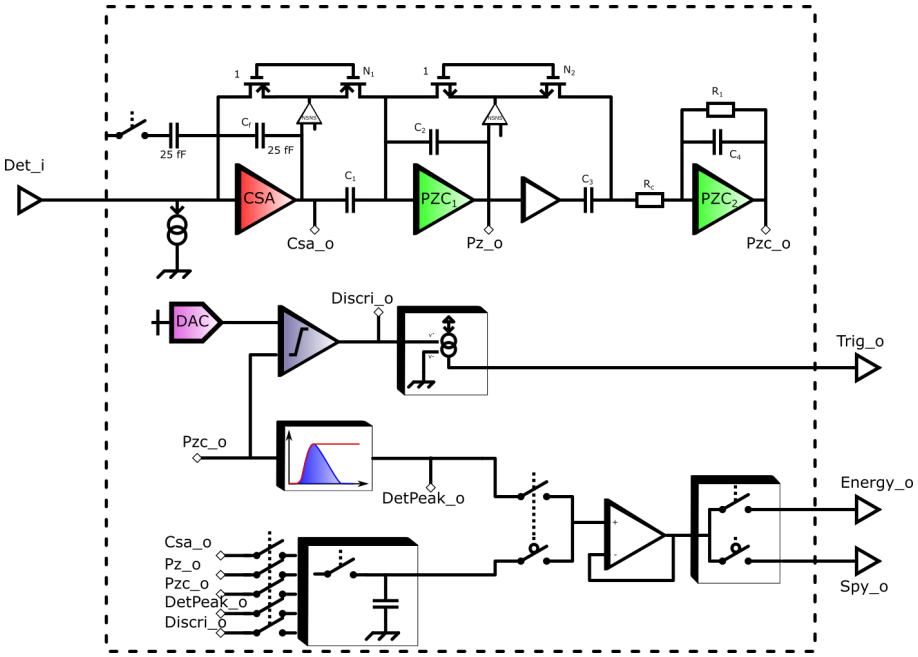

FIGURE 4.3 – *Pixel Architecture of D^2R_2 ASIC.*

A Charge Sensitive Amplifier (CSA) converts the charge into voltage. Its MOS feedback circuitry, combined with the Non-Stationary Noise Suppressor (NSNS detailed later) passively resets the circuit by acting as a high value resistor. A first stage made of a Pole Zero Cancellation (PZC) circuit is followed by a second stage and a properly designed resistor to filter the CSA signal. It acts as a first order $CR - RC$ shaper. The filtered signal is compared to a digitally controlled threshold value in order to discriminate the charge arrival (Discri). This same filtered signal is sent to a peak detector/stretcher circuitry (DetPeak) in order to memorize the maximum value of the signal. A set of multiplexors are used to read out different test points in the pixel. Finally, a sample and hold circuitry samples any data from any part of each pixel at any time for different purposes explained later in this chapter.

After an event has occurred, pixels send their triggers to row and column hit registers. The external controller (FPGA) analyse the hit register and compute the location of fired pixels in the ASIC. Analogue values for each column is multiplexed column by column to 32 output buffers connected to an external parallel ADC (OWB-1 [1]).

The pixel architecture has been kept as simple as possible to be small. Anyway, several parameters can be tuned by a digital custom SPI interface for debugging or optimization to the detector (peaking time, compensating current, power consumption,...).

II.2. Matrix readout

In the ASIC, a state machine drives the multiplexing of inputs and outputs, allowing for matrix to be read as desired. The state machine, referred here as the readout, requires an external controller with the right sequence of input signals. The readout strategy is explained below.

II.2.a. Typical Readout Scheme

Let us assume the ASIC, bump bonded to a detector. We can sum up the behaviour in three steps illustrated on Figure 4.4:

• **Step 1: Charge Integration.** Charges corresponding to the energy of photon interacting into the detector pixel is integrated. The signal passes through the whole spectroscopic channel, until it reaches the discrimination stage. Inside each pixel, when the signal is above the threshold, a digital trigger is generated (global OR over all the pixel discriminators). This signal is converted into a current to reduce spurs injection. Trigger signals are distributed into 32 rows and 32 columns registers. The combination of both registers allows to locate the pixel hit.

Note that such strategy may lead to event mis-location in case of multiple hits in coincidence. In that case, the analysis of the hit registers is insufficient to unambiguously determine which pixels have been hit: for instance, two simultaneous hits will lead to three or four possible positions. To lift the degeneration when four positions are possible, the user will have to read the energy of the four possible locations and confirm wheter the energy is above the threshold or not.

•**Step 2: hit pixel localisation.** Once a Trigger has occurred in the ASIC, a flag is sent back to the chip by external controller named "READ" to start the readout sequence of the matrix. At this time, the hit registers are frozen as well as the peak detectors. 32 strobes have to be sent in order to read on two pads both the column and hit registers. At the end of these 32 strobes, analogue signal can be read out.

•**Step 3: Signal digitization.** At the end of step 2, each following strobe multiplexes the energy signal to the outputs. One strobe multiplexes one column and 32 lines at the same time. It is possible in the state machine to configure the multiplexing in three different ways.

The whole matrix can be read whatever the number of hit pixels. In this case, multiplexing takes 32 strobes.

Otherwise, only a given list of columns can be read. In this case, a mask is sent to choose which columns have to be read and then multiplexing starts.

A last way is to read only the hit columns. This is the nominal readout mode. The controller knows the number of hit column, hence the number of strobes to send.

At the end, the read signal is set to 0 by the external controller, the pixels are reset and step 1 can start again.

A typical readout frame is expressed in the figure 4.4.

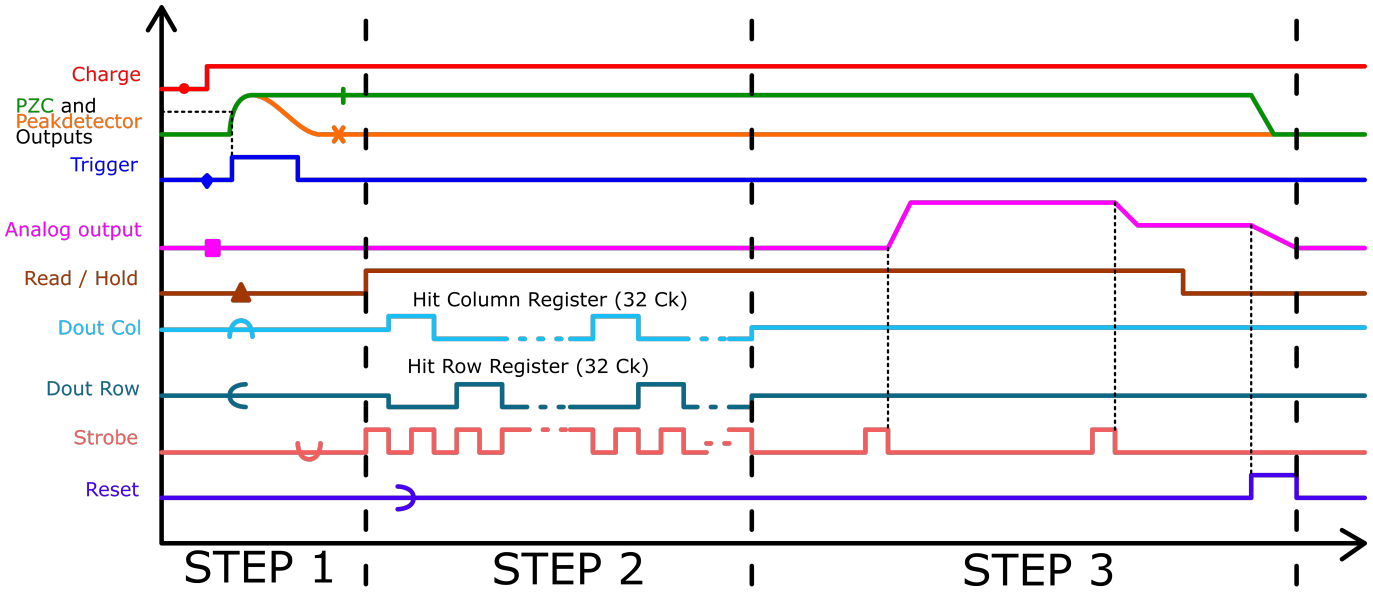

FIGURE 4.4 – *Typical readout frame in nominal mode. Here two pixels have been hit: Pixel (31,30) and (1,0).*

II.2.b. SPY mode

In order to debug the circuitry, a SPY mode has been implemented. SPY mode is controlled by a custom SPI interface and is pixel addressable. It consists in a common signal line between every pixel. By setting up the SPY register on a desired pixel, the signal is buffered in pixel and sorted out through the common SPY line out of the ASIC.

Inside each pixel, another register named "Mode" allows to select the desired signal to be observed through SPY mode. The principle of in pixel multiplexing through SPY mode is expressed on the figure 4.5. The "Debug" or "Engineering mode" has been extensively used and does not require any sophisticated readout implementation in the controller.

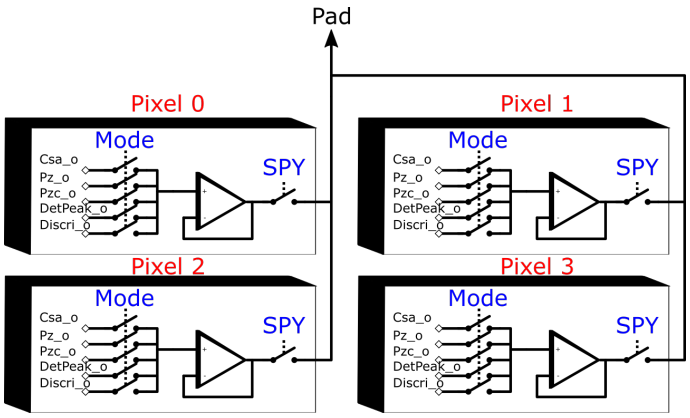

FIGURE 4.5 – *Schematic of SPY mode functionality with four pixels.*

II.2.c. System integration and OWB-1

The IDeF-X D^2R_2 architecture is designed to match the interface of a 32 parallel channel ADC named OWB-1 [1] previously designed in our lab. This low power ADC can digitize simultaneously 32 channels by the use of a Wilkinson architecture. A ramp is created and compared to the signal for each channel. For each channel, the measurement of the time between the start of the ramp and its crossing with the value to convert using a DLL-based TDC allows the parallel digitization of the 32 channels of 13 bits (2V swing) in less than 3 μs.

To match the range of OWB-1, IDeF-X D^2R_2 integrates a 3.3V output buffer with gain 2. The pad ring of D^2R_2 has been designed to allow direct bonding to OWB-1 inputs.

Finally, OWB-1 allows for zero suppression by the use of a mask signal send before acquisition. Linking the row hit register signal from D^2R_2 to OWB-1 allows for sending the information just before sampling. If the photon interaction leads to a pattern of 4 x 4 pixel hit, 2 rows needs to be read and 2 column, meaning 64 x 13 bits = 832 bits would be read without zero suppression. With zero suppression, only 4 x 13 bits = 52 bits area read out, compressing data by a factor 16.

II.2.d. Readout Speed and Dead time consideration

Readout time is known in such architecture but dependant on the hit geometry. It can be expressed as:

$$\begin{aligned} T_{readout} &= T_{WaitDelay} + T_{HitReg} + T_{Sample} \\ T_{readout} &= 2T_{peak} + \frac{32}{F_{readout}} + Nb_{Hit_{Column}} \cdot 2.86\mu s \end{aligned} \tag{4.1}$$

2.86 μs corresponds to the sampling time of OWB-1 with 13 bits accuracy.

Considering a peaking time of 144 ns, a typical readout frequency of 10 MHz, the whole matrix is read out in 95 μs. It also corresponds to the deadtime of the chip in this mode. The absolute maximum readout rate is approximately 10 000 frames/s in this case. Assuming all pixels to be hit simultaneously, this means 10 million events/s.

Conversely, in the nominal readout mode, a single event is read out in 6.3 μs while a split event shared in a 2 x 2 hit pattern is read out in 9.2 μs. The corresponding absolute maximum rates are ˜159 kHz for singles and ˜109 kHz for split events respectively.

Typical rates in hard X-ray astronomy are closer to 1-100 event/s in the point spread function of a mirror. Assuming the optimal peaking time to be 3 μs for high resolution, and a bright source with a rate of a 100 counts/s, 50% single and 50% double, triple or quadruple events, the average dead time would be ˜10 μs per hit. Consequently, the fraction of deadtime of the circuit would be essentially negligible, in the range of 1‰.

II.3. General discussion and Special modes

II.3.a. Power Consumption

Power consumption is an important constraint for space missions, not only for power supply but also for heat management keeping in mind that the CdTe detectors are stable and low current below 0^oC. In the beginning of this chapter, I mentioned a targeted power consumption of 2 mW/mm^2. The table below shows the repartition of this power consumption between the blocks:

TABLE 4.2 – *D2R2 Power Consumption*

Bloc	Power supply	Power Consumption (for all channel)
LVDS drivers	3.3V	13.6 mW
Output buffers	3.3V	16 mW
Spy buffer	3.3V	5.4 mW
Readout	1.8V Digital	2.35 mW (no readout)
Delay Line	1.8V Digital	7.8 mW
Bandgap	1.8V Analog	450 μW
References	1.8V Analog	270 μW
Pixel analog chain	1.8V Analog	154 mW
Total	Both	200 mW
Total Per pixel	Both	200 μW
Total Per Active Area	Both	3 mW/mm^2

In my design, I ended with a power consumption 50% larger than specified. This is mostly due to in pixel consumption, where pole zero and CSA contribute largely to the power consumption. Nevertheless, paying the price of a higher thermal noise, it is possible to decrease the total power consumption by a factor two in the pole zero and CSA blocks. Such reduction leads to a total power consumption per area of 2.2 mW/mm^2 close to initial expectations.

II.3.b. Radiation Hardening

The radiation hardened necessity has been detailed in chapter 1. Technological characterization has been done and explained in chapter 2. My ASIC has not been tested yet for both single event latchups/upset and dose. However several mitigation techniques have been used to anticipate radiation hardness.

The digital circuitry controlling the custom SPI (slow control) has been duplicated. Registers are separated in the layout by a minimum distance of 11 μm to prevent two registers to suffer from a single event upset at the same time. A signal compares each duplicated register. In case of a difference, a signal is sent out of the ASIC and the controller will automatically reconfigure the slow control.

Readout is not duplicated as a SEU could only cause the state machine to give false information on hit pixel address, that can be corrected by reading the energy.

Every analogue part of the system has a substrate connection between PMOS and NMOS to avoid any latchup. However, it is not the case for digital part that can be at risk and needs to be tested with heavy particles before optimization.

Finally, the dose behaviour is expected to be similar to the Caterpillar chip, as its architecture is quite similar. This will have to be tested and qualified later.

II.3.c. Global References

The ASIC has 135 pads for I/O's in addition to the 1024 pixel pads. Except for the 32 outputs pads and 4 others, all pads are on the same side of the chip. They provide current and voltage references, as well as readout signals, slow control signals, and power supplies.

A bandgap and current mirrors have been designed to provide the proper references to the circuit.

II.4. Test Setup

The ASIC has been tested using 3 mezzanine PCB boards illustrated on figure 4.6.

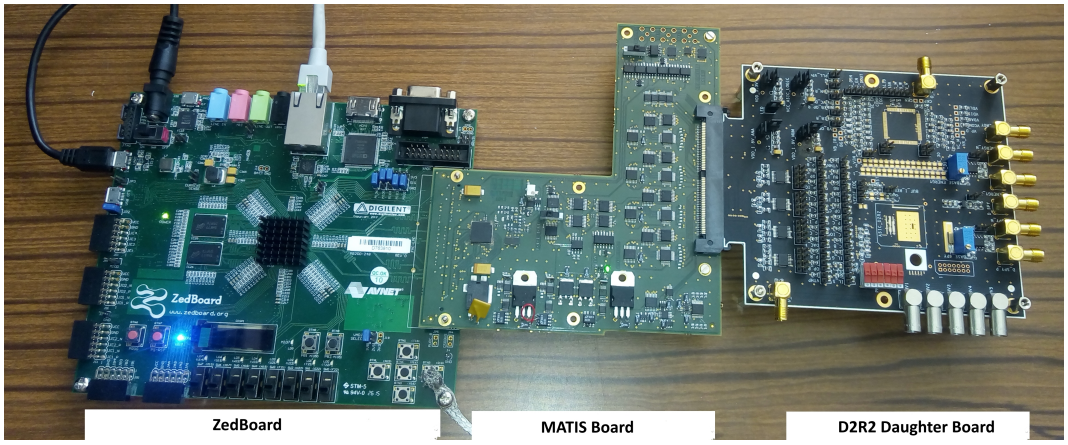

FIGURE 4.6 – *Picture of Test Setup*

The rightmost board on figure 4.6 is the ASIC D^2R_2 **Daughter board** that houses the naked ASIC with 135 gold bonding wires. This board also hosts components such as the OWB-1 parallel ADC [1], voltage and current references, and low noise voltage regulators.

The second custom board in the middle of figure 4.6 is named **MATIS**. It is a multi-purpose mother board for chip interface. It contains digitally controlled references, charge injection circuitry, voltage regulators, CMOS to LVDS, LVDS to CMOS converters, and power supplies.

Finally, the leftmost board in figure 4.6 is the controller. It is a **ZedBoard** system (equipped with a zynq 7002 FPGA) embedding a Petalinux operating system and custom IPs. The firmware handles the digital signals for I2C control or custom slow control SPI used inside the ASIC.

At this stage of development, the readout state machine for D^2R_2 ASIC has not yet been implemented and no high speed readout has been performed yet not crosstalks evaluations. A deeper study will be performed in the future and will not be described here. I focused my evaluations on the pixel behaviour and performance in a "spy mode".

Prior to tests, ASIC registers are programmed with corresponding values. Charge is sent by the means of an on-chip injection capacitance (on for each pixel). The voltage is delivered to the injection capacitor by MATIS or by an arbitrary waveform generator. I have developed a graphical user interface to user control injections values and setup the ASIC registers. A snapshot view of the software is illustrated in figure 4.7.

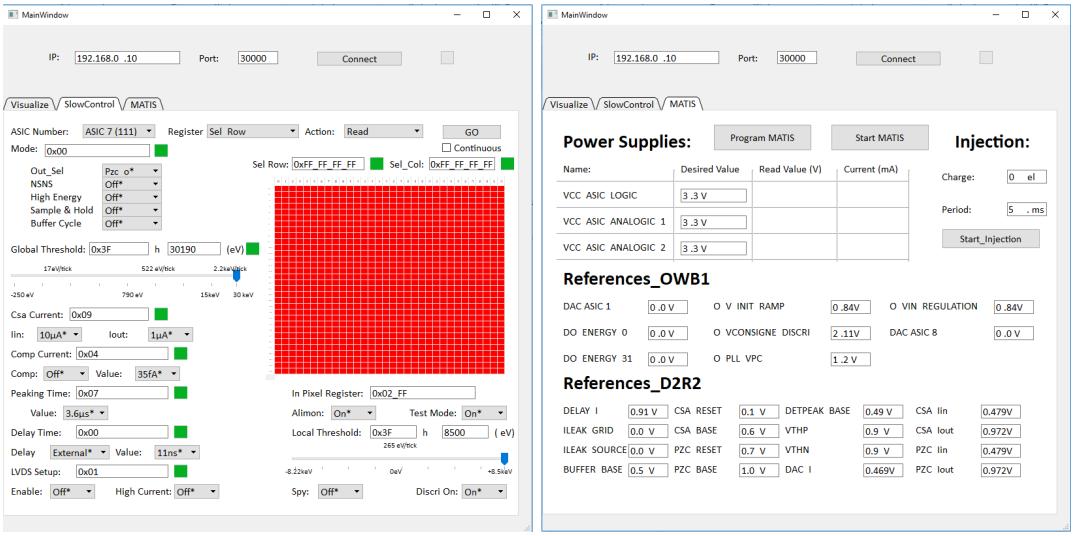

FIGURE 4.7 – *Graphical user interface for controlling MATIS I2C accessible components (right) and ASIC slow control registers (left)*

Tests have been performed using the Spy mode of the ASIC. Data is digitized by an external ADC module CAEN DT5724 and metrics are extracted off-line with dedicated scripts.

III. Charge Sensitive Amplifier

III.1. CSA Design

III.1.a. Architecture

The architecture of the Charge Sensitive Amplifier used in D^2R_2 is depicted in Figure 4.8. It is composed of a NMOS input folded cascode voltage amplifier fedback with a 25 fF capacitance and a PMOS transistor in parallel.

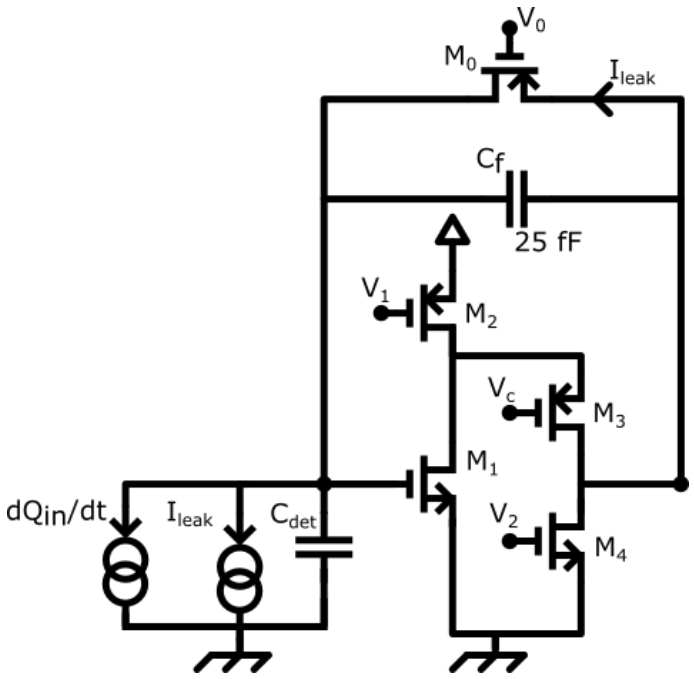

Figure 4.8 – *Nmos folded Cascode Charge Sensitive Amplifier with MOS reset circuitry*

Considering $A_0.C_f >> C_{in}$ the output voltage of the CSA response can be expressed as the composition of equations 2.5 and 2.8:

$$V_{out_{Csa}}(t) = \frac{Q_{in}}{C_f}.[1 - \exp(\frac{-C_f.A_0.t}{\tau.(C_{in} + C_f)})]exp(\frac{-qI_{leak}t}{C_f nkT}) \tag{4.2}$$

With:
- τ the amplifier time constant
- A_0 its open loop gain
- C_{in} the input capacitor composed of M1 gate capacitance, parasitic capacitance of interconnection and detector capacitance.
- I_{leak} the leakage current

I have made the choice not to use the CMOS architecture depicted in Chapter 3 developed in IDeF-X HDBD. The first reason is the need for a power supply dedicated to the CSA with an integrated voltage regulator that would need to provide the current for all the matrix without distortion. The second reason was the availability of a new low flicker noise NMOS transistor (nelna in XFAB 0.18μm) that allows in simulations to improve dramatically the noise performances to make it similar to the one of the CMOS architecture.

III.2. FeedBack

III.2.a. Capacitance

Choice of the feedback capacitance relies in a trade-off between, **closed loop gain, matching, and input dynamic range**.

• **Closed loop Gain:** The smaller C_f is, the larger is the closed loop gain, hence the easier it is to reach low noise because the second stage relative contributions to the noise are lower. However, with a given open loop gain, C_f must be large enough to neglect C_{in} compared to $A_0.C_f$.
• **Missmatch**[1]**:** Smaller capacitance means higher variation between capacitances which would lead to gain variation from channel to channel and chip to chip as well as non-proper pole zero cancellation stage.
• **Input dynamic range:** In the case of D^2R_2 a minimum energy range of 160 keV with CdTe is required (meaning 36 000 electrons at least). According to the folded cascode design, maximum output swing is expressed as $Vdd - 3.V_{sat}$ which is in my case around 750 mV. Thus, if I assume to have the entire gain in the first stage, a gain of 21 $\mu V/el$ is required, which is equivalent to a feedback capacitance of 8 fF.

As a response, I chose a 25 fF feedback capacitance. With such a design, and according to simulation models, I performed missmatchs only montecarlo analysis resulting in a CSA gain expected to be 6.4 $\mu V/el$ with a standard deviation of 4 nV/el.

• **Measurements:** For pixel (0,31) the charge to voltage gain of charge sensitive amplifier has been measured to be 6.3 $\mu V/el$ close to the expected value. Spread between channel has not been measured yet.

III.2.b. Reset MOS transistor

Each pixel of the ASIC is DC connected to each anode of the detector. Thus, the ASIC delivers the leakage current to the detector. After a charge integration, CSA output voltage falls and recovers its baseline. The CSA is reset.

In order to reset without adding too much noise, I have introduced on Chapter 2 the choice of a MOS transistor biased in the subthreshold region acting as a high value non-linear resistor. To feed the detector with leakage current, I used a PMOS with its source to the output of the CSA, its drain at the CSA's input while its gate is externally biased (see M_0 figure 4.8).

When no charge is integrated, transistor acts as a high value resistor which can be approximated by $R = \frac{1}{gm} = \frac{nkT}{qI_{leak}}$.

After filtering, such reset circuit adds a noise that is proportional to the transistor transconductance. Hence, a low value of the transconductance is needed, leading to use the transistor in its strong inversion region.

1. With 8 fF capacitance, standard deviation variation of capacitive matching is around 0.17 % which is relatively large and could lead to non proper pole zero cancellation. A non proper pole zero cancellation leads the system to have a gain varying with leakage current, not suitable for high spectroscopic measurements. The spread I decided to accept was 0.01 % leading in 25 fF capacitance

With leakage currents lower than 1 pA, having the reset transistor working in strong inversion region would require such a large length to width ratio that it could not be implemented in a small area. Nevertheless, I chose a ratio L/W large enough (12.5 see table 4.3) not to dive too deeply into the weak inversion region. On the other hand, I chose width of the transistor large enough to avoid mismatches for pole zero cancellation stage and to provide high value equivalent output resistance.

III.3. Noise Optimization

In chapters 2 and 3, I have expressed the equivalent noise charge at the filter output.

$$ENC^2 = A_{th}\frac{\alpha_{th}^2(C_f + C_{in})^2}{T_{peak}} + A_f\alpha_{1/f}^2(C_f + C_{in})^2 + A_pT_{peak}\alpha_{//}^2 \tag{4.3}$$

This equation is highly linked with the CSA design parameters as its input capacitance and transconductance are both factor of noise. The CSA design can be optimized to minimize ENC for a given use. This optimization process is expressed in Appendix A. It gives the different values for a CSA input transistor when the noise is optimized for thermal noise ($C_{Csa} = \frac{1}{3}C_{det}$) or for flicker noise ($C_{Csa} = C_{det}$) in the strong inversion region. In my case X-FAB provides a low flicker noise NMOS transistor so that I decided to optimize the transistor with regards to the thermal noise.

In order to find the appropriate value, I developed a multidimensional optimization using simulations with a 10 μA bias current. These results are shown in the figure 4.9

The optimization results in an optimal peaking time of 3 μs and input transistor size of W = 90 μm and L = 180 nm for the input transistor with a detector capacitance and interconnection of 300 fF. Knowing the gate area capacitance given by the technology - 8.46 $fF/\mu m^2$ - I derive C_{Csa} optimal value to be 137 fF which is close to the optimization for thermal noise found analytically.

According to my calculations, this leads to an equivalent noise charge with detector of 11 el.rms. I made my simulations considering an ideal amplifier with a low flicker NMOS input transistor (nelna).

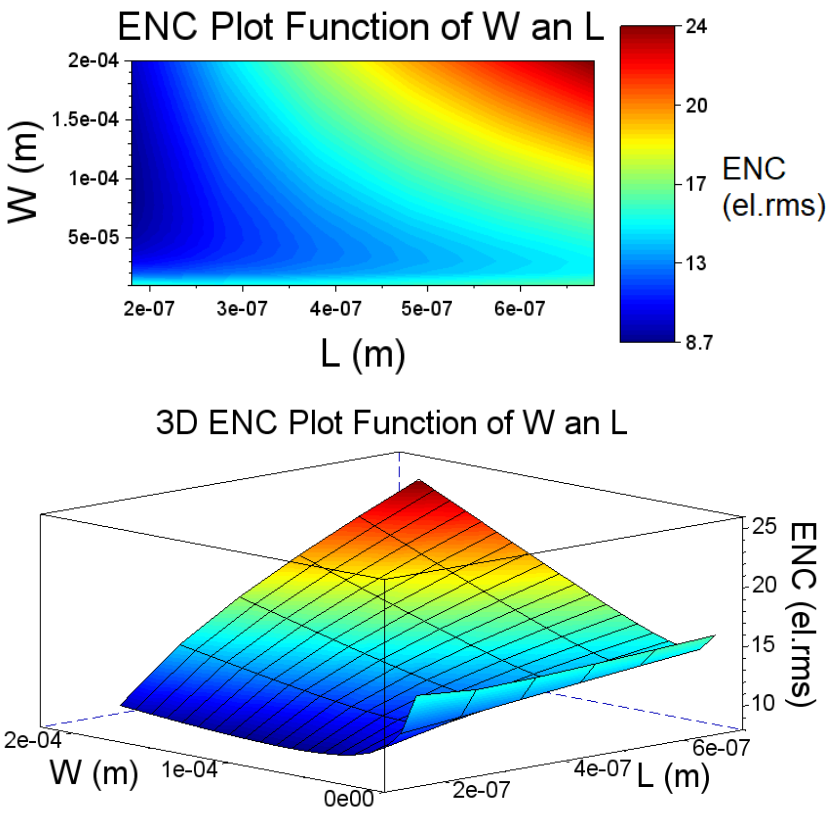

FIGURE 4.9 – *ENC curve for Tpeak = 3µs with ideal CR-RC filter for different Width and Length of input NMOS transistor for 10 µA bias current*

However, in this region, the transistor is biased in weak inversion region where optimum is relatively flat with respect to W as soon as the width is larger than to 30 μm as shown in figure 4.9. It is optimum for minimum L, and W has been chosen as the minimum point of the curve.

The size of input transistor has been fixed, and a careful optimization on other transistors in the circuitry lies in table 4.3 which describes the influence on transistor sizes on the design.

TABLE 4.3 – *Optimization scheme for CSA transistor dimensions excluding the input one*

Transistors dimensions	Gain (Open Loop)	Bandwidth	Dynamic	Thermal noise	Flicker noise
W_0	NA	NA	NA	↘	↗
L_0	NA	NA	NA	↗	↗
W_2	NA	NA	↗	↘	↗
L_2	↗	↘	↘	↗	↗
W_3	↗	↗	↗	↗	↗
L_3	↘	↘	↘	↘	↗
W_4	↘	↗	↗	↗	↗
L_4	↗	↘	↘	↘	↗

The main objective was to have an open loop gain larger than 1000 V/V and a bandpass larger than 100 kHz, while having a small proportion of noise generated by transistors inside the circuitry below 10 el.rms. For this reason, transistor M0 has been chosen to have a large L/W ratio (12.5) to reduce its thermal noise. For M2 transistor, the length has been chosen large enough to reduce flicker noise and a medium W/L ratio has been taken to decrease overdrive voltage down to 400 mV, while not generating thermal noise at a measurable level. M3, the cascode transistor is desired to have a large W/L ratio in order to provide a large transconductance. Finally, M4, the output transistor has been chosen small enough to increase the bandwidth while having a large length for to increase output resistor up to several $M\Omega$ and provide an open loop gain up to 8000 V/V.

Table 4.4 gives the chosen dimensions following the previous discussion.

TABLE 4.4 – *Charge Sensitive Amplifier size and noise repartition. The rest 16% of noise is the detector shot noise*

Name	Type	W	L	Values	Noise percentage $T_{peak} = 4\mu s$	Comments
C_f	cmmh4	2 μm	5.15 μm	25.2 fF		
M0	pe	1.6 μm	20 μm	gm=31 pS gds = 9 fS	20%	$I_{leak} = 1pA$
M1	nelna	90 μm	180 nm	gm=240 μS gds = 5 μS	40% Flicker: 12 % Thermal: 28 %	$I_d = 9.8\mu A$
M2	pe	8 μm	6μm	gm=29 μS gds = 3.6 μS	12%	Mode: $I_{in} = 10uA$
M3	pe3lna	50 μm	500 nm	gm=23 μS gds = 77 nS	6%	$I_d = 1\mu A$
M4	nelna	1 μm	500 nm	gm=5.6 μS gds = 7 nS	6 %	Mode: $I_{out} = 1uA$

III.4. Measurements results

We have performed measurements at the CSA output with external $CR - RC^2$ and $CR - RC$ filters. I used different peaking times and measured noise on the baseline level. Results are given below:

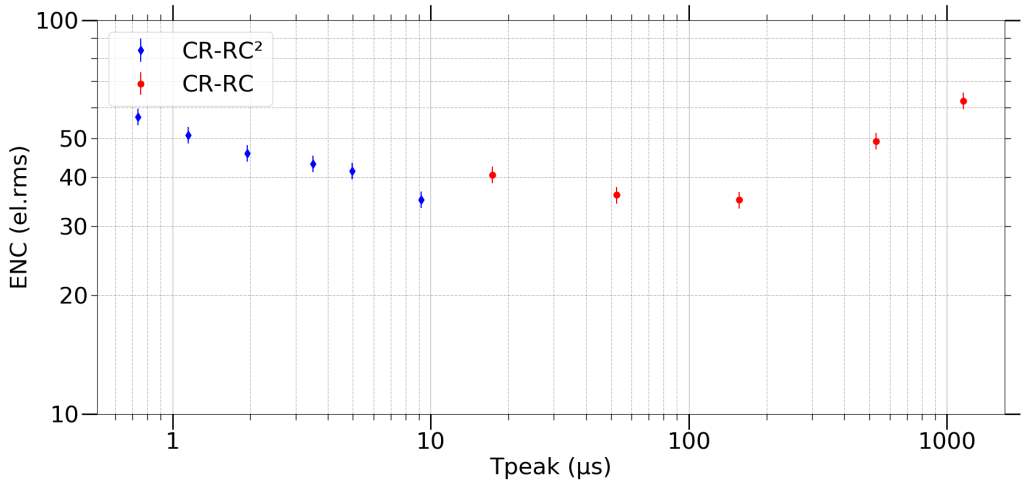

FIGURE 4.10 – *ENC curve function of Tpeak measured at the CSA's output with external $CR - RC^2$ and $CR - RC$ filters for pixel (0,31). Bias current inside CSA was set to 9 μA on the input transistor and 1 μA on the output.*

Unfortunately, I measured a noise **4 times larger than expected**. Considering the very flat curve of the ENC over a wide range of peaking times, it appears quite clearly that it could not be imputed to the input transistor thermal noise nor parallel noise up to 200 μs.

In order to understand the equivalent noise charge value larger than expected I have investigated several possibilities. Such an excess floor noise could be due to 1/f noise excess, noise from power supplies or second stage noise.

• **Power supplies:**

I first considered this excess noise was due to noise on the ASIC power supply. CSA transfer function with respect to the variation on power supply is expressed as a Power Supply Rejection Ratio (PSRR) in figure 4.11.

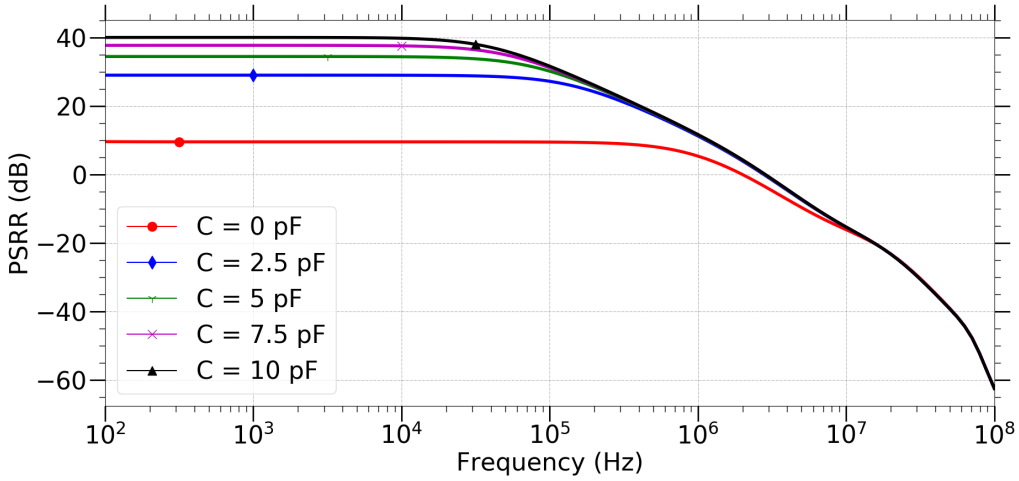

FIGURE 4.11 – *Power Supply Rejection Ratio simulated for different input capacitances at the CSA + Buffer output. The value of 9 dB for no input capacitance, expresses the fact that a 1 mV power supply ripple creates an output ripple of 2.82 mV equivalent to a charge of 200 electrons*

As system is sensitive to power supply ripples, I have added decoupling capacitors and low noise regulators. It did not improved the performance.

• **Voltage references**

Increase of noise might be due to non-perfect references, hence I have decoupled every references with 47 μF capacitances in order to reduce their influences on output noise. This did not reduce the noise at a measurable level.

• **Shielding**

To isolate the setup from FPGA disturbances as well as from the other potential external perturbations, I have developed a metal box that isolates the D^2R_2 Daughter board from disturbances by creating a ground shielding. No noise reduction at the external filter has been experienced, however, the filtered signal, non filtered appeared to be more stable than before, which was a good point for long running time measurements that I performed and will detail later in this chapter.

• **Variation with Capacitances**

In order to try to localize the excess noise source, I have performed noise measurements with a set of capacitors soldered on an external PAD wirebonded to the pixel (1,1) input (as shown in figure 4.12). Measurements are shown figure 4.13.

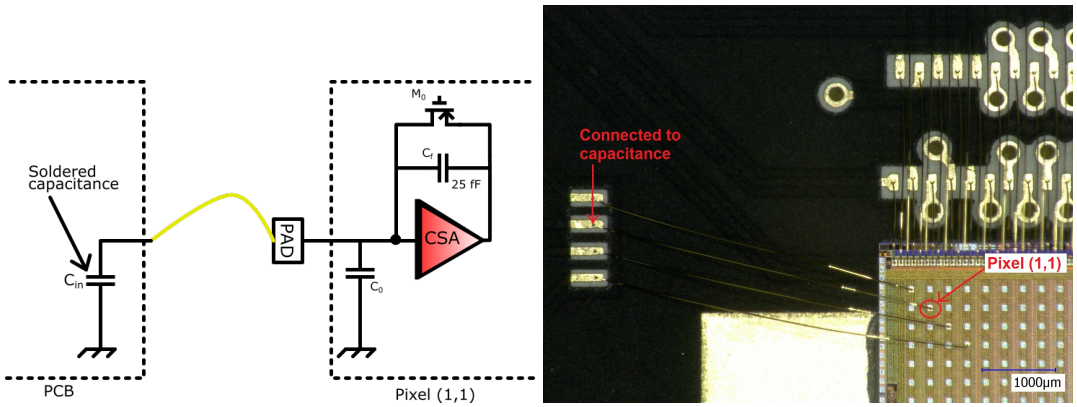

FIGURE 4.12 – *D^2R_2 schematic for pixel (1,1) linked with an external capacitance (left) and picture of the bonded pixels (right)*

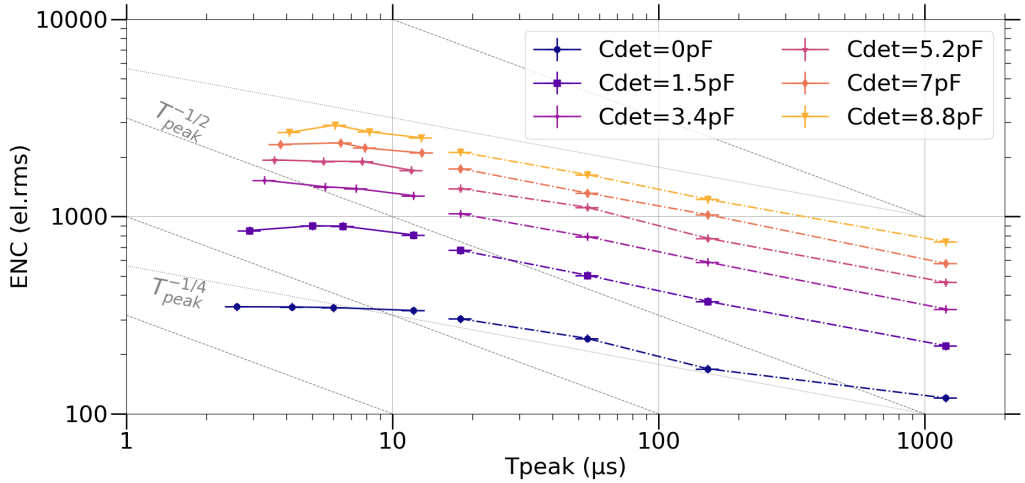

FIGURE 4.13 – *ENC curve function of Tpeak measured at the CSA's output with external $CR - RC^2$ (continuous lines) and $CR - RC$ (dash lines) filters for varying capacitances at 10µA of bias current.*

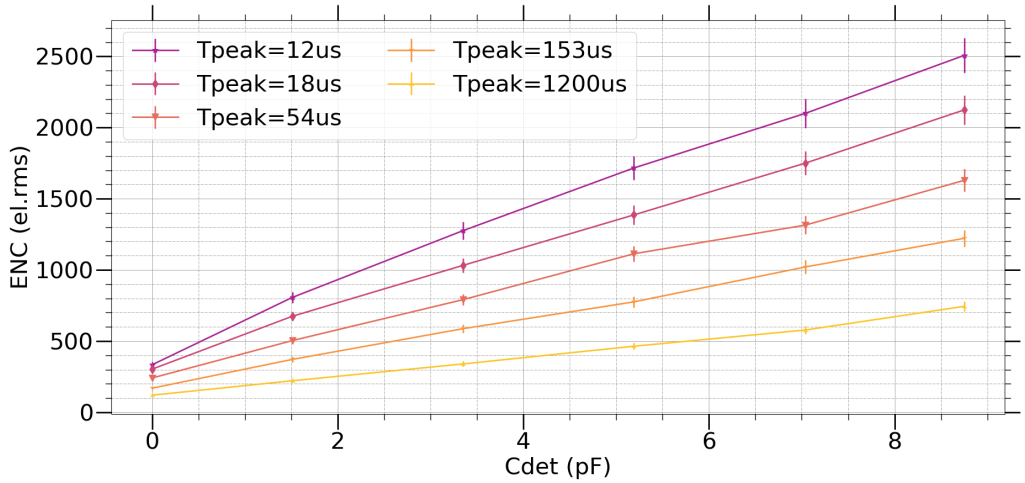

FIGURE 4.14 – *ENC curve function of C_{det}measured at the CSA's output with external $CR - RC^2$ and $CR - RC$ filters for varying capacitances at 10µA of bias current.*

Figure 4.14 shows the linear variation of ENC versus input capacitor value. This effect is clearly varying with peaking time which may indicate a thermal noise component. The variation to capacitance is **300 el/pF** at 4 μs peaking time while 20 el/pF was expected in simulations.

However, as shown in figure 4.13, the slope of ENC vs peaking time appears to be constant for lower peaking times and varying with $T_{peak}^{\frac{-1}{4}}$ at higher peaking times. In the case of a pure thermal noise, filter type does not change the slope of ENC to the peaking time and variation are normally with $T_{peak}^{\frac{-1}{2}}$.

Note that noise variation with capacitance excludes the possibility of constant external noise or output buffer noise, reducing the number of parameters to inspect. Three noise sources can be at stake as shown in equation 3.2, the thermal noise, the ground noise (not expressed in the equation but directly injected through the input capacitance) and the flicker noise.

• **CSA current**

To investigate the thermal noise part, I tuned the CSA bias current by a factor up to 4. The following figure shows the ENC measurement with an external capacitance C_{det} of 1.5 pF.

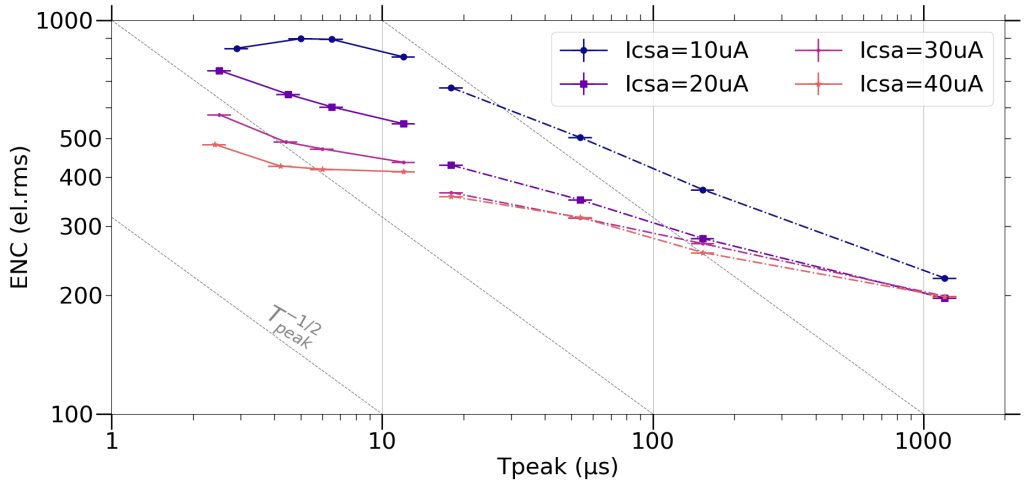

FIGURE 4.15 – *ENC variation with peaking time for CSA output with varying bias currents for* $C_{det} = 1.5\ pF$

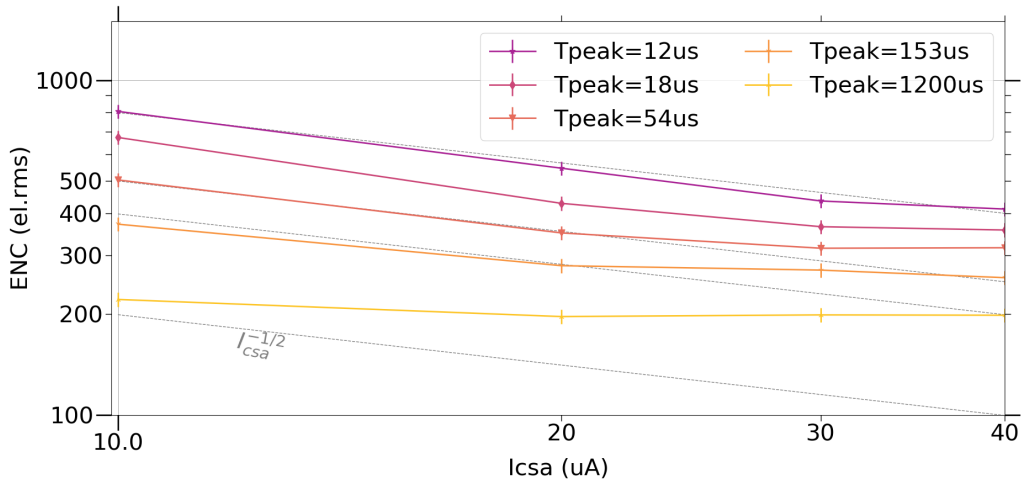

FIGURE 4.16 – *ENC variation with leakage current for different peaking times with* $C_{det} = 1.5\ pF$

Results reveal two different behaviours, depending on the I filter used i.e. $CR - RC^2$ or $CR - RC$.

• $CR - RC^2$ at low peaking times: ENC is almost constant with respect to peaking time (see figure 4.15), consistent with a 1/f noise. However, ENC varies with a factor $\sqrt{I_{csa}}$ (see figure 4.16) which is consistent with thermal noise for a weak inversion biased transistor.

• $CR - RC$ at high peaking times: a variation on ENC with a factor $T_{peak}^{\frac{1}{4}}$ appears with the same dependency on CSA bias current. This effect is not understood for the moment.

• **Ground**

Since the system is composed of three different boards, I suspected grounding to be noisy enough to decrease performances. I have modified the grounding scheme of the whole circuitry, with no major changes on noise behaviour.

• **Flicker**

For flicker noise, I am waiting for the response of the foundry to confirm their models in the weak inversion region with relatively small dimension (W=90 μm / L = 180 nm). I also wait for the confirmation that the low noise optional mask has been implemented in the processed wafers.

Considering, measurements, BSIMV4 model provided by the foundry, SPICE2 model provided by the foundry, and the behaviour of a normal "ne" transistor, figure 4.17 shows the different values expected for different peaking time with a 8.75 pF input capacitance.

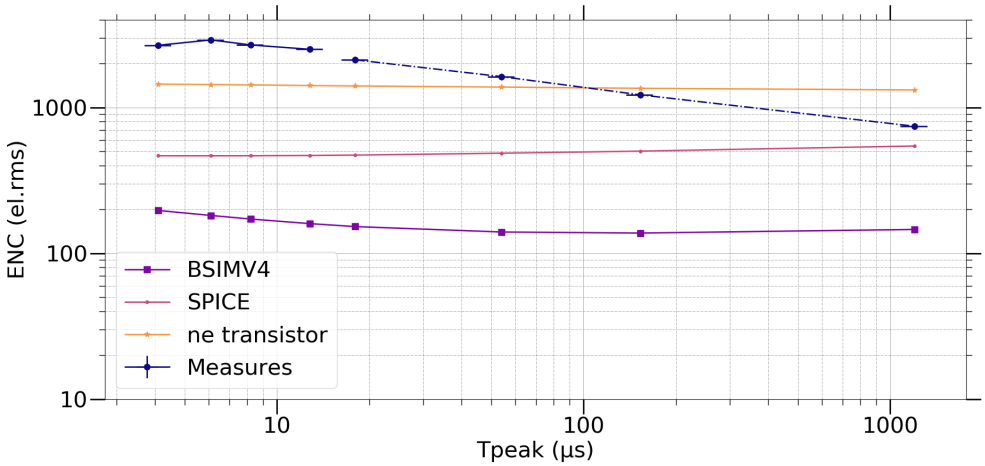

FIGURE 4.17 – *ENC curve for different model in simulation and with measurements, for pixel (31,0) with 10 μA biasing current.*

The noise excess is not fully understood despite my systematic analysis. In the following, I will focus on the detail of following blocks in order to confirm the functionality of the whole spectroscopic chain.

IV. Non Stationary Noise Suppressor (NSNS)

IV.1. Non Stationary Noise

I have described the reset transistor acting as a resistor with a constant value $\frac{nkT}{qI_{leak}}$. This assumption is only true when no charge is integrated. As soon as a charge is integrated, the CSA output voltage rises. This voltage directly controls the source of reset transistor M0, v_{gs} increases, and transconductance increases. This behaviour leads to one issue but also brings an advantage:

• **Noise:** When the transconductance of M0 starts to increase, the noise expressed as $4kT\gamma g_m$ also increases. Noise increases when charge increases, which means it is non stationary. This effect has already been shown with IDeF-X HDBD on chapter 3

• **Saturation protection:** Despite the above mentioned disadvantage, having a non-linear fall time can be advantageous to reduce saturation time when measuring a high charge. Indeed, the higher the charge, the quicker is the recovery of the baseline.

In chapter 3 we have demonstrated that low pass filtering between CSA's output and reset transistor overcome the noise problematic. This function is named NSNS. On top of that, such circuitry adds the possibility to fix the CSA output DC value to a reference voltage.

The NSNS transfer function H(s) is not exactly a low pass filter. Here, I prove that a simple low pass filtering would create oscillations so that a special function needs to be designed carefully.

IV.2. Design

IV.2.a. System analysis

Let us consider the design of an ideal CSA followed by a system providing a transfer function H(s) between CSA's output and the reset transistor. To simplify the calculation, the reset transistor M_0 has been replaced by a resistor R_f. Such a design is illustrated in the figure below.

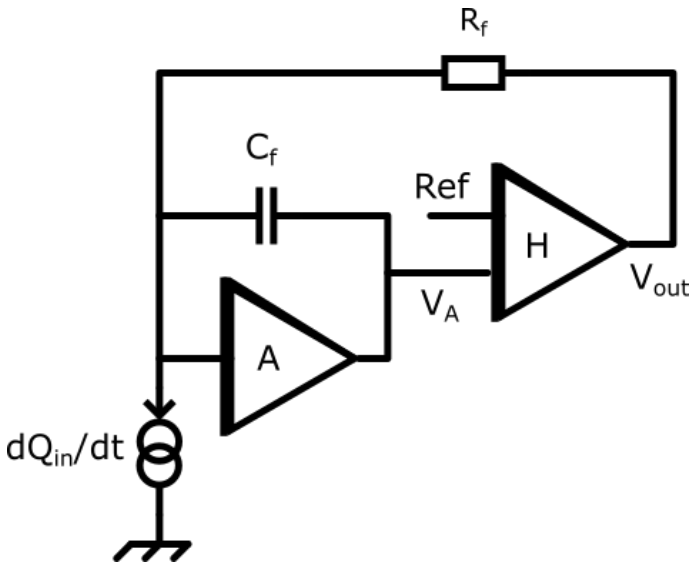

FIGURE 4.18 – *CSA (A) followed by the NSNS with H(s) transfer function.*

The CSA response to a charge step is:

$$\frac{V_A}{Q_{in}} = \frac{R_f}{H(s) + R_f.C_f.s} \tag{4.4}$$

Let us now consider H as a 1^{st} order low pass filter with a pole $H(s) = \frac{H_0}{1+P_1.s}$. Considering this, the transfer function can be expressed as follow:

$$\frac{V_A}{Q_{in}} = \frac{R_f(1 + p_1 s)}{H_0 + R_f C_f s + p_1 R_f C_f s^2} \tag{4.5}$$

According to equation 4.5, the stability condition implies the separation of the two denominator's poles. In other words, $p_1 < 0.25\frac{R_f C_f}{H_0} = p_c$. The charge sensitive amplifier output is stable only when the NSNS pole is at a higher frequency than the reset $\frac{1}{R_f C_f}$ pole. This condition is met with a pole frequency around 1 kHz. Assuming a slope of -20 dB per decade, at the CSA frequency (around 1 MHz), the signal is attenuated by a factor of $1000.H_0$.

However, if leakage current is larger than expected, R_f (equivalent resistance of the MOS reset) decreases and the stability condition is no longer fulfilled, leading the system to oscillate.

A first solution to avoid an oscillation is simply to increase the low pass cut-off frequency of the NSNS block. This way, p1 is lower than p_c whatever the leakage current. However, increasing cut-off frequency limits the efficiency of NSNS as the signal attenuation is reduced (considering a slope of -20 dB every decade).

IV.2.b. NSNS design

As a matter of fact, I propose a second solution expressed in figure 4.19.

The design of a high value resistor taking advantage of an inverted diode based resistance using a MOS transistor is detailed in [2], and [3]. I call R this resistance in the schematic below:

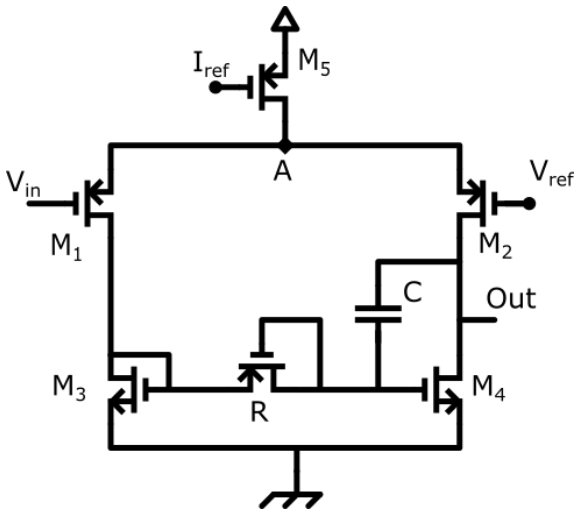

FIGURE 4.19 – *NSNS schematic. High value resistor is made with an inverted diode connected MOS transistor. The equivalent resistor R is in the range of TΩ.*

The schematic is based on a differential pair architecture. Transistor M5 biases the circuitry providing a current of 2 μA to node A. In DC analysis, the system of gain $\frac{gm_2}{gds_2+gds_4}$ forces Vin to be equal to the Vref value once in the CSA feedback.

The high value resistance experiences only little potential variation between its two pads, allowing for a correct high resistive value.

Once the input frequency is larger than the RC first pole, the transfer function starts to decrease until it reaches the zero of the system. This zero is created by the counter reaction of C on gm_4. At this point the signal is attenuated by a value corresponding to the ratio of $\frac{gm_2}{gm_4}$. Finally, a high frequency pole, created by M1 and M2, cuts higher frequencies.

This schematic results in a transfer function that can be expressed as:

$$H(s) = \frac{H_0(1+z_1 s)}{(1+p_1 s)(1+p_2 s)} \tag{4.6}$$

In IDeF-X D^2R_2, I have simulated the AC behaviour to have a first pole at 70 μHz, a zero at 20 mHz, a DC gain of 130 V/V, and an attenuation of CSA output of 0.15 V/V. The behaviour of NSNS is shown in the figure 4.20.

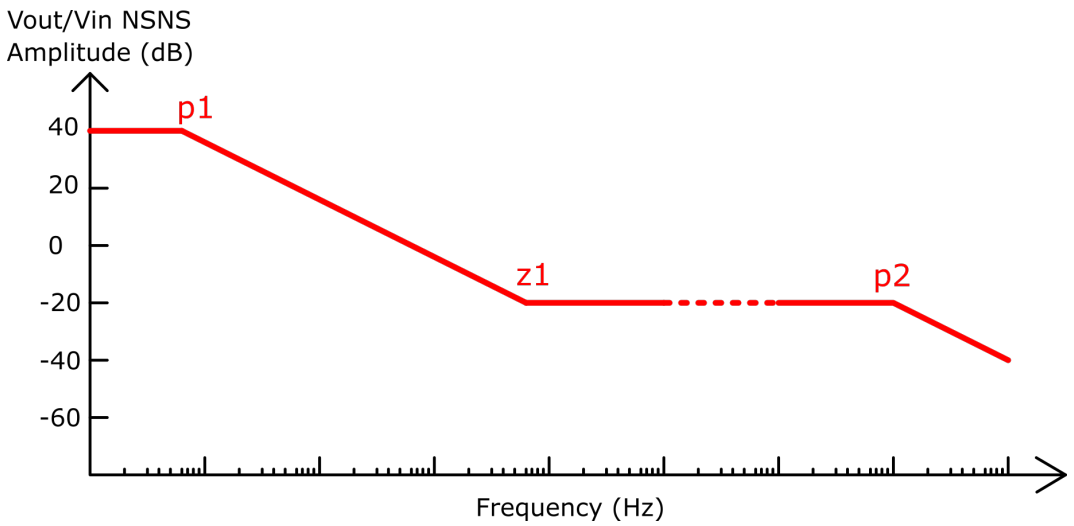

FIGURE 4.20 – *NSNS transfer function*

Let us consider $H(s) = \frac{A_0(1+Z_1 s)}{(1+P_1 s)(1+P_2 s)}$. The closed loop transfer function to a charge step can be expressed as:

$$\frac{V_A}{Q_{in}} = \frac{R_f}{H_0} \frac{1 + (p_1 + p_2)s + p_1 p_2 s^2}{1 + (z_1 + \frac{R_f C_f}{H_0})s + \frac{R_f C_f}{H_0}(p_1 + p_2)s^2 + \frac{R_f C_f}{H_0} p_1 p_2 s^3} \tag{4.7}$$

This solution allows to prevent oscillations as well as providing a proper biasing circuitry for the behaviour of the high-value resistor.

Contrary to the previous analysis on a first order low pass filter in the CSA feedback circuitry, here stability conditions are met when the low pass pole of the NSNS schematic expressed as $R.C$ is smaller than the $R_f.C_f$ pole of CSA reset.

The problem is shifted to the other direction, oscillations start when R_f value is high i.e. a when the leakage current is low.

Designing the solution with a current below 10 fA, far below any expected detector leakage current, assures us to have no oscillation. Hence, assuring a first pole $p_1 = R.C$ with a lower value than the $R_f.C_f$ equivalent pole for low leakage current, leads to a stable circuit. This induces a relatively large resistor of several TΩ and a capacitance of 2 pF.

A bode plot showing the three different cases (no NSNS, low pass NSNS, $D^2 R_2$ NSNS) is depicted figure 4.21.

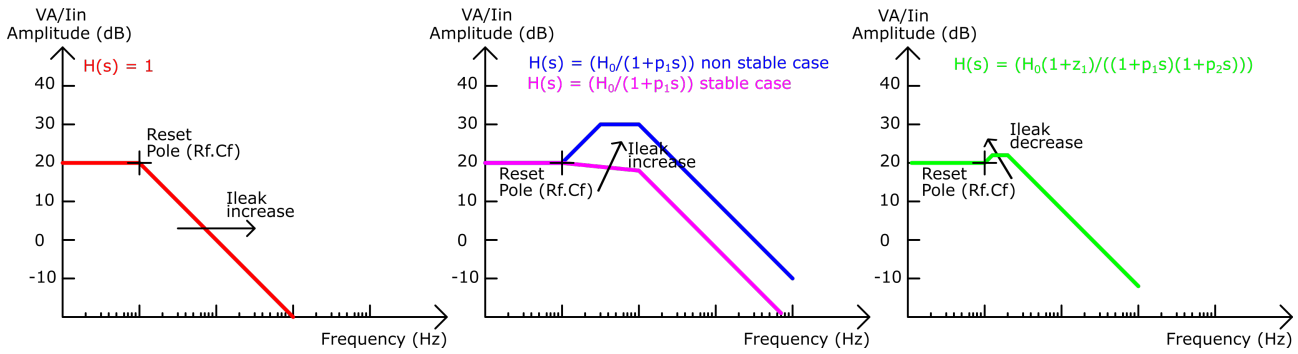

FIGURE 4.21 – *Amplitude VA/Iin value function of H(s). Emphasize is made on the stability cases for low path filtering NSNS*

IV.3. Simulation and measurements

For testing purpose, NSNS can be switched on or off by commanding a switch between CSA output and reset transistor, present in each individual pixel.

I have measured the transient response at the output of the CSA with and without NSNS. This measurement is shown on Figure 4.22.

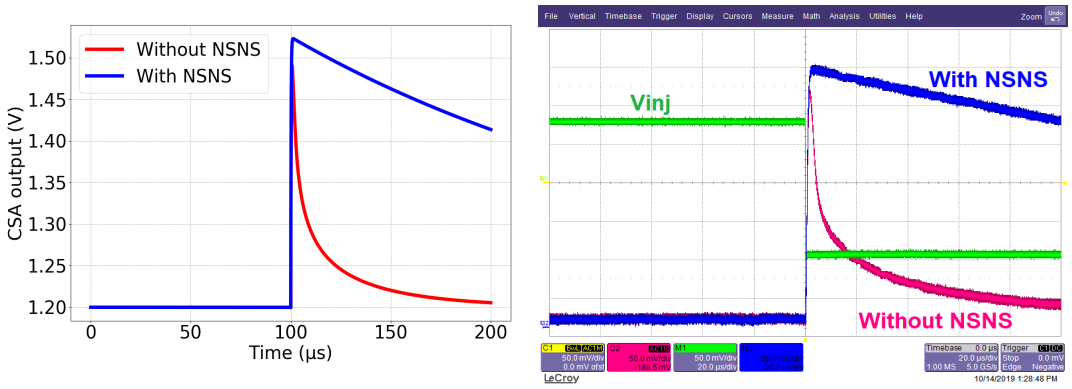

FIGURE 4.22 – *Non-Stationary Noise Suppressor simulation (left) and test results (right). Injection of 27 000 electrons is shown as the green curve (Voltage pulse of 173 mV). Red curve shows the behaviour without NSNS and blue with NSNS activated.*

Results show that the behaviour of the system is close to the simulations. The slope decrease is varying with the input leakage current but not with the charge.

In order to prove the ability of NSNS to effectively reject non-stationary noise, I performed noise measurements for different charges, with and without NSNS activated in chip. Results are given in figure 4.23.

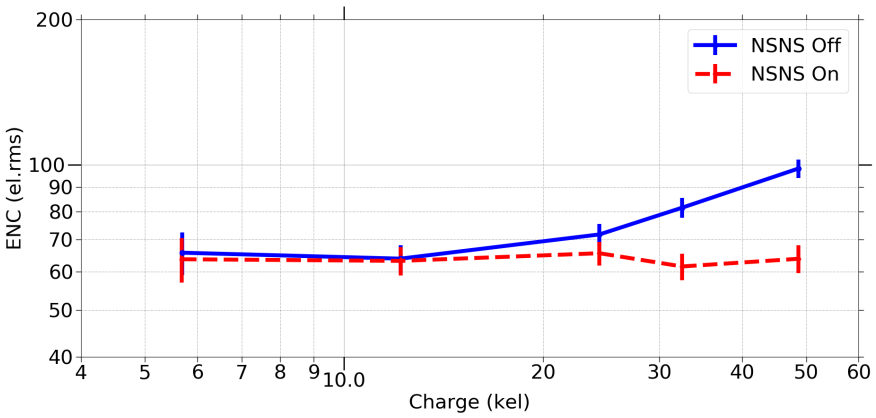

FIGURE 4.23 – *Noise after filter for different charges with and without NSNS with 10 μA bias current and with internal shaper at $T_{peak} = 3.6\ \mu s$.*

Results show that NSNS provides a protection to high charges non-stationary noise due to reset circuitry. This noise increases from 60 el.rms to 80 el.rms at the internal shaper output detailed below. Hence, we can state that non-stationary noise contributes to 53 el.rms at 30 000 electrons of input charge, proving the importance and working behaviour of the NSNS circuitry.

V. FILTERING STAGE OPTIMIZATION FOR LOW AREA

V.1. Description

As shown in Figure 4.3, channel is composed of a CSA with NSNS followed by a pole zero cancellation and a filter stage. Such architecture is based on the fully continuous reset circuitry described in [4]. The basis of such a circuitry is to use N replicas of the reset transistor to cancel the reset pole in the charge sensitive amplifier and replace it by a desired pole of a higher frequency. It creates a $CR - RC^n$ shaper as described in chapter 2. As explained in this section, my design is slightly different:

First of all, I made the peaking time programmable to get more flexibility and to optimize the electronics for various detector configurations and operating conditions.

Secondly, the system is based on a 2-stages pole zero cancellation instead of single stage as described in literature or in chapter 3. The goal is to reach high value peaking times (i.e. high value capacitances and resistances) with only small silicon area (two third of the total pixel area, which means, 200 μm x 200 μm).

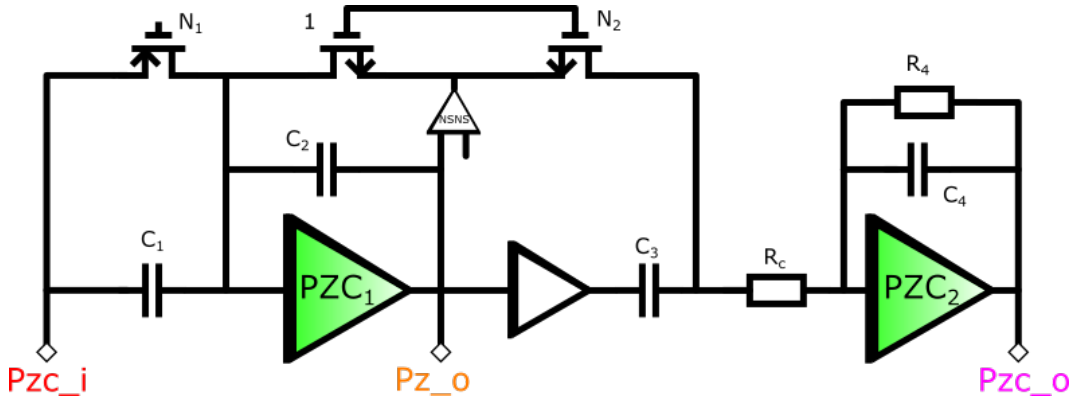

FIGURE 4.24 – *Filtering stage schematic; The first two parts act as a pole zero cancellation circuit. The last amplifier acts as a low pass filter. A resistor R_c has been inserted between pole zero cancellation and lowpass filter to provide an additional pole.*

To explain the behaviour of the block let us consider the bode diagram to an input current expressed in Figure 4.25:

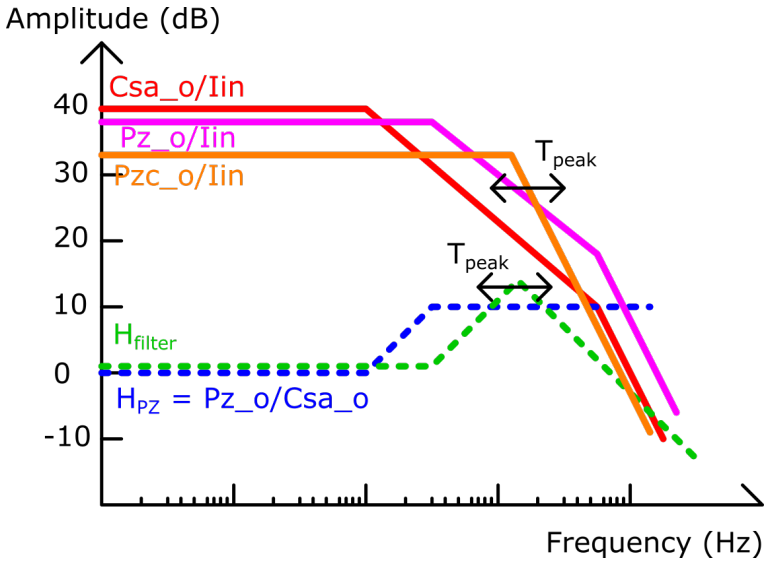

FIGURE 4.25 – *Bode diagram of different signals in the Pole Zero cancellation stage to a current sinusoidal input. For simplicity, NSNS is not taken into account.*

The CSA first pole, corresponding to the reset time constant, is cancelled by the first stage pole zero cancellation stage (H_{PZ}), and a new pole is added to the circuitry at a higher frequency.

This last pole is cancelled on a second stage to create a pole a the desired T_{peak}. This results in having a filter output varying with two poles at T_{peak} value, creating a -40 dB/decade decrease in frequency domain, and a semi gaussian shape in the temporal domain.

This is mathematically written in the equation below, expressing the whole filter transfer function:

$$H_{filter}(s) = \frac{V_{Pzc_o(s)}}{V_{Pzc_i}(s)} = 1\frac{R_4 N_2 N_1 gm_1(1+\frac{C_1 s}{N_1 gm_1})(1+\frac{C_3 s}{N_2 gm_2})}{(1+\frac{C_2 s}{gm_2})(1+R_4 C_4 s)(1+R_c N_2 gm_2 + R_c C_3 s)} \tag{4.8}$$

With gm_1 and gm_2 the reset transconductance of first (CSA) and second stage (PZC).

By setting $C_1 = N_1 C_f$, $C_3 = N_2 C_2$, $C_3 = 3C_4$, $R_c = \frac{1}{3}R_4$, and assuming $Rc << \frac{1}{N_2 gm_2}$, the transfer function becomes:

$$H_{tot}(s) = \frac{V_{Pzc_o}}{Q_{in}} = \frac{NR_4 s}{(1+R_4 C_4 s)^2} \tag{4.9}$$

With N = $N_1 N_2$.

Gain is proportional to N and $\frac{1}{C_4}$. With C_4 defining the peaking time along with R_4. Note that in this case, R_c and C_3 are defining a second pole at the same frequency than $R_4.C_4$

V.2. Peaking Times

As previously mentioned, various peaking times can be selected in the ASIC for filtering. Their values, defined as the time from 1% of the signal to its maximum value, varies following the table below:

TABLE 4.5 – *Simulated peaking times*

Peaking Time	Value	Unit
0	144	*ns*
1	212	*ns*
2	377	*ns*
3	550	*ns*
4	980	*ns*
5	1.8	*µs*
6	2.7	*µs*
7	3.6	*µs*

These values have been chosen to cover a large range with an upper limit fixed by the noise optimization for our detector system combined with the low area requirement. The lower limit has been chosen to perform high speed measurement when high flux is needed.

V.3. Area optimization

The whole system could have been designed with only one stage instead of two pole-zero cancellation stages. A single stage architecture would have the advantage of simplicity and would provide a better cancellation as it only relies on one matching parameter instead of two. However, 2-stages pole zero cancellation is more efficient to fit into a small area as I explain here:

Let us consider two systems, one with a single stage and the other with a second stage. I assume that the area required for amplifiers is small compared to the one for passive components and reset transistors. The two areas corresponding to both architectures are given by:

$$
\begin{aligned}
S_1 &= \frac{1}{\epsilon}(C_f(1+N) + \frac{Nq}{3G_{tot}}) + \frac{1}{\gamma}(\frac{4}{3}R_4) + W_{reset}L_{reset}(1+N) \\
S_2 &= \frac{1}{\epsilon}(C_f(1+N_1) + \frac{N_1.C_f}{Gain_{PZ}}(1+\frac{N}{N_1}) + \frac{N.q}{3.Gain_{tot}}) + \frac{1}{\gamma}(\frac{4}{3}R_4) \\
&\quad + W_{reset}L_{reset}(2+N_1+\frac{N}{N_1})
\end{aligned}
\tag{4.10}
$$

With ϵ the capacitance surface, γ the resistor surface (considering resistor width fixed), $Gain_{PZ}$ the gain in the first stage of the filter, and $Gain_{tot}$ the total gain.

The noise optimization of the channel gives an optimum N ($= N_1.N_2$) factor of $N_{min} = 820$. I have used this value to plot (see figure 4.26) the ratio between S_2 and S_1 as a function of N_1 and the PZC gain.

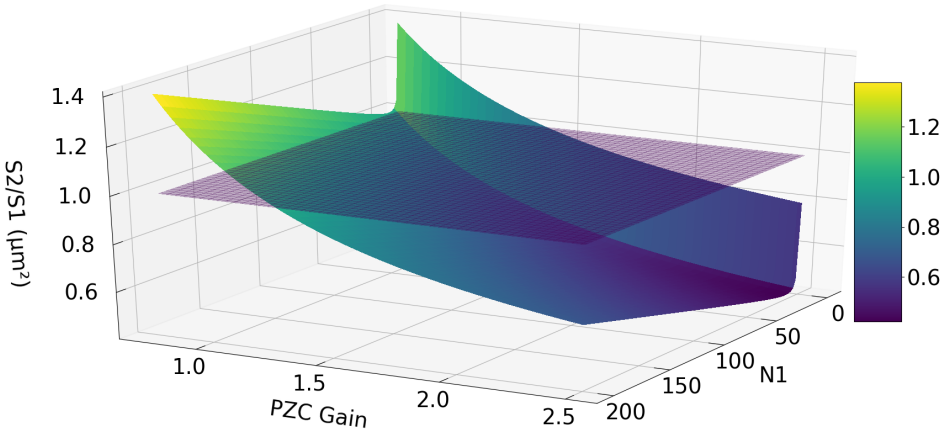

FIGURE 4.26 – *Surface ratio between one stage PZC and two stages PZC. The plot shows that for a PZC gain larger than 1, the 2-stage solution is smaller.*

As a result, a 2-stage architecture is smaller.

For capacitor, on the single-stage architecture, compensation requires $N.C_f$ capacitances. On the 2-stage architecture it needs $N_1C_f + N_2C_2$.

If no gain is desired, previous calculation results in $C_2 = N_1C_f$. Consequently, the two stages architecture uses more area than the single stage architecture.

Conversely, if gain is desired in the first stage of the PZC, then $C_2 = \frac{N_1C_f}{Gain_{PZ}}$ and 2-stages architecture starts to take less area than single stage architecture even for capacitors.

With respect to the reset transistors, 2-stages architecture requires $N_1 + N_2$ transistors instead of $N_1.N_2$. The occupied surface is reduced by a factor 14 for N=820.

I proved that it is relevant to use the 2-stages architecture in my design where gain is allowed and compensation transistors represent a large part of the final area. All of the discussion above relies in a compensation factor named N. This factor is directly linked to the noise created by the filter (assumed from the beginning to be noiseless) and is detailed below.

V.4. PZC Design and results

V.4.a. Design

Let us consider the design expressed in Figure 4.24. In such design several parameters need to be fixed:
• Compensation factors: N_1 and N_2
• Peaking time resistor: R_4
• Pole resistor: R_c
• Peaking time capacitance: C_4

Peaking time Resistor

According to the equation 4.9, modifying the peaking time by modifying C_4 leads to modification in the whole circuitry. To cover this aspect, capacitors have been designed with a set of selectable components as well as reset transistors, that follow each other when peaking time is modified. To illustrate this aspect, let us consider two extreme settings, when $T_{peak} = 3.6\ \mu s$ and when $T_{peak} = 144\ ns$. On the first case, $N = 820$, $C_4 = 3\ pF$. On the second case $N = 20$, $C_4 = 74\ fF$.

Setting the peaking time by modifying R_4 does not change the gain and reduces the amount of switched components. However, for low peaking time, it is convenient to have a low C_4 to reduce the power taken by the amplifier to perform a gain at a reasonable speed. Thus I have chosen to keep R_4 fixed and modify N and C_4.

The noise optimization leads to an optimal peaking time of 3 μs (see page 145). The highest aimed peaking time is 3.6 μs (expressed in table 4.5). Hence the first equation to fix one parameter is:

$$R_4 = \frac{T_{peak}}{C_4} = \frac{3.6 \cdot 10^{-6}}{C_4} \tag{4.11}$$

Pole resistor R_c

From equation 4.8, when R_c is negligible in front of $\frac{1}{N_2 g m_{r_2}}$, an additional pole is created. Assuming that the reset transistor is operating in the subthreshold region with a current $N_1 I_{leak}$, then we should have $R_c << \frac{nkT}{N_1 N_2 q I_{leak}}$.

For area optimization, the gain must be added in the first stage of PZC as mentioned before. Hence the last stage of the PZC should have a gain equals to 1 in AC. Following the temporal expression of the filter, I fixed $C_3 = C_4.e^1$. Approximating e^1 with 3, we can fix $C_3 = 3.C_4$. Then, R_c value is derived from $R_c C_3 = R_4 C_4$:

$$R_c = \frac{R_4}{3} \tag{4.12}$$

Peaking time capacitance

The thermal noise of R_4 is integrated through C_4 which leads to an equivalent noise charge created by the PZC inversely proportional to C_4 value. To fix this value, I expressed the C_4 value as below:

$$C_4 = \frac{1}{3} \frac{4kT.T_{peak}}{Gain^2 \beta_{th}^2 . K_{th}} \tag{4.13}$$

Where Gain is the total chain gain (I chose 16 $\mu V/el$ to comply with energy range)
β_{th}^2 represents the thermal noise component of ENC for the whole chain
K_{th}, is the squared ratio of the PZC noise contribution over the total thermal noise.

The PZC must have a negligible noise with respect to the CSA noise. The resistance noise is referred to the input as a thermal noise. I extracted the thermal noise part of CSA by simulation and I found $\beta_{th}^2 = 160 \cdot 10^{-6} el^2.t$. Choosing $K_{th} = 0.02$ (PZC exhibits 15% noise compared to CSA), I found $C_4 = 2.7pF$ which leads to $C_3 = 3C_4 = 8.1pF$. The area required for both these capacitors is 63 x 63 $\mu^2 m$, fully compatible with the available area in a pixel. With such values, noise contribution for PZC at highest peaking time is expected to be lower than 2 el.rms.

Compensation factors

Following the previous analysis, the total compensation factor is expected to be:

$$N = \frac{Gain.C_3}{q} = 820 \tag{4.14}$$

N being fixed, I now have to choose N_1 and N_2. I can use a similar approach than in the previous paragraph based on the noise created by reset transistors. Such study find that the reset noise referred to the input is seen as a flicker noise. Hence the optimal

N_1 value leads to:

$$N_1 = \frac{16qI_{leak}T_{peak}}{3nq^2K_f\beta_f^2} \tag{4.15}$$

With β_f^2 the flicker noise factor
K_f is the squared ratio of the PZC reset noise contribution over the total flicker noise.

Choosing $K_f = 0.03$ leads to $N_1 = 41$ and $N_2 = 20$. With these values, reset transistors exhibit only 1.6 el.rms noise referred to the input.

Discussion and conclusion on the design

Area optimization and noise reduction are constraining my design study, leading to values for the highest peaking time. In the overall analysis I neglected the noise of the amplifiers. I designed the amplifiers carefully. In fact they are replica of the Charge Sensitive Amplifier.

I also did not discuss the voltage follower depicted in Figure 4.24 between PZC_1 and C_3. Such amplifier has been implemented to allow system to respond in less than 100 ns.

The value of N_x is a tradeoff between speed and noise. Noise requirements are less stringent at faster peaking times as the CSA is more noisy anyway. Hence, reducing N for smaller peaking times reduces capacitances and therefore increases the speed of the channel. This allows for more flexibility in the design and compactness. The whole values are summarized in the table below.

TABLE 4.6 – *PZC optimized values for different peaking times*

Peaking Times	N_1	N_2	N	C_1	C_2	C_3	C_4	ENC_{PZC}
144 *ns*	1	20	20	25 fF	10 fF	200 fF	67 fF	10 el.rms
212 *ns*	2	20	40	50fF	20 fF	400 fF	133 fF	7 el.rms
377 *ns*	4	20	80	100 fF	40 fF	800fF	267 fF	5 el.rms
550 *ns*	6	20	120	150 fF	60 fF	1.2 pF	400 fF	4 el.rms
980 *ns*	11	20	220	275 fF	110 fF	2.2 pF	733 fF	3 el.rms
1.8 μs	21	20	420	525 fF	210 fF	4.2 pF	1.4 pF	2 el.rms
2.7 μs	31	20	620	775 fF	310fF	6.2 pF	2.07 pF	2 el.rms
3.6 μs	41	20	820	1 pF	410 fF	8.2 pF	2.73 pF	2 el.rms

V.4.b. Results

In order to test the performances of the chain at the output of the PZC block using the spy mode, I used two different test setups. Firstly, I performed measurements of ENC on the baseline at different peaking times using an oscilloscope. The ENC variation with peaking times is shown on figure 4.27

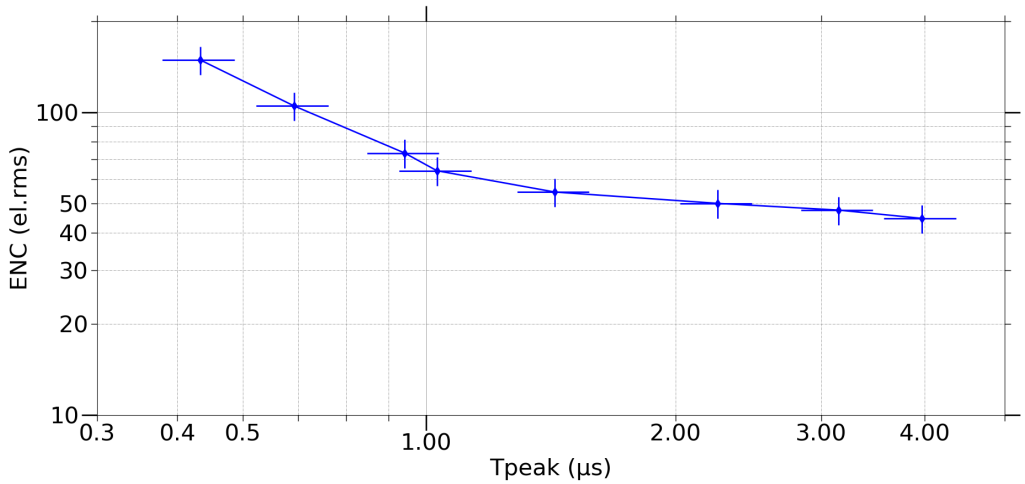

FIGURE 4.27 – *Results for a non wire bonded pixel (0,31) which exhibits the best noise floor (as no supplementary capacitance nor dielectric noise exists).*

The minimum ENC was found to be 45 el.rms for a standalone pixel (no bonding, no detector). This value is still far from the 11 el.rms expected in simulations, but corresponds to the ENC measured with external filter. The same way as with CSA, output signal is filtered by the spy circuit, which is the reason why I cannot reach the expected faster peaking times.

In order to analyse the behaviour of the circuitry with respect to the input charge, I modified the previous setup to allow for digitizing the signal with a DT5724G CAEN ADC (14 bits for 2.25V). At first, I tested the pixel (0,31) against injection charge levels from 1450 electrons up to 120 000 electrons. I took 1000 acquisitions for each charge.

Amplitude variation of output signal versus charges is shown on figure 4.28. As expressed before, pixel gain can be set to two values depending on the desired energy range. For the nominal behaviour (Gain 1), the dynamic range is found to be linear up to 39 400 el (174 keV (CdTe)). From this curve, I extracted the integral non-linearity as the deviation of the signal from a linear fit which crosses the first and last point of the range depicted before, divided by the full range. Dynamic range and linearity is illustrated on figure 4.28 and 4.28

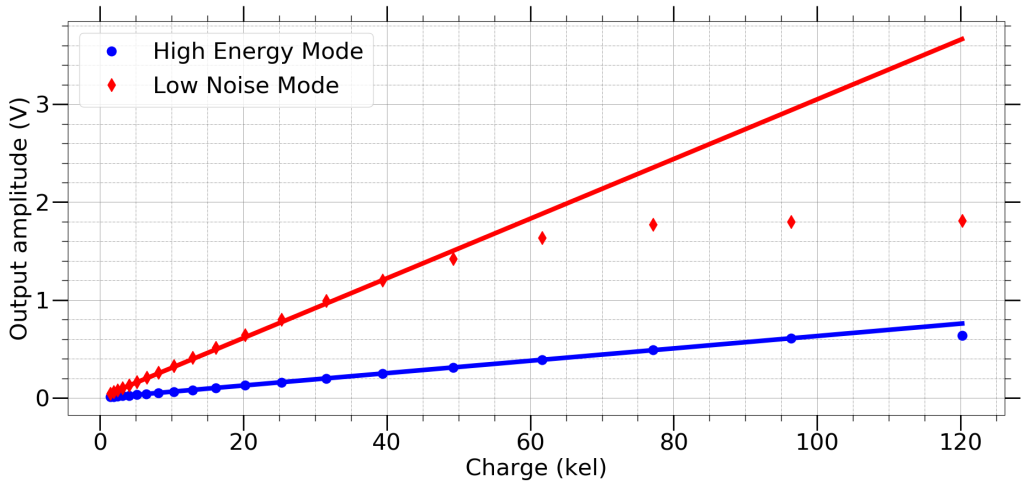

FIGURE 4.28 – *Amplitude variation for D^2R_2 with both gain. Line corresponds to the linear curve used for INL depicted on Fig 4.29*

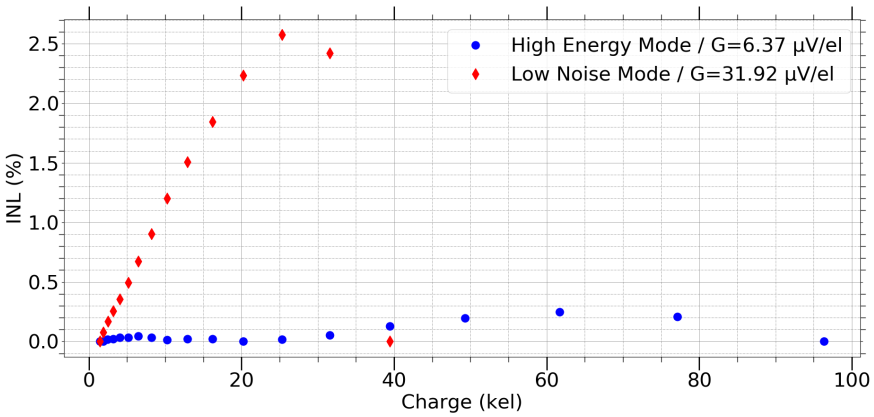

FIGURE 4.29 – *Integral Non Linearity expressed for the two gains on pixel (0,31).*

The maximum integral non-linearity occurs for the higher gain of 32 μV/el with a value of 2.6%. On the whole energy range of 39 400 electrons, such non linearity is high and can be reduce down to 0.24% with energy range is lowered to 25 000 electrons.

Noise has also been measured through the standard deviation of maximum values of digitized signals as shown on figure 4.30.

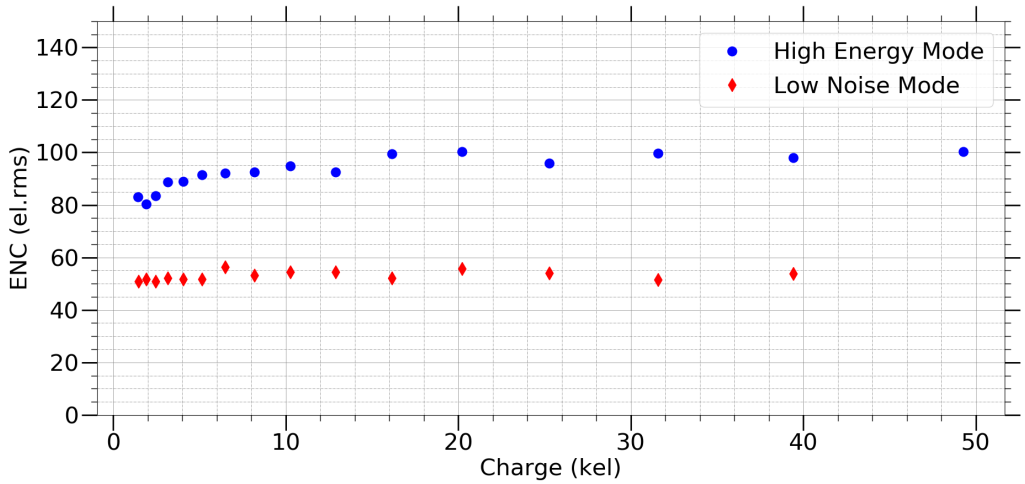

FIGURE 4.30 – *Equivalent Noise Charge for versus input charge in both low noise and high energy modes.*

Equivalent noise charge is approximately constant over the whole charge range, except for saturation regions. Mean values of 50 el.rms are relatively consistent with the 45 el.rms found before and the increase of 5 electrons is likely to be due to 50 Ohms buffers used to digitize the signal with the external ADC. On top of that, low gain ENC is, as expected larger (around 100 el.rms compared to 35 el.rms in simulation).

In order to test the uniformity of the whole matrix, I made the same measurements and data analysis on a lower statistic, using 100 event per charge and per pixel over the entire array matrix. The results are shown in figure 4.31

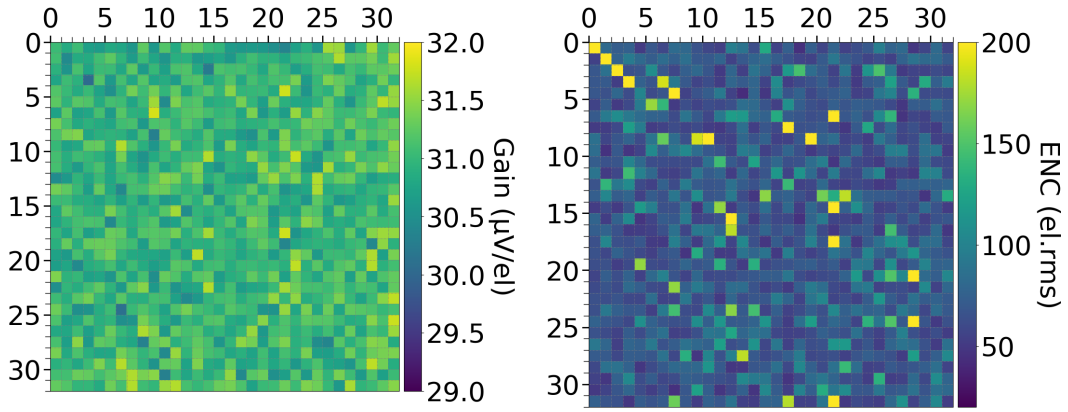

FIGURE 4.31 – *Measurements of gain values for each pixels (left). And equivalent noise floor for every 1024 pixels of the matrix (right). Averaged gain value on the whole matrix is 31 µV/el as expected with a standard deviation of 271 nV/el. Mean ENC is 74 el.rms with a standard deviation of 21 el.rms which is larger than expected. Note that noise distribution over the whole matrix is non gaussian.*

First, the circuit is fully functional. Performances of every pixels is measurable and statistics can be extracted. Larger values on pixels (1,1), (2,2) and (3,3) are expected and due to wire bonds on these inputs, increasing input capacitance.

The mean ENC is found to be 74 el.rms with a standard deviation of 21 el.rms (˜30 %). The standard deviation is larger than expected and follow a non-Gaussian distribution as on figure 4.32.

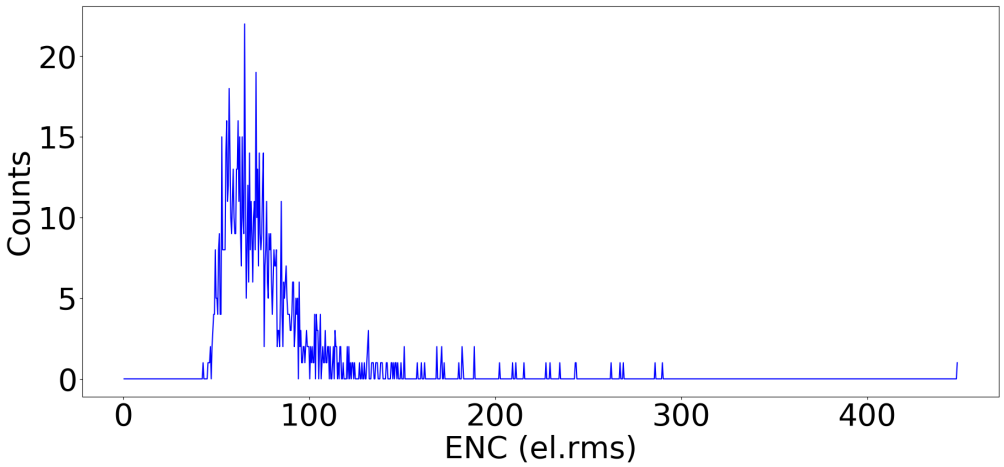

FIGURE 4.32 – *Distribution of noise on the matrix.*

No geometric effects appear to take place. The noise dispersion is randomly distributed across the array. Conversely, the gain distribution is Gaussian with a small standard deviation. The mean gain is found to be 31 $\mu V/el$ and the standard deviation is lower than 1 %

VI. Peak detection

IDeF-X D^2R_2 uses a peak detection unit to store the maximum voltage occurring at the shaper output. Such system is detailed below.

VI.1. Architecture Presentation

The peak detector architecture is based on the architectures described in [5], [6]. If pile-up rejection, or offset suppression is necessary in the case of high precision peak and hold circuitry, I recommend to read [7] describing more advanced peak and hold circuits. In the case of IDeF-X D^2R_2, I chose a simple version using only one reset signal.

It is depicted below and is relatively similar to the one described in IDeF-X HDBD:

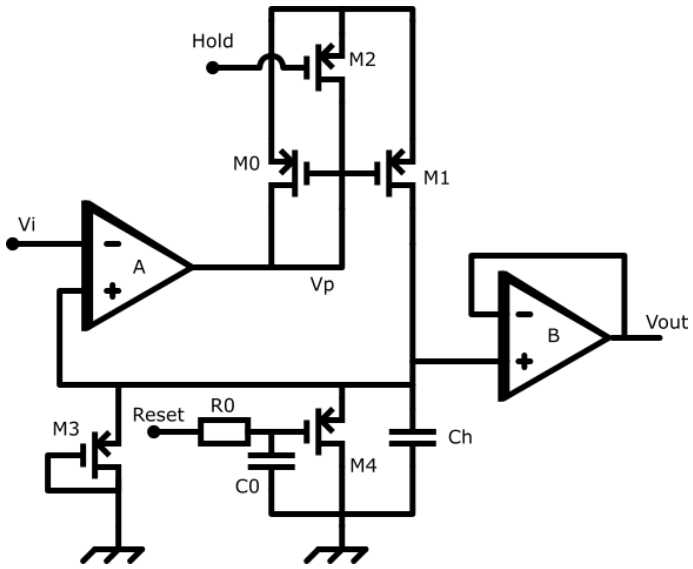

Figure 4.33 – *Peak detect and hold schematic*

VI.1.a. Functional behaviour:

The first step of peak detection is the reset step. A reset signal is sent to transistor M4 to allow a path to discharge C_h . A resistance, capacitance network filters the rising edge of the reset signal in order to reduce the charge injection it would create otherwise.

In a second step, when a charge is integrated into the CSA and filtered, a semi gaussian shape signal reaches to the peak detector at the input V_i. The amplifier "A" amplifies the signal $\epsilon = V_{out} - V_i$. As output signal is close to zero at the beginning, signal at the output of voltage amplifier tends to be close to its lowest value (around 0V). Hence M0 and M1 are conducting and current can start charging capacitance C_h.

The third step starts when signal V_i decreases. At this time V_i is lower than V_{out} and V_p tends to saturate to V_{dd} voltage. Transistors M0 and M1 are now "OFF" and current cannot flow anymore to the hold capacitance. The maximum value of the signal is memorized.

In order to prevent circuit to continue its peak detection in case a larger signal arrives, a hold transistor M2 is externally controlled to fix the output amplifier voltage to Vdd and block the hold capacitance. A simulation of the system is shown in figure 3.27 on chapter 3.

Finally, a buffer sends the maximum value out of the pixel, providing a high impedance to the hold node. Transistor M3 in figure 4.33 forces some leakage currents in M1 and M0. It allows the system to be stable if no charge is coming.

VI.2. Simulation and Results

In simulation, signal can be stored during several milliseconds. The slope decrease, due to leakage currents in the hold part of the design is dependant with temperature and has been estimated to be -2.5 el/ms for 27^{o}C.

Figure 4.34 shows the measured peak detector output on the prototype. No major differences with the simulation has been noticed. The slope decrease has been measured to be -2.89 el/ms corresponding to the expected value. More thorough analysis with other charges and pixel to pixel variations has not been performed yet.

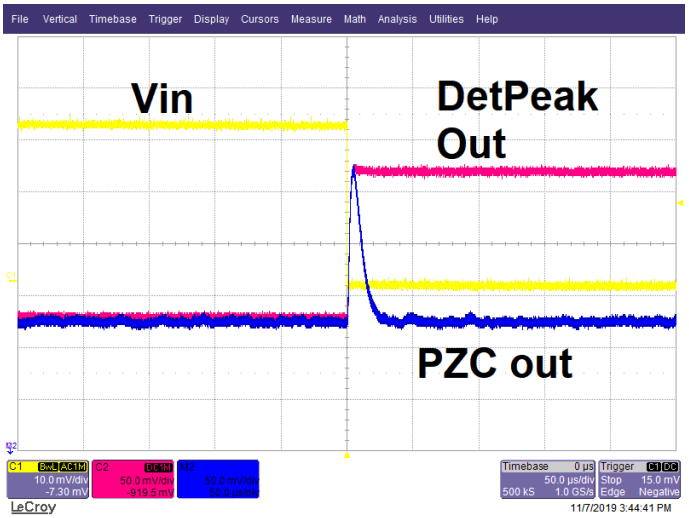

FIGURE 4.34 – *Peak Detector output to a charge injected corresponding to 5 000 electrons. Measured amplitude of 160 mV corresponds to the expected value of 160 mV and slope decrease is -2.89 el/ms, close to the expected value.*

VII. SAMPLE AND HOLD

VII.1. Introduction

In order to access a specific signal at a specific time, in parallel to the peak detector, a sample and hold circuit has been implemented. Such circuit can be linked to 5 internal signals by slow control configuration (CSA output, Pole zero first stage, Filter output, Peak detector output, and Discriminator output) as shown in figure 4.35. In the nominal mode, sampling is disabled and the circuit can be used to multiplex a desired output to the SPY signal.

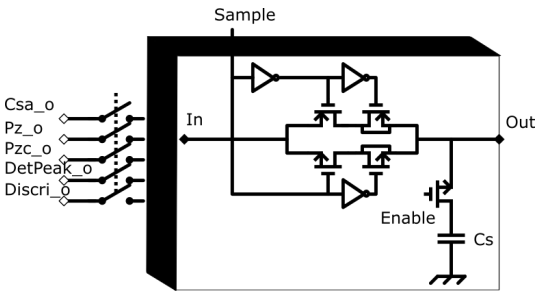

FIGURE 4.35 – *Schematic of the Sample and hold and its multiplexed input*

The sampling mode is enabled by slow control to select and drive a specific signal to the output. The sampling signal is either controlled by an external controller, or internally, using a controllable signal, which is a delayed replica of the triggering signal.

This block has been developed for specifics main reasons:

• **Baseline Sampling:** In IDeF-X D^2R_2, no Baseline holder is implemented to save area. Therefore, the baseline depends on the operating temperature of the detector, as its leakage current. With a Schottky CdTe detector, a temperature variation of 3^oC leads to a baseline variation larger than noise. The temperature will have to be finely controlled and the baseline eventually measured periodically or after each event. Linking the sampler to the filter output, and sampling it several microseconds after an event has occurred allows to monitor the baseline. Energy corrections with temperature are doable.

• **Subpixelisation:** Interestingly, when reaching electrodes, electrons (and holes) follow a different path depending on their interaction position in the crystal. The charge carriers experience specific weighting fields. If a pixel is hit by a photon, neighbour pixels would "feel" a variation of induced current at the input (with null integral). Such a signal can be seen by the charge amplifier if the signal is relatively slow compared to the CSA time constant. For thick CdTe pixel (few mm), it is reasonable to think that it would be possible to read such signal. A deep study on modelling such interactions has been performed in literature [8] [9]. It allows for subpixelisation, which consists in determining the interaction position with a resolution higher than the pixel size.

VIII. Discrimination

VIII.1. Discriminator Architecture

In chapter 2 I described several design particularities of a discriminator and its basic use. I discussed on the accurate time information that several types of architectures can assess, allowing for compensating the time walk. In my application, time accuracy is not a hard constraint. We do not aim in compensating time walk as threshold is expected to be low.

Desired characteristics are presented on the table below, and are linked to expected noise and speed performances.

Table 4.7 – *Discriminator development constraints*

Metric	Value	Unit
Gain	75	dB
Bandwidth	5	MHz
Maximum trigger delay	50	ns
Minimum threshold	500	eV

The implemented architecture is shown below:

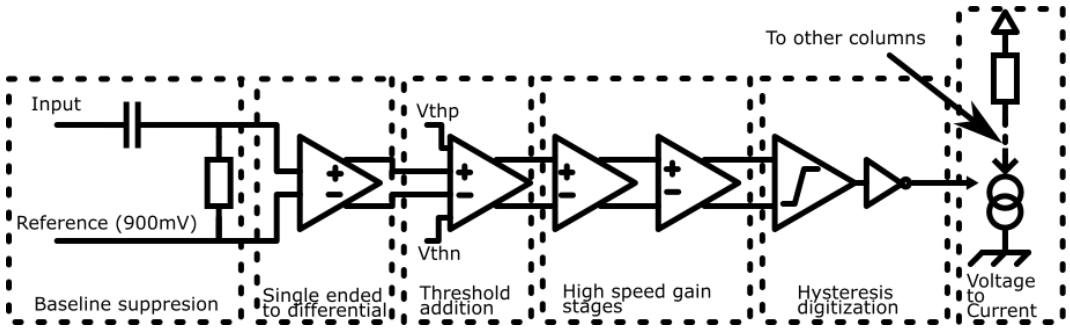

Figure 4.36 – *D2R2 Discriminator schematic.*

A total gain of 2400 allows for discrimination of signal to threshold difference of 450 μV. However, the design of the chain exhibits a non-negligible offset of up to 35 mV due to different stage of amplifiers, designed to keep a low input impedance hence i.e. mismatch variations.

To compensate for this offset, I implemented a 6 bits DAC inside each pixels. The DAC takes two references as input coming from a global DAC. Such system is described below.

VIII.2. Double DAC presentation

Two DACs have been designed and added to the chip implementation.

The first one is pixel addressable and is a 6 bits DAC allowing for having a reference variation ($V_{thp} - V_{thn}$) of +-30 mV with 940 μV step. It is depicted as the "In pixel DAC" in the global DACs architecture in figure 4.37.

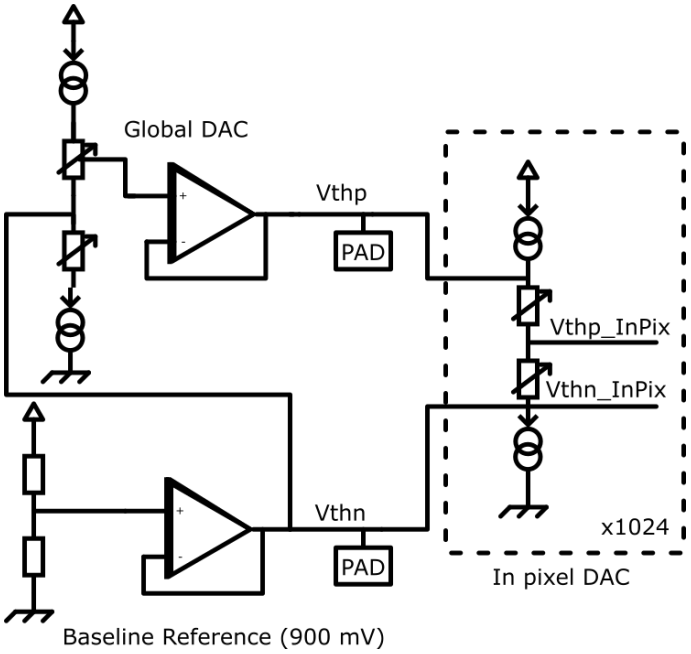

FIGURE 4.37 – *D2R2 In pixel DAC schematic.*

The second one is the global DAC, allowing for moving the threshold globally for each pixel. Hence, the system is designed for compensating each pixel variation with the "In pixel DAC", and moving the global threshold for filtering low energy threshold when desired.

Contrary to the "In Pixel Dac", the global DAC is not linear but based on three steps. It can be set from -880 μV to 106 mV. The first 32 codes correspond to a 60 μV step, the next 16 bits correspond to a 1.8 mV step and last 8 bits allow for 7.5 mV step. This has been implemented in order to perform S-curve measurement, and determine the minimum threshold precisely, but still allow large value threshold when necessary, in case of a noisy pixel for instance.

For both DACs, LSBs can be adjusted by modifying the current value externally (PADS).

VIII.3. Results

On the prototypes, I checked the functionality of the DACs and discriminator. Due to a design error on global DAC current biasing, the global DAC cannot be used. However, Discriminator and "In pixel DACs" are functional and tests have been performed with an external DAC acting in place of the internal global DAC.

A pixel has been powered on and the codes of the DAC were scanned to measure the triggers of the pixel. The first code with no trigger within an acceptable time window has been measured for pixel (15,15) and corresponds to a -12 mV offset value which is in the predicted baseline spread of +-35 mV.

An external DAC was used as a global fine threshold. We counted the number of trigger for a given time window (1 min) for each threshold. Then, I have renormalized the number of trigger to express the probability of trigger within this time window.

The same principle has been used in simulation, with varying input noise (30 el.rms, 60 el.rms, and 90 el.rms).

Results are given in figure 4.38. The expression of number of event passing a threshold has been expressed with Rice [10]. The more noisy is a signal, the more extended is the Gaussian shape of the trigger probability.

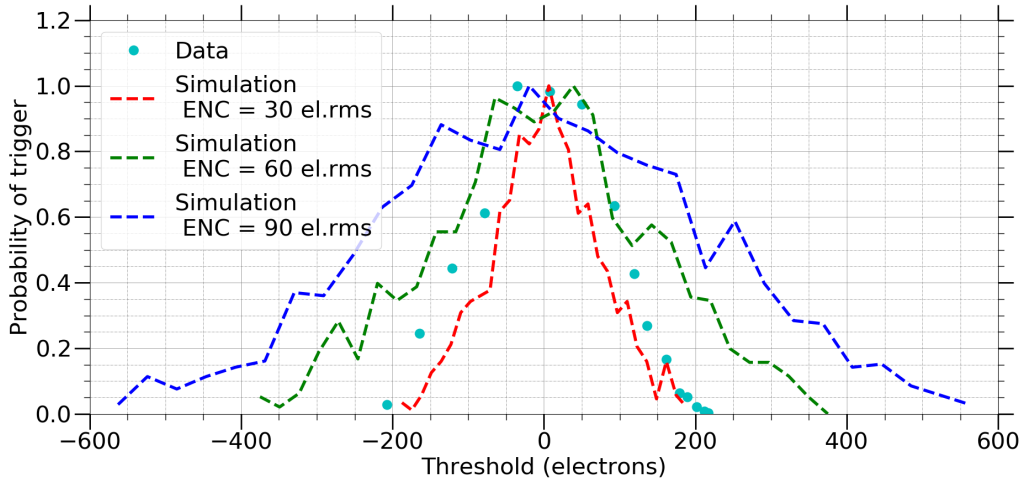

FIGURE 4.38 – *D^2R_2 hit probability within a 60 s time window, function of threshold. Simulations are shown to frame the noise value*

Considering both simulations for a noise of 30 el.rms and 60 el.rms (red and green curve respectively), we can estimate measured noise to be 50 el.rms, in between the two simulated values. With filter output, noise has been measured previously to be 56 el.rms on pixel (15,15). Both measurements, discriminator output and filter output are consistent.

As a conclusion we can estimate the low energy threshold at six times the noise at discriminator level corresponding to 350 el (1.5 keV CdTe). This is more than the expected 500 eV threshold because of the unexpected excess noise of the CSA.

IX. Conclusion

In this chapter, I have described the ASIC named $IDeF - X\ D^2R_2$ that I developed during this thesis. It is specified to readout charges coming from a pixelated CdTe detector with low noise. This ASIC has been designed, and manufactured in the X-FAB 0.18 μm technology. It is a matrix of 32 x 32 pixels with the modular possibility to create a 64 x 64 pixel system butting four ASICs next to next.

This chapter detailed the whole electronic chain of the ASIC from general view of the readout circuitry to basic blocks such as CSA, NSNS, PZC, peak detector/stretcher and discriminator. Despite a non-expected excess noise, the whole matrix is able to perform charge conversion with a minimum noise floor of 38 el.rms in a small pixel size of 250 x 250 μm for a 190 $\mu W/pixel$ power consumption.

In order to cope with the requirements expressed on the beginning of the chapter, several adjustments on the ASIC have been identified, and test will continue in order to precise the different modifications required to comply with hard X-ray imaging spectroscopy for future highly sensitive space missions.

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[10] S. O. Rice, "Mathematical analysis of random noise," *The Bell System Technical Journal*, vol. 23, no. 3, pp. 282–332, Jul. 1944.

Chapter 5: Conclusion

I. Introduction

Hard X-ray grazing angle mirrors have improved tremendously in the last decades. The same path has been followed by Cadmium Telluride semiconductor detectors that now combine good spectrometry performances, near the Fano limit, with small pixel size. In our lab, the current best spectral performance has reached ~600 eV FWHM at 60 keV in a 300 μm pitch pixelated array with a total active surface of 23 mm^2 (4.8 mm by side).

Both improvements lead to develop a new generation of ASICs, able to read out these detectors with higher spatial (down to 250 x 250 μm^2) and better spectral resolution close to the Fano limit ~500 eV FWHM at 60 keV on a wide surface, gradually up to several 100's of mm^2. The development through this thesis aimed such a goal in being able to cope with future hard X-ray imaging satellite missions.

With tests ASICs IDeF-HDBD and Caterpillar, we paved the way towards development of a highly segmented and low noise ASIC for fine spectroscopy in photon counting mode. I designed and tested the full custom ASIC IDeF-X D^2R_2 for that purpose. This step forward is important to take advantages on the experience we got and pursue the development and reach the goal of a high performances, HXR spectro-imaging device, beyond the state of the art. In my concluding remarks, I propose my personal vision on the future developments that I would plan to reach this goal.

II. ASICs promising results

During the thesis work, I have produced two major ASICs, IDeF-X HDBD and IDeF-X D^2R_2 in order to fulfil the HXR future spectro-imaging requirements.

The first one, IDeF-X HDBD, aimed the reduction of noise as well as the possibility to read electron or holes induced charges. This ASIC, reached a spectacular noise floor of 17 el.rms on its 32 channels of 150 μm large and 3 mm width, with both charge polarities. This ASIC has been connected to a Silicon Drift Detector reaching an energy resolution of 227 eV at 5.9 keV with a wide energy range (122 keV gamma-ray line measured on a ^{57}Co spectra with 604 eV FWHM). Such an ASIC even allows for sub keV low level threshold and is a promising system for future spatial missions.

The second one, IDeF-X D^2R_2, aimed the reduction of noise and improvement of spatial resolution. I have tested the whole matrix in a debug mode, proving the functionality of the 1024 pixels within an area of 250 x 250 μm^2 per pixel. Minimum floor noise is 38 el.rms with a mean value on the whole matrix of 74 el.rms. The high spatially resolved and low noise ASIC are promising results, prior to high speed tests and detector hybridization.

III. Ongoing Tests a system behaviour

IDeF-X D^2R_2 has not been tested in nominal mode yet but in a "SPY" mode only, i.e. using the debugging structure I implemented into the circuit to probe detail response of each individual blocks in the pixels. The nominal mode is a fully automatic configuration able to record individual events using all digital communication and state machine sequence, already implemented in the chip. This will need to develop a digital readout sequence, possibly in a FPGA based firmware. The nominal mode will not only allow the characterization of the circuit with faster test sequences, or the possibility to complete evaluations of the triggering circuitry and sequencing but also, will permit to prepare the evaluation of the circuit response once equipped with a CdTe Schottky detector bump bonded on top. Consequently, I consider the development of a FPGA based IP, compatible with the existing firmware as a high priority milestone to investigate further the circuit properties and performance at the level of the whole matrix at nominal speed.

This system will also allow to test for the performances of the sample and hold block. On top of that, the existing test board allows to connect the OWB-1 ADC together with the D^2R_2 ASIC. The test of compatibility between both ASIC is crucial and needs to be performed to allow for simplicity and compactness in the ongoing more experiment-based test benches.

Eventually, once the full system, including D^2R_2 and OWB-1 will have been tested, I would dream to have a detector bump bonded to it and record a spectra with high resolution. At the time being, the circuit is considered sufficiently good to start the preparation of the detector flip-chip process while the FPGA firmware will be implemented.

IV. Module development

IDeF-X D^2R_2 has been designed as a building block of a larger system. The whole system has been thought to be interconnected together, providing a single detection unit performing energy detection, integration, digitization, and calibration.

For focal planes involving large field of view, the 32 x 32 pixels is not sufficient. The use of larger systems and/or several ASICs is therefore mandatory. To avoid having blind gap in the focal plane, it is necessary to abut several ASICs one to another and/or to have bigger sized ASICs.

Considering D^2R_2, only 2 sides are covered with pads. The two other sides are free of I/O's, hence it is possible to build a mosaic of four ASICs keeping a small blind gap in between (typically 50~100 μm wide), due to sawing width. This way, we will end up with an array comprising 64 x 64 pixels. A single monolithic crystal will be flip chip bonded on top. The total detection surface will be 16 x 16 mm^2. Critical electronics parts will be installed as close as possible in a 3D configuration (including the ADC and passive parts for power supplies filters).

The combination of four D^2R_2 with 4 OWB-1 ASICs will allow to have a full spectroscopic chain with digitized data in the same unit.

On top of the idea of having a 2 x 2 ASIC array, following the development of the Caliste technology, the idea is to build a detection module using 3D interconnection as depicted in the following sketch:

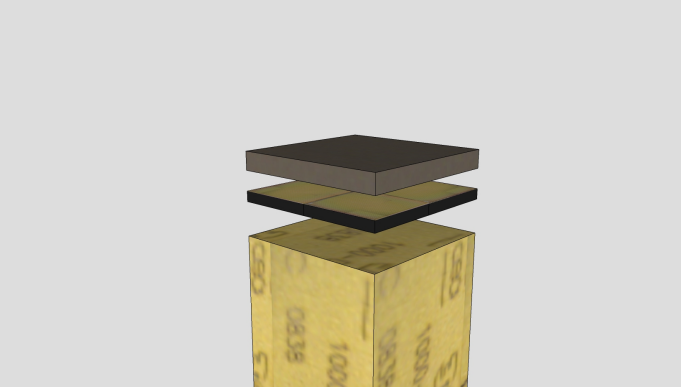

Figure 5.1 – *3D module project. Four ASICs are connected together by the use of a Wirefree Die on Die (WDoD) process perform by an industrial partner. Signals are multiplexed if possible and are sent to the border of a module. A laser cutting allows to interconnect such signals to another stage with OWB-1 ASICs. Other stages with references and several passive components follow. Finally the module send signal at the bottom with a PGA or BGA interconnection.*

This new system will allow to abut several detection units with a small amount of blind spot between modules to cover an arbitrarily large detection plane, up to tens of cm^2. Hence a versatile focal plane can be built. This project is currently ongoing in the laboratory in collaboration with an industrial partner.

V. Toward the development of a final Matrix

On IDeF-X D^2R_2, a low noise "nelna" has been used in order to reduce the flicker noise and reach spectacular spectral performances at the system level. Unfortunately, silicon results have not yet confirmed my simulation expectations. In order to understand this issue, and reach the expected 15 el.rms equivalent noise charge, I recommend to develop a test chip, composed of different CSA with different input transistor sizes and types (similar to Caterpillar). I would also take advantage of this to add some single standalone transistor test structures in order to derive a "home made" model of flicker noise/ thermal noise/ and transconductance, in the regime we intend to operate them.

Getting these information is crucial and would lead to be able to determine whether or not nelna is advantageous in our case. This could lead to the fabrication of another chip composed of only one (or more likely four) pixel with the chosen transistor. Such a chip would be useful to test the analogue performance of one pixel and secure the future performance of a matrix. One could also take advantage of this new pixel development to reduce the pixel area. I think that without moving toward a new technology, adjusting the existing layout, and getting rid of the different "debug" mode, and reducing the number of peaking times to 2 selectable values, a surface of 200 x 200 μm^2 is feasible.

I would also take advantage of this chip to develop and test other devices, such as voltage references, buffer amplifiers, DACs. Development of on-chip low drop out voltage would also be a good opportunity in order to power the chip only with one power supply of 3.3V, saving I/O's and anticipating a much easier 3D integration into a detection module.

The maximum reticle size of the foundry (X-FAB 0.18) is 24 x 30 mm. Hence a design should be limited to 22 x 22 mm. Having the pixel size given above (200 x 200 μm^2), the development of a matrix of 96 x 96 pixel seems reasonable. This matrix could be a scaled-up version of D^2R_2 with several precautions. Voltage supplies (reference and power) should be studied to be able to provide 1 A to the circuit (instead of 100 mA with D^2R_2). Supply lines in D^2R_2 have been developed for 32 x 32 pixels. Having an even smaller pixel would reduce these lines. Hence, I would propose in the 96 x 96 pixel a separation every 32 x 32 pixel of about the size of the pixel to provide supply lines homogeneities (see figure 5.2). Readout circuitry and addressing logic should be adapted as well.

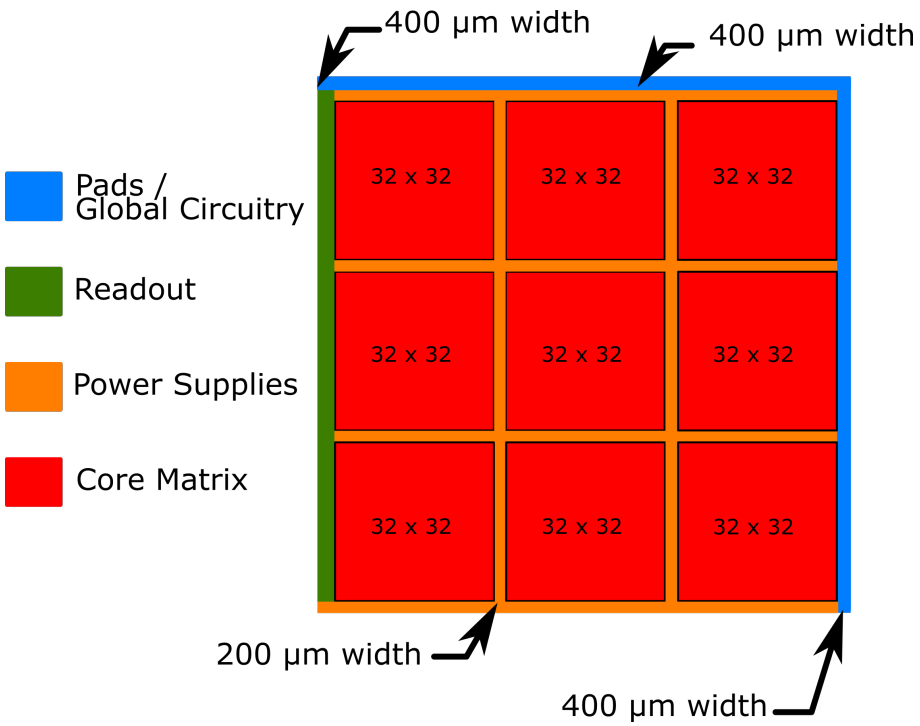

FIGURE 5.2 – *Sketch of a proposed 96 x 96 matrix pixel, compatible with D^2R_2 design.*

Finally, according to my own experience, I would deeply consider for a large matrix, to reduce significantly the number of input outputs. This is the reason why I proposed the development of references and LDOs into chip before, to allow pad ring to be significantly smaller and reduce risk design I have experienced while wire bonding the system.

Honestly, the story could be largely different. I propose here a solution that seems reasonable to me with a relatively low risk, effort and cost. More ambitious project could rely on in-pixel ADCs or automatic atomic compound measurement by means of in-chip machine learning algorithm.

I conclude this thesis with such ongoing developments and hope for the best results on the modular and system aspects with a detector plugged to my D^2R_2.

Appendix A: NMOS Amplifier Optimization

On this appendix I present a common NMOS folded cascode architecture and emphasize the analysis on the optimization of input transistor size with respect to noise sources.

I. Architecture presentation

NMOS folded cascode architecture can be define as shown in Fig A.1. As we already mentionned in the thesis, we can consider it a non noisy CSA with 2 input noise sources. One is a voltage sources representing flicker and thermal noise of the input transistor and the other is the parallel one, non dependant on the input transistor. The Equivalent Noise Charge can be expressed as:

$$ENC^2 = (\frac{A_{th}\alpha_{th}^2}{T_{peak}} + A_f\alpha_{1/f}^2)(C_{det} + C_{csa})^2 + A_{//}\alpha_{//}^2 T_{peak} \quad (A.1)$$

Where A_{th}, A_f, $A_{//}$ are the thermal, flicker, and parallel filter coefficients expressed in 2.1 on chapter 2,
α_{th}, $\alpha_{1/f}$, $\alpha_{//}$ are the thermal, flicker and parallel noise coefficients,
C_{det} is the detector, parasitic and feedback capacitances,
C_{csa} is the input transistor (M1) gate to source capacitance.
and T_{peak} is the filter peaking time. [1]

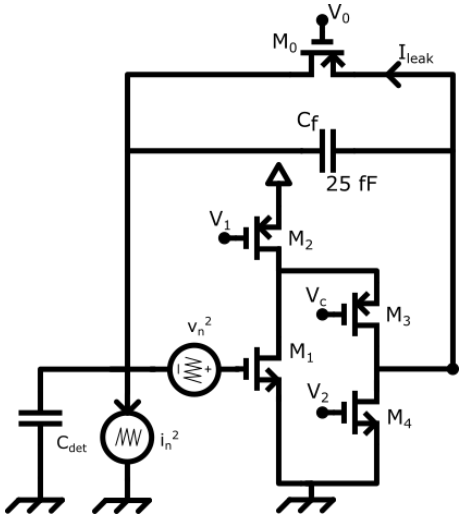

Figure A.1 – *NMOS folded cascode amplifier with noise sources*

1. The variables that I define are the same for Appendix A and B and are expressed in a Table at the end of Appendix B

II. Thermal noise optimization

Firstly, let us consider only the thermal noise contribution. We can express eq A.1 as below:

$$ENC_{th}^2 = (\frac{A_{th}\alpha_{th}^2}{T_{peak}})(C_{det} + C_{csa})^2 \tag{A.2}$$

When M1 is in the strong inversion region, we can express the input capacitance as:

$$C_{csa} = \frac{2}{3}C_{ox}(W_1 L_1) \tag{A.3}$$

Where C_{ox} is the oxide capacitance per area

The noise spectral density of the input transistor is:

$$\begin{aligned} \alpha_{th}^2 = v_{M1_{th}}^2 &= \frac{8}{3}\frac{kT}{gm_1} \\ \text{With: } gm_1 &= \sqrt{2k'_n I_d \frac{W_1}{L_1}} \end{aligned} \tag{A.4}$$

k'_n is the gain factor, technology dependant.

Considering equations A.2, A.3, and A.4 we can express the thermal equivalent noise charge as:

$$\begin{aligned} ENC_{th}^2 &= \frac{8kTA_{th}}{3T_{peak}\sqrt{2k'_n I_d}\sqrt{\frac{W_1}{L_1}}}(C_{det} + \frac{2}{3}C_{ox}W_1 L_1)^2 \\ ENC_{th}^2 &= \frac{\alpha'_{th}}{\sqrt{\frac{W_1}{L_1}}}(C_{det} + \frac{2}{3}C_{ox}W_1 L_1)^2 \end{aligned} \tag{A.5}$$

As the square function is increasing on $\mathbb{R}^+$ finding the minimum for ENC_{th}^2 will be equivalent as finding the minimum for ENC_{th}.

Considering the function, it appears that the length of our transistor L_1 only acts on the numerator. Thus we can express the minimum point of the equivalent noise charge to be verified only if L_1 is the minimum value accessible via technology. Then

we have to find the optimal for W_1.

$$\frac{\mathrm{d}ENC_{th}^2}{\mathrm{d}W_1} = 0 \text{ if and only if:}$$

$$0 = \frac{\alpha'_{th}[\frac{4}{3}C_{ox}L_1(C_{det}+\frac{2}{3}C_{ox}W_1L_1)\sqrt{\frac{W_1}{L_1}} - \frac{1}{2\sqrt{W_1L_1}}(C_{det}+\frac{2}{3}C_{ox}W_1L_1)^2]}{\frac{W_1}{L_1}} \quad \text{(A.6)}$$

$$C_{csa} = \frac{C_{det}}{3}$$

And, the thermal noise becomes:

$$\boxed{ENC_{th_{opt}} = ENC_{C_{csa}=\frac{C_{det}}{3}} = \frac{4}{3}\sqrt{\frac{8kTA_{th}}{3T_{peak}\sqrt{k'_n I_d}}}(2C_{ox})^{\frac{1}{4}}\sqrt{L_1}C_{det}^{\frac{3}{4}}} \quad \text{(A.7)}$$

We have expressed that the minimum thermal ENC is reached when $C_{csa} = \frac{C_{det}}{3}$ and its optimum value is expressed in equation A.7. Once the geometry of the input transistor is optimized, to reduce the thermal nosie, several solutions appear:

a) The first one is to increase the peaking time of the filter. Unfortunately, considering equation A.1, increasing the peaking time also increases the parallel noise. An optimum on the peaking time has to be found.

b) A second solution is to decrease the temperature. Reducing the temperature will have two effects:
• It reduces the thermal noise kT factor
• It reduces the detector leakage current (exponentially), thus parallel noise, thus allows an increase of the peaking time.

c) A third solution is to reduce the detector capacitance. Considering a fixed amount of power per area available for a spectroscopic measurement. The ENC can be expressed as $ENC_{th_{opt}} = \epsilon\frac{C_{det}^{\frac{3}{4}}}{I_d^{\frac{1}{4}}}$. Reducing the size (area) of a detection unit by a factor 2 reduces the noise by a factor $\sqrt{2}$.

d) Another solution, is to increase the bias current (Id). Increasing the current by a factor 16 decreases the noise by a factor 2.

We have assumed a transistor biased in the strong inversion region. If the power consumption is limited, transistor will be biased in weak inversion region. In this region, transconductance is no longer modified by transistor geometry. Hence, the noise is optimized with minimum dimensions. Thus, the optimum is found at the limit between strong and weak inversion region.

III. Flicker noise optimization

Now, let us consider only the flicker noise acting in equation A.1. It can be expressed as:

$$ENC_f^2 = (A_f \alpha_{1/f}^2)(C_{det} + C_{csa})^2 \tag{A.8}$$

Considering our transistor still in strong inversion we can assume equations A.3 and A.4. The flicker noise is then express as:

$$\begin{aligned} \alpha_{1/f}^2 = v_{M1_{1/f}}^2 &= \frac{K_{f_n} I_d^{AF}}{(C_{ox} L_1^2)(gm_1)^2} \\ \alpha_{1/f}^2 &= \frac{K_{f_n} I_d^{AF}}{2k'_n I_d C_{ox} W_1 L_1} \\ \alpha_{1/f}^2 &= \frac{K_{f_n} I_d^{AF-1}}{2\mu_n C_{ox}^2 W_1 L_1} \end{aligned} \tag{A.9}$$

With μ_n the channel electron mobility Considering equations A.9, A.3 we have:

$$\begin{aligned} ENC_{1/f}^2 &= \frac{A_f K_{f_n} I_d^{AF-1}}{2\mu_n C_{ox}^2 W_1 L_1} (C_{det} + \frac{2}{3} C_{ox} W_1 L_1)^2 \\ ENC_{1/f}^2 &= \frac{\alpha'_{1/f}}{L_1 W_1} (C_{det} + \frac{2}{3} C_{ox} W_1 L_1)^2 \end{aligned} \tag{A.10}$$

Considering an optimum for W_1, we can compute the derivative of the previous expression equal to zero to find the minimum point (assuming our curve to be decreasing and increasing).

$$\begin{aligned} \frac{\mathrm{d}ENC_{1/f}^2}{\mathrm{d}W1} &= 0 \text{ if and only if:} \\ 0 &= \frac{4\alpha'_{1/f} C_{ox} L_1}{3 W_1 L_1} (C_{det} + \frac{2}{3} C_{ox} W_1 L_1) - \frac{\alpha'_{1/f}}{W_1^2 L_1} (C_{det} + \frac{2}{3} C_{ox} W_1 L_1)^2 \\ C_{det} &= C_{csa} \end{aligned} \tag{A.11}$$

For this value, the equivalent noise charge becomes:

$$\boxed{ENC_{1/f_{opt}} = \sqrt{\frac{A_f 4 K_{f_n} I_d^{AF-1}}{3k'_n}} C_{det}} \tag{A.12}$$

Note that contrary to thermal noise, for flicker optimization the optimum is found on the surface of input transistor and does not require a particular value of W or L as soon as WxL is optimized. Equation A.12 shows that only few parameters allows for reduction of such a noise.
a) First of all, the current could be decreased in order to reduce flicker noise constants. However, for a majority of technology the AF coefficient is relatively low and decreasing current leads to increase thermal noise more quickly than decrease flicker noise (for X-FAB, with normal ne transistor AF is equal to 1.1).

b) Another solution is to decrease the detector capacitance.

IV. Thermal and Flicker optimization

Considering equations A.5, and A.10 we can express the noise as:

$$\begin{aligned} ENC^2 &= ENC_{1/f}^2 + ENC_{th}^2 \\ ENC^2 &= (\frac{\alpha'_{th}\sqrt{L_1}}{\sqrt{W_1}} + \frac{\alpha'_{1/f}}{W_1 L_1})(C_{det} + \frac{2}{3}C_{ox}W_1 L_1)^2 \end{aligned} \tag{A.13}$$

Thus optimizing such an equivalent noise charge returns to find the optimal point for W_1 and L_1.

$$\begin{aligned} &\frac{\mathrm{d}ENC^2}{\mathrm{d}W_1} = 0 \text{ If and only if:} \\ &\quad 0 = (-0.5.\frac{\alpha'_{th}\sqrt{L_1}}{W_1\sqrt{W_1}} - \frac{\alpha'_{1/f}}{W_1^2 L_1}).(C_{det} + \frac{2}{3}C_{ox}W_1 L_1)^2 \\ &\qquad + (\frac{\alpha'_{th}\sqrt{L_1}}{\sqrt{W_1}} + \frac{\alpha'_{1/f}}{W_1 L_1}).(\frac{4}{3}C_{ox}L_1).(C_{det} + \frac{2}{3}C_{ox}W_1 L_1) \end{aligned} \tag{A.14}$$

$$0 = -C_{ox}\alpha'_{th}L_1\sqrt{L_1}W_1^{\frac{3}{2}} - \frac{2}{3}C_{ox}\alpha'_{1/f}W_1 + \frac{\alpha'_{th}\sqrt{L_1}C_{det}}{2}W_1^{\frac{1}{2}} + \frac{\alpha'_{1/f}C_{det}}{L_1}$$

In order to solve such equation we can fix $x = \sqrt{W_1}$ leading to a 3 order polynomial expression as below:

$$-C_{ox}\alpha'_{th}L_1\sqrt{L_1}\mathbf{x^3} - \frac{2}{3}C_{ox}\alpha'_{1/f}\mathbf{x^2} + \frac{\alpha'_{th}\sqrt{L_1}C_{det}}{2}\mathbf{x} + \frac{\alpha'_{1/f}C_{det}}{L_1} = 0 \tag{A.15}$$

In order to fix the length as well, we need to solve:

$$\frac{\mathrm{d}ENC^2}{\mathrm{d}L_1} = 0 \text{ If and only if:}$$
$$0 = (0.5.\frac{\alpha'_{th}}{\sqrt{L_1}\sqrt{W_1}} - \frac{\alpha'_{1/f}}{W_1 L_1^2}).(C_{det} + \frac{2}{3}C_{ox}W_1L_1)^2$$
$$+ (\frac{\alpha'_{th}\sqrt{L_1}}{\sqrt{W_1}} + \frac{\alpha'_{1/f}}{W_1 L_1}).(C_{det} + \frac{2}{3}C_{ox}W_1L_1) \tag{A.16}$$
$$0 = \frac{5}{3}\alpha'_{th}C_{ox}\sqrt{W_1}L_1^2\sqrt{L_1} + 0.5\frac{\alpha'_{th}}{\sqrt{W_1}}C_{det}L_1\sqrt{L_1} + \frac{2}{3}C_{ox}\alpha'_{1/f}L_1 - \frac{\alpha'_{1/f}}{W_1}C_{det}$$
$$\frac{5}{3}\alpha'_{th}C_{ox}\sqrt{W_1}\mathbf{y^5} + 0.5\frac{\alpha'_{th}}{\sqrt{W_1}}C_{det}\mathbf{y^3} + \frac{2}{3}C_{ox}\alpha'_{1/f}\mathbf{y^2} - \frac{\alpha'_{1/f}}{W_1}C_{det} = 0$$

With: $y = \sqrt{L_1}$

The analytical solution of both equations leads in having different solutions in the complex plane (3 for the first one and 5 for the second one). Solving analytically these equations with different methods (as Cardan method) leads to a rather complex set of solutions, that does not allow us to derive easy to read capacitive matching such as before ($C_{csa} = C_{det}$ or $C_{csa} = \frac{1}{3}C_{det}$).

For equation A.15 the real and positive solution can be expressed as $x = \sqrt{a\frac{C_{det}}{C_{ox}L_1}}$ which is similar to $W_1 = Var.\frac{C_{det}}{C_{ox}L_1}$ and leads the equation A.15 to be equals to:

$$-Var\sqrt{Var}\frac{\alpha'_{th}C_{det}\sqrt{C_{det}}}{\sqrt{C_{ox}}} + \frac{\sqrt{Var}}{2}\frac{\alpha'_{th}C_{det}\sqrt{C_{det}}}{\sqrt{C_{ox}}} - Var\frac{2}{3}\frac{\alpha'_{1/f}C_{det}}{L_1} + \frac{\alpha'_{1/f}C_{det}}{L_1} = 0 \tag{A.17}$$

Var is a variable, which is relatively complicated to express analytically, and depends on technological parameters. However, we can emphasize two values:
If $Var = \frac{3}{2}$ flicker noise is cancelled. This is the optimum when no thermal noise is expressed ($C_{Csa} = C_{det}$).
If $Var = \frac{1}{2}$ thermal noise is cancelled. This is the optimum when no flicker noise is expressed ($C_{Csa} = \frac{1}{3}C_{det}$).

The optimum for both noises together is in between these two values depending on the technological parameters. Expressions were computed for a strong inversion region. In the case of low current and a optimum leading to high value width, the region would shift to the weak inversion and channel capacitance and transconductance would be subject to different expressions and noise optimum.

Hence the limit for optimization is relatively complex to analyse, and is strongly dependant on the technology. Proposed solution is usually to optimize the system to a thermal or flicker noise depending on the system requirement. Fine tuning the best value is done by simulation in order to correct capacitive matching. A typical model curve, expression of equation A.13 is expressed as an exampled below:

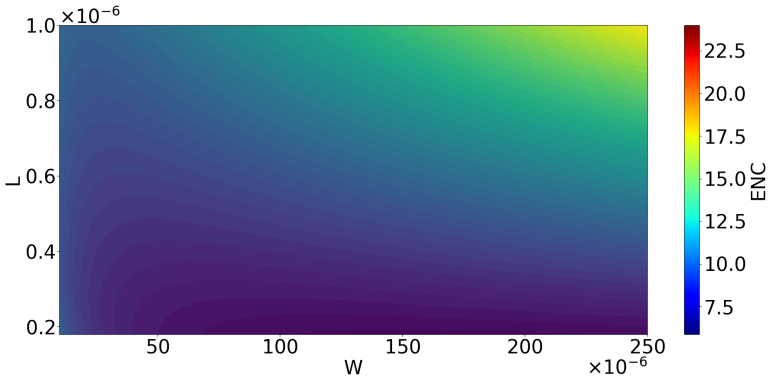

FIGURE A.2 – *ENC optimization function for both flicker and thermal noise together. Plot has been made using equation A.13 with 300 fF of detector capacitance*

V. OPTIMUM WITH PEAKING TIME

In previous optimization we did not discussed on parallel noise. We stated that different optima would exist in the case of a pure flicker or pure thermal noise. For thermal noise, we discussed quickly that increasing the peaking time of filtering stage would reduce its value. However, such increase directly worsen the parallel noise.

Considering equation A.1, an optimum for the value of peaking time can be found be derivation of the ENC in function of peaking time. This is expressed in equation A.18.

$$\begin{aligned} \frac{\mathrm{d}ENC^2}{\mathrm{d}T_{peak}} &= 0 \text{ if and only if:} \\ 0 &= -\frac{A_{th}\alpha_{th}^2}{T_{peak}^2}(C_{det}C_{csa})^2 + A_{//}\alpha_{//}^2 \\ T_{peak_{opt}} &= \sqrt{\frac{A_{th}}{A_{//}}}\alpha_{th}\frac{(C_{csa}+Cdet)}{\alpha_{//}} \end{aligned} \tag{A.18}$$

Considering the expression of $\alpha_{//} = i_p$ expressed as the addition of equation 2.13 and 2.17 giving $\alpha_{//}^2 = 2q(1+2\frac{\gamma}{n})I_{leak} = \alpha_{//}'^2 I_{leak}$ the optimum peaking time can be expressed as:

$$T_{peak_{opt}} = \sqrt{\frac{A_{th}}{A_{//}}}\frac{\alpha_{th}(C_{csa}+C_f+C_{det})}{\alpha'_{//}\sqrt{I_{leak}}} \tag{A.19}$$

At this point, the equivalent noise charge, can be expressed (in electron rms) as:

$$ENC_{opt} = \frac{1}{q}\sqrt{\begin{aligned} &2\sqrt{A_{//}A_{th}}\alpha_{th}\alpha'_{//}\sqrt{I_{leak}}(C_{Csa}+C_{det}+C_f) \\ &+ A_f\alpha_{1/f}^2(C_{Csa}+C_{det}+C_f)^2 \end{aligned}} \tag{A.20}$$

Replacing the expression on capacitance found for the different capacitive matching leads to find the optimum peaking time in relation with the optimum value for a given technology and detector.

Appendix B: CMOS Amplifier Optimization

This Appendix presents the noise optimization of a CMOS charge sensitive amplifier. This amplifier [1] is composed of two input transistors, one is a PMOS and the other one is a NMOS. I will quickly describe its architecture and then the optimization of such an amplifier and its consequences.

I. Architecture Presentation

The architecture is presented on fig B.1. The input of the charge sensitive amplifier is made of a NMOS transistor (M1) and a PMOS transistor (M2) connected together to form an inverter amplifier. Their bias current is fixed by an external voltage regulator (Reg) connected to the source of the PMOS transistor of the inverter. All other devices are similar to ones used in a classical folded cascode architecture: M3 is the NMOS cascode transistor and M4 makes the final current to voltage conversion.

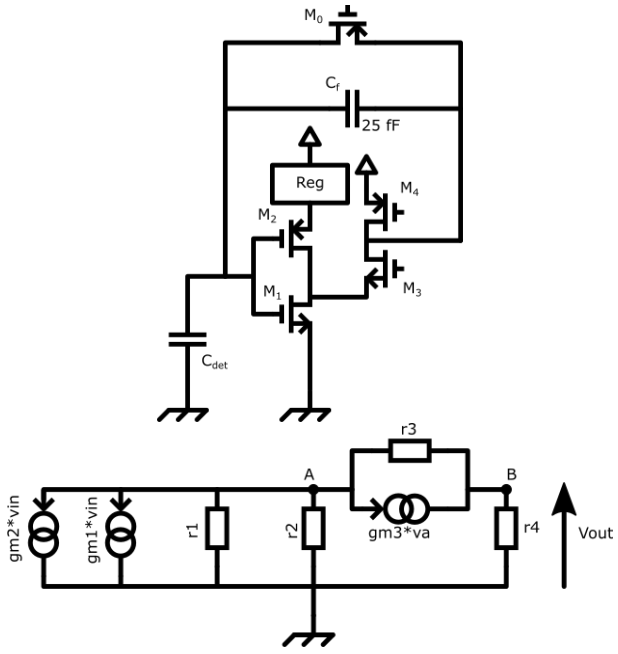

Figure B.1 – *CMOS charge sensitive amplifier schematic (top) and small signal circuit(bot)*

The open loop gain of the amplifier is:

$$\frac{v_{out}}{v_{in}} = -(gm_n + gm_p)r_4 \frac{1}{1 + \frac{(r_3+r_4)(r_2+r_1)}{(r_2 r_1)(1+gm_3 r_3)}} \tag{B.1}$$

Where gm_n is the transconductance of M1 transistor and gm_p, the transconductance of M2 transistor.

The system behaviour is close to the one expressed for NMOS input. The difference lies in the input transistors composed of one PMOS and one NMOS. In the following, I propose an optimization process to calculate the best ratio between NMOS and PMOS transistor sizes.

II. Thermal noise optimization: particularities of the CMOS preamplifier

Considering the Figure B.1 we can compute the serial noise as the square sum of two independent noise sources (one for the NMOS thermal noise and the other as the PMOS thermal noise). Thus we can consider two noise sources at the output:

$$\begin{aligned} \bar{v_{out_{th_n}}}^2 &= \bar{i_{th_n}}^2 \frac{r_4^2}{(1+\frac{(r_3+r_4)(r_2+r_1)}{(r_2r_1)(1+gm_3r_3)})^2} \\ \bar{v_{out_{th_p}}}^2 &= \bar{i_{th_p}}^2 \frac{r_4^2}{(1+\frac{(r_3+r_4)(r_2+r_1)}{(r_2r_1)(1+gm_3r_3)})^2} \end{aligned} \tag{B.2}$$

By dividing output noise by squared gain we finally have the following input noise:

$$\begin{aligned} \bar{v_{th}}^2 &= \frac{\bar{v_{out_{th_n}}}^2}{(\frac{v_{out}}{v_{in}})^2} + \frac{\bar{v_{out_{th_p}}}^2}{(\frac{v_{out}}{v_{in}})^2} \\ \bar{v_{th}}^2 &= \frac{4kT}{3}.(\frac{\Gamma_n gm_n}{(gm_n+gm_p)^2} + \frac{\Gamma_p gm_p}{(gm_n+gm_p)^2}) \\ \bar{v_{th}}^2 &= \frac{8kT}{3}.(\frac{1}{(gm_n+gm_p)}) \end{aligned} \tag{B.3}$$

Considering $\Gamma_n = \Gamma_p = \Gamma = \frac{2}{3}$.

We have expressed the thermal noise as a function of its transconductance. The expression of the transconductance depends on the bias region of the transistors. In the following sections, I calculate the noise for both transistors biased in strong inversion first and then in weak inversion.

II.1. Strong inversion region

In this region, transconductance is proportional to the square root of width over length ratio (see Appendix A). Equivalent noise charge can be expressed as follow:

$$\begin{aligned} ENC_{th}^2 &= \frac{\alpha''_{th}}{\beta_n\sqrt{\frac{W_n}{L_n}} + \beta_p\sqrt{\frac{W_p}{L_p}}}(C_{det} + \frac{2}{3}C_{ox}(W_nL_n + W_pL_p))^2 \\ \text{Where: } \alpha''_{th} &= \frac{8kTA_{th}}{3T_{peak}} \\ \beta_n &= \sqrt{2k'_nI_d} \quad \beta_p = \sqrt{2k'_pI_d} \end{aligned} \tag{B.4}$$

A_{th} is the filter constant and T_{peak} the filtering peaking time.

Considering the equation above, the length of both transistors are on the numerator part. Hence increasing length increases thermal noise. Thus we can consider in our equation a first simplification by stating $L_n = L_p = L_{min} = L$.

Fixing the ratio $a = \frac{W_p}{W_n}$ and $b = \frac{(\beta_p)^2}{(\beta_n)^2} = \frac{k'_p}{k'_n}$ and $C_{csa} = \frac{2}{3}C_{ox}(W_nL + W_pL)$ we can state:

$$C_{csa} = \frac{2}{3}C_{ox}LW_n(1+a)$$

$$\frac{1}{gm_{tot}} = \beta_n\sqrt{\frac{W_n}{L_n}} + \beta_p\sqrt{\frac{W_p}{L_p}} = \frac{L\sqrt{2C_{ox}}}{\beta_n\sqrt{3C_{csa}}}\frac{\sqrt{1+a}}{1+\sqrt{ab}} \tag{B.5}$$

$$ENC_{th}^2 = \frac{\alpha''_{th}}{gm_{tot}}(C_{det} + C_{csa})^2$$

Optimization of the thermal noise consists in finding the optimal Capacitance C_{csa} for which the thermal ENC is minimized. This can be done by setting the partial derivative to zero:

$$\begin{aligned} &\frac{\partial ENC_{th}^2}{\partial C_{csa}} = 0 \\ &\alpha''_{th}(\frac{2(C_{det} + C_{csa})}{gm_{tot}} + 2(C_{det} + C_{csa})^2\frac{\partial(\frac{1}{gm_{tot}})}{\partial C_{csa}}) = 0 \end{aligned} \tag{B.6}$$

Which leads to the following result :

$$C_{csa} = \frac{C_{det}}{3} \tag{B.7}$$

Such a result follows directly the conclusion drawn in the NMOS optimization. We can now use this result to calculate the optimal ratio between PMOS width and NMOS width. It is done by finding the extremum of ENC_{th} on the variable a.

$$\begin{aligned} \frac{\partial ENC_{th}^2}{\partial a} &= 0 \\ \alpha_{th}''(\frac{4C_{det}}{3})^2 \frac{\partial \frac{1}{gm_{tot}}}{\partial a} &= 0 \\ a &= b \end{aligned} \tag{B.8}$$

Thus, the optimum is found when the total sum of transistor dimension is equal to $\frac{C_{det}}{3}$ and when the ratio between NMOS dimension and PMOS dimension corresponds to the channel mobility ratio.

Hence, resolving the system give us the value of NMOS and PMOS width to be:

$$\begin{cases} W_n = \frac{C_{det}}{2C_{ox}L(1+b)} \\ W_p = b.W_n \end{cases} \tag{B.9}$$

At this optimum we can compute the equivalent noise charge expressed as:

$$ENC_{th_{opt}}^2 = \alpha_{th}''(\frac{4}{3}C_{det})^2 L \sqrt{\frac{C_{ox}(1+b)}{2I_d k_n' C_{det}}} \frac{1}{1+b}$$

$$ENC_{th_{opt}}^2 = \alpha_{th}''(\frac{4}{3})^2 C_{det}^{\frac{3}{2}} L \sqrt{\frac{C_{ox}}{2I_d k_n'}} \frac{1}{\sqrt{1+b}}$$

$$\boxed{ENC_{th_{opt}}^2 = ENC_{th_{opt_{NMOS}}}^2 \frac{1}{\sqrt{1+b}}} \tag{B.10}$$

Hence, this novel architecture exhibits a thermal noise $(\frac{1}{1+b})^{\frac{1}{4}}$ times better than the one obtained with the classical NMOS architecture. Such improvement is due to the increase of transconductance without surface nor bias current increase. The increase of transconductance improves also the open loop gain of the amplifier as well as with the rising time. Depending on the technology, this parameter could range between 1.07 (for AMS 0.35 μm technology) to 1.2 in the case of b = 1 (same mobility for both transistors).

II.2. Weak inversion region

In the weak inversion region transconductance is no longer an expression of transistor width but only proportional to the square root of its bias current. Hence the total transconductance gm_{tot} can be expressed as:

$$gm_{tot} = \frac{I_d}{T}.(a_n + a_p) \tag{B.11}$$

Where a_n and a_p are technology dependant coefficients.
T is the temperature in Kelvin

In weak inversion region, input capacitance is smaller than the strong inversion one for the same geometry, and dependant on the biasing as composed mainly of the channel capacitance. However, we can state the value to be around $C_{csa} = \frac{1}{2}.C_{ox}(W_nL_n + W_pL_p)$.

Considering both assumption on transconductance and capacitance, the thermal ENC can be expressed as:

$$ENC_{th}^2 = \frac{T}{(a_n + a_p)I_d}(C_{det} + \frac{1}{2}C_{ox}(W_nL_n + W_pL_p))^2 \tag{B.12}$$

The optimum would be found for a minimum $W_nL_n + W_pL_p$ provided the fact that ratio are large enough to stay in weak inversion region. Hence for relatively large detector capacitance the decrease of thermal noise is close to $\sqrt{(a_n + a_p)} \simeq \sqrt{2}$.

III. Flicker noise optimization

On the previous section, I demonstrated that CMOS configuration reduces the noise compared to a NMOS configuration. Considering the flicker noise, the optimum has to be recalculated to prove that using CMOS configuration reduces flicker noise as well.

Let us assume the previous schematic, with only M1 and M2 transistor generating flicker noise. Considering the noise as expressed in equation 2.20, and transistor acting in strong inversion region, we can state:

$$ENC_f^2 = \frac{A_f Id^{AF}}{C_{ox}} \frac{\frac{K_{fn}}{L_n^2} + \frac{K_{fp}}{L_p^2}}{(gm_n + gm_p)^2}(C_{det} + C_{csa})^2 \tag{B.13}$$

Where K_{f_n}, K_{f_p} are flicker noise parameters for NMOS and PMOS respectively
α is another flicker noise parameter common to both transistors.

This equation can be rewritten assuming a constant length $L_n = L_p = L$ and

considering $gm_x = \beta_x \sqrt{\frac{W}{L}}$, $a = \frac{W_p}{W_n}$, $b = \frac{\beta_p^2}{\beta_n^2}$, and $c = \frac{K_{fp}}{K_{fn}}$:

$$ENC_f^2 = \frac{A_f K_{f_n} Id^{AF}}{\beta_n^2 C_{ox} W_n L_n} \frac{gm_n^2 + \frac{c}{a} gm_p^2}{(gm_n + gm_p)^2} (C_{det} + C_{csa})^2 \tag{B.14}$$

Considering $W_n = \frac{3}{2} \frac{C_{csa}}{C_{ox} L_n (1+a)}$:

$$ENC_f^2 = \frac{Id^{AF} A_f K_{f_n}}{\beta_n^2} \frac{2}{3} \frac{(1+a)(1+cb)}{C_{csa}(1+\sqrt{ab})^2} (C_{det} + C_{csa})^2 \tag{B.15}$$

Solving the partial derivative with C_{csa} leads to an optimal point as:

$$C_{det} = C_{csa} \tag{B.16}$$

Solving the partial derivative with a leads to a ratio between NMOS and PMOS:

$$a = b \tag{B.17}$$

Note that we found the same optimal geometrical ratio between NMOS and PMOS for thermal and flicker noise optimization.

At this point the equivalent noise charge is equal to :

$$ENC_{f_{opt}}^2 = \frac{8 Id^{AF} A_f K_{f_n} C_{det}}{3\beta_n^2} \left(\frac{1+cb}{1+b}\right) = ENC_{f_{opt_{NMOS}}}^2 \left(\frac{1+cb}{1+b}\right) \tag{B.18}$$

Considering the ratio c as the ratio between PMOS and NMOS flicker noise factors, it can be seen that flicker noise is better with the CMOS configuration. Such assumption is relatively straightforward, adding a PMOS transistor would reduce the flicker noise.

Comparing to the flicker noise expression of a PMOS configuration alone, the equivalent noise floor can be expressed as:

$$\boxed{ENC_{f_{opt}}^2 = ENC_{f_{opt_{PMOS}}}^2 \left(\frac{b}{c}\right)\left(\frac{1+cb}{1+b}\right)} \tag{B.19}$$

The last equation can be interpreted as the fact of increasing transconductance by introducing a NMOS transistor decreases the noise if and only if this increase is larger than the flicker noise factor introduced by the NMOS. Or, if the mobility ratio is larger than the noise factor ratio.

IV. Conclusion

Expression on optimization for both flicker noise and thermal noise in strong inversion region has been expressed by equation B.18 and B.10. We can summarize these results by presenting a table which compares noise factors in front of the three different architectures as below.

Table B.1 – *Comparison of three architecture (NMOS input, PMOS input, CMOS input)*

ENC ratio	NMOS	PMOS	CMOS
Flicker	$\sqrt{\frac{b}{c}}$	1	$\sqrt{\frac{b}{c}} \cdot \sqrt{\frac{1+cb}{1+b}}$
Thermal	1	$(\frac{1}{b})^{\frac{1}{4}}$	$\frac{1}{(1+b)^{\frac{1}{4}}}$

For more relatable results, I have applied the table to the AMS 0.35μm technology (used in IDeF-X HDBD). In this technology, we have b=0.34 and c=0.28. I have renormalized (1 for PMOS flicker noise and 1 for NMOS thermal noise) to compare more accurately the gain of using a CMOS architecture compared to NMOS and PMOS.

Table B.2 – *Comparison of three architecture (NMOS input, PMOS input, CMOS input) for AMS 0.35 µm technology with Ibias=10 µA*

ENC ratio	NMOS	PMOS	CMOS
Flicker	1.1	1	0.95
Thermal	1	1.3	0.93

To conclude, we have the proof here, for strong inversion region, that the CMOS architecture exhibits a smaller noise (at least for AMS 0.35 μm technology). For other technologies, a trend can be found. The smaller the node is, the less difference there are between NMOS and PMOS mobilities, leading in a b factor closer to 1 [2]. Hence it appears promising using such architecture with even smaller node than the numerical application stated here.

TABLE B.3 – *Glossary of defined variables*

Designation	Value	Unit [1]
Appendix A		
α'_{th}	$\frac{8kTA_{th}}{3T_{peak}\sqrt{2k'_n I_d}}$	$Q^2.F^{-2}$
k'_n	$\mu_n C_{ox}$	$A.V^{-2}$
$\alpha'_{1/f}$	$\frac{A_f K_{f_n} I_d^{AF-1}}{2\mu_n C_{ox}^2}$	$Q^2.m^2.F^{-2}$
$\alpha'_{//}$	$2q(1+2\frac{\gamma}{n})$	$Q^{-1/2}$
Appendix B		
gm_n	gm_1	$A.V^{-1}$
gm_p	gm_2	$A.V^{-1}$
W_n/L_n	W_1/L_1	m
α''_{th}	$\frac{8kTA_{th}}{3T_{peak}}$	$Q^2.F^{-1}.s^{-1}$
β_n	$\sqrt{2k'_n I_d}$	$A.V^{-1}$
β_p	$\sqrt{2k'_p I_d}$	$A.V^{-1}$
a	$\frac{W_p}{W_n}$	
b	$\frac{\beta_p^2}{\beta_n^2} = \frac{k'_p}{k'_n}$	$A.V^{-1}$
gm_{tot}	$gm_n + gm_p$	$A.V^{-1}$

1. Unit are not given in Standard International to help comprehension

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Résumé en Français

Chapitre 1: Spectro-imagerie en X Durs

L'astronomie en rayon X-durs est une branche de l'astrophysique qui vise à regarder les phénomènes les plus violents de l'univers, souvent liés aux dernières étapes de l'évolution des étoiles.

L'atmosphère terrestre est opaque au rayonnement X. Par conséquence, l'observation du ciel en hautes énergies à réellement commencé dans la fin des années 60, avec l'avènement de la conquête spatiale et le développement de satellites scientifiques.

Le développement d'instruments en X-durs est très important notamment pour l'observation de sources célestes faiblement lumineuses et d'événements fugaces. Dans cette thèse, j'illustre cela par l'exigeant cas scientifique de l'étude de la création d'éléments lourds durant l'explosion de supernovae de type Ia.

Les instruments utilisés de nos jours comme *INTEGRAL*, *NUSTAR*, ou *HITOMI*, manquent de sensibilité pour accéder à une complète détection et mesure d'explosion de supernovae Ia au delà de notre galaxie. Afin de combler ce manque, des progrès constants ont été faits, à la fois dans l'optique focalisante, mais aussi dans les détecteurs dans le plan focal. Mon travail anticipe les défis posés au niveau du détecteur afin d'en améliorer ses performances spatiales et spectrales.

I. Principaux défis scientifiques en X-durs

I.1. Supernovæ thermonucléaire

Durant toute sa durée de vie, un étoile consomme de l'hydrogène, créant de la chaleur et des composés lourds par réactions de fusion nucléaire. Lorsque l'hydrogène se raréfie, les réactions de fusion ne peuvent plus être maintenues, et l'étoile sort de sa séquence nominale.

Si l'étoile est de faible masse (< 4 fois la masse du soleil), elle se dilate pour faire fusionner les composés externes à son noyau. Cette phase d'expansion est la phase de géante rouge. A un certain point, le combustible de la fusion nucléaire est épuisé, laissant place à une nébuleuse planétaire et une naine blanche en son centre.

Si deux étoiles sont à proximité, la matière de l'étoile encore dans sa séquence nominale est attirée par la naine blanche. Lorsque la naine blanche atteint la limite de Chandrasekhar (1.4 masse solaire), une explosion disperse des atomes lourds à haute vitesse dans le milieu interstellaire. Ce procédé est appelé supernova thermonucléaire ou supernova type Ia (SN Ia).

I.2. Construisons notre télescope

Afin d'observer l'émission d'une telle supernova, et spécifiquement étudier la physique d'effondrement de la naine blanche, il est nécessaire d'observer les rayons X

durs émient par la décroissance du ^{56}Ni. Les instruments existants sont limités notamment dans leurs sensibilité pour donner une vue précise de ce type de phénomène même lorsqu'il arrive dans notre galaxie. Le projet PHEMTO, propose la construction d'un instrument permettant l'étude d'un tel événement fixant les caractéristiques nécessaires:

TABLE 1.1 – *besoin scientifique du projet PHEMTO*

Paramètre	Valeur	Unité
Bande d'énergie	1 - 200	keV
Sensibilité en ligne	$1.8 \cdot 10^{-7}$ à 158 keV	$cts.cm^{-2}.s^{-1}$
Polarisation détectable	1	%
Résolution angulaire	1	" (HEW)
Résolution spectrale	1 à 100 keV	keV (FWHM)
Champs de vue	6 x 6	$arcmin^2$
Distance focale	100	m

Ces besoins fixent les performances souhaitées par un détecteur afin de pouvoir étudier un tel cas scientifique.

II. PRINCIPE DE DÉTECTION

II.1. Interaction lumière-matière

Je me limiterai dans le cadre de cette thèse portant sur les rayons X-durs aux détecteurs semi-conducteurs (Si, CdTe, Ge, ...).

Dans ce cadre, le phénomène prépondérant est l'absorption photo-électrique qui correspond à l'interaction d'un photon avec un électron du noyau du médium utilisé.

En moyenne, le passage d'un photon absorbé, créer un nombre de pairs électrons-trous proportionnel à l'énergie de départ du photon. Cela peut être considéré au travers de l'équation ci-dessous:

$$N_{pair} = \frac{E_\phi}{w} \tag{1.1}$$

Où w est l'énergie d'ionisation (4.42 pour le CdTe).

Le choix du CdTe vient alors des besoins de sensibilité détaillés précédemment. Plus le cristal est dense, plus l'efficacité du détecteur sera grande et donc plus celui-ci sera sensible.

II.2. Création du Signal

Un détecteur peut-être schématiquement illustré figure 1.1. Un cristal semi-conducteur est soumis à un champ électrique ϵ entre ses deux électrodes. Lorsque les paires électrons-trous sont générées par le passage d'un photon, les électrons sont attirés vers l'anode de fort potentiel, alors que les trous sont attirés vers la cathode. Ce mouvement de porteur de charges génère un courant qui dure jusqu'à ce que les porteurs de charge

aient atteint leurs anodes respectives ou aient été piégés ou recombinés par des défauts du cristal.

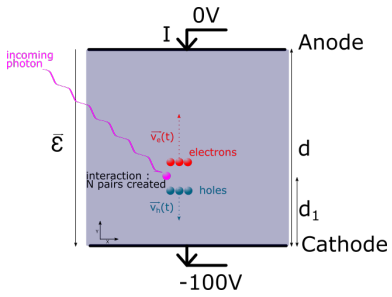

FIGURE 1.1 – *Schéma d'un détecteur plan monopixel*

Le signal de sortie du détecteur est donc une charge proportionnelle à l'énergie du photon incident. Pour pouvoir localiser l'interaction, l'utilisation d'électrodes pixelisées devient nécessaire, imposant ainsi la nécessité de circuit de lecture de faible tailles.

III. TENDANCE POUR LES FUTURES SPECTRO-IMAGEURS

Afin d'atteindre les objectifs donnés, ma thèse se focalise sur le développement d'un circuit de lecture pour CdTe spécifié table 1.2.

TABLE 1.2 – *Caractéristiques du détecteur choisit*

Caractéristique	Valeur
Semi-conducteur	CdTe
Contact	Schottky (Al)
Température de fonctionnement	253 K
Côté exposé	Cathode
Épaisseur	750 μm
Tension de dérive	-250 V
Taille de pixel	250 x 250 μm^2
Capacité	200 fF
Courant de fuite	400 fA

Chapitre 2: Chaine d'acquisition pour la spectro-imagerie

Le signal en sortie de détecteur doit être mesuré par un système de lecture afin de permettre de connaitre l'énergie du photon en question et sa position d'interaction.

Il est donc nécessaire de développer un circuit de mesure permettant de convertir cette charge en une valeur utilisable, comme une tension par exemple. Ce circuit doit suivre la segmentation et la taille du détecteur en question. Dans notre cas, le détecteur étant pixélisé, le circuit de lecture doit l'être de même.

La capacité d'interconnexion limitant les performances spectrales, elle doit être minimisée à quelque centaines de femtofarad. Pour cela, on relie le système de lecture au plus près du détecteur.

Cette dernière spécificité justifie le développement d'un circuit spécifique qui permet la mesure de charge pour la même surface qu'une unité de détection visée à 250 x 250 μm^2. Un tel circuit ne peut pas être développé avec des composant discret, d'où le sujet de cette thèse portant sur le développement d'un circuit intégré ASIC fortement pixélisé.

I. Description d'une chaine de mesure

L'architecture d'une chaine d'acquisition permettant la mesure de charge généralement utilisée peut être résumée dans la figure 2.1

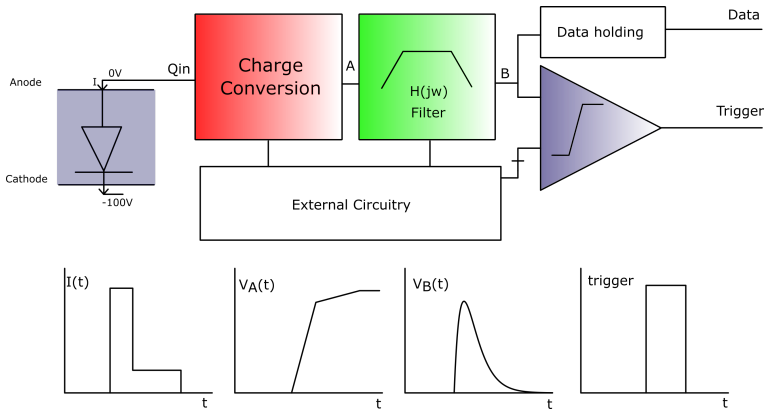

Figure 2.1 – *Schéma d'une chaine de mesure de charge typique (haut) et les signaux importants (bas)*

Le premier étage converti la charge en tension. Ce bloc peut être exprimé comme une capacité équivalent convertissant la charge en une tension.

Un deuxième étage traite le signal pour en augmenter son rapport signal à bruit.

En fonction de l'application, le signal doit être lu entièrement ou seulement la valeur maximale image de la charge reçue est suffisante. Ainsi, en fonction du besoin on peut utiliser un convertisseur analogique numérique, une mémoire analogique, un détecteur de pic, ou un circuit de mesure de temps au dessus d'un seuil (Tot).

II. La conversion de charge

Pour convertir la charge on utilise un amplificateur de charge (CSA), utilisant l'effet Miller illustré figure 2.2.

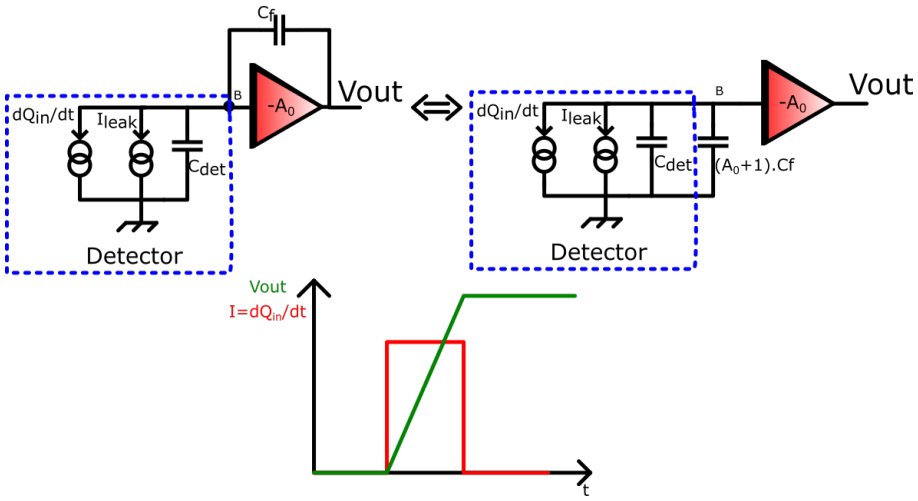

Figure 2.2 – *Illustration de l'effet Miller dans un CSA*

Si on considère un amplificateur de gain $-A_0$, et un échelon de charge, on peut calculer la réponse transitoire en passant par la fonction de transfert et sa transformée inverse:

$$V_{out_{Csa}}(t) = \frac{Q_{in}}{(C_f + \frac{C_{in}}{A_0})}\theta(t) \simeq \frac{Q_{in}}{C_f}\theta(t) \tag{2.1}$$

Où $\theta(t)$ est la fonction d'Heaviside et C_{in} représente la capacité d'entrée totale (composée de la capacité détecteur, de l'interconnexion et de la capacité d'entrée du CSA).

On remarque que pour garder toutes les fonctions d'un CSA, $C_f A_0$ doit être plus grand que C_{in} afin de garder un insensibilité à la capacité détecteur.

La conversion de charge nécessite un amplificateur de tension qui va avoir un bruit intrinsèque limitant les performances du signal.

Usuellement, nous représentons le bruit dans un système de détection de charge comme étant un bruit équivalent en entrée exprimé en charge comme ci-dessous:

$$ENC = Q_{in} \frac{\sqrt{\frac{1}{\pi} \int_0^\infty v_{noise_{Out}}(j\omega)^2 \, \mathrm{d}\omega}}{V_{Out_{Max}}} \tag{2.2}$$

Où $V_{Out_{Max}}$ représente la tension de sortie maximum pour une charge d'entrée Q_{in}.

En fonction de la position d'une source de bruit dans le système, son comportement est différent. On peut considérer deux sortes de bruit: • **Le bruit parallèle i_{p_i}:** contribution considérée comme un bruit en courant en entrée (exemple: le bruit de reset)

• **Le bruit série v_s:** contribution considérée comme un bruit en tension en entrée (exemple: le bruit thermique du transistor d'entrée).

On obtient alors le schéma figure 2.3.

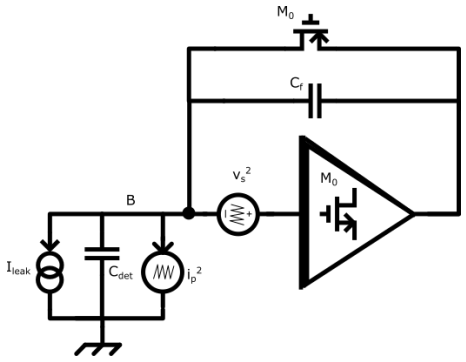

FIGURE 2.3 – *Amplificateur de charge avec ses sources de bruit utilisé pour le modèle.*

L'étude d'un tel schéma permet alors d'optimiser la conception de l'amplificateur pour réduire ses composantes de bruit (bruit de grenaille du détecteur, bruit thermique des transistors, bruit de scintillation des transistors,...).

III. Filtrer le signal

Le filtre permet d'adapter la bande passante de la chaine pour augmenter le rapport signal à bruit. Plusieurs architectures de filtres existent. Tous essaient de se rapprocher du filtrage idéal exprimé par Turin et par Gatti, nommé cusp.

Après filtrage, l'ENC peut se réécrire comme dans l'équation 2.3 donnant la courbe 2.23.

$$ENC = \sqrt{\frac{1}{q^2}\left(\frac{A_{th}\alpha_{th}^2}{T_{peak}} + A_f \alpha_{1/f}^2\right)(C_f + C_{in})^2 + \frac{1}{q^2} A_{//} \alpha_{//}^2 T_{peak}} \tag{2.3}$$

Avec: α_{th}^2, $\alpha_{//}^2$, et $\alpha_{1/f}^2$ les coefficients des différentes sources de bruit.

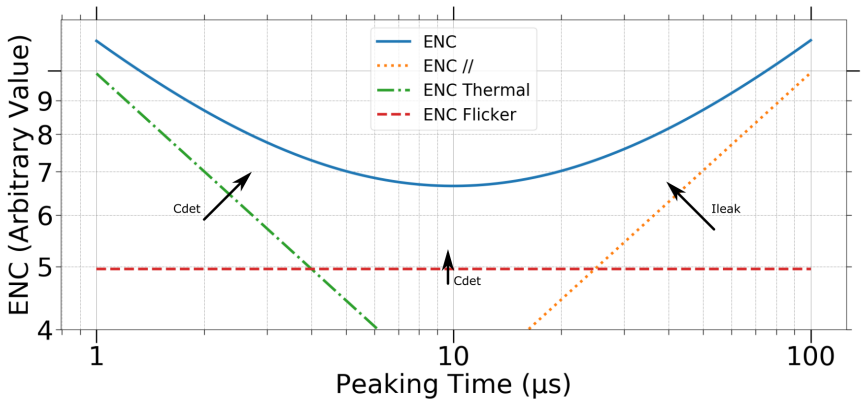

FIGURE 2.4 – *ENC en fonction du temps de peaking en valeur arbitraire.*

IV. ASICs POUR LA SPECTRO-IMAGERIE EN RAYON X DURS

Durant les dernières années, la multiplication des applications a poussé le développement de nombreux ASICs pour lire les détecteur sur la gamme d'énergie des X durs. Ici, je propose une brève comparaison de ces ASICs.

TABLE 2.1 – *ASIC pour la spectro-imagerie X*

Nom	**Agencement**	**Taille de pixel**	**Nombre de Pixel**	**ENC planché (el.rms)**	**Puissance (W/cm^2)**	**Bande d'énergie (kel)**
HEXITEC	2D	250 x 250 μm^2	80 x 80	20	NA	0.9 - 45
Timepix3	2D	**55 x 55 μm^2**	**256 x 256**	60 (ToT)	1	0.3 - 30
CAMEX	1D pnCCD	75 μm	128	2.5	0.32	0.09 - 7
D2R1	2D	300 x 300 μm^2	16 x 16	29	0.3	0.5 - 56
IDeF-X HD	1D	150 μm	32	33	0.13	0.45 - 223
AGIPD	2D	200 x 200 μm^2	64 x 64	322	NA	0.8 - 5
H02	2D	200 x 200 μm^2	32 x 32	300	0.28	2.3 - 20
VEGA	1D	200 x 500 μm^2	32	12	0.42	0.05 - 16.7
VATA451	1D	NA	64	30	NA	-10 - 10
XRS Asic	1D	350 x 2000 μm^2	16	**7**	**0.015**	0.04 - 2.8
NuASIC	2D	600 x 600 μm^2	32 x 32	50	0.13	0.2 - 30
DANA-3	2D	500 x 500 μm^2	16 x 16	200	0.08	2 - 340
VIP-PIX	2D	700 x 800 μm^2	10 x 10	98	0.04	**-438 - 438**

Chapitre 3: Conception préliminaires

Dans les premiers chapitres, nous avons montré le besoin de nouveaux systèmes de détection pour les mesures dans la gamme des rayons X durs composés de détecteur CdTe couplé à des circuit intégrés bas bruit. Dans le but d'optimiser la conception d'un tel ASIC, il est nécessaire de fixer certains paramètres. Premièrement, le choix de la technologie microélectronique (taille de grille et fabricant), ensuite la faisabilité de l'hybridation CdTe / ASIC, et enfin les choix d'architecture.

Le choix de la technologie a été fait avant le début de mon projet de thèse, comme étant un compromis entre les performances aux radiations, le prix, et la densité. Le nœud choisit est le 180 nm. Deux prototypes ont alors été fabriqués dans deux technologies différentes AMS et XFAB pour comparer les performances.

Pour évaluer la faisabilité de l'hybridation entre le détecteur et l'ASIC, une puce nommée D2R1 a été produite en XFAB 0.18 μm.

Enfin, j'ai développé et testé un nouvel ASIC dans la technologie AMS 0.35 μm nommé IDeF-X HDBD dans le but de me familiariser avec les architectures bas bruit et de valider des détails de conception avant la conception de l'ASIC matriciel final, sujet de cette thèse.

L' ASIC, nommé IDeF-X D^2R_2, résulte alors des choix et développement exprimés tout au long de ce chapitre et sera détaillé dans le chapitre 4.

I. Les puces Caterpillar, pour qualifier les technologies aux radiations

Les circuits intégrés fonctionnant dans l'espace, subissent des dégâts dus aux radiations. Ces dégâts peuvent soit endommager de manière définitive l'ASIC (Latchup, Dose), soit modifier le comportement des parties logiques (modification des registres).

Je me suis concentré sur les dégâts dus aux particules ionisantes modifiant le comportement appelés dégâts de dose, particuliers pour chaque technologie. Pour cela, j'ai testé deux technologies AMS 0.18μm et XFAB 0.18μm aux moyens de puces appelées "Caterpillar".

I.1. Descriptions des puces Caterpillar

Les puces Caterpillar comportent plusieurs CSA avec différentes tailles et types de transistor d'entrée pour pouvoir regarder l'optimisation de ce dernier.

Chaque cellule de base est un CSA de type cascode replié avec une capacité de contre-réaction de 25 fF et un transistor de reset de type PMOS.

I.2. Résultats

Les résultats de mesures viennent de deux campagnes de test différentes. J'ai personnellement testé la technologie AMS 0.18 μm. Dans les deux cas, le système de mesure était le même.

Tout le système a été irradié à deux périodes différentes en utilisant la même source gamma de ^{60}Co avec une activité de 60 GBq qui simule l'interaction de rayons cosmiques. Les résultats sont exprimés figure 3.1, et 3.2.

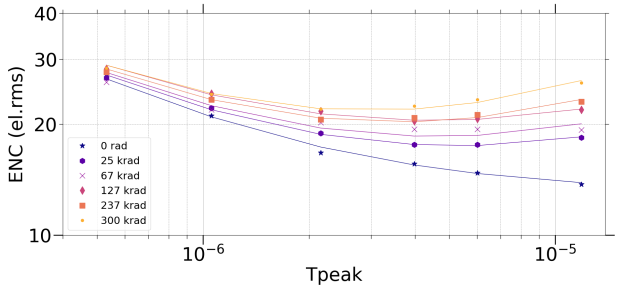

FIGURE 3.1 – *Variation de L'ENC en fonction des radiations pour Caterpillar AMS.*

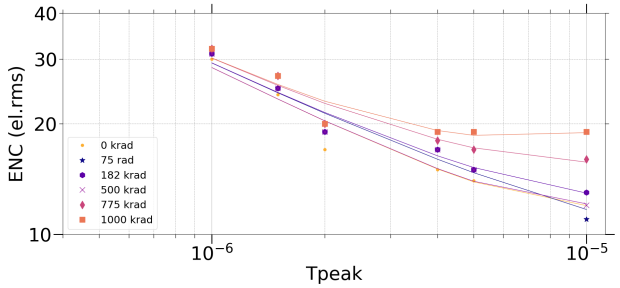

FIGURE 3.2 – *Variation de L'ENC en fonction des radiations pour Caterpillar XFAB.*

I.2.a. Comparaison

Pour les deux ASICs, le bruit parallèle augmente avec la dose accumulée. A la même dose de 300 krad, le bruit augmente de 20 % pour XFAB et de 86 % pour AMS.

Au vu des résultats, j'ai décidé de choisir la technologie XFAB 0.18 μm notamment car au moment du début de ma thèse, l'interconnexion entre le détecteur et l'ASIC avait été validée. De plus, un transistor bas bruit a été ajouté en 2017, ce qui m'a motivé à développer dans cette technologie pour pouvoir atteindre des performances plus spectaculaires.

II. D^2R_1: UNE MATRICE POUR L'INTERCONNEXION DIRECTE AU DÉTECTEUR

Pour tester l'interconnexion au détecteur et les performances spectroscopiques de l'assemblage, une puce a été développée dans la technologie XFAB 0.18 μm. Une complète description d'une telle puce se trouve dans la thèse de Mme Michalowska. Le détecteur quand à lui est décrit avec précision dans celles de Bob Dirks et Sebastien Dubos. D^2R_1 est une matrice de 16 x 16 pixels de chacun 300 x 300 μm^2. Chaque pixel est composé d'une chaine spectroscopique complète. La consommation totale est de 81 mW (315 μ/Pixel).

Un détecteur a été interconnecté à l'ASIC (voir figure 3.3) et des mesures ont été faites aux moyens de deux sources X, l'^{241}Am et le ^{57}Co. L'interconnexion à été faite grâce au procédé "d'indium gold stud bump bonding" de la JAXA/HMI.

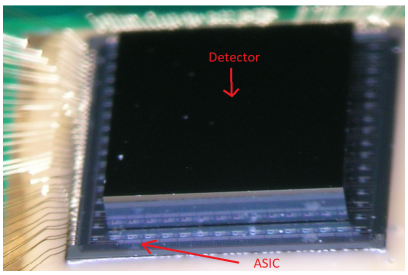

FIGURE 3.3 – *Photo de D^2R_1 (en bas) et le détecteur Schottky (en haut)*

Les résultats sont alors montrés figure 3.4.

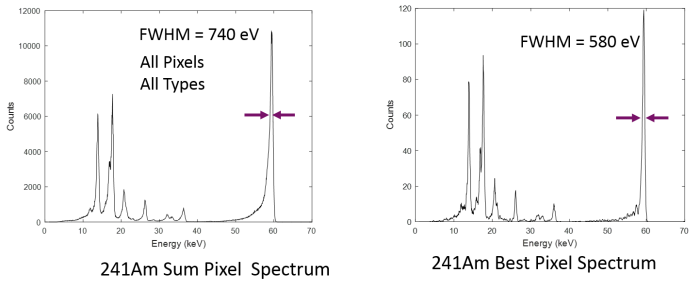

FIGURE 3.4 – *Spectre de la source d'^{241}Am effectué à -6°C. A gauche les spectres sommés des pixels, à droite le spectre du meilleur pixel*

Le meilleur pixel a une résolution de 580 eV FWHM à 60 keV ce qui correspond à la valeur prévue. En prenant en compte tous les pixels, la résolution est de 740 eV soit un ENC de 55 el.rms, bien plus élevé, et due essentiellement aux évènements où l'interaction est partagé entre plusieurs pixel, qui partagent alors leurs bruit.

III. IDeF-X HDBD: un ASIC bidirectionnel bas bruit

IDeF-X HDBD est un système de mesure de charge de 32 canaux basé sur un ASIC précédent nommé IDeF-X HD. J'ai développé cet ASIC de m'accoutumer à l'architecture à reset continue, de réduire d'un facteur deux le bruit, et de développer de nouveaux concepts dont je pourrais me servir dans la puce D^2R_2.

III.1. Description du canal

La figure 3.5 montre le schéma d'un canal de l'ASIC. Afin de permettre la bidirectionalité, deux reset NMOS et PMOS peuvent être sélectionné.

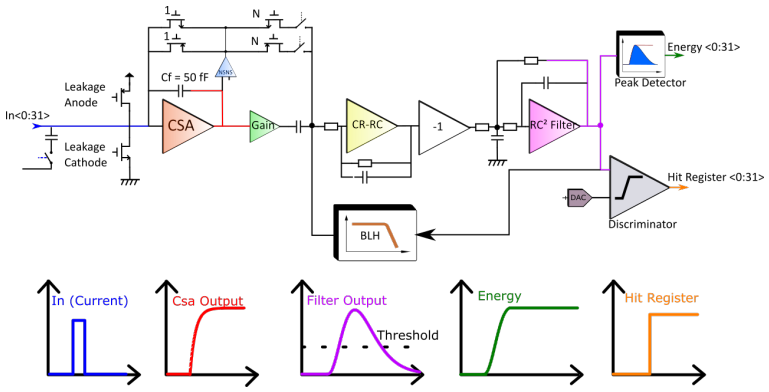

FIGURE 3.5 – *Architecture du canal d'IDeF-X HDBD*

III.2. Résultats des tests électriques

IDeF-X HDBD a été reçu en Aout 2018, nous avons développé une carte fille permettant d'accueillir l'ASIC et les composants passifs et utilisé le banc de test de l'ASIC IDeF-X HD. Les résultats montrés ci-dessous ont été effectué via une injection d'échelon de tension, à la manière des tests effectués avec D^2R_1.

Plusieurs paramètres ont été extraits de ces mesures. En effectuant pour chaque charge 1000 évènements, nous avons pu tester avec une statistique significative les performances du circuit.

La figure 3.6 montre les mesures d'un canal typique (canal numéro 15) à une variation de charge.

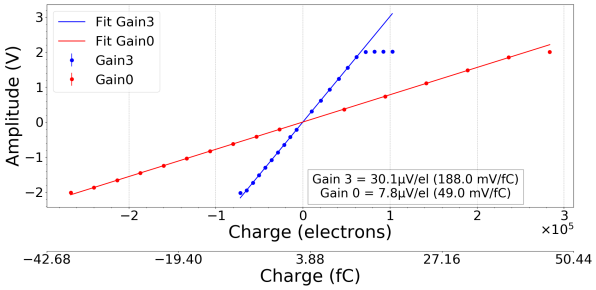

FIGURE 3.6 – *Variation d'amplitude pour les deux modes de gain de l'ASIC (gain 1 et gain 4) dans les deux modes de polarité, anodes et cathode.*

L'INL maximum pour le mode cathode est de 0.09% un peu supérieur au 0.07% du mode anode, essentiellement du à l'inverseur.

l'ENC a été calculée avec les même valeurs que montrées précédemment, considérant la déviation standard du maximum de la valeur de sortie de filtre. Ces mesures ont été faites pour chaque canal en mode anode.

La valeur moyenne de bruit est de 17.3 el.rms avec une déviation standard entre canaux de 1.6 el.rms.

III.3. Résultats des tests spectroscopiques

Grâce au groupe de travail de INAF Rome, deux ASICs ont été reliés à un détecteur Silicon Drift Detector (SDD) montré figure 3.7.

Un pixel a été relié à un pad de l'ASIC, et j'ai testé le système avec une source radioactive d'^{241}Am. La calibration et l'extrapolation ont été faites sur les raies faibles énergies autour de 14 keV.

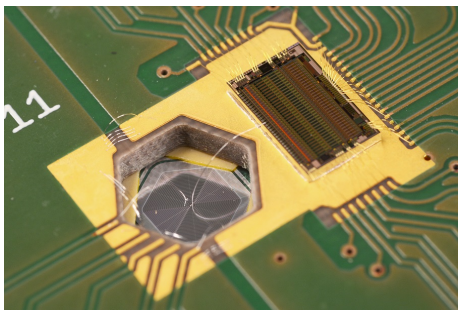

FIGURE 3.7 – *Photo d'HDBD (à gauche) connecté au SDD (à droite). Le détecteur est composé d'un pixel de 11 mm de diamètre, de 450 µm d'épaisseur et polarisé à 110 V.*

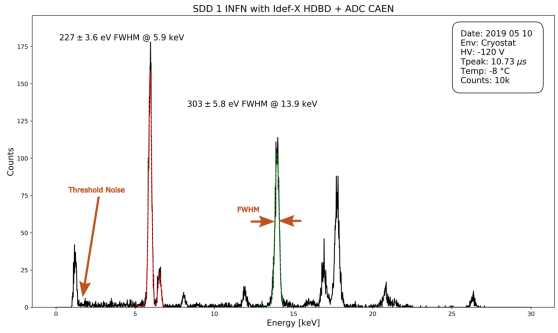

FIGURE 3.8 – *Superposition de source d'^{241}Am et de ^{55}Fe sur le système refroidit à -8 °C. la courbe rouge correspond aux deux raies de Fer K_α et K_β à respectivement 5.9 et 6.4 keV. La courbe verte correspond à la raie L_α de l'^{241}Am à 13.9 keV.*

Les résultats illustrés figure 3.8 montrent une résolution spectrale de 303 eV FWHM à 14 keV. En supprimant la composante de bruit Fano, cela revient à un bruit de l'ASIC de 28 el.rms. Avec le modèle de bruit, j'estime le détecteur ayant un courant de fuite de 1.5 pA et une capacité d'interconnexion de 500 fF. De telles valeurs sont proches de celles qui peuvent être attendues.

Chapitre 4: D^2R_2: Un circuit intégré haute résolution spatiale et spectrale

J'ai mis l'accent sur les différents défis dans l'optimisation des performances des ASICS (protection contre les radiations, bas bruit, interconnexion,...).

Dans le chapitre 1, j'ai montré le besoin d'un capteur à base de CdTe fortement segmenté et ai pris pour objectif raisonnable des pixels de 250 x 250 μm^2. J'y ai mentionné la nécessité de développer un circuit intégré spécifique pour lire un tel détecteur et y ai mentionné la volonté de baisser le bruit en dessous des 20 el.rms. Durant mon travail de thèse, j'ai développé une puce bidimensionnelle nommée IDeF-X d^2R_2 signifiant "Imaging Detector Front-end in X-rays Dimension 2 Revision 2". Ce circuit consiste en une matrice de 32 x 32 pixels conçue dans la technologie X-FAB 0.18 μm, optimisée pour la lecture d'un détecteur lui aussi pixelisé de 32 x 32 pixels avec pour objectif d'avoir une haute résolution spatiale et spectrale.

D^2R_2 est le successeur de D2R1 avec quatre fois plus de pixels, une meilleur résolution spatiale, et une architecture totalement différente. Celle-ci ressemble plus à l'architecture de IDeF-X HDBD mentionnée dans le chapitre 3, tout en tenant en compte la forte contrainte surfacique.

I. Vue globale de l'ASIC et du banc de test

I.1. Architecture général

L'ASIC IDeF-X D^2R_2 a été fabriqué dans la technologie XFAB XH018 avec les options MIM / ULN / METMID. J'ai reçu trois wafers de 200 mm avec chacun 280 puces. J'ai fait découpé l'un des wafer pour tester la fonctionnalité et les performances du prototype. Celui-ci a été connecté à une carte fille PCB que j'ai développé spécialement pour la lecture de l'ASIC. La figure 4.1 montre un tel assemblage.

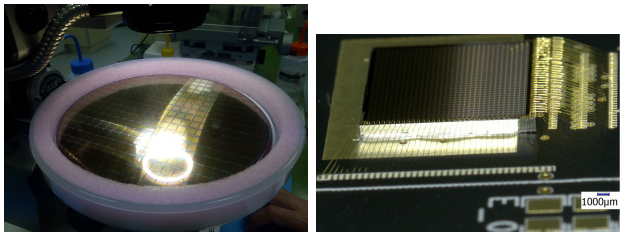

Figure 4.1 – *Photo d'un wafer de puces D^2R_2(à gauche), et photo de l'assemblage de la puce sur le PCB(à droite).*

L'architecture générale de la matrice IDeF-X D^2R_2 est montrée dans la figure 4.2

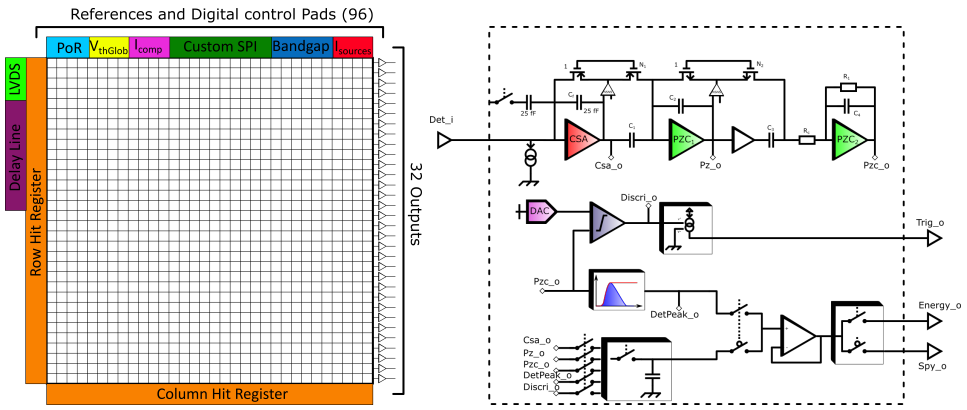

FIGURE 4.2 – *Vue schématique générale de la matrice D^2R_2 à gauche et du pixel (à droite).*

L'architecture de chacun des pixel est basée sur l'architecture mentionnée dans le chapitre 3 pour IDeF-X HDBD. La principale différence viens de la suppression de zéros faite en deux temps pour optimiser la surface.

II. CSA

II.1. Architecture

L'architecture du CSA est composé d'un amplificateur de charge de type cascode replié avec un transistor d'entré NMOS, une contre-réaction capacitive de 25 fF et une contre-réaction résistive faite d'un PMOS en faible inversion.

L'optimisation numérique (voir figure 4.3) en plus de l'optimisation analogique a permit de fixer la taille du transistor d'entrée de W = 90 μm et L = 180 nm. Le bruit simulé est alors de 11 el.rms à 4 μs de temps de pic.

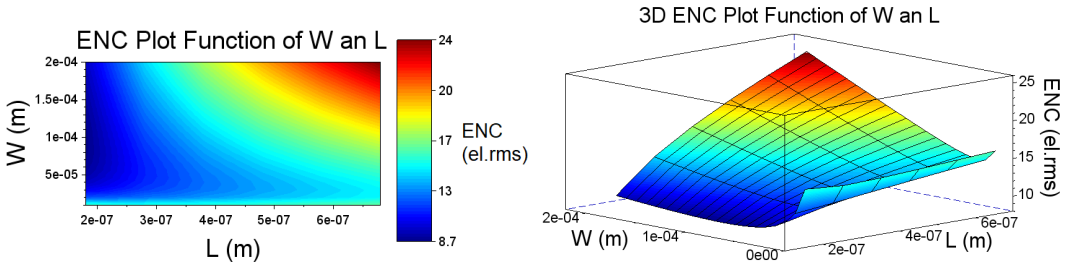

FIGURE 4.3 – *Courbe d'ENC pour un temps de pic de 4 µs avec un filtre CR-RC idéal pour différentes largeurs et longueurs de grille du transistor d'entrée.*

II.2. Resultats de mesure

L'ASIC permet de multiplexer directement la sortie de CSA des pixels. J'ai donc mesuré le signal en sortie de CSA, en le faisant passer par des filtres $CR - RC^2$ et $CR - RC$ externes. le résultats des mesures de bruit sont donnés figure 4.4.

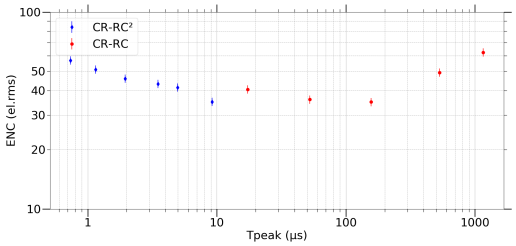

FIGURE 4.4 – *ENC fonction du temps de pic pour le pixel (0,31). Le courant dans le CSA est de 9 µA dans sa branche d'entrée et 1 µA dans sa branche de sortie.*

On remarque un excès de bruit 4 fois plus grand que prévu.

J'ai étudié la variation de bruit avec la capacité d'entrée et le courant de polarisation, il apparait que le bruit de scintillation soit mal modélisé.

III. SUPPRESSEUR DE BRUIT NON STATIONNAIRE (NSNS)

III.1. Conception

Lorsqu'une charge est intégrée, le transistor de reset subit une augmentation de sa tension de source, son bruit va donc lui aussi augmenter.

Pour empêcher cela, l'idée est de faire suivre au CSA un filtre passe bas appelé NSNS explicité figure 4.5. On peut avoir une constante de temps faite par la résistance R suffisamment grande pour éviter toute oscillation et réduire le bruit non stationnaire.

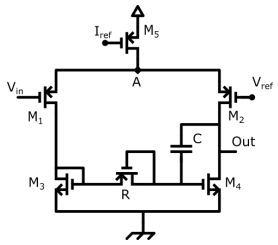

FIGURE 4.5 – *Schéma du NSNS.*

Ainsi, on peut empêcher le reset de varier avec l'intégration de charge et alors réduire l'influence du bruit non stationnaire.

III.2. Simulation et mesures

J'ai mesuré le bruit en sortie de filtre avec et sans NSNS comme montré figure 4.6

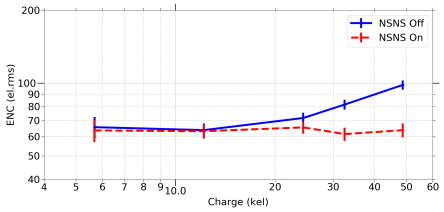

FIGURE 4.6 – *Bruit après filtre, avec et sans NSNS pour un courant de polarisation de 10 µA à un temps de pic de 3.6 µs.*

Les résultats montrent une réduction du bruit non stationnaire de 53 el.rms pour une charge de 30 000 électrons.

IV. Filtre et optimisation surfacique

IV.1. Description

Afin de permettre un filtrage semi-gaussien, j'ai mis en pratique la chaine exprimée dans IDeF-X HDBD en deux étages illustrée figure 4.7 afin de réduire la surface occupée.

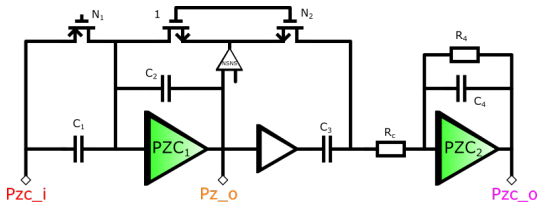

Figure 4.7 – *Schéma de l'étage de filtrage ; les deux premières parties agissent comme une suppression zéros-poles, le dernier amplificateur agit comme un filtre passe bas. Une résistance R_c permet de gagner un ordre sur le filtre de manière astucieuse.*

IV.2. Résultats

Le filtre a donc été dimensionné afin d'optimiser l'aire, tout en faisant en sorte que son bruit soit négligeable devant le CSA. Afin de prouver ce dernier point, j'ai effectué différent tests sur la sortie de filtre, en multiplexant directement la sortie d'un pixel.

Ces mesures on été faites pour tous les pixels permettant de faire une cartographie de bruit et de gain montré figure 4.8.

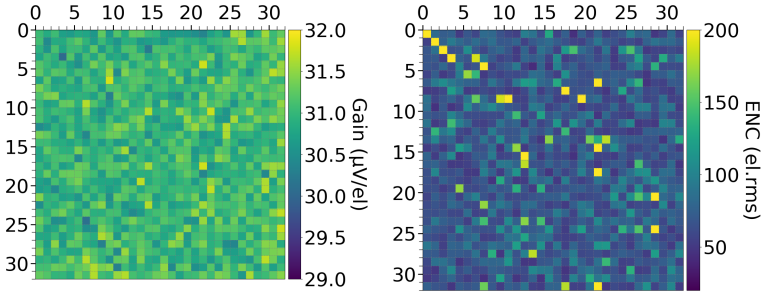

Figure 4.8 – *Carte de gain pour les 1024 pixels (à gauche). Et ENC pour les 1024 pixels (à droite).*

Le gain moyen est de 31 μV/el avec une déviation standard de 271 nV/el. Le bruit moyen est lui de 74 el.rms (35 el.rms minimum) avec une déviation standard de 21 el.rms ce qui est bien plus élevé que prévu.

La gamme de charges sur laquelle ces mesures sont valides va jusqu'à 39 400 el (175 keV CdTe) pour une non linéarité intégrale maximale de 2.4%.

Chapitre 5: Conclusion

I. Introduction

Les miroirs pour rayons X durs ont grandement été améliorés durant la dernière décennie. Il en va de même pour les détecteurs semi-conducteurs notamment le CdTe, qui permettent d'avoir de bonne performance spectrales et spatiales. Dans le laboratoire, les meilleurs performances atteintes correspondent à un détecteur de 4.8 x 4.8 mm^2 avec 16 x 16 pixels de 300μm et une résolution de 600 eV FWHM à 60 keV.

Durant cette thèse, je me suis concentré à améliorer les performances spectrales et spatiale de tels circuits intégrés afin de continuer le chemin afin d'aboutir au besoin d'une mission telle que la mission PHEMTO proposée dans le Chapitre 1.

Ainsi, j'ai développé deux principaux ASICs: IDeF-X HDBD et IDeF-X D^2R_2 dans ce but. Le premier ASIC, IDeF-X HDBD, a permit d'arriver à des spectaculaires performances spectrales avec 17 el.rms de bruit pour 32 canaux de 150 μm de large. Cet ASIC a même été connecté à un détecteur semi-conducteur de type SDD permettant de mesurer la raie du ^{57}Co à 122 keV avec une résolution de 604 eV FHWM définitivement Fano limitée.Le second ASIC, IDeF-X D^2R_2 a quand a lui permit d'améliorer la résolution spatial avec une grande matrice de détection de 1024 pixels de chacun 250 x 250 μm^2. La résolution spectrale quand à elle donnée par son bruit électronique en moyenne de 70 el.rms par pixel, reste à améliorer même si l'objet complet est prometteur.

II. Tests à venir

Au moment de rédaction, l'ASIC n'a pas été testé dans son mode nominal mais par l'utilisation du mode d'espionnage. Il est donc nécessaire de tester le circuit intégré avec le séquencement approprié qui requiert un peu de travail, afin de pouvoir avoir une vue des performance globales dans un mode nominal.

Le système a été pensé pour permettre la numérisation du signal par un ADC spécifique appelé OWB-1. Le test de la compatibilité des signaux des deux ASICs est donc aussi à développer afin de valider le système.

Enfin, le test ultime sera d'adjoindre au système D^2R_2 + OWB-1, un détecteur CdTe bump bondé sur l'ASIC D^2R_2 pour vérifier la fonctionnalité et les performances du système entier.

III. Le module Caliste D^2R_2

Pour pouvoir créer des plans focaux modulaires, l'idée de la thèse est de permettre d'adjoindre 4 ASICs D^2R_2, et de faire passer les signaux par un module 3D tels que montré figure 5.1. le détecteur et l'ASIC de lecture front-end seront au dessus du module et l'ADC en dessous.

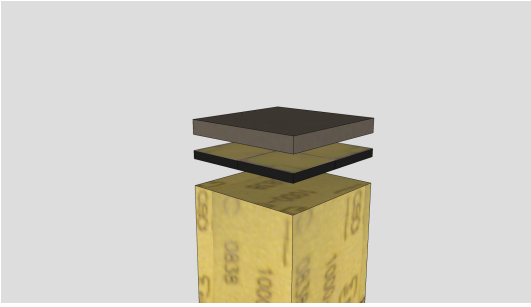

FIGURE 5.1 – *Projet de module 3D. Détecteur (en haut), ASIC (au mileu), module composé d'ADC OWB et autres composants génériques (bas)*

Ce nouveau système va alors permettre de créer des plan de détection variés par composition de modules de 64 x 64 pixels.

IV. VERS LE DÉVELOPPEMENT D'UNE MATRICE "DE VOL".

Pour autant, je ne considère pas l'ASIC IDeF-X D^2R_2 comme terminé dans son développement. Des améliorations doivent être effectuées pour comprendre la hausse du bruit par rapport aux simulations, et pouvoir atteindre le bruit espéré inférieur à 20 el.rms avec détecteur.

Je recommande donc de continuer le projet du côté circuit intégré par le développement d'un circuit de test permettant de résoudre ce problème.

Enfin, une fois ce circuit développé et testé, une matrice plus grande pourrait être développée afin d'arriver à la taille maximale que la technologie autorise de 22 x 22 mm, soit une matrice de 3 x 3 D^2R_2 comme illustrée figure 5.2.

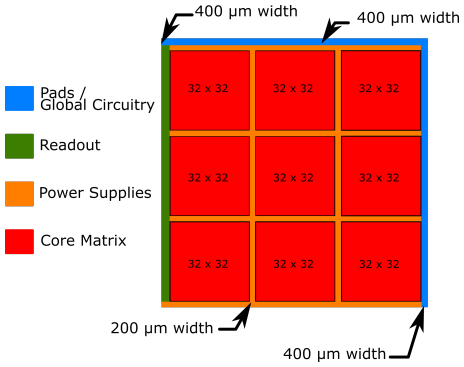

FIGURE 5.2 – *schéma de la matrice 96 x 96 pixels, compatible avec le circuit D^2R_2.*

Je conclus alors cette thèse avec ces proposition en espérant les voir aboutir dans un avenir proche.

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Ecole Doctorale N° 127
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Titre: Développement d'un spectro-imageur CdTe pour application spatiale

Mots clés: Circuit intégrés, rayons X, bas bruit

Résumé:
Ce manuscrit présente le travail de thèse effectué dans le cadre d'un projet de développement d'instrumentation spatiale pour rayons X-durs. Des développements précédents ont permit la conception d'un détecteur en tellurure de cadmium (CdTe) permettant la conversion photoélectrique du spectre lumineux dans la gamme spectrale des rayons X (1keV – 100 keV).
Cette thèse décrit l'ensemble des étapes de conception d'un circuit intégré de conversion de charge permettant de lire le détecteur précédemment développé avec pour spécificités : une haute résolution spectrale, une haute résolution spatiale, et une aboutabilité sur quatre cotés.
Ce travail s'est organisé selon trois principales étapes. Le choix de la technologie du circuit intégrés. La conception, fabrication et test de prototypes dédiés à mettre en place l'architecture du système. Et la conception et test du circuit, sujet de ce travail de thèse, nommé IDeF-X D^2R_2.
Ce dernier circuit intégré de 8.5 mm x 8.5 mm, contient 1024 pixels (matrice de 32 x 32) de 250 x 250 μm^2 permettant chacun la lecture de charge avec un bruit de 40 électrons, une dynamique allant jusqu'à 110 000 électrons (500 keV CdTe), pour une puissance consommée de 200 μW/pixel. Une approche système a été pensée pour être compatible à un convertisseur numérique analogique nommé OWB-1 permettant une sortie numérique du spectro-imageur.
Les résultats sont prometteurs pour le développement de plans de détections modulaires pour de futures missions spatiales dans la gamme des X-durs, permettant l'étude d'objets stellaires et inter-stellaires.

Title: Development of a CdTe spectro-imaging for space application

Keywords: ASIC, X-Rays, low noise

Abstract:
This manuscript details the work in the scope of a hard X-Ray spatial instrumentation project. Previous developments have reached the design and fabrication of a Cadmium Telluride detector (CdTe) allowing precise photoelectric conversion of light in the hard X-Ray energy range (1keV – 100 keV).
This thesis describes all of the design steps of a charge conversion integrated circuit with several specificities: a good spectral resolution, a good spatial resolution, and a four-side abutability.
This work organizes through three principal steps. The technology choice for integrated circuit fabrication. The design, fabrication and test of prototypes dedicated to develop the circuit architecture. In addition, the design and test of the final circuit named IDeF-X D^2R_2.
This circuit of 8.5 mm x 8.5 mm, contains 1024 pixels (matrix of 32 x 32) of 250 x 250 μm^2 each of one allowing charge measurement with a low noise of 40 electrons, a dynamic up to 110 000 electrons (500 keV CdTe), for a nominal power consumption of 200 μW/pixel. A system approach has been done to be compatible to a 32 channel analog to digital converter developed prior to the thesis named OWB-1 leading to a digital output spectro-imaging system.
Developments and results are promising for the conception of modular detection plan for future spatial missions in the hard X-Ray energy range, allowing study of energetic celestial objects.

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