Application Specific Integrated Circuits for ANTARES Offshore Front-end Electronics

D. Lachartre, F. Feinstein

CEA, DSM/DAPNIA, CE-Saclay, F-91191 Gif-sur-Yvette Cedex, France

On behalf of the ANTARES collaboration

Abstract

The ANTARES undersea neutrino telescope will consist of an array of mooring lines carrying photomultiplier tubes enclosed in pressure resistant glass spheres (optical modules). They detect the Cherenkov light emitted by the muon produced by the charged current interaction of the parent neutrino. Data are transmitted to the shore through an electro-optical cable. Two ASICs have been developed in order to process the photomultiplier tube signals. The SPE_PSD chip discriminates between single photo-electron pulses for which the integrated charge and the arrival time are measured, and more complex pulses to be processed by the ARS0 chip. The ARS0 is a 5-channel 128-memory-cell 1GS/s analogue sampler, read out by a 1 MHz ADC. This array of switched capacitors is equivalent to a 1 GHz flash ADC of several orders of magnitude less power consumption. Since single photo-electron pulses amount to 99% of the total, this dual path of the signal processing provides a strong reduction of the power consumption as well as of the amount of transmitted data.

1. Introduction

The ANTARES [1] collaboration plans to deploy an undersea neutrino detector consisting in an array of Optical Modules (OM). The OM detects the Cherenkov light emitted by the muon produced by the charged current interaction of the parent neutrino. The main goal of the offshore electronics is to read out signals from the OM photomultiplier tubes (PMT) and process them in view of particle track determination. The information is digitised and sent to the shore through a single optical link. This architecture bottleneck imposes to minimise power consumption and data flow by using low power and data compression techniques for which ASICs are mandatory [2].

In 1996, ANTARES started to develop two CMOS mixed analogue-digital circuits. The ARS0 and SPE_PSD chips implement the signal processing detailed in chapter two. They were manufactured and tested in 1997, results of the measurements are described in chapter three. The next step of the development will be the ARS1 chip which will integrate the ARS0, the ARS_SPE and the other features described in chapter four.

2. Design Description

A block diagram of the signal processing is shown in Fig. 1.

The ANTARES solution is based on two ideas :

- Pulse shape discrimination (PSD) between Single Photo Electron (SPE) and complex (Waveform) shapes.
- Fast sampling and digitisation of the Waveform pulses (ARS0), time and charge determination of the SPE pulses (SPE_PSD).

The fast sampling feature is implemented in the ARS0 chip. The SPE_PSD chip contains the Pulse Shape Discriminator, the Integrator and the Time to Voltage Converter.

Amplitudes of the PMT anode pulses are compared to the adjustable threshold voltage of a comparator which generates a level 0 trigger (L0). L0 triggers are then sent to an external level 1 trigger (L1) builder where coincidences between neighbouring Optical Modules are performed. Before digitisation, information stored either in the ARS0 or in the SPE_PSD chip is validated by the result of the L1 trigger. The two ADCs permit digitisation of the SPE values in one ADC cycle, the waveform samples in 128 cycles. Data are then formatted with a header

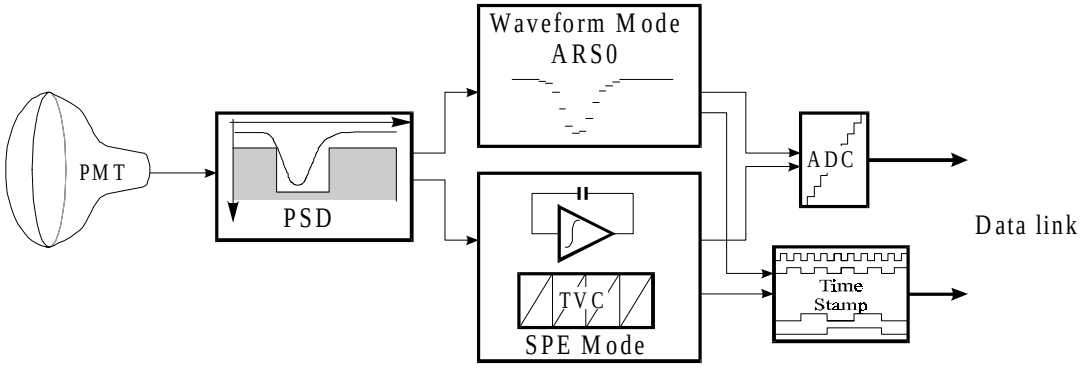


Fig. 1. Local signal processing bloc diagram

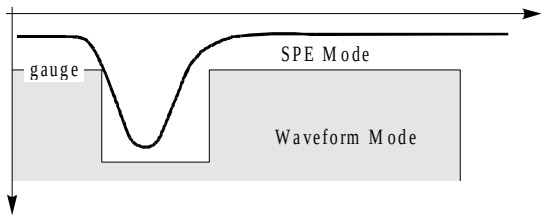


Fig. 2. Discrimination gauge

(OM number, PSD result) and with a 24-bit Time Stamp value of the pulse arrival. The Time Stamp is the latched value of the reference clock binary count. The two 8-bit ADCs and Time Stamp are not integrated in the ASICs.

2.1. Pulse Shape Discrimination

Since SPE pulses have a generic shape, it is not needed to digitise at 1 GHz such signals which are characterised by their charge and their arrival time. It represents about 40 times less data than the detailed pulse shape. On the contrary, Waveform pulses consist of superimposed shapes, they are unpredictable and must be completely digitised. The discrimination is performed on (Fig. 2) :

- Pulse height,
- Pulse width above a threshold level,
- Pulse multiplicity above threshold during a given time window τ.

Waveform shapes proportion Q_w depends on the L0 trigger counting rate F :

$$Q_w = 1 - (1 - Q_0).e^{-\tau.F}$$

where $Q_0 = 0.005$ is the proportion of large or multiple pulses originating from the OM itself and τ=50 ns.

With the PSD, at F = 60 kHz, the Waveform proportion is less than 1 %, the data flow and the dead time reduction factors are about 30.

The PSD, implemented in the SPE_PSD chip, consists in a threshold comparator, a Time-Over-Threshold detector and a multiple pulses detector. The PSD is triggered by the L0 trigger and works until the pulse charge integration is finished (during τ). At this moment, the binary result is latched and directly used to select which of the fast sampling data or charge-TVC data should be digitised on a positive result of the L1 trigger.

2.2. SPE mode

The SPE mode, part of the SPE_PSD chip, consists in charge integration and arrival time determination of the PMT anode pulses within the reference clock period of 50 ns.

Integration is performed by an OTA amplifier (gm = 3mA/V) and a feedback capacitor (5 pF) where the charge is collected during the integration gate (typically 50 ns). The output voltage which is directly proportional to the charge, is digitised by one of the two external ADCs.

Timing determination is performed by the Time-to-Voltage Converter. It generates ramp signals at the reference clock frequency with a slope of 60 mV/ns. When a L0 trigger occurs, the current ramp value is latched and digitised by the second ADC.

The SPE mode generates only 2 bytes of digital data where the Waveform mode generates 256 bytes.

2.3. Waveform mode

The Waveform mode, implemented in the ARS0 chip, consists in a fast sampling of the PMT signals and a 20 MHz reference clock. The sampling frequency can be adjusted between 300 MHz and 1 GHz and locked to an external quartz. The ARS0 is a

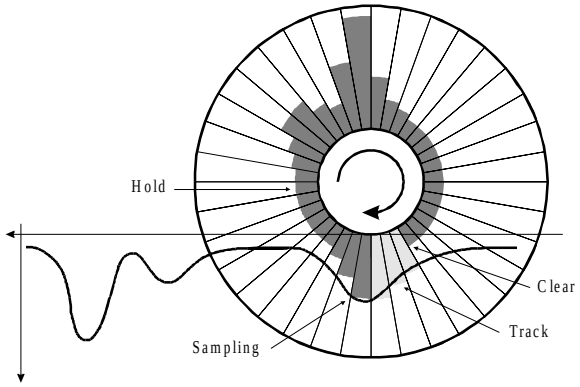


Fig. 3. Ring Sampling principle

5-channel analogue memory of 128 switched capacitor cells per channel.

In addition to the anode signal and the reference clock, up to three other signals (intermediate dynodes) are sampled synchronously. The inputs of the chip have amplifier-followers allowing, when selected, isolation between the input signals and the internal cell capacitor lines. When inputs are directly connected to these lines (amplifiers disabled), the input capacitance of the chip is of the order of 40 pF.

The Ring sampling principle, shown in Fig. 3, is based on a track and hold cycle. Before any pulse arrival, the ARS0 is sampling continuously. Some of the cells are in track state while others are in hold state. Cells are cleared when they turn to track state. At any time, the last nanoseconds of the input signals are recorded in the cells in hold state. The number of hold cells is a constant number provided by a 7-bit input bus of the circuit.

Memory cells switches are controlled by command signals coming from an internal loop delay line. The sampling frequency is defined by the elementary delay between two consecutive command signals.

When a L0 trigger occurs, the ARS0 stops overwriting. Until the memory is full, the last cells in track state continue to turn in hold state while none of the cells already in hold state are cleared. Sampling is completely stopped when all of the cells are in hold state. On validation of the sampled pulse by the L1 trigger, an internal shift register will sequentially read out the 128 samples through an OTA amplifier. On each read cycle, the OTA is first reset and then its feedback loop connected to the addressed cell capacitor.

The ring structure of the ARS0 avoids the use of coaxial cable for delay as it is needed for other similar circuits [2,3] having no such structure. The ARS0 chips can also be chained together in order to extend the number of samples (256, 384, etc.).

3. Measured Performances

The performances of several ARS0 and SPE_PSD chips have been studied on test bench, 80 % over 30 ARS0 chips were found good and 95 % over 150 SPE_PSD chips.

Either an 8" PMT or a pulse generator with 50 Ω coaxial cable and impedance matching, were used for the analogue inputs.

3.1. Measurements of the SPE_PSD chip

Table 1 shows the main characteristics of the chip. Measurements were performed on the integrator using a 2.2 kΩ resistor at the input in order to deviate 1/50 of the anode current. Fig. 4 shows the integrator transfer function, the curve is linear until 20 photo-electron (60 mV/PE).

Fig.5 shows the TVC input error (difference with linear fit) over the reference clock period of 50 ns. With correction, the TVC could achieve a precision better than 200 ps.

Table 1
Chip characteristics and measurements

Technology	AMS CMOS 0.8 µm
Chip dimension	2.8 mm^2
Number of transistors	1625
Power consumption @ 5 V power supply	< 50 mW
Integrator typical transfer function	4.3 mV/pC
Integrator input noise	0.7 pC RMS
TVC typical transfer function	60 mV/ns
TVC input noise	45 ps RMS
PSD typical width criteria	15 ns
PSD typical amplitude criteria	180 mV

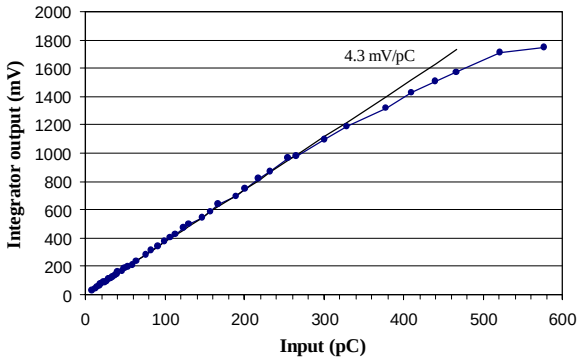


Fig. 4. Integrator transfer function

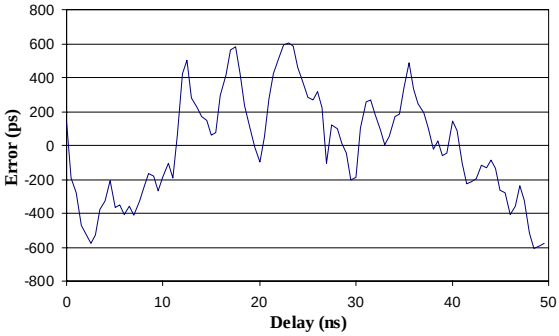


Fig. 5. TVC measured error versus delay

3.2. Measurements of the ARS0 chip

Table 2 shows the main characteristics of the chip and Fig. 6. is an example of the output when a 8" PMT is connected to one of the ARS0 inputs.

Measurements of the maximum power consumption were performed at the maximum sampling frequency and at a low counting rate as power consumption is lower during digitisation (125 mW @ 10 Hz counting rate, 80 mW @ 2.5 kHz).

The total output noise was obtained on a 2000*128-sample histogram. The noise includes non uniformity, thermal noise and parasitics.

As the first sample is located anywhere in the memory, the ARS0 returns the 7-bit address of the readout cell. With this information, the cell-to-cell non uniformity was obtained on sorted data. One thousand measurements of each cell provided an histogram of 128 averaged values from where the sigma was extracted.

The harmonic distortion was measured using a 1 V peak-to-peak 10 MHz sinus wave signal at the ARS0 input. The sampled curve has been fitted to the sinus function.

The Fig. 7 histograms were obtained from 10^4 events of a 8" PMT sampled at 1 GHz whose gain was set in order to have a Single Photo-Electron of 60 mV. The pulse charge Q_N was calculated directly by summing 64 of the 128 samples.

Table 2
Chip characteristics and measurements

Technology	AMS CMOS 0.8 µm
Number of channels	5
Number of memory cells/channel	128
Chip dimension	16 mm^2
Number of transistors	28,200
Maximum power consumption @ 5 V, 1 GHz	125 mW
Sampling frequency range	300 MHz to 1 GHz
Maximum readout frequency	700 kHz
Nominal gain (voltage)	0.945
Output dynamic range	3.2 V
Total output noise	2.5 mV RMS
Cell-to-cell non uniformity over 128 cells	0.8 mV RMS
Harmonic distortion (1 Vpp 10 MHz sinus wave)	1.7 %
Input bandwidth	110 MHz @ -3 dB

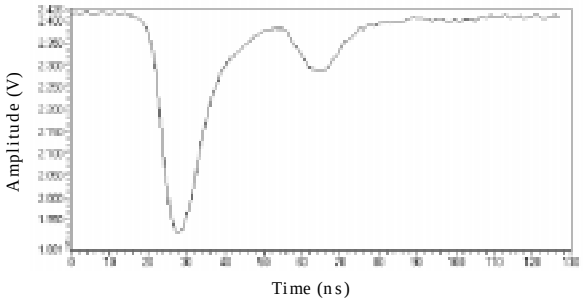
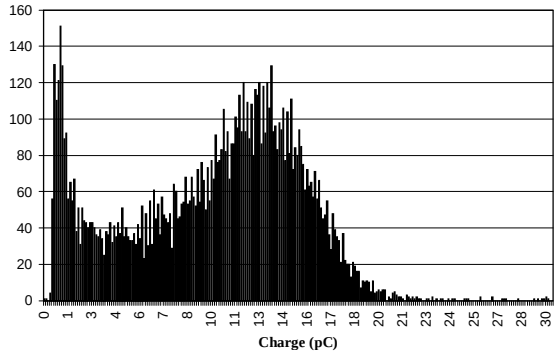


Fig. 6. ARS0 output example of a 8" PMT pulse



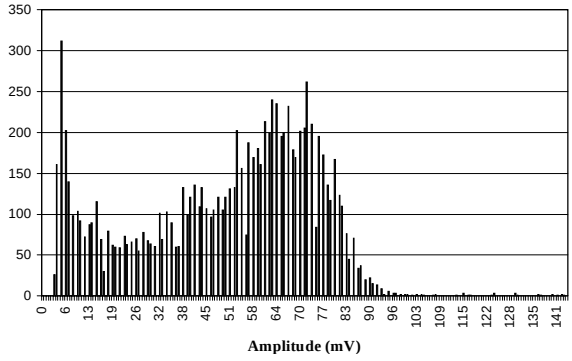


Fig. 7. ARS0 charge (left) and amplitude (right) histograms of a 8" PMT dark count

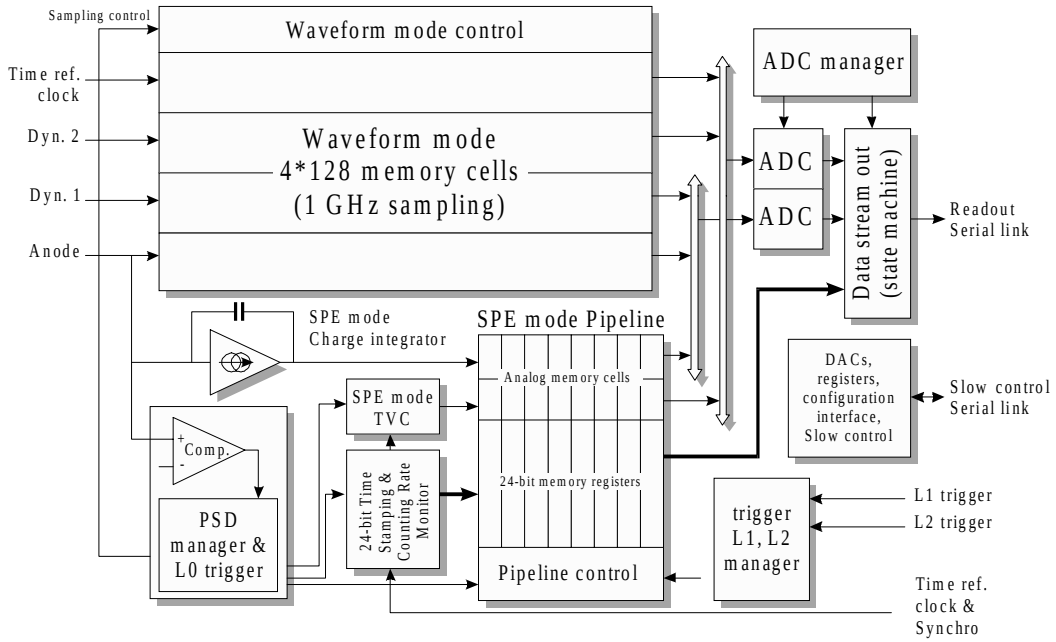


Fig. 8. ARS1 bloc diagram

4. Further developments

The ARS0 and SPE_PSD chips were the first step of the ANTARES front-end electronics. Not all of the needed features were implemented. The main one is the ability of the electronics to accept, with a reasonable dead time, a level 2 trigger (L2) which is returned on time coincidences between L1 triggers of distant OM clusters.

The ARS1 has been designed to keep pulse information in memory (pipeline) the time needed for the L2 request to propagate through the detector to all OM. When a L2 request occurs, any pulse that belongs to the L2 time window is validated and digitised.

The ARS1 bloc diagram of Fig. 8 shows that a 16-cell pipeline has been introduced before the integrated 8-bit ADCs. The pipeline cells contain two switched capacitors for charge and TVC voltages, and a 24-bit register for Time Stamp. Each cell has also a time window feature in the pipeline control allowing to flag cells in coincidence with the L2 request.

The L2 trigger rate of the detector will be 10 kHz with a time window of 2 μs, so that 2 % of the L0 trigger events will be validated and read out. Besides, L1 requests at 400 Hz will validate cells during the write operation.

The ARS1 also includes improved versions of the ARS0 and SPE_PSD circuits as well as new features such as Counting Rate Monitor, slow control configuration, 8-bit ADCs and 24-bit Time Stamp.

5. Conclusion

The two first chips, ARS0 and SPE_PSD, were successfully tested in 1997. It has been shown that they both meet the ANTARES specifications. They are now in production test and should be used for some of the ANTARES immersions and for other collaborations.

The ARS1 chip design is currently achieved, it has been sent to the foundry and should be tested in the year 2000.

References

[1] ANTARES proposal : http://antares.in2p3.fr/antares/proposal99.html

[2] Chaloupka V. et al., Technology development for a neutrino astrophysical observatory, L.O.I .to the D.O.E., LBL-38321, UC-412, Feb. 1996.

[3] Haller G., Wooley B., A 700-MHz Switched-Capacitor Analog Waveform Sampling Circuit, IEEE J. Solid-State Circuits, vol. 29, pp. 500-508, Apr. 1994.