



GTS Ancillary Detectors meeting

Legnaro, November 17, 2004

November 28, 2004

Present: D. Bazzacco, P. Bednarczyk, M. Bellato, A. Czermak, B. Dulny, A. Gadea, R. Isocrate, L. Olivier, V. Pucknell, Ch. Theisen, G. Wittwer, M. Zieblinski.

This meeting with a limited number of participants (experts) was devoted to discuss the specifications of the interface between ancillary detectors and AGATA.

Discussions started on the latency times. The delay between a trigger request and a validation/reject answer from the GTS supervisor is at least $7\mu\text{s}$. It was agreed that this time is too long; therefore, a fast signal (for instance multiplicity signal) is mandatory for triggering ancillary detectors having standard electronics.

Action: D. Bazzacco to find a solution within the LLP group.

VME standard for the interface with VXI backplane compatibility was agreed. Main specifications of the interface were discussed and are summarized in the document entitled "Specifications of the AGATA Ancillary Detector GTS Interface (Version 0.2)".

Ganil and IJF Krakow have shown their interest in building the interface. Since manpower is available at Krakow starting from January 2005 (1.5 M.Y.), it has been decided to design the interface at Krakow. Detailed specifications will be written by Ganil and Krakow. A strong collaboration between these two laboratories is strongly encouraged. Design will be made at Krakow. Two prototypes will be built, one tested at Ganil, the other at Krakow. Production will be made at Krakow. M. Bellato, V. Pucknell and J. Hoffmann (the GSI Titris designer) will collaborate during the whole project.

Action: contacts with GSI engineers. Piotr Bednarczyk?

A time schedule for design, prototyping, tests and production was proposed. No objections were raised.

The possibility of having funds in the frame of the Polish/IN2P3 collaboration was suggested.

Action: M. Zieblinski to check whether it is possible to have money from the Polish/IN2P3 collaboration for technical purposes.

Cost estimates were given and fit inside the Agata allocated funds.

Forthcoming meetings:

- Video conference in January 2005.
- Meeting during the next Agata week (GSI, 21-24 February 2005).

Addendum:

The members of the Ancillary Detectors working group in the last meetings (Orsay June 2004 and LNL November 2004) have shown a clear concern on the difficulties to couple ancillary detectors with AGATA with the present version of the low level processing electronics.

We are concern by the specificity of the interfacing with the AGATA electronics and by the difficulties to have a “prompt” (with delay below 1 μ s) first level trigger to be used by the ancillary detector electronics.

The electronics of many existing ancillary detectors was not build to wait 6 to 7 μ s minimum latency time to have a response from the gamma-array. We do not foresee problems for very low counting rate devices for which we can work with analog electronics in almost total data recording mode. Since most of conventional ADCs have contributions to the dead time ranging from 10 to 30 μ s (or more), we expect to start having problems with rates ranging from 100KHz to 30kHz, depending on the total dead time of the acquisition system. The effect foreseen is that, depending on the efficiency of the AGATA subset used, we might loose a large fraction of good events (in case we define good event the ones containing the AGATA and the ancillary device information), and therefore the efficiency of the AGATA-Ancillary system complex will drop.

Another source of concern is the increase of the use of highly integrated analog electronics ASICs in ancillary systems. It is obvious that an highly segmented device build to fit in the AGATA inner space (for instance light charged particle with large angular resolution) and with the present status of art electronics, cannot use the same electronic philosophy than AGATA without disturbing largely the functionality of the array (for instance thousands of cables going out from the inner AGATA volume).

Most of the present ASIC electronics require an external trigger in a reasonable time to build the timing of the single segments (TAC inside the ASIC, example MUST II).

For the reasons mentioned above, we have arrive to the conclusion that a “fast” (as fast as possible) pre-trigger signal probably in the form of sumbus, will be necessary for an efficient coupling ancillary devices to the AGATA Demonstrator, and we should be aware that this signal might as well necessary for the full AGATA project.

