IDeF-X ASIC for Cd(Zn)Te spectro-imaging systems

O. Limousin, O. Gevin, F. Lugiez, R. Chipaux, E. Delagnes, B. Dirks, B. Horeau

***Abstract*—Progress in the fields of Cd(Zn)Te detector development, microelectronics and interconnection technologies open the way for a new generation of instruments for physics and astrophysics applications in the energy range from 1 to 1000 keV. Cd(Zn)Te based instruments operating in the range between –20 and 20°C, will offer high spatial resolution (pixel size ranging from 300 × 300 µm² to few mm²), high spectral response and high detection efficiency. To reach these goals, reliable, highly integrated, low noise and low power consumption electronics is mandatory. Our group is currently developing a new full custom ASIC detector front-end named IDeF-X, for modular spectro-imaging systems based on the use of Cd(Zn)Te detectors. We present here the first version of IDeF-X that consists of a set of ten low-noise charge sensitive preamplifiers (CSA). It has been manufactured using the AMS 0.35 µm CMOS technology. The CSAs are designed to be DC coupled to detectors having low dark current at room temperature. We have optimized the various preamplifiers to match detector capacitances in the range from 0.5 to 30 pF.**

I. Introduction

SINCE our previous development, IBIS/ISGRI gamma-ray camera [1] on board the INTEGRAL Satellite, we have demonstrated that it is possible to reliably use a large number of CdTe detectors associated with microelectronics front-end in space. On the other hand, progress in the manufacturing of CdTe detectors in terms of crystal quality and volume size and progress in the field of microelectronics and interconnection technologies open the way for a new generation of 1 to 1000 keV photon energy detectors for physics and astrophysics. The next generation of instruments based on these technologies will have high spatial resolution (pixel size: ~ 300 × 300 µm² to few mm²), high spectral response and high detection efficiency operating in the range between –20 and 20°C. To reach these goals, reliable, highly integrated, low noise and low power consumption electronics is mandatory.

Our group is currently developing a new modular spectro-imaging system based on CdTe detectors coupled to a dedicated full custom readout ASIC, named IDeF-X for Imaging Detector Front-end. This device will be used in large area cameras (100 to 1000 cm²) for space borne astrophysics, either on focusing telescope (e.g. SIMBOL-X [2] and MAX [3]), operating in hard X-rays (4 to 150 keV) or gamma-rays (511 and 847 keV), or on a large area detector for coded aperture instruments (4 to 600 keV) (e.g. ECLAIRs [4]).

This paper is structured as follows: Section II presents the IDeF-X ASIC design. Section III discusses its performance in terms of noise measurements, and the spectral response of one of the charge sensitive preamplifiers (CSAs) connected to a set of moderate capacitance CdTe detectors (< 5 pF). Finally, section IV is devoted to the results of Total Ionizing Dose tests performed on the chip with a ^{60}Co source up to 224 krad.

II. IDeF-X ASIC design

The development of the IDeF-X front-end ASIC will include several steps from its first version as a set of stand-alone preamplifier prototypes to a complex multi-channel (32 to 256) circuit for high-pixel density CdTe readout. We present here the very first version of IDeF-X.

TABLE I
IDeF-X CSAs Characteristics

CSA #	*Input transistor type*	*Input transistor size W/L (µm/µm)*	*Input capacitance range (pF)*	*Detector application*
0	PMOS	310/0.5	0.5	NA (no pad)
1	PMOS	1000/0.5	2 to 5	Cd(Zn)Te
2	PMOS	1550/0.35	5 to10	Cd(Zn)Te
3	PMOS	1600/0.5	5 to10	Cd(Zn)Te
4	PMOS	1400/0.75	5 to 10	Cd(Zn)Te
5	NMOS	1550/0.35	5 to 10	Cd(Zn)Te
6	NMOS	1600/0.5	5 to 10	Cd(Zn)Te
7	NMOS	1400/0.75	5 to 10	Cd(Zn)Te
8	PMOS	4000/0.5	30	cooled Ge
9	PMOS	2700/0.75	30	cooled Ge

The goal of this first prototype is to evaluate the AMS 0.35 µm CMOS technology capabilities for low noise and low power consumption analog design (less than 60 electrons noise rms for 50 µW per CSA). Therefore, we have built a set of ten low noise CSAs, well suited to high energy detectors.

The CSAs are designed to be DC coupled to detectors with a low dark current (< 5 nA). The geometry of the input transistors (W/L) has been optimized for detector capacitances in the range of 0.5 to 30 pF (see table I). Most of the CSAs (#1

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to #7) are designed for low capacitance detectors like Cd(Zn)Te small crystals or pixels. Nevertheless, we have also designed two CSAs (#8 and #9) matching larger detector capacitance (e.g. cooled germanium). CSAs were defined to study the *1/f* noise behavior with respect to the type (NMOS and PMOS) and gate length (L) of the input transistor. In order to secure the tests, the input pads are equipped with anti-ESD protections.

The CSA electrical design is based on a "folded cascode amplifier" [5, 6] with either a PMOS or a NMOS input transistor. The value of the feedback capacitance is 300 fF for CSAs #0 to #7, and 500 fF for CSAs #8 and #9. The DC feedback is done by a PMOS transistor biased by the detector leakage current. Each CSA output is connected to a 10× voltage gain stage.

These stages are multiplexed toward a low output impedance buffer. All channels are connected to an input pad except CSA #0. Inputs can be connected to a test input *Ve_test* with an individual 300 fF and 500 fF on-chip injection capacitor, respectively for CSAs #0 to #7 and CSAs #8 and #9.

On the other hand, in order to simulate a detector current or to compensate a reverse detector current, each channel includes a tunable current source *il* driven by the gate voltage V_{il} (Figure 1). The IDeF-X layout is represented in Figure 2.

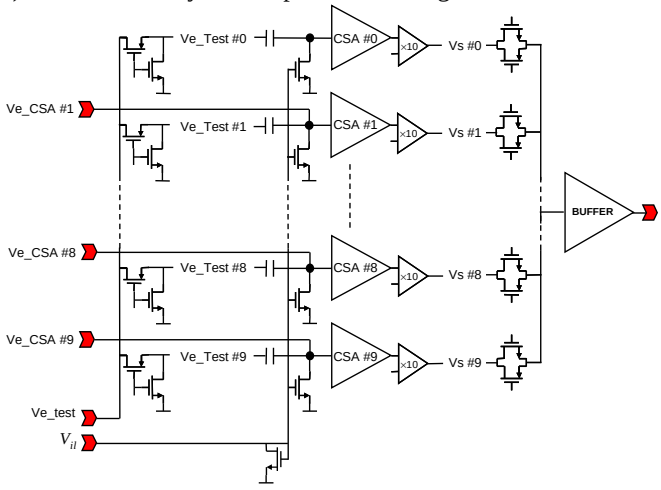

Figure 1: IDeF-X synoptic: Ten CSAs are placed before a gain amplifier, a multiplexer directed to a low impedance output buffer. At the input, each CSA has its own test capacitor. All CSAs are connected to a pad except CSA #0.

III. RESULTS

A. *Equivalent noise charge measurements*

The first characterization of the circuit consists in measuring the Equivalent Noise Charge (ENC) of each channel as a function of the peaking time when the CSA is placed at the input of a tunable CR-RC² or CR-RC filter. To perform the measurements, the circuit is packaged into a standard JLCC chip-carrier and mounted on a standard printed circuit board (PCB) into the setup described below.

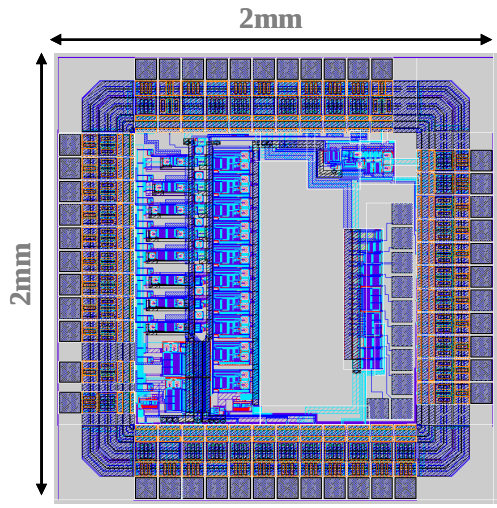

Figure 2: IDeF-X Layout. Ten preamps are placed on the left hand side of the 4 mm² circuit.

1) *ENC measurements test bench*

The JLCC carrier is mounted on a test board allowing biasing, configuration, injection and response measurements. This board is inserted in an automatic ENC vs. peaking time test bench shown in Figure 3 [7]. This setup includes a CR-RC² filter with tunable peaking times ranging from 20 ns up to 10 µs. It also includes a wave form generator. The pulse shapes and the noise are alternately recorded on a digital oscilloscope for the various filtering time-constants and analyzed with a computer. ENC measurements for larger peaking times (up to 1 ms) are done manually with a CR-RC filter but are not performed systematically.

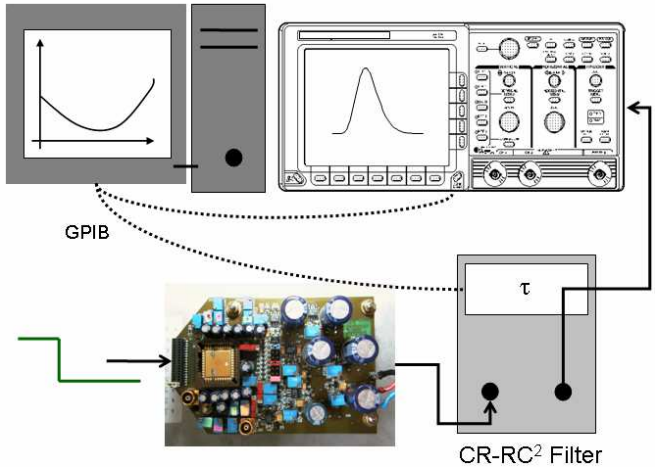

Figure 3: Setup for ENC measurement is operated with an external programmable CR-RC² shaper.

2) *Main ENC results for all of the CSAs*

A significant part of the noise is due to the setup itself (JLCC parasitic capacitance, connectors, PCB parasitic capacitance and dielectric losses). Therefore, we have performed two types of ENC measurements:

- In the first, the inputs were totally disconnected from the setup - no bonding on the inputs - in order to measure the intrinsic performances of the circuit, i.e. the floor noise of each CSA.
- In the second, the inputs were connected to the JLCC carrier with wire-bonding thus allowing the chip to be used with a detector. Nevertheless, the JLCC input pads were not connected to the PCB nor to the connector. Detectors were installed directly on the JLCC by wire soldering.

We measured the ENC for each of the ten CSAs without bonding, the results of which are shown in Table II. These measurements illustrate the intrinsic performances without assumption on the setup quality. Depending on the input transistor type and size, the floor noise was found to be between 31.5 and 49.3 electrons rms. In this set of tests, the CSAs were polarized with 1 mA / 3.3 V to reach the very best performances.

TABLE II
IDEF-X CSA MAIN PERFORMANCES

CSA #	*Min ENC (electrons rms)*	*Peaking time at ENC min (µs)*
0	12.4 (no pad)	8.9
1	31.5	9.1
2	33.1	9.1
3	32.3	9.1
4	34.1	9.1
5	44.8	4.5
6	49.3	4.5
7	47.6	4.5
8	30.4	4.5
9	29.2	4.5

We have estimated the influence of additional parasitic capacitances on the noise of each CSA. The measurements were taken with a 9 µs peaking time for PMOS type CSAs and 4.5 µs for the NMOS type (values for minimizing the noise level when no detector is connected). We obtained 3 to 5 electrons/pF for PMOS type CSAs and 5 to 6 electrons/pF for NMOS type.

In the following sections, we will concentrate on the PMOS type CSA #0 and CSA #3, and on the NMOS type CSA #6, to analyze their performance in greater detail. Those were chosen for the following reasons:

- CSA #0 does not have any input pad thus can be used as a reference for the design noise behavior (not sensitive to external noise sources).
- The PMOS CSA #3 has the least noise among the CSAs of the same type optimized for the range from 5 to 10 pF (see Table I). This preamplifier best matches the typical CdTe pixel detector capacitance.
- The NMOS CSA #6 was used to test the NMOS type and because it has the same input transistor dimensions as CSA #3.

3) ENC vs. peaking time for CSA #0, #3 and #6

We have measured the ENC vs. peaking time characteristics with the CSAs input pads bonded to the JLCC chip carrier without connecting any detectors. The minimum noise level in the ENC vs. peaking time characteristics was 69 electrons rms at 9.1 µs for the PMOS type input transistor (CSA #3) and 76 electrons rms at 4.5 µs peaking time for the NMOS input transistor (CSA #6). In NMOS type CSAs, injection of a current *il* is required for proper response. This current compensates the reverse current from the anti-ESD input diodes but adds a parallel noise contribution to the ENC vs. peaking time characteristics. This is the reason why the minimum value of the noise occurs for shorter peaking times than in the PMOS case where no additional current is necessary. On CSA #0, without input pad, we can measure intrinsic performances and limits of the design. Its minimum noise level is 12.4 electrons rms for a 9.1 µs peaking time. ENC vs. peaking time characteristics are plotted for CSA #0, CSA #3 and CSA #6 in Figure 4.

Forthcoming ENC evaluation on new IDeF-X versions will be done using a ceramic board (or another type of low dielectric loss factor material), to maximize the chip's performances.

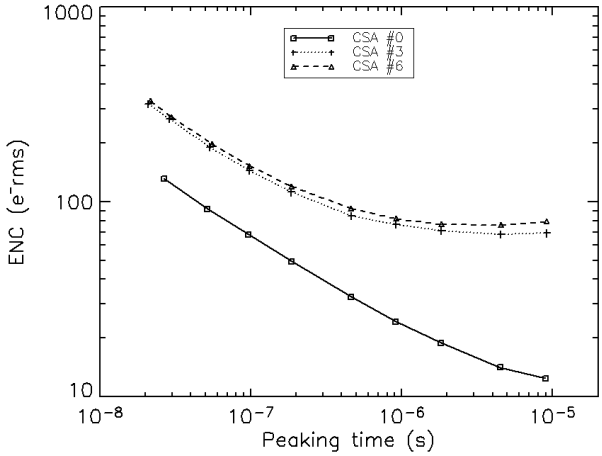

Figure 4: ENC vs. peaking time measurement results for CSA #0, CSA #3 and CSA #6. The CSA #0 has no input pad. On CSAs #3 and #6, the inputs are connected to the JLCC chip carrier but no detector is present. CSAs are biased with 1mA current through the input transistor.

4) ENC behavior with different biasing conditions

Until now, our tests were performed under conditions of high power consumption – 3.3 mW i.e. 1 mA. The power consumption can be reduced by limiting the total current I_0 passing through the input transistor. We have recorded the noise behavior of the CSA #3 as a function of I_0 (200 µA i.e. 660 µW and 50 µA i.e. 165 µW) and present the results in Figure 5. As expected, when the total current I_0 in the CSA is reduced, the series noise increases. The series noise is inversely proportional to the square root of the input transistor

transconductance g_m (see eq. 1), and roughly inversely proportional to the square or fourth root of I_0 (eqs. 2 and 3) depending on the input transistor regime (weak, moderate or strong inversion).

$$ENC^2_{series} \propto \frac{C_t^2}{g_m} \quad \text{(eq. 1)}$$

$$g_{m\ strong\ inversion} = \sqrt{2\mu\, C_{ox} \frac{W}{L} I_0} \quad \text{(eq. 2)}$$

$$g_{m\ weak\ inversion} = \frac{I_0}{n} \frac{q}{kT}, \quad \text{(eq. 3)}$$

where :

- C_t is the total input capacitance,
- μ is the majority carrier mobility,
- C_{ox} is the gate oxide capacitance per unit area,
- n is the sub-threshold slope factor (n > 1),
- k is the Boltzmann constant,
- T the temperature
- and q the electron charge.

For instance, the PMOS CSA #3 operates in weak inversion when I_0 = 50 µA and I_0 = 200 µA and operates in strong inversion when I_0 = 1 mA.

For long peaking times (above 8 µs), the parallel and *1/f* noise contributions begin to dominate and the influence of the bias condition on the ENC drops significantly.

We conclude that our design can be easily used in a low power input stage if large peaking-times (> 8–10 µs) are applicable. This requires detectors with leakage current as low as possible. This current has to be lower or equal to the chip internal leakage currents we found to be primarily due to the anti-ESD diodes of the input pads. The dark current has to be less than few picoamperes, as shown in section IV. A moderately cooled – around 0°C – Schottky CdTe detector or pixel CdZnTe detector can reach such values.

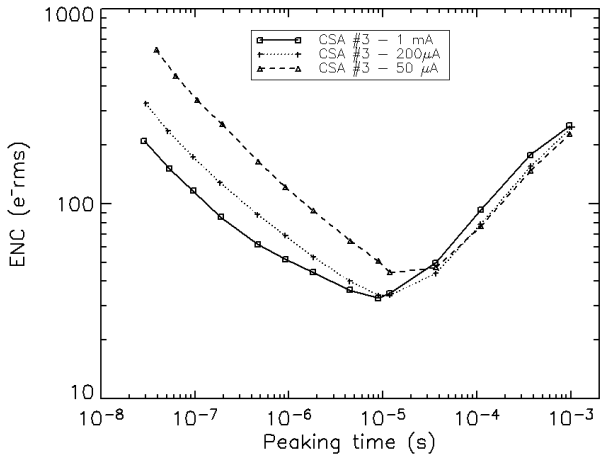

Figure 5: ENC vs. peaking time as a function of the bias current in the CSA #3 input stage of IDeF-X. The ENC are obtained on a chip without input bonding to avoid noise due to the setup conditions (PCB, JLCC, connector contributions).

B. Spectroscopy measurements

These promising results allowed us to consider a direct application for spectroscopy. We connected the PMOS CSA #3 of IDeF-X biased with I_0 = 200 µA (660 µW) to a set of CdTe detectors at room temperature (21-24°C). The detectors were DC coupled to the input of the CSA, whose output was connected to a Canberra 2025 amplifier with an adjustable Gaussian shaping time in the range 0.5 to 12 µs, corresponding to a peaking time of 1.5 µs to 36 µs.

Firstly, we plugged a 2 × 2 × 2 mm^3 Travelling Heater Method grown (THM) CdTe detector (Eurorad) equipped with quasi ohmic platinum electrodes. This detector showed a dark current of 5 nA when biased at 100 V. The intrinsic capacitance of the CdTe detector is ~0.2 pF. However, this value is negligible compared to the other parasitic and interconnection capacitances of the setup that amount to ~5 pF. The lowest noise was obtained for a 0.5 µs shaping time. As a matter of fact, the parallel noise increases rapidly with the shaping time because the current is not negligible. The series and *1/f* noise are moderate thanks to the low input capacitances. We obtained satisfactory lines with a 3.5 keV FWHM at 59.5 keV and 2.2 keV FWHM at 17.8 keV (see Figure 6).

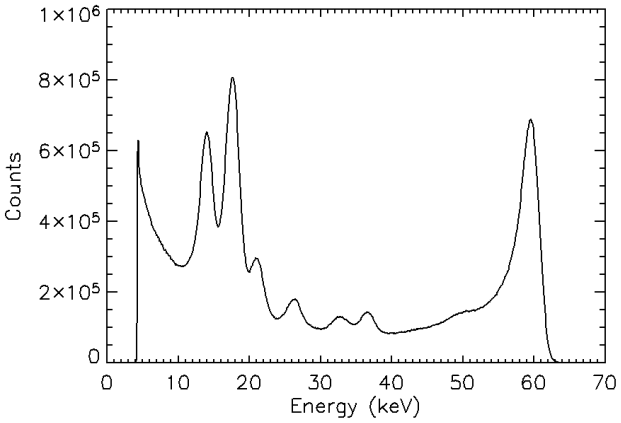

Figure 6: Spectrum of a ^{241}Am source obtained with a 2 × 2 × 2 mm^3 CdTe detector equipped with Pt contacts on both electrodes (EURORAD, France) plugged on CSA #3, biased with 200 µA. The detector is biased under 100 V at 24°C. The spectral response is good (3.5 keV FWHM at 59.5 keV). The broadening on the left hand side of the 59.5 keV line is mainly due to the charge loss and ballistic deficit in the 2 mm thick CdTe.

Using the same setup, we connected CSA #3 to a 4.1 × 4.1 × 0.5 mm^3 THM grown CdTe (ACRORAD) equipped with a Schottky contact at the anode and a guard ring at the cathode (1 mm guard ring surrounding the 2 × 2 mm² pixel). The reverse dark current of the CdTe diode is very low (< 10 pA under 200 V bias voltage at 21°C) and the capacitance of the pixel is 0.7 pF. The spectrum shown in Figure 7 illustrates the results with 2 µs shaping time: 1.6 keV FWHM at 59.5 keV and 1.4 keV FWHM at 13.8 keV.

In the ISGRI CdTe gamma camera equipped with mixed analog and digital ASIC [1, 8, 9], 2.8 mW power consuming,

the best spectral resolution measured during the ground calibration phase, with 4 × 4 × 2 mm^3 THM CdTe crystals (ACRORAD), biased under 100 V at 0°C, was 5.6 keV FWHM at 60 keV.

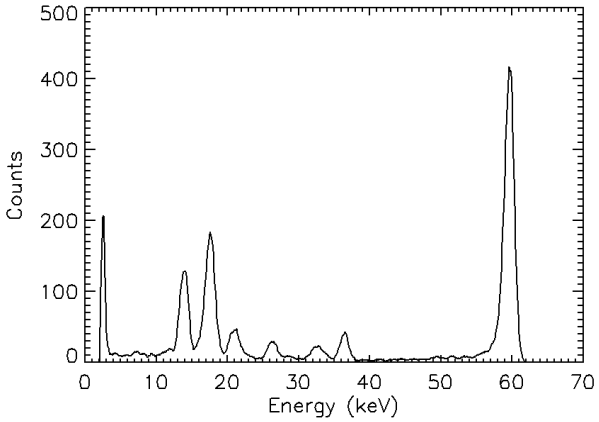

Figure 7: Spectrum of a ^{241}Am source obtained with a 4.1 × 4.1 × 0.5 mm^3 CdTe detector equipped with a Schottky contact at the anode (ACRORAD, Japan) plugged on CSA #3, biased with 200 µA. The cathode is 2 × 2 mm² pixel surrounded by a 1 mm guard ring. The detector is biased under 200 V at 21°C. The spectral response is very good (1.6 keV FWHM at 59.5 keV and 1.4 keV FWHM at 13.8 keV). The very low threshold value around 3 keV is noticeable.

IV. Irradiation with ^{60}Co

Since the development of the IDeF-X ASIC is intended for future space-borne application in astrophysics, it was necessary to evaluate our first prototype's sensitivity to radiation. We irradiated two IDeF-X circuits with a 589 GBq ^{60}Co source during 224 hours. The ASICs were placed 13 cm from the source and were thus subjected to a 1 krad/h dose rate. We performed a set of nine irradiation tests starting from 10 up to 224 krad of accumulated dose.

One chip was used to analyze the behavior of the PMOS type CSA #3 and another for the NMOS type CSA #6. Both CSAs were correctly biased to ensure their functionality during the runs with a 200 µA current in the input transistor. All other CSAs in the chip were also biased but not multiplexed to the output and therefore, not systematically monitored. During the irradiation runs, the injected current *il* in the reset transistor of the NMOS type CSA #6 was raised high enough to compensate a potential shift of the internal leakage current, minimizing the effect of this shift on the preamplifier that could cause it to stop working. The spectral response of the two circuits was monitored during each irradiation stage. A calibrated injected signal was sent to the ASIC inputs and we recorded the response using a 3 µs shaping time amplifier (ORTEC DUAL SPEC 855) and a standard acquisition chain. Between irradiation runs, the two CSAs #3 and #6 were fully characterized (ENC, gain, rise-time and fall-time, polarization currents) with the test bench described in section III-A-1. During fine characterization, the compensation current of the NMOS CSA #6 was readjusted to its optimal minimum value.

A. Results

1) Amplification gain

We monitored the amplification gain of the CSAs throughout the irradiation, and measured the output voltage level directly after the output buffer. No shift was found in either the PMOS or the NMOS type CSAs. The amplitude was found to be constant at 37 mV and 35.5 mV respectively for the CSA #3 and #6 when a 4 mV square signal was injected through the 300 fF internal injection capacitor.

2) Output signal rise-time and fall-time

The signal output rise-times were also found to remain constant in both CSAs at 35 ns and 38 ns for the CSA #3 and #6. However, we noticed that the irradiation caused slight changes in the output signal fall-times in both preamplifiers:

- CSA#3: for this type of preamplifier, the current through the reset transistor is very low in nominal conditions (~ 380 fA). Consequently, the output signal fall-time is long (> 35 ms). Fall-time decreased to 13 ms after 95 krad, and dropped to 10 ms after 224 krad. This effect is typically associated with an increase in the current I_R through the reset transistor that acts as a feedback resistor R_R, inversely proportional to I_R (see eq. 4). After 224 krad, the current through the reset transistor was found to be ~1.5 pA.
- CSA #6: for this type of preamplifier, we had to tune the compensation current *il* after each run in order to reach fall-time values as long as possible. Therefore, the evolution of the fall-time is not directly related to the effects of irradiation. We will detail this point later in the paper.

$$R_R = \frac{1}{I_R} n \frac{kT}{q} \qquad \text{(eq. 4)}$$

3) Power consumption

At the end of the campaign, we measured the power consumption (current level in the 3.3 V power supply) and we concluded it was not affected by the irradiation. The measured current is the total current of the circuit (Ten CSAs, amplifiers, multiplexer and output buffer). It is not possible to distinguish between the NMOS and PMOS CSAs in this case.

4) ENC measurements

We systematically measured the ENC vs. peaking time characteristics of the CSA #3 and CSA #6. As shown in Figure 8, the minimum ENC increases linearly with increasing dose. Furthermore, the two CSAs appear to be slowly degrading at a similar rate (0.09 and 0.1 electrons rms/krad respectively for PMOS and NMOS type CSA). The minimum ENC values were found to be between 1.8 and 4 µs peaking time for the NMOS CSA. This short peaking time was constrained by the compensation current *il*, unfortunately causing a strong parallel noise structure. But for the PMOS CSA, the minimum ENC values occurred at 9 µs peaking time until 111 krad. For higher doses, the minimum ENC occurred at 4.5 µs peaking time

which is typically associated with a progressive increase of the parallel noise contribution.

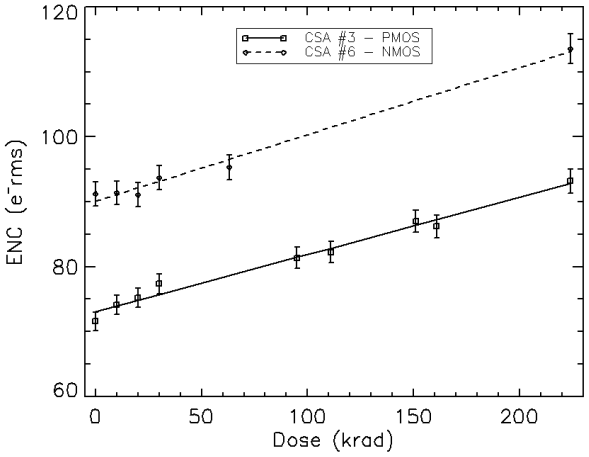

Figure 8: Minimum of the ENC vs. peaking time characteristics as a function of the absorbed dose in PMOS CSA #3 and NMOS CSA #6. Both CSAs are polarized under 200 µA / 3.3 V conditions. A linear function fits both sets of data.

In order to monitor the evolution of the CSAs response following the irradiation campaign, these were annealed for two months at room temperature. No further post-irradiation degradation or recovery was observed, and the circuit characteristics remained remarkably stable.

B. Discussion

In this section, we focus on the analysis of the noise structure for the PMOS and NMOS CSAs, before and after the 224 krad irradiation dose. Results and parameters are derived by fitting the ENC vs. peaking time characteristics data to the following equations 5-8 [10]:

$$ENC_{series}^2 = A \times \frac{C_t^2}{g_m} \times \frac{1}{\tau_P} \qquad \text{(eq. 5)}$$

$$ENC_{//}^2 = B \times \left[2q(il + Ip) + \frac{4kT}{R_R} \right] \times \tau_P \qquad \text{(eq. 6)}$$

$$ENC_{1/f}^2 = C \times \frac{C_t^2}{WL} \qquad \text{(eq. 7)}$$

$$ENC^2 = ENC_{series}^2 + ENC_{//}^2 + ENC_{1/f}^2 \qquad \text{(eq. 8)}$$

Where:

- ENC_{series} is the equivalent series noise charge,
- $ENC_{//}$ is the equivalent parallel noise charge,
- $ENC_{1/f}$ is the equivalent *1/f* noise charge,
- I_p is the total current from the pads as defined in Figure 10,
- *A* and *B* are constants that depend on the filter order,
- *C* is a constant that depends on the filter order as well as technological parameters,
- τ_P is the peaking time.

1) Noise structure in PMOS input CSA

Figure 9 illustrates the ENC vs. peaking time characteristics for the PMOS CSA #3, before and after irradiation. The shape of the curves clearly reveals the high frequency series noise, the low frequency parallel noise and the base level *1/f* noise. Using the AMS CMOS technology parameters, we have fitted the date and derived the total capacitance C_t at the CSA input, the transistor transconductance g_m, the total parallel noise and the *1/f* noise level.

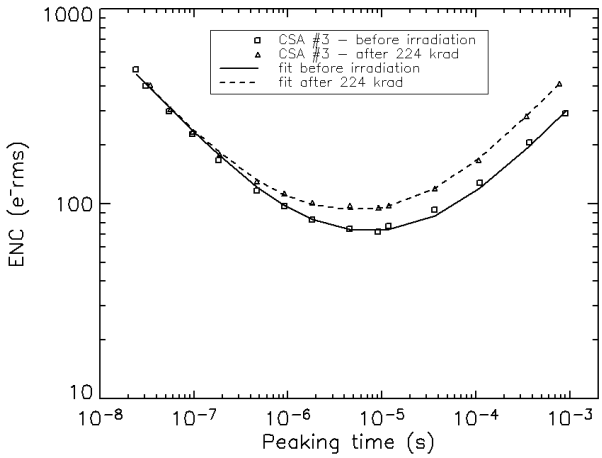

Figure 9: ENC vs. peaking time for the CSA #3 before and after 224 krad of irradiation. CSA #3 is polarized with 200µA current through the input transistor. Lines represent the noise model that fits the data.

We found that the series noise was not affected by the irradiation which means that the transconductance of the input transistor (3.2 mS for 200 µA) remained unchanged with the dose. The total capacitance was estimated to be 6.1 pF. At very low frequencies, the noise is totally dominated by the parallel noise contribution that increases with the dose. This is consistent with the decreasing of the output signal fall-time as it was presented in section IV-A-2. The total current I_{tot}, responsible for the parallel noise, includes the following contributions (see Figure 10 for current definitions):

- The pad leakage current I_1+I_2 (two reverse bias diodes),
- The compensation current *il* driven by V_{il}
- The reset transistor noise, depending on $I_R = I_2 - I_1 + il$

The total current I_{tot} is defined by the following relation:

$$2q \cdot I_{tot} = 2q \cdot (I_1 + I_2 + il + I_R) \qquad \text{(eq. 9)}$$

The current I_R is derived from the CSA output signal fall-time. The current *il* is derived from the CSA #0 output signal fall-time. In fact, since CSA #0 has no pad, I_R is equal to *il*. When V_{il} = 0V in the PMOS case, we found *il* ~ 200 fA before irradiation and ~ 1 pA after being subjected to 224 krad. This increase is probably due to the threshold voltage shift of the NMOS current mirror transistors. As mentioned before, the current through the reset transistor I_R increases and goes from 380 fA to 1.5 pA.

The model fitting of the parallel noise allowed extracting the total current I_{tot}. It was found to be 8.7 pA before irradiation and increased to 17 pA after 224 krad.

At this point in our analysis, we can conclude that the reverse current of the anti-ESD pad diodes is by far the main parallel noise contribution, even if the current through the reset transistor increases more rapidly with the dose.

We also noted that the ENC vs. peaking time characteristics shows a 25% increase of the *1/f* noise with the dose.

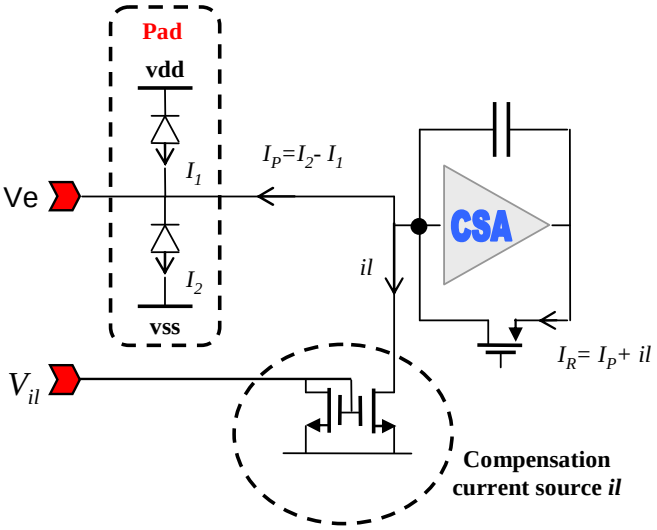

Figure 10: Scheme of the CSA. Definition of the currents: I_1 and I_2 are the reverse bias diode currents of the pad, *il* is the compensation current (or residual current when V_{il} = 0 V), I_R is the current through the reset transistor.

2) Noise structure in NMOS input CSA

Figure 11 illustrates the ENC vs. peaking time characteristics for the NMOS CSA #6, before and after irradiation. We see that the series noise is not affected by the 224 krad irradiation dose. Therefore, the transconductance appears to be stable at ~ 3 mS for 200 µA polarization. Note that the CSA #6 NMOS has exactly the same dimensions as the CSA #3 PMOS input transistor. We saw a similar value of the transconductance g_m for both CSAs, as expected.

At very low frequencies, the noise is dominated by the parallel noise. It increased with the dose because the compensation current *il* had to be raised to ensure CSA #6 proper response. Note that NMOS or PMOS CSAs need the current $I_R = I_P+il$ to remain positive for proper operation. In the NMOS case, this means that the compensation current $|il|$ has to stay larger than the current from the pad $|-I_P|$. The necessity to enforce a positive *il* current in the NMOS CSA seems to demonstrate that the current I_P is negative. In the PMOS CSA, since no adjustment of *il* is necessary, I_P must be positive (see Figure 10 for current sign definition). The current I_P is negative in the NMOS CSA probably because the gate of the input transistor has a much lower voltage (typically 0.5 V) than in the PMOS CSA (typically 2.8 V).

The gate of the compensation current mirror (see Figure 10) was set to V_{il} = 198 mV prior to irradiation and drifted upwards to reach 235 mV after 224 krad. In order to determine the corresponding values of the compensation current *il*, we measured I_R using the output signal fall-time of the CSA #0 for which $I_R = il$. Since all CSAs have the same compensation current source, they all have the same *il*. As mentioned before, the fall-time is directly linked to the current through the reset transistor. We found that *il* was ~ 40 pA before irradiation and ~ 80 pA after.

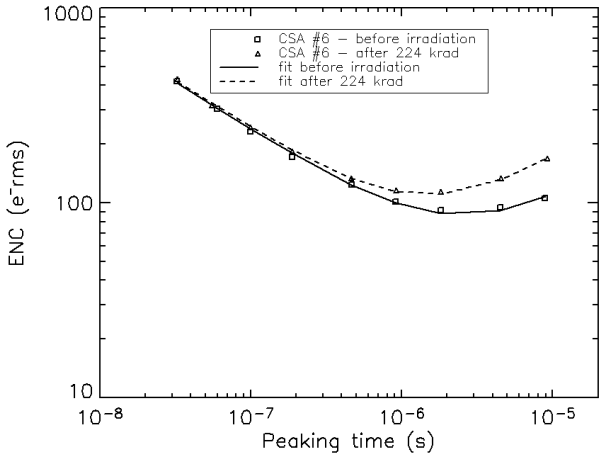

Figure 11: ENC vs. peaking time for the NMOS type CSA #6 before and after 224 krad of irradiation. CSA #6 is polarized with 200 µA current through the input transistor. Lines represent the noise model that fits the data.

Model fitting of the ENC vs. peaking time characteristics for CSA #6 give us the total current responsible for the parallel noise. This total current includes the pad contribution, the compensation current level *il* and the reset transistor noise. We found I_{tot} ~ 80 pA before irradiation and ~ 160 pA after 224 krad. Finally, measuring the output signal fall-time on the CSA #6, we found the current through the reset transistor I_R decreased from 35 pA before irradiation to 2.5 pA after. From all those estimations, we derive $I_1 + I_2$ ~ 5 pA for the pad current before irradiation and ~ 80 pA after irradiation.

The ENC vs. peaking time characteristics shows a 35% increase of the *1/f* noise.

We conclude for the NMOS type CSA #6:

- The main noise source is probably the anti-ESD pad leakage current I_1+I_2.
- This pad current generates a negative I_P which obliges us to use a strong compensation current *il*, leading to an even more important parallel noise.
- The pad current is strongly sensitive to the radiations.

V. Conclusions

IDeF-X is the very first version of our analog front-end electronics mainly devoted to Cd(Zn)Te spectro-imaging

systems in space where low noise, low-power consumption and radiation tolerance are essential design requirements.

We have designed and tested a set of ten very low noise charge sensitive preamplifiers manufactured using the standard AMS 0.35 µm CMOS technology. Depending on the type and size of the input transistors, we could obtain a floor noise ranging from 31 to 49 electrons rms using 3.3 mW of power in the CSA. However, we can obtain almost the same floor noise with a much lower power consumption of 165 µW.

We have identified the PMOS type input CSA as the best candidate for future use in a fully integrated spectroscopic chain. As a matter of fact, its noise level is lower than the NMOS type design and works properly without making use of any compensation current source, limiting intrinsically its parallel noise. Hence, it is well adapted to low current applications with CdTe detectors at room or moderately low temperatures.

Inspired by these results, we used this chip for hard X-Ray spectroscopy at room temperature with CdTe detectors, and obtained a spectral resolution of 1.6 keV FWHM at 59.5 keV with only 660 µW to the CSA. Compared with the ISGRI detectors and ASIC, this represents a spectral resolution improvement of more than a factor of 3.

We irradiated the circuit with a ^{60}Co source up to 224 krad at 1 krad/h dose rate and demonstrated the good tolerance of the design submitted to the total ionizing dose test. We observed a slow increase in the noise level (~30%) for irradiation doses much higher than those of typical space conditions for high-energy astrophysics experiments (~ 1 krad/year). We believe that this increase is primarily due to the standard AMS pads and not to the CSA design itself. We did not expect such a high leakage current in the anti-ESD pads. Future designs will need specific pads with lightened anti-ESD protections to limit their contribution to the parallel noise.

We conclude that the AMS 0.35 µm CMOS technology appears to be well adapted to a low noise and low power consumption analog front end design devoted to high energy spectroscopy with CdTe. Furthermore, our irradiation tests show that this technology is also tolerant to gamma-rays irradiation.

VI. Acknowledgement

The authors wish to thank B. Rattoni from CEA/DRT/FAR/LIST/DETECS for his help during the irradiation tests.

VII. References

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