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Design of fundamental building blocks for fast binary readout CMOS sensors used in high-energy physics experiments

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ABSTRACT

In this paper, design details of key building blocks for fast binary readout CMOS monolithic active pixel sensors developed for charged particle detection are presented. Firstly, an all-NMOS pixel architecture with in-pixel amplification and reset noise suppression which allows fast readout is presented. This pixel achieves high charge-to-voltage conversion factors (CVF) using a few number of transistors inside the pixel. It uses a pre-amplifying stage close to the detector and a simple double sampling (DS) circuitry to store the reset level of the detector. The DS removes the offset mismatches of amplifiers and the reset noise of the detector. Offset mismatches of the source follower are also corrected by a second column-level DS stage. The second important building block of these sensors, a low-power auto-zeroed column-level discriminator, is also presented. These two blocks transform the charge of the impinging particle into binary data. Finally, some experimental results obtained on CMOS chips designed using these blocks are presented.

1. Introduction

Since the early 1990s, CMOS image sensors built using standard commercially available CMOS processes earned more and more customer interest thanks to its characteristics like miniaturization, low power and low cost [1]. The growing demand for CMOS image sensors demonstrates its successful applications in the domain of visible light photon detection.

Meanwhile, in the domain of high-energy particle physics, some future applications and their experimental conditions require to integrate the detecting elements with the front-end electronics on the same silicon substrate. The recent advancements of CMOS sensors make it a promising candidate. The use of CMOS sensors for charged particle tracking was firstly proposed by the Strasbourg group [2]. In these monolithic sensors, 3-T photodiode pixels together with simple analog serial readout were used.

In the application of visible light domain, the photons reach a depth of only a few micrometers inside the CMOS sensor because of their low energy. The charge collection principle of high-energy ionizing particles is quite different from the detection of visible light photons (Fig. 1). The high-energy particles at the Ionizing Minimum (MIPs) penetrate through the sensor and therefore electron–hole pairs will be generated along the particle's track. Only a small part of the active volume near the charge collecting n-well/p-epi diode is depleted. So, the electrons generated in the epitaxial-layer diffuse thermally underneath the readout electronics, until they reach the low-potential region in the n-well. A near 100% fill factor [3], as required in particle tracking applications, is then obtained. The doping gradient results in a potential minimum in the middle of the epi-layer, limiting charge spread. The thickness of the epi-layer is typically about 10 μm, and the signal collected from an MIP traversing the detector is only a few hundreds of electrons. In the case of a high-resistivity substrate without epi-layer, the charges diffuse more laterally and vertically, the n-well/p-substrate diode collects less charge consequently. Note that, in twin-tub (double well) processes, PMOS transistors being fabricated in n-wells, only NMOS transistors can be used in this type of pixel aiming at charged particle detection. The pixel pitch needed in this domain is often above 10 μm.

Full digital output data and on-chip real time data processing are required for future high-energy experiments like the vertex detector of the future international linear collider. In this paper, design details of the basic components of a fast, binary readout CMOS Monolithic Active Pixel Sensor (MAPS) will be presented. The all-NMOS pixel presented in Section 2 is the first key element of such a monolithic sensor. The second basic block, a high-speed, low-power auto-zeroed discriminator (comparator) realized at the end of each column will be presented in Section 3. These two blocks transform the charge of the impinging particle into binary data.

The blocks described in this paper were successfully used in fast binary readout prototypes designed in two different CMOS

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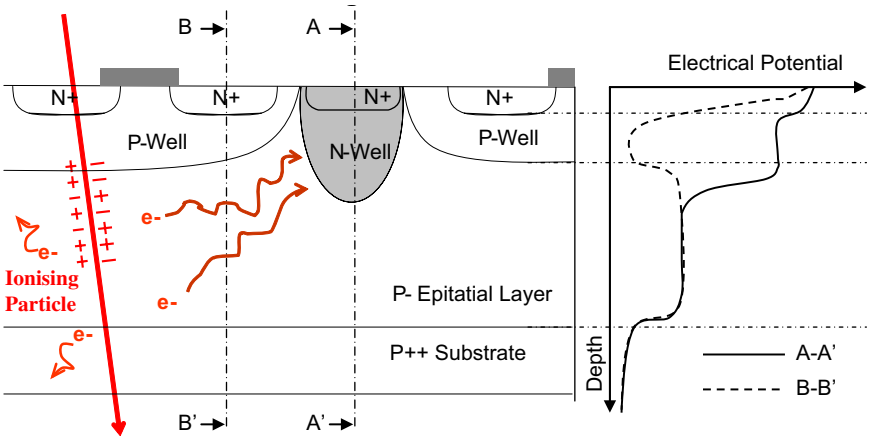

Fig. 1. Principle of charge collection in photo-diode type CMOS sensors.

processes: The first on the TSMC 0.25 μm CMOS digital process without analog options, and the second on the AMS 0.35 μm CMOS process with different substrate types. Some experimental results obtained on these chips will be given in Section 4.

2. Pixel design

To integrate on-chip data sparsification (or zero suppression) with fast readout, the classical CMOS 3-T photodiode pixels need several modifications. Firstly, (correlated) double sampling (DS) is required to suppress the reset noise of the small diode capacitance. Also all the pixel-to-pixel and column-to-column process related transistor offset non-uniformities (fixed pattern noises-FPN), which would be of the order of the signal generated by an impinging particle, have to be suppressed inside the pixel. The maximum achievable Charge-to-Voltage Conversion Factor (CVF) is limited to $\sim 20\,\mu V/e^-$ with n-well/p-epi diodes in mainstream CMOS processes. This is not sufficient to overcome the residual noises, even after correction with DS. In order to increase the *Signal-to-Noise* ratio (S/N), the detector signal must be amplified *as close as possible* to the charge collecting diode.

2.1. Reset noise suppression

Some methods have been presented in the literature to reduce or remove the reset noise of 3-T photodiode pixels [4–10]. While these methods are theoretically efficient, they need often long durations of the reset for a good reduction of noise, and in practice present high FPN due to the increased number of transistors and capacitors used inside the pixels.

The reset noise suppression method proposed in [4] consists of the use of a serial capacitor, a switch and a source follower (SF) to store the reset level of the detector capacitance in the pixel. This pixel could be used for charged particle tracking, if some issues are addressed. The high readout rates required in most of the high-energy physics experiments (integration times of at least a few tens of μs/frame) and the 100% fill-factor property of the pixel with an n-well/p-epi diode give the opportunity to store easily the reset level of the detector on an in-pixel analog memory. The pixel presented here is based on this architecture (Fig. 2), but several important changes were made to the pixel presented in [4]. Firstly, a simple n-well/p-epi diode with reset transistor as the detector was used instead of a photodiode with readout floating capacitor separated by a transfer gate. In fact, as the transfer transistor operates in the sub-threshold regime, a charge transfer problem occurs in this pixel [11,12]. Very long integration times are needed for an efficient transfer, which are not possible in our applications. To increase the CVF and improve the *S/N*, an amplifying stage was used instead of the first SF. A basic common-source (CS) stage with diode-connected NMOS load is the simplest way to realize this amplifier (Fig. 3). The CS stage is switched instead of continuous bias of the SF, in order to save power consumption. The small-signal voltage gain of this amplifier is given by

$$v_{out}/v_{in} \cong -g_{m1}/g_{m3} \quad (1)$$

where g_m is the transconductance of the MOS transistor. The simulations show that a gain of about 10 can be obtained keeping a reasonable dynamic range. To remove the offset voltages of the output SF, its offset is sampled externally during the measure of reset level of the detector on the in-pixel serial capacitor. To increase the readout speed, the gate voltage of the output SFs bias transistor is switched. This limits signal variations on the column bus by avoiding the bus capacitance discharge. In this pixel, all the signal swings were reduced to maximize the readout speed.

The key points of the design are as follows:

- The reset transistor should remain in linear region for a fast reset (called 'hard reset').
- The MOS capacitor (MOSCAP) should remain in inversion for better linearity.
- The CS stage should remain in appropriate operating region.
- The second switch transistor should remain in linear region for a fast reset.
- The SF should remain in appropriate operating region.

The choices of the diode voltage V_{r1} and the clamping voltage V_{r2} are very critical to satisfy these requirements.

2.2. Noise sources

The main temporal and FPN sources of this pixel are well known: All the noises generated by the first switch transistor (thermal noise, low-frequency noise, channel charge injection, clock feed-through etc.) and sampled on the detector capacitance are removed through in-pixel correlated double sampling (CDS) circuitry. The offset of the CS stage is also removed through CDS. It should be noted that the CDS doubles its thermal noise power [13], and the $1/f$ noise is not removed. However, as a high CVF is obtained close to the detector, input referred noise remains small. The thermal noise generated by the second switch and sampled on the MOSCAP is not removed, but this noise is small compared to the other temporal noises. The channel charge injected by this switch and the clock feed-through are removed through DS

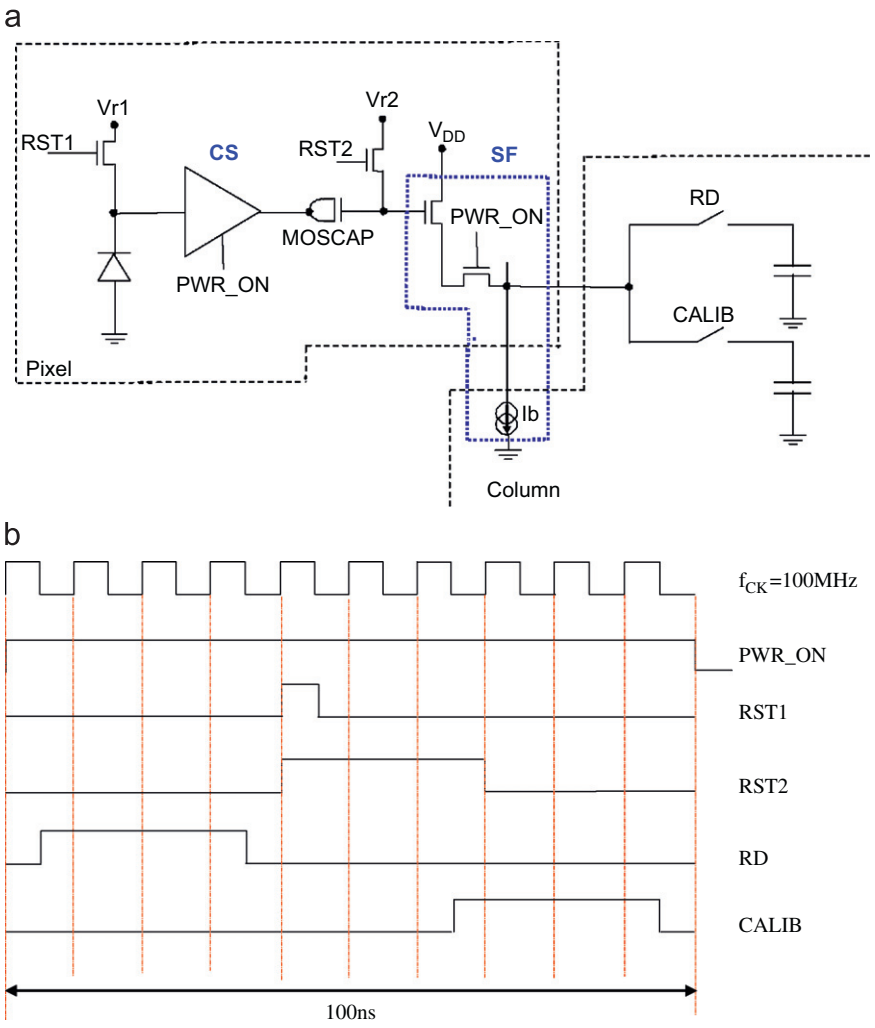

Fig. 2. (a) Schematic of the proposed pixel and, (b) related timing (clocking stimuli) with $f_{CK} = 100$ MHz.

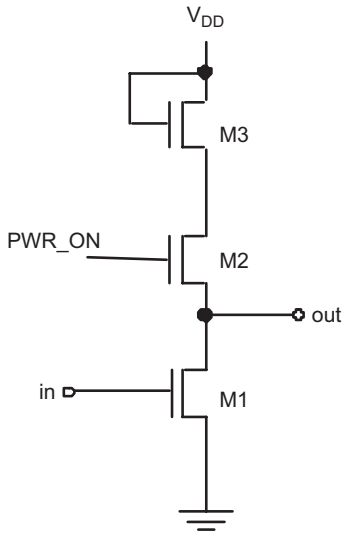

Fig. 3. The simplest realization of the in-pixel amplifier: a common source NMOS amplifier with diode-connected load transistor.

(not correlated), provided that the reset level of the input of the SF after RST2 is constant for successive resets in the same pixel. This is the case if a "clean" power supply for the pixel is provided. The offset and $1/f$ noise of the SF are suppressed through column-level CDS, and the thermal noise power is doubled.

3. Column-level offset-compensated low-power discriminator

The comparator (or discriminator) transforms the output analog signal of the pixel into a 1-bit digital code by comparing it to an external threshold level. Considering the small value of analog signal (which means that the sensitivity of comparator has to reach a few hundreds of μV), the offset mismatches resulting from various sources and the very high signal processing speed (the period is the same as the readout time of a pixel), the design of this comparator is not a trivial task.

For the comparator design, it is mandatory to use an offset compensated amplifying stage, which corrects the intrinsic offset of comparator. Two main techniques are widely used: the IOS (Input Offset Storage) and the OOS (Output Offset Storage) [14]. Considering the advantages and the draw-backs of both IOS and OOS architectures, a combination of them has been chosen to realize the high-speed column level comparator. The block diagram of this comparator, consisting of an auto-zeroed pre-amplifying stage and a dynamic latch, is shown in Fig. 4. It is a modified and improved version of the previous design presented in [15]. The total input referred residual offset of this comparator

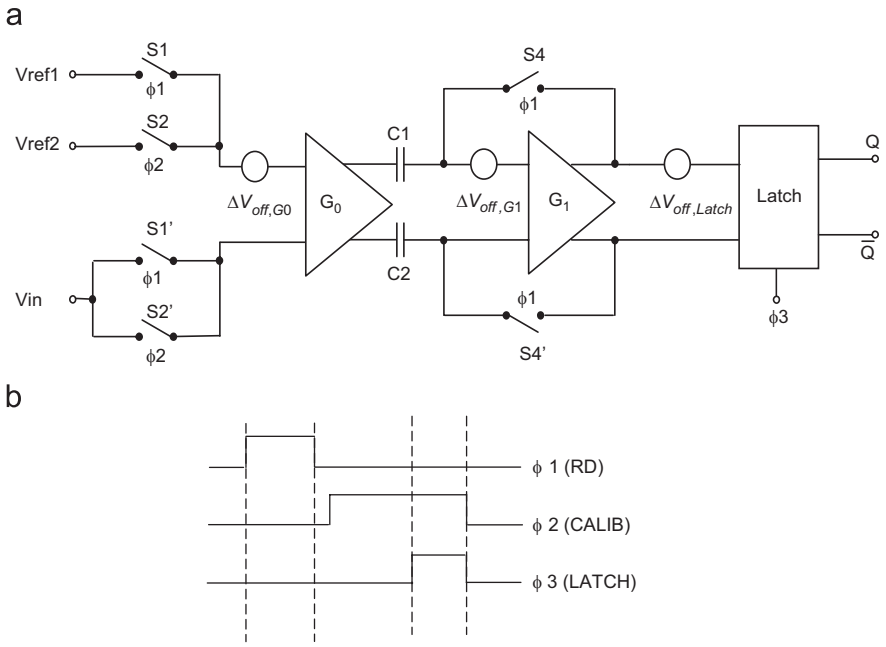

Fig. 4. Block diagram of offset-compensated column level comparator: (a) architecture and (b) timing diagram (not to scale).

is given by

$$V_{OSR} = \frac{\Delta V_{off,G1}}{G_0(1+G_1)} + \frac{\Delta Q}{G_0 C} + \frac{\Delta V_{off,Latch}}{G_0 G_1} \quad (2)$$

where G_0 and G_1 are the static gains of pre-amplifiers, $\Delta V_{off,G1}$ and $\Delta V_{off,Latch}$ are respectively, the input-referred offsets of preamplifier 1 and latch, ΔQ is the charge injected mismatch from S4–S4′.

A more detailed schematic of the comparator is shown in Fig. 5. The cascade of low-gain differential gain stages allows high operation speed together with high pre-amplifying gain. The input switches were modified to sample voltage signal values. If MOS capacitors are used in a digital process, to obtain a good linearity, the capacitors have to be biased in the deep inversion regime. SFs as level shifters before capacitors were used for this purpose. These SFs increase the operation speed by lowering the output impedances of the gain stages. The gain stage used in the comparator is shown in Fig. 5b. This is a very simple differential amplifier with diode-connected PMOS transistor loads. The static voltage gain is about 4. The cascade of four gain stages guaranties a total gain of above 200. The output common voltage of this amplifier being well-defined, it does not need a common-mode feedback circuit. The detailed schematic of the dynamic latch used is shown in Fig. 5c. A dynamic latch is very fast and has no static power dissipation.

The total static power dissipation of the comparator is $70\,\mu A \times 3.3\,V \cong 230\,\mu W$.

Three phases are needed for a complete offset auto-zero and pixel output stage offset cancellation:

- Firstly, when $\phi 1$ is activated, S1–S1′, S3–S3′ and S4–S4′ are switched on, S2–S2′ are switched off. During this time, the offsets of the gain stages are memorized in C1–C1′ and C2–C2′. Besides, $\phi 1$ is equivalent to the RD phase used to read out the signal level of the pixel (Fig. 2), this signal is also amplified and stored in C1–C1′. Moreover, this signal includes the non-corrected offset of the in-pixel SF which varies from one pixel to another. This offset is corrected during next phase. The external threshold value (Vref1) of the comparator is also sampled during this phase.
- When $\phi 2$ is activated, S2–S2′ are switched on, the other switches are switched off and the comparator enters its auto-zeroing mode. As $\phi 2$ is equivalent to the CALIB phase of the pixel, the pixel output stage's offset value is readout once and automatically used to compensate the offset value stored in C1–C1′ capacitors during $\phi 1$. The threshold common mode value (Vref2) of the comparator is also sampled during this phase and is compared with the pixel output signal value. The effective threshold value is $\Delta Vth = Vref1\text{-}Vref2$.
- At last, the activation of $\phi 3$ (LATCH), while $\phi 2$ is still activated, activates the latch, which rapidly amplifies the difference between the pixel output signal and the comparator threshold level. A logical signal is given according to the difference. If the difference is positive, the output of latch is 1; on the contrary, it is 0.

In addition to compensation of the pixel output stage offset and the offsets of amplifiers, the charges injected by the switches used in comparators and the parasitic effects related to substrate coupling in the mixed-signal environment are also effectively reduced thanks to the fully differential architecture.

4. Chip implementation and experimental results

Using the two blocks described in the previous sections, two chips with very similar architectures were designed on two different CMOS processes. The first process used is the TSMC 0.25 μm CMOS digital process featuring ~8 μm epi-layer (MIMOSA8 chip), and the second is the AMS 0.35 μm CMOS Opto process without epi-layer (MIMOSA16). The latter has the advantage of being a mixed-signal process featuring poly–poly capacitors.

Each chip includes a serially programmable sequencer, an array of 128×32 pixels, 24 column-level comparators and a serialization logic block. Eight columns of pixels are output directly to

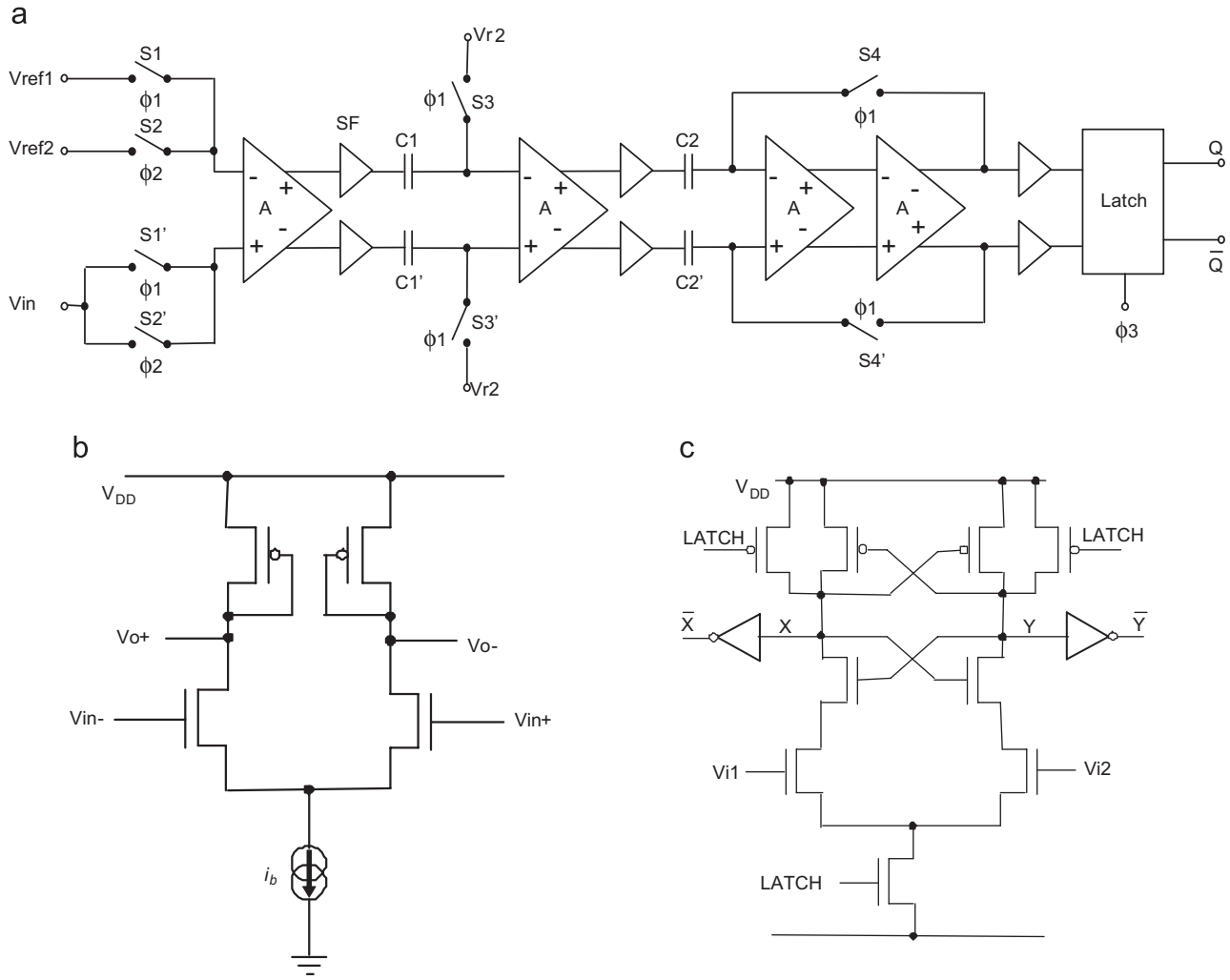

Fig. 5. (a) Detailed schematic of the offset-compensated discriminator, (b) detailed schematic of the gain stage, and (c) detailed schematic of the dynamic latch used in the discriminator.

characterize the pixels. The imager arrays consist of 4 different sub-arrays of 32×32 pixels with different diode sizes. The pixel pitch is $25\,\mu m \times 25\,\mu m$ for the whole array. In the TSMC 0.25 μm digital process, MOS capacitors were used in the comparators. The dimensions of the comparators are $\sim 220\,\mu m \times 25\,\mu m$ in both the designs. The logic part is behind the objectives of this paper and details can be found in Ref. [17].

The chronogram applied to the pixels and comparators is the combination of the chronograms shown in Figs. 2b and 4b with 16 clock cycles (160 ns). The chips were optimized to work at a clock frequency of 100 MHz, leading to a readout speed of ~20 μs/frame (50,000 frames/s).

Firstly, thanks to the test comparator separated from the pixel array, the comparators were characterized thoroughly. Once the chip is programmed, the control signals needed for the comparator are also available. The inputs of the comparator are shorted to a common-mode voltage and different threshold voltages are applied (Fig. 6a). In this case, the comparator responds on its own temporal noise and offset. The threshold voltages are generated by a precision voltage generator. A digitizing scope is used to visualize the output of the comparator and also to compute the average number of "1" over a significant number of cycles for each threshold value. In this way, the most important characteristic of the comparator, the transfer curve is obtained. Then one can fit an *error function* (*erf*) to this curve; its derivative gives a gaussian (normal) distribution. The full width of the gaussian curve at half the maximum is $\sim 2.35\sigma$, and its mean gives the offset of the comparator, where σ is the rms temporal noise. Fig. 6b shows a typical transfer curve measured on a test comparator at $f_{CK} = 100$ MHz from MIMOSA8. The corresponding values for this curve are $\sigma = 0.2\,mV_{rms}$, $V_{offset} = 0.25\,mV$.

As we have only one test comparator on each chip, to have an idea of the dispersion of residual offsets (FPN), the offsets of the test comparators for *different* chips available were measured. The results are shown in Fig. 6c. We notice that the fluctuation of offsets between different comparators is very small, only about $0.22\,mV_{rms}$. This value is well below the temporal noise of the pixel.

The basic parameters of the pixels, temporal noises, FPNs, CVFs and Charge Collection Efficiencies, were characterized in laboratory tests with a dedicated test bench. The two latter were obtained using an ^{55}Fe X-ray source. The output temporal noise value is $\leqslant 0.9\,mV_{rms}$ for MIMOSA8, and $\leqslant 0.7\,mV_{rms}$ for MIMOSA16, which correspond to an input refered noise of 11–16e^-. The noise values were verified up to $f_{CK} = 150$ MHz, and no significant change was observed for both chips. The FPN, dominated by the FPN of comparators, is well below the temporal noise values. The CVFs were measured using the ^{55}Fe X-ray source with the method described in Ref. [16]. They are typically about $50\,\mu V/e^-$. The CCE, as expected, is lower for the process without

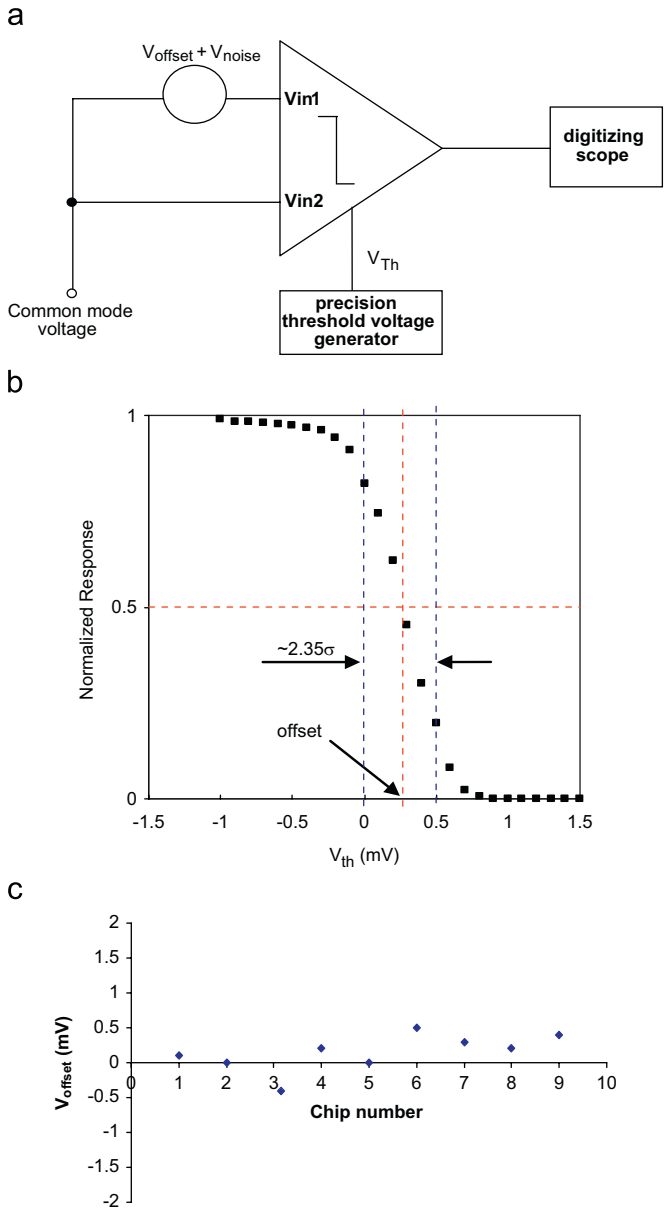

Fig. 6. (a) Test system with its precision threshold voltage generator, a digitizing scope and the comparator, (b) normalized noise response measured on a comparator, and (c) offset dispersion of comparators on different MIMOSA8 chips ($f_{clock} = 100$ MHz).

epi-layer. In this case, only a small part of the charges generated in the high-resistivity substrate are collected by the diode, as already explained in the introduction. Larger diodes are necessary in this process to get a reasonable CCE, increasing the input-referred noise. The chips were also tested at CERN using a 180 GeV/c positive pions beam. A spatial resolution better than 7 μm was obtained on binary outputs with the two chips. The complete test results of these chips can be found in Refs. [17–19].

5. Conclusions and perspectives

Fundamental building blocks for fast CMOS monolithic sensors with discriminated outputs suitable for high-energy physics experiments were presented. In these blocks, on-chip analog offset correction techniques are used extensively to suppress process related mismatches. These two blocks transform the charge of the impinging high-energetic particle into 1-bit digital data, allowing on-chip data sparsification and zero suppression.

The blocks described in this paper were successfully implemented in two commercially available CMOS processes. MIMOSA8 is the first fast successful monolithic CMOS sensor prototype with integrated signal discrimination developed for high-energy physics applications. Its architecture is a good candidate for the vertex detector of a future linear collider. A spatial resolution better than 7 μm was obtained with MIPs on binary outputs with pixels of 25 μm pitch using column-level discriminators. In the near future, to improve the spatial resolution, it is planned to replace these discriminators by column-level 4 or 5 bits ADCs. Several ADCs are under development by different groups.

CMOS processes with ~10 μm epi-layer thickness seem to be a good compromise for high-energy physics applications. Larger epi-layer thicknesses donot improve the spatial resolution, the generated charge by the impinging particles diffusing more laterally and not vertically.

A larger chip based on these blocks presented will be designed in collaboration with the Strasbourg group for the beam telescope of EUDET-JRA1 project, which will be installed at DESY (Hamburg) in 2009. This chip will also include on-chip digital zero suppressing circuitry.

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