Chapter number

Total Dose and Dose Rate Effects On Some Current Semiconducting Devices

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1. Introduction

This chapter will overview some of the aspects of Total Ionizing Dose and Dose rate Effects On Semiconducting Devices especially those used in High Energy and Radiation Physics. First material aspects and interaction of Ionizing Radiation with Matter will be reviewed with emphasis on defect creation and carrier generation. Radiation induced defects are detrimental to device operation but electron-hole pair generation by impinging particles is the basis of all semiconductor detectors. In a second stage, problems related to transistor devices will be discussed with particular emphasis gate oxide issues and on Silicon On Insulator technologies, radiation hardened by design. Although some of the phenomenological physics and chemistry related to ionizing irradiation and its effects on MOS oxides, were reviewed by Oldham (Oldham, 1989) and earlier authors (Ma & Dressendorfer, 1989), there is no finalized view of defect physics and chemistry in the device oxides, mainly because the related problems are very complex. However, most of the experiments regarding ionizing irradiation effects on electronics were made both at room temperature or above and at a relatively high dose rate (Messenger & Ash, 1986). For some present day practical applications in space or in high-energy physics low dose rates effects were important and are investigated to usefully complement single event effect studies. Effects at lower temperatures were scarcely investigated (Saks et al., 1984) leading to a rather piecemeal knowledge of transport of photo-generated carriers and as so for the activation energies of deep defects centers. As most important devices are silicon based, ionizing radiation effects studies of bulk silicon were made very early (Willardson, 1959; Sonder & Templeton, 1960; Cahn, 1959; and the Purdue Group). This is of special importance for silicon detectors or other semiconductor detectors. Many good studies and reviews were made on semiconductors detectors mainly in the framework of LHC experiments (Wunstorf, 1997; Leroy, 2007). In the last part of this chapter progress made on new pixel detectors such as CMOS sensors will be reviewed because they constitute a very active field of research and development.

2. Interaction of Ionizing radiation with a semiconductor material

2.1 Energy deposition and electron-hole pair generation

The interaction of radiation and both non-ionizing and ionizing will be the starting point of this discussion. The main issue is related to the damage generated in the materials both by the non-ionizing and ionizing irradiation. These can be classified as permanent effects as they have a long lasting influence in the materials (a few minutes to many years). Other effects should be regarded as transient effects, and have many consequences and applications. Ionization generates electron-hole pairs, which in a semiconductor are charge carriers and may be used for device operation, such as particle detectors. Generation of carriers can occur in a semiconductor with photons of energy of the order of the bandgap. At higher energies, electrons from inner shells are excited and result in a high number of photo-generated carriers. Similar processes occur with other charged particles, the total number of generated electron-hole N pairs being given by a simple expression:

N=Ed/Eg (1) where Ed is the total energy deposited and Eg is the direct bandgap.

In practice most of these pairs recombine, either directly or indirectly. An applied electric field to the device may dissociate these pairs and lead for a semiconductor detector to a current flow that can induce a signal through the Ramo-Shockley theorem. Silicon, Germanium, Diamond counters, and other compound semiconductor detectors operate on this principle and have limited bulk sensitivity to Total Ionizing Dose (TID), but are most of the time very sensitive to Non-Ionizing-Effects.

The interaction of photons in the keV energy region with silicon dioxide results in the generation of electrons-hole pairs that dissociate in the presence of the electric field applied to the oxide in the case of a MOS gate oxide. In the case of charged particles with sufficient energy like protons, alphas, electrons, pions or so, the interaction with the oxide also generates electron-holes pairs according to ionization models originating in the Bethe-Bloch theory (Bethe, 1930,1934).

The Bethe-Bloch formula is valid at relatively large energies whereas in the lower range of energies, LSS (Lindhard,Scharff,Schiott, 1963) and Ziegler models should be taken into consideration.

$$\frac{-dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_ec^2\beta^2\gamma^2T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right] \quad (2)$$

Where T_{max} is the maximum energy transmitted to a free electron in a collision, $\delta(\beta\gamma)$ is the density effect correction to ionization energy loss, the mean excitation energy which value can be derived experimentally, related to oscillator frequency, the other parameters being having their normal physical meaning. Ziegler published a review (Ziegler, 1988) of the detailed stopping laws derived from the original Bethe-Bloch formula. Except at very low energies where LSS models hold with a dominant contribution of nuclear collisions, most of the energy deposited result in ionization. This leads to applications in radiation detection and also to many detrimental effects on semiconducting devices exposed to harsh ionizing environments. These effects together with the efforts devoted to overcome them have been studied for many decades (since the early sixties), with the advent of the satellite era. Thus, except for some recent applications in high-energy physics, most studies were motivated by spatial or military purposes. Therefore, whatever particle is responsible for the energy deposition, the results are expressed in terms of Total Ionizing Dose (TID) with units most often derived from the Gy(Si) or the rad(Si). A diagram summarizing the effects of irradiation on materials is proposed below. Both ionizing irradiation, charged particle effects and neutral particle (Non Ionizing) effects are taken into consideration (Fig. 1). The results are mainly lattice defects that have an impact on the properties of the material.

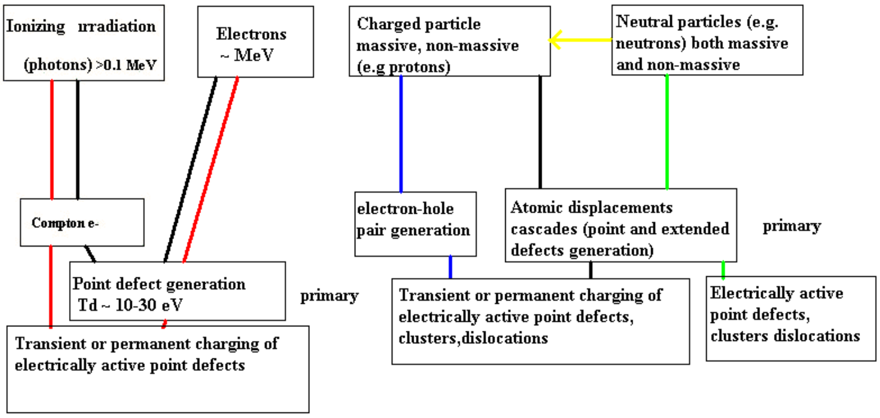


Fig. 1: Diagram summarizing the effects of ionizing irradiation, charged particle and neutral particles on matter with no annealing considered.

2.2 Creation of defects by ionizing radiation

The point that should be discussed is whether ionizing irradiation creates directly or not point defects in the material. At high enough energy (~1 MeV) the impinging particles will create energetic electrons or nuclear recoils that should result in atomic displacements (Fig. 2). This is valid either for uncharged or charged particles (neutron and protons, respectively). Defect creation has been reported even for neutrinos (Brüssler et al., 1989). Depending on the recoil energy single displacements or a displacement cascade will occur leading to the appearance of point or extended defects respectively

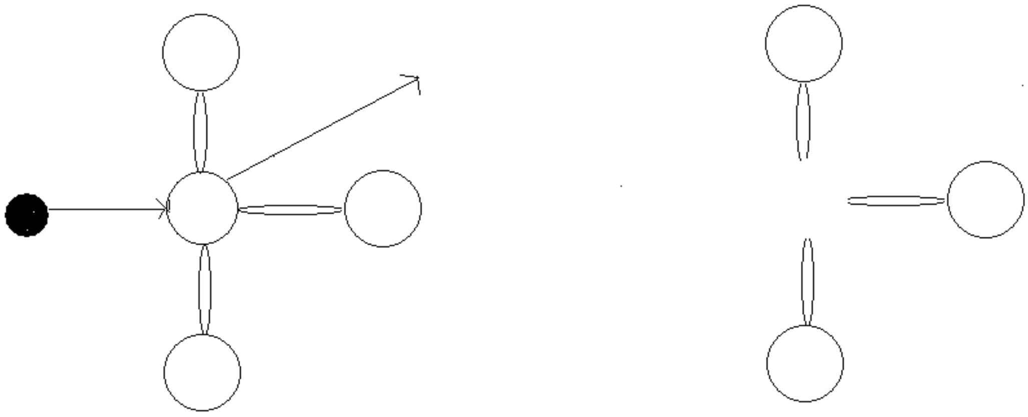


Fig. 2: sketch of an interaction of a particle (charged or neutral, black on the schematic) with an atom in a plane lattice. A vacancy is created. Depending on the energy of the primary-knock-on the interstitial is ejected close to the vacancy and induces a Frenkel pair or result in a displacement cascade

Point defects such as vacancies or interstitials are not always stable in semiconductors such as germanium and silicon. Experiments with electron irradiation show a different picture when made at room temperature (300 K) or at very low temperature (Mooney et al., 1983).The comparison with non-ionizing irradiation (neutron) shows a very close behavior (Fourches et al.,1991), because extended defect generation has a weak influence (Fourches,1995). Direct defect creation by ionizing particles such as electrons was widely studied because of fundamental considerations, but purely ionizing effects in semiconductors due to photons and defect creation due to photons has not been investigated so extensively (Sonder and Templeton,1960). For purely ionizing radiation such as gamma rays, this effect is clearly limited even in very sensitive HPGe detectors used for photons detection. In contrast, these materials are prone to degradation under non-ionizing irradiation, even when a very low fluence is considered (a few 10^{9} /cm^{2}) (Fourches et al.,1991a,1991b). These non-ionizing irradiation effects are often expressed in terms of non-ionizing energy loss (NIEL) in order to reduce the damage effects to a global parameter independent of the nature of the impinging particles. These are still the basis of many studies devoted to device and process development. Recent studies made in silicon for high energy developments or CMOS device improvements have resulted in some new data on the defect introduction rate of Co^{60} irradiated silicon. According to Pintile et al. (Pintille et al. 2009), the introduction rate for room temperature induced interstitial related defect in silicon is of the order of 10^{3} cm^{-3}/rad. This means that to obtain defect concentrations of the order of 10^{10} cm^{-3}, the TID should reach 10^{7} rad (10 Mrad (Si)) which is a very important TID. This has two consequences. First, this means that the integrated photon flux required to degrade very defect sensitive detectors such as HPGe detectors is of the 10^{16}/10^{17} cm^{-2} which is a high value compared to other particle effect introduction rates (Fourches et al. 1991).

Direct defect creation by photons at least in the MeV range should be considered as a negligible effect with respect to other massive particle defect production. Even in silica widely used in MOS devices, the defects directly induced by irradiation are in negligible concentrations compared to precursors (oxygen vacancies for E′ centers) as long as ordinary oxides are considered. This is the reason all the studies of ionizing radiation effects in MOS oxides focus on defect charging and charge carrier migration and annealing mainly observed through electrical measurements.

2.3 Defect transformation and annealing : device implication

Most devices using semiconductors operate at room temperature with the notable exception of cryogenic detectors such as HPGe. The concentration of defects in a material such as silicon, germanium and silicon dioxide depends significantly on the annealing processes of elementary defects created during irradiation. Most of the defects investigated are point defects as some of the experimental models used until now were simpler than for many atom defects such as dislocations and vacancy clusters (voids). Moreover, ionizing irradiation studies have focused on electrical measurements either of macroscopic physical quantities or on the investigation of thermal relaxation behaviors, leading to the estimation of activation energies. The picture of the irradiated material is such that only a fraction of the defects introduced by irradiation remains in a stable form at room temperature. This has been established in a variety of semiconducting materials both elemental and compound. Most stable defects both in germanium and silicon are divacancy or vacancy related. Some doubt still exist in germanium because of the lack of symmetry sensitive experimental results such as uniaxial stress DLTS or ESR. Interstitial related defects were detected in later studies (Song et al. 1989) in silicon and interstitials related defects in germanium (Carvalho et al., 2007) were not clearly identified.

3. Devices questions and issues

3.1 Ionizing irradiation issues

3.1.1 Semiconductor detectors (new detector issues)

In the last twenty years, many groups undertook empirical investigations in order to determine the behavior of semiconductor detectors damaged by ionizing and charged particles. Most of these studies focused on detector characteristics directly related to operational performance. The huge leakage current increase observed after irradiation has a great impact on the power management and furthermore the most important characteristic affected is the charge collection efficiency. The charge collection efficiency depends on the concentration of deep traps localized in the fiducial (i.e. the sensitive) volume of the detector (sensor). They act as recombination or trapping centers. In the full depletion mode often used in semiconductor or semi-insulating detectors the defects act as carrier generation centers. The bulk-generated carriers are responsible for the bulk leakage current of the detectors, surface leakage current related to ionization induced defects at the interface dominates in Si silicon detectors/sensors passivated by silicon dioxide. This is strong evidence for these effects in CMOS (Monolithic Active Pixel Sensors) sensors recently under investigation. (Fourches et al., 2009) in which sensitivity to ionizing (gamma ray) radiation was compared to the sensitivity to neutron irradiation (Fig. 3). Clearly, the CMOS sensors are very sensitive to bulk damage, this being only dependent on the material characteristics and the bias scheme, these devices not being bias in the depletion mode. Ionizing irradiation effect (TID) can be strongly reduced by process and layout improvements (Ratti et al.).For other pixel detectors, in order to match future SuperLHC requirements, tolerance to TID and bulk damage can be enhanced by using structures that reduce the charge collection length (i.e; the average length taken by one carrier to be collected by the electrodes), using TSV (Through Silicon Vias). Defect engineering has been fruitful to reduce the sensitivity to structural defects of many silicon detectors through impurity density modulation. Fewer results were published concerning high-purity germanium detectors for which early efforts were significant. Published results seems to show that annealing is not complete, although radiation induced point defects anneal out circa 200°C (Mooney et al.,1983; Fourches et al.,1991) , clusters and other extended defects remain in the bulk of the crystal and only disappear at higher temperatures (Kuitunen et al.,2008). Other materials are used for semiconductor detectors, but have not attracted so much interest in terms of radiation tolerance. Diamond is the case in point but recent investigations were scarce [Velthuis, 2008]. Their potential high radiation hardness is the result of higher atomic displacement energies, than in silicon for instance and also of a higher bandgap which result in less electron-hole pairs generated. Applications are sought for LHC upgrades. III-V materials were also investigated (Bourgoin et al. 2001) In present times there is no definitive choice of either material or detector technology for future application in HEP, with regard to radiation hardness issues.

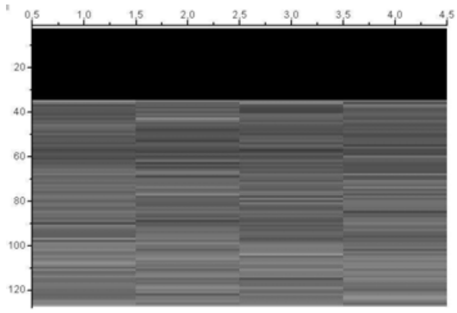
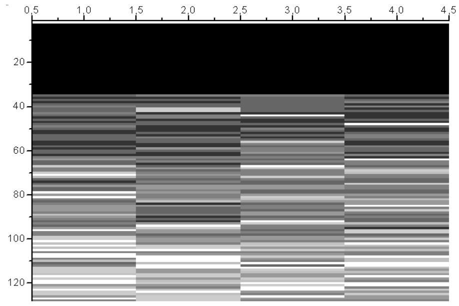


Fig. 3: comparison between ionizing (upper) and neutron (lower) irradiated pixels arrays. Note the uniform effects of ionizing (gamma) irradiation (after Fourches et al., 2008).



3.1.2 Microelectronic devices issues

The use of microelectronic devices, circuits, and processes in harsh ionizing irradiation environments is common for many decades now. Efforts were pursued many years during to obtain processes less sensitive to TID, Dose Rate Effects, and Single Event Effects (SEE) such as Single Event Upset, Latch-up, both destructive or non-destructive, and Single Event Gate Rupture. A lot of review papers and books exist on that subject this paragraph will emphasize only on the key technological advancements and on the TID effects that are the dominant problem in accelerator-based experiments. SOS technologies and subsequent SOI technologies were first developed to overcome SEE with great success but some progress in purely bulk processes made possible high radiation hardness. Downscaling the device dimensions along with the Moore's law has decreased the sensitivity to TID provided special layout design precautions are taken. Most of the problems related to ionizing irradiation sensitivity are linked to MOS devices although bipolar and JFETs can be affected by TID (Fourches et al., 1998; Citterio et al. 1995; Dentan et al.1993,1996). Former MOS devices required gate special gate oxides, which were engineered in order to limit the total bulk positive charge induced by ionizing irradiation. Careful oxidation of the silicon has allowed a reduction of Pb (Pending Bonds) centers and theretofore to a reduction of the interface charge. This results in a lower Threshold Voltage Shift (Fig. 4). It is also sometimes necessary to use closed shape MOS structures to limit leakage current especially for bulk processes.

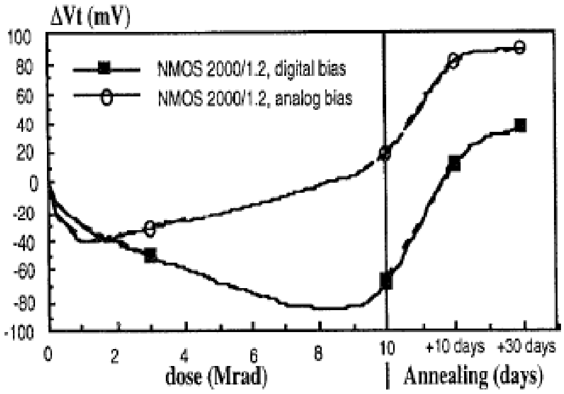


Fig. 4: Threshold voltage shift versus Total Ionizing Dose of a typical DMILL SOI NMOS device with different biasing schemes applied (out of M.Dentan et al.,1996). Digital bias corresponds to a nil source-drain voltage.

The R&D efforts made by many teams around the world have resulted in a very high radiation tolerance for n-channel SOI devices as well as p-channel ones. This has been confirmed during the development of the DMILL technology.

3.2 MOS device hardening issues

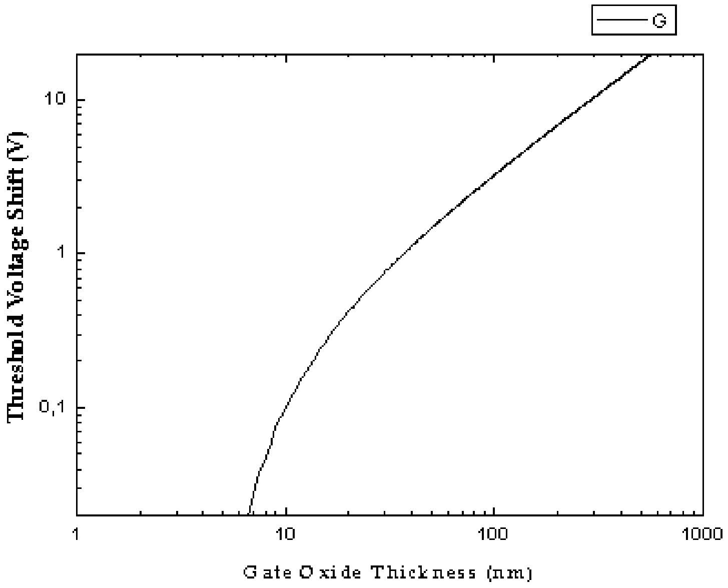


Fig. 5: Absolute threshold voltage shift versus gate Oxide Thickness (in nm) for a 100 krad Total Ionizing Dose received assuming the conditions introduced in the text.

The radiation hardness increases along with the reduction of the oxide thickness, this being first observed in the 1970s and confirmed later (Saks et al., 1984). Simple models derived from classic carrier tunneling from a defect level and first used by Manzini and Modelli (Manzini & Modelli, 1983) in the reliability context show that the sensitivity to TID is negligible up to a few Mrads for oxide thicknesses less that 5nm, which are common in modern sub-micronic MOS low voltage processes.

Using the analytical expression published by the original Manzini and Modelli paper one can compute the threshold voltage shift of a MOS device versus oxide thickness for a given TID. Total Ionizing Dose received assuming realistic e-h pair generation energies and total hole trapping with no electron trapping in the whole volume of the gate oxide. Figure 5 summarizes the results. A commercial computer code was used to obtain numerical results using a trapping depth of the order of 0.18 eV.

3.3 Total dose and dose rate effects; electronic devices

3.3.1 Ionizing effects at moderate cryogenic temperatures

Many applications require the operation of nano-microelectronic devices below room temperature. In the nineties, I and some of my colleagues embarked on the possibility of making a SOI process suitable for 90 K operation. n-channel and p-channel MOSFETs had very good characteristics at these temperatures, making these devices usable for amplifier and detector signal readout applications (Fourches et al., 1997). The questions arising were related to the TID radiation hardness at these temperatures. I embarked in a thorough study of the effects of ionizing dose, dose rate effects, annealing and geometric effects. Fig. 6 and 7 demonstrate clearly the existence of favourable dose rate effects in the sense that a reduced dose rate results in a less important Vth shift at equivalent total ionizing dose.

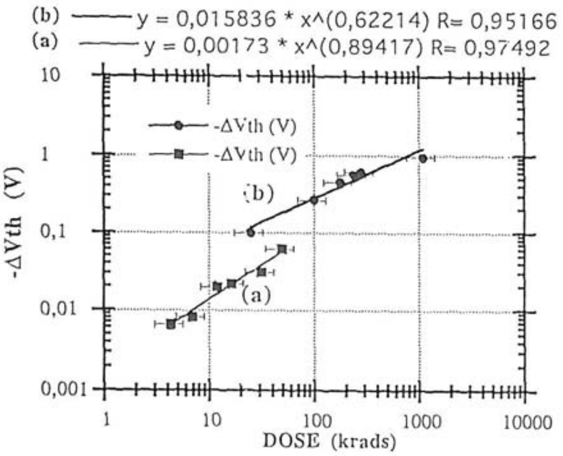


Fig. 6: Threshold voltage shift versus TID for different dose rates (a) low dose rate, (b) high dose rate. (b) high dose rate (50 krads/hour), (a) low dose rate 0.018 krads/hour both made at ~ 80 K on n-channel devices.(a + 5 V bias was maintained on the gate).

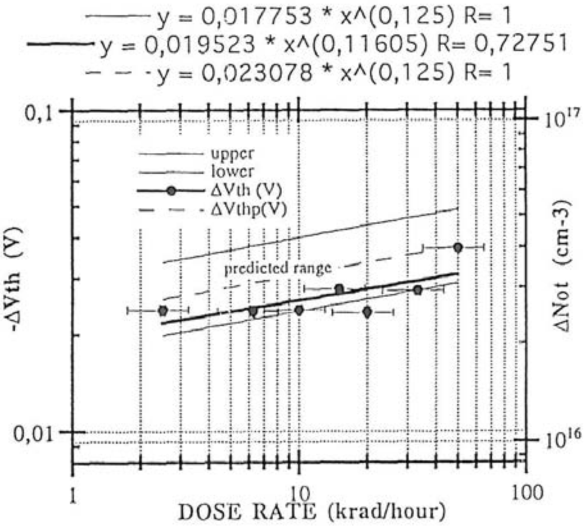


Fig. 7: double scale plot showing the dose rate dependence of the threshold voltage shift in the range 1 krad/hour to 100 krad/hour. The net positive trapped oxide charge is indicated on the left scale. The shift follows a D'^{α} law. The law can be derived from CTRW (Continuous Time Random Walk) analytical approaches.

The TID response also strongly depends on the electric field in the gate oxide. Fig. 8 clearly exhibits the difference in the slopes of the threshold voltage versus the Total Ionizing Dose (gamma rays) with electric Bias applied to the gate. At 0 V the dissociation of the electron-hole pairs is uncompleted and a low charge generation yield results. When a moderately strong bias is applied (5V) the charge dissociation is almost complete and the slope is at its highest value. This effect is strongly reduced when the electric field is increased. Field assisted tunneling of trapped holes towards the silicon can explain the phenomenon in addition of field assisted hopping transport. The activation energy for dispersive transport is lowered when the electric field is increased. ($E_a(E)=E_a-kE$). This results in a faster hole hopping frequency, between random sites.

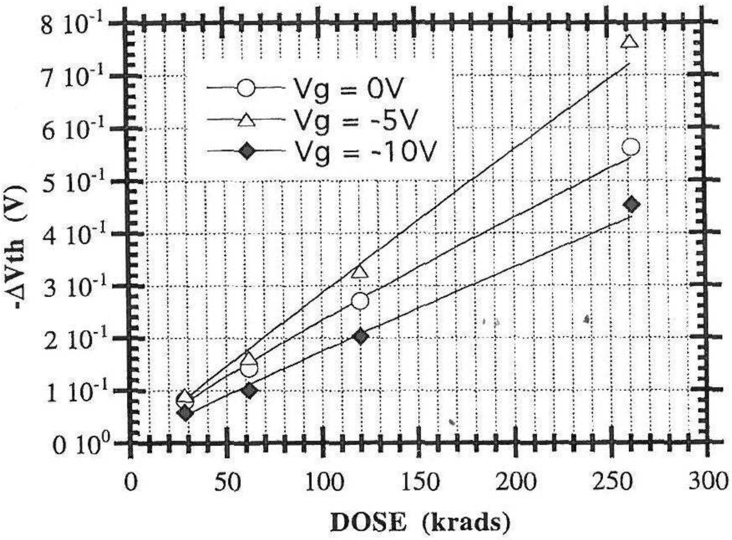


Fig. 8: Vth shift versus TID for p-channel devices with increasing voltage bias on the gate. The measurements were carried out at moderate cryogenic temperature. Notice the importance of the shift with oxide thicknesses of 20 nm.

Transport of holes within a temperature range extending from liquid nitrogen to room temperature, shows a temperature and field dependence, the same being true for the conduction of electrons in the oxide, these carriers being much more mobile than holes. The holes are trapped at low temperature, where they exhibit a very low mobility. They can be trapped either at E centers (oxygen vacancies) or more probably as can be self trapped as polarons, which have a very low mobility particularly below room temperature. At higher temperatures, the mobility is enhanced and they can anneal out rapidly. Experiments, carried out in the nineties on DMILL thick film SOI devices showed the thermal anneal of trapped holes in the gate oxide (Fig. 9).

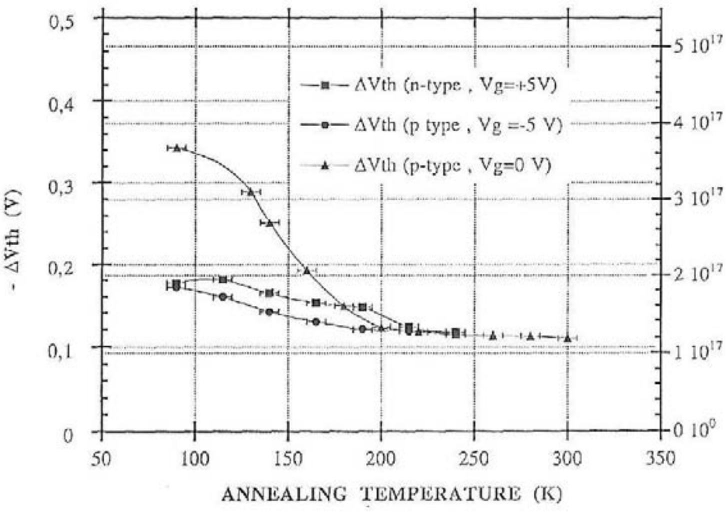


Fig. 9: Isochronal anneal of n-channel and p-channel transistors (30 minutes at each temperature). The Vth shift of the n and p channel devices with bias on was identical. The original Vth shift of the p- channel device with 0 V bias on was different due to a 300 krad TID compared to the 80 krad TID received by the two former devices.

The activation energy deduced from the annealing diagram is approximately 0.12 eV, this corresponds to the detrapping energy of the self-trapped holes and is very small compared with the silica bandgap. As this diagram shows most of the charge (at least 50 %) has annealing up to room temperature.

Early studies of hole transport in thick silica has confirmed the validity of the CTRW (Continuous Time Random Walk) theory (Sheer & Montroll, 1975) for hole-polaron transport in different conditions of field and temperature (McLean, Boesch, Jr. & Garrity in Ma & Dressendorfer,1989; McLean, Boesch, Oldham Ma & Dressendorfer,1989) . Analytical models were proposed a long time ago and it was reasonable to extend them to take into consideration the effects of dose rate, under continuous irradiation. Using signal theory and considering the physical processes as being causal a convolution of annealing effects and irradiation effects can be the basis of a simple analytical model. One obtains a dose and dose rate dependence of the threshold voltage shift of the form:

$$\Delta Vth \approx KoxD^{1-\alpha}D'^{\alpha} \quad (3)$$

Kox is a parameter that depends on the oxide characteristics, D the Total Ionizing Dose and D′ the dose rate. See (Fourches, 1997) for details.

A power law dependence on the dose and dose rate is obtained, with a value for derived from Fig. 7 of approximately 0.125, this value is lower than the values deduced from older experiments made on thicker oxides (Ma & Dressendorfer and corresponding chapter herein). Additionally it seems clear that the annealing process cannot be simply interpreted by a first order kinetic, as it would be the case for single deep traps. A saturation would occur at a very low TID level (Fourches, 2000), which is not observed at all in the measurements. Further investigations show that saturation is clear at much higher TID, for which threshold voltage shifts exceed 1 V. A numerical treatment was introduced (Fourches, 1998) taking into account the presence of deep hole and electron traps together with CTRW transport, which fits with the saturation observed on some devices exposed to very high TID. The existence of a strong annealing between 80-90 K and room temperature has consequences on the behavior of devices. Cryogenic operation of CMOS SOI electronics had been considered for Liquid Argon Calorimeters, but mainly due to some of the shortcomings of the processes of the 1990's this could not be implemented.

3.3.2 Consequences on hardening issues at room temperature

These modeling issues have had some direct consequences on the hardening techniques to be used especially at low temperatures but also for the normal operation of MOS devices. First, it is clear that the Manzini-Modelli-Saks models is key to these issues. A good fit can be found between measurements results at low temperature and mathematical predictions leaving aside the annealing effects that result in the power law dependence. For instance a 20 nm oxide irradiated at high dose rate, leads to a Vth shift of 0.3 V at 100 krads according to our measurements. This is very close to the value deduced from Fig. 5. This experimental verification of the Manzini-Modelli model could only be made on modern hardened oxides, which exhibit a low intrinsic defect density, compared to early oxides, on which Saks et al. made the first experiments. On this basis on can deduce a roadmap for hardening issues to TID. Modern processes either bulk or SOI have thin gate oxides (at the expense of supply voltage range) and this improves radiation hardness. Leakages currents due to interface and surface effects have been somehow reduced over the years by process improvements and layout techniques.

Other data obtained at 90 K show that the sensitivity to TID of the SOI process studied reduces when the dimensions of the device decreases. This is verified by plotting the prefactor Kox of expression (1) versus the gate length of each device. The exponent of the power law is also gate length dependent although to a lesser extent. Fig. 10 and 11 show the results. The fact that a shrink in device dimensions has very favourable effects on tolerance to TID has had a lot of implications for future processes both bulk and SOI. In retrospect one can express the fact that today nanometric or deep submicronic technologies are intriscally TID hardened on the basis of some of the scaling laws discussed here and verified experimentally in the 1990's papers (Fourches, 1997) for Silicon On Insulator processes.

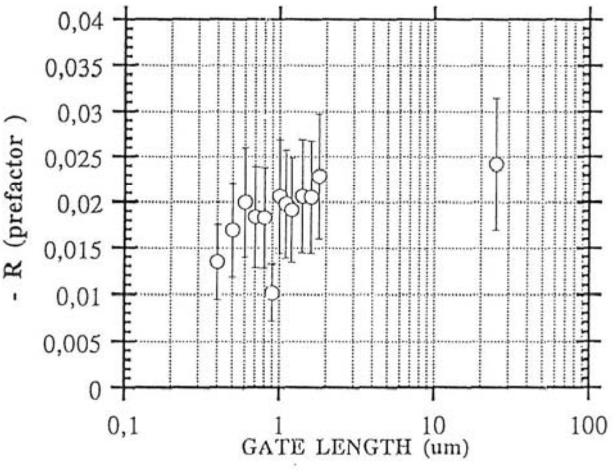


Fig. 10: dependence of the pre-factor, with the gate length of a n-channel transistor, each transistor having received the same total ionizing dose for the same dose rates. It is clear that low gate length result in a reduced effect of radiation. The measurements were made at 90 K.

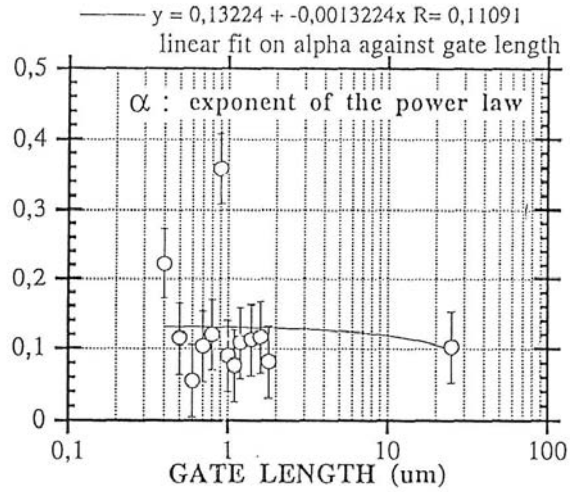


Fig. 11: similar plot for the exponent of the power law. There is no clear dependence on the gate length.

The interpretation of this effect at least at low temperature is relatively simple and was introduced in (Fourches, 1997). Charge tunneling and simply migration is faster when the dimension of the device are lowered, resulting in an accelerated annealing of the positive charge. This should have favorable consequences even for room temperature operation of bulk device, because this concerns the gate oxide.

This is one of the reasons the TID response of MOS devices is a today an issue of less importance for most applications, except perhaps for the upgrades of the LHC and for the future Linear Colliders and in lower extent for nuclear power plant applications. Most of the research focuses on Transient Effects, destructive or not, due to charged particles in available bulk processes. The SOI processes are immune to these transient effects by design; because of device/device insulation systematically implemented.

3.3.2 TID and dose rate effects on other devices

TID effects were reported and sustained efforts were made reduce them on bipolar transistors. DMILL technology was developed with a vertical npn bipolar transistor in order to obtain a radiation hard device, by a reduction of the passivation Si/SiO_2 interface. In spite of this TID effects still appear with enhanced effects on npn devices due to the higher base current due to minority electron carriers, the oxide being positively charged. In addition to this dose rate effects were reported in 1991 on polysilicon bipolar transistors, and later enhanced low dose rate effects were confirmed (Pease, 2004). Studies on JFETs and MESFETs have also shown the existence of ionizing dose effects, extensive studies were not very developed (Citterio et al., 1995; Fourches, 1998), mainly because the main constraints with preexisting large channel devices such as JFETs is their limited tolerance to displacement damage.

4. Irradiation : Detectors

4.1 Total dose and dose rate effects; silicon detectors

In this paragraph emphasis will be on new semiconductor detectors such as CMOS sensors that are now good candidates for high radiation hardness, high spatial resolution

Sensitivity to Total Ionizing Dose for silicon detectors is clearly dependent on surface effects, the silicon surface being oxidized either naturally or for passivation purposes. Depending on the thickness of the oxide the sensitivity of the detector to leakage currents will be enhanced or limited. Recent studies have focused on CMOS Sensors (Fig.12) and CCDs. Sensitivity to bulk ionizing damage is limited and was not thoroughly investigated except for charged particles. The striking result is the limited Fixed Pattern Noise increase due to ionizing irradiation, which is much less pronounced than it is when induced by displacement damage. Total Ionizing Dose induced displacements is often limited to the creation of Frenkel pairs and other point defects in the bulk that are less effective in reducing the free drift length of the carriers than displacement cascades. This induces a reduction of the Charge Collection Efficiency which characterizes the effectiveness of the sensor/detector to collect all the generated carriers. Ionizing Dose effects can reduce the charge collection efficiency through surface/interface carriers recombination. Fig. 13 seems to confirm this effect. The CMOS sensors degrade rapidly with TID. In this case the layout of the sensing diode was not optimized so high recombination and leakage current can occur even at small TID.

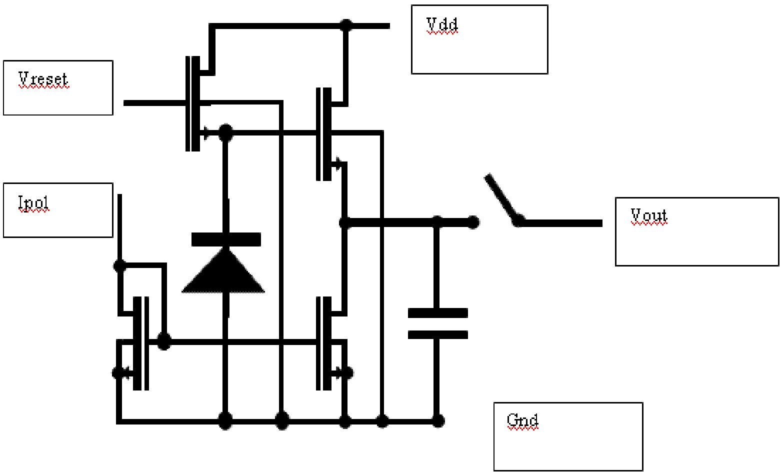


Fig. 12: schematic structure of the CMOS sensor proposed for charged particle detection.

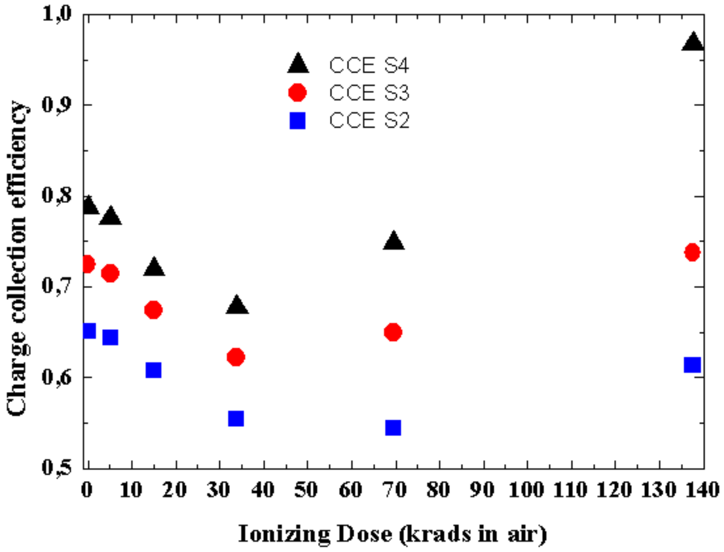


Fig. 13: CCE versus TID for different sensor diode sizes: (S4, S3, S2).The increase in the CCE along with the TID could find its origin in a high surface local electric field, which results in carriers' multiplication.

This Figure (Fig.13) shows that the degradation in charge collection efficiency is very fast at TID for these un-optimized pixel devices. This is due to the high surface leakage current that limits the current signal. CCE increase due to carrier multiplication has been recently reported and was the basis of possible radiation tolerant CMOS particle detectors (E. Villela et al., 2010).

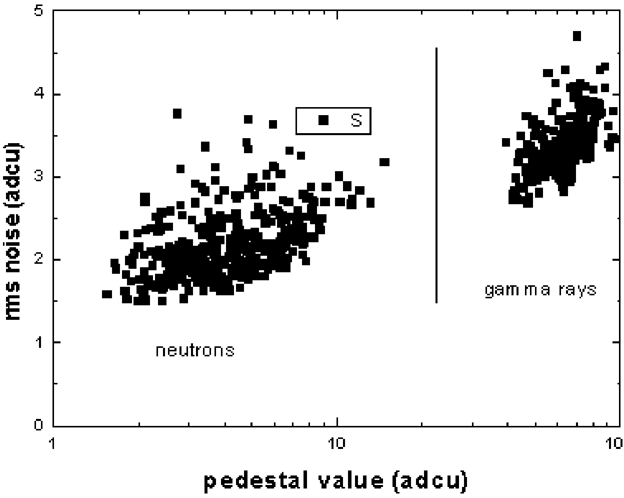


Fig. 14 : Root Mean Square value of the temporal noise plotted versus the corresponding Pedestal (offset) values for pixels irradiated with neutrons (left) and pixels irradiated at a dose of 137 krads (Si)(right).

The last figure (Fig.14) clearly shows that the spread of pedestals values is greater in neutron irradiated CMOS sensors than for ionizing irradiated ones. Moreover, the temporal noise increases very slowly with pedestal value, in contrast with the neutron irradiated pixels, for which low pedestal pixels correspond to low temporal noise pixels. These relatively new results obtained on very small pixels (a few tens of cubic microns) indicate that the temporal noise is very high after 137 krads and this originates in the shot noise induced by the interface leakage current. The pedestal value shift is probably due to the threshold voltage shift of the follower n-channel MOS transistors. This threshold voltage shift is much lower in the case of neutron-irradiated pixels as displacement damage has a limited impact on the threshold voltage of MOS transistors.

On other processes where radiation tolerance layout techniques were implemented, show a better response to ionizing irradiation. Up to now no long term dose rate effects were observed, nor really studies on these novel CMOS detectors. On the basis of these measurements the TID tolerance of CMOS sensors is higher that that of Charged Coupled Devices, which render CMOS sensors suitable for future ILC experiments. Radiation hardness up to several Mrads was reported on CMOS sensors using a Deep N-Well structure with a charge amplifier readout (L. Ratti et al., 2010).

Other comments should follow concerning CMOS sensors and their counterparts CCDs and DEPFETs. In these devices transport is simply not due to the drift of charged carriers, diffusion is also very important and this has dramatic consequences on the migration length of carriers and subsequently on the signal build-up. Simulation with a software package may help obtaining predictive results but this was limited so far to displacement damage (Fourches, 2009).

4.2 Total dose and dose rate effects: other detectors

Other materials have been proposed and used for particle detection and has been investigated, in terms of both ionizing irradiation-induced defects and displacement induced defects. Up to now, diamond has a good potential for charge particle detection and radiation tolerance, mainly because of the large amount of energy required to create a vacancy-interstitial pair, and was proposed for LHC applications. Compound an alloy detectors have been not so successful because the density of residual defects remains high. This limits the CCE from the start, and affects the charge transport trough the fiducial zone. In spite of this, there have been recent studies of thick GaAs pixel detectors for medical applications (Bourgoin, 2001). Future proposals for high radiation hardness, both for ionizing radiation and displacement damage were recently presented (Fourches,2010). The main idea is to reduce the fiducial value and to introduce a deep trapping gate below the channel of a MOS transistor which would act either as a detector (electron-hole pairs would be created along a charged particle track) or /and a volatile memory (Fig.15). As the trapped positive charge modulates the channel current of the MOS transistor the readout is simplified and can be implemented by a circuitry similar or to the one used for CMOS sensors. As the deep trapping gate is made of a high density of structural defects, these results additionally in a high tolerance to displacement damage, confirmed by device simulation (Fourches, 2010).

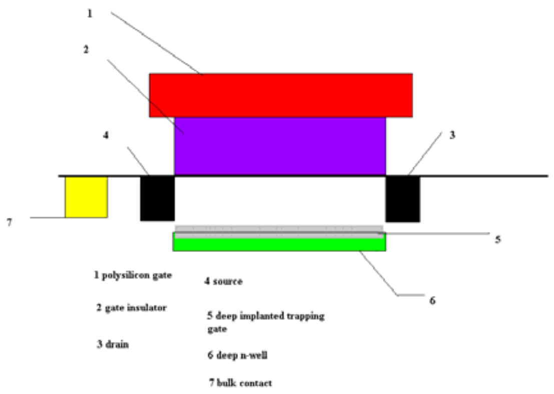


Fig. 15: schematic structure of the deep trapping gate MOS detector structure.

3. Conclusion

Future developments about the TID effects are manifold. First, there is still some interest about the TID hardness at very high doses for high energy physics applications (SuperLHC). New nanoscale technologies, because of their reduced dimensions and the presumable existence of scaling laws will ease the development of new radiation hard ICs. On the detector side, similar advances are expected for reduced dimensions pixels, mainly for displacement damage but also for ionizing effects. Geiger mode Si detectors are also promising (Ratti. L et al., 2006). Dose rate effects have been somehow investigated on silicon detectors for medical X ray imaging and much remains to be done to improve these sensors.

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