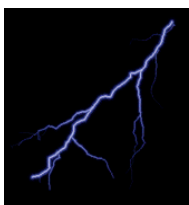


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The CEA logo consists of the letters 'cea' in a stylized, lowercase, sans-serif font. The 'c' and 'e' are connected, and the 'a' is separate. The logo is positioned between two horizontal lines: a yellow one above and a green one below.

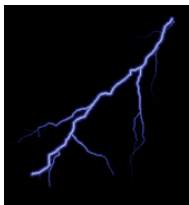
*ECLAIRS*

# Lab. Activity at CEA Saclay

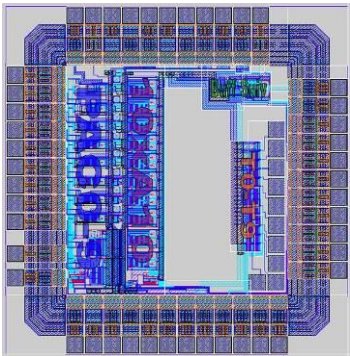
## *IDeF-X*

*Imaging Detector Front-end*

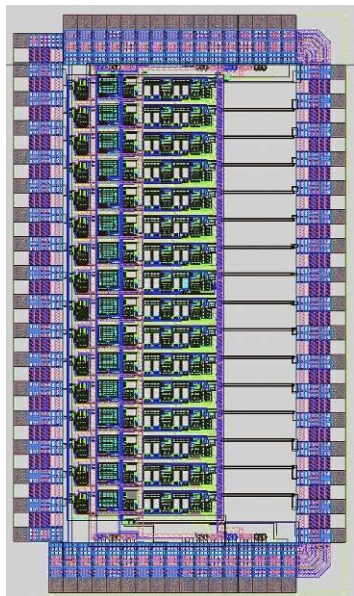
*O. Limousin, O. Gevin, F. Lugiez, P. Baron,  
et al.*



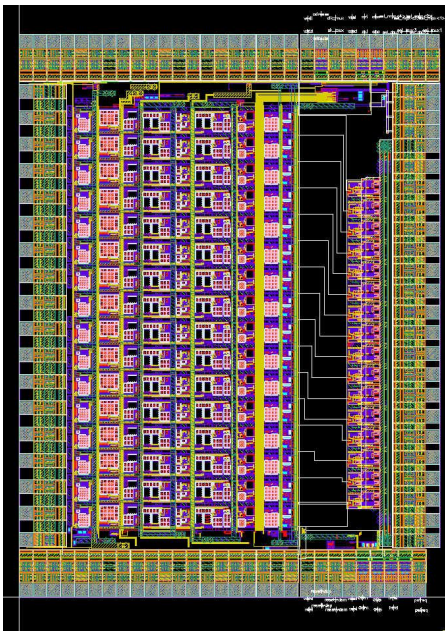
ECLAIRS



*IDeF-X V0*

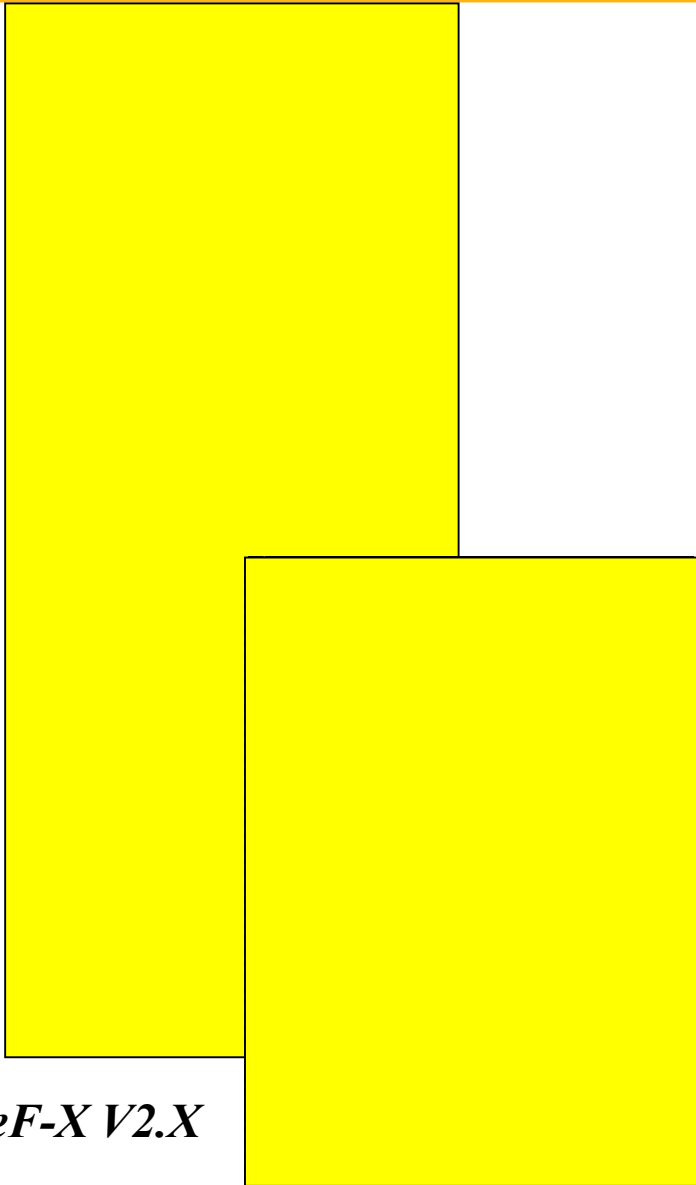


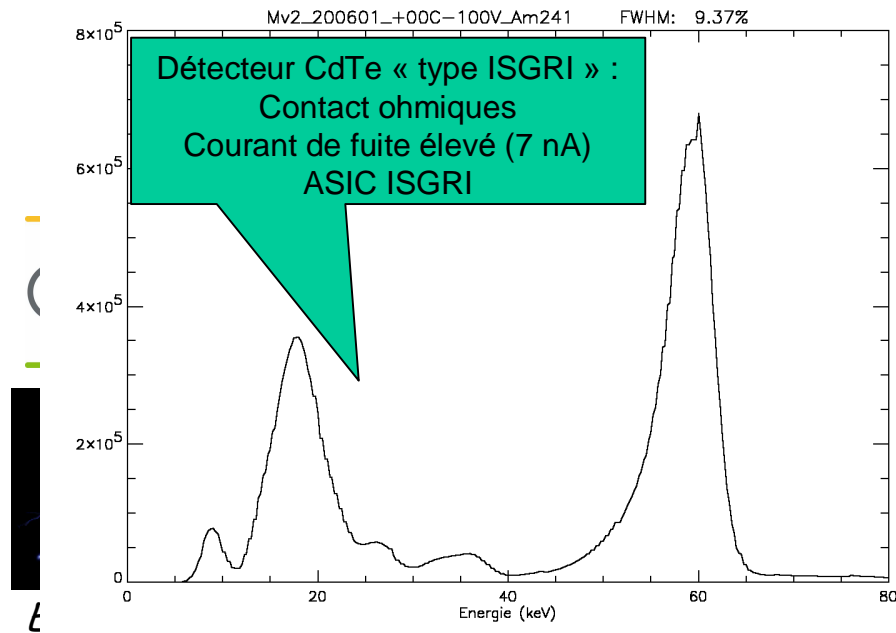
*IDeF-X V1.0*



*IDeF-X V1.1*

*IDeF-X V2.X*

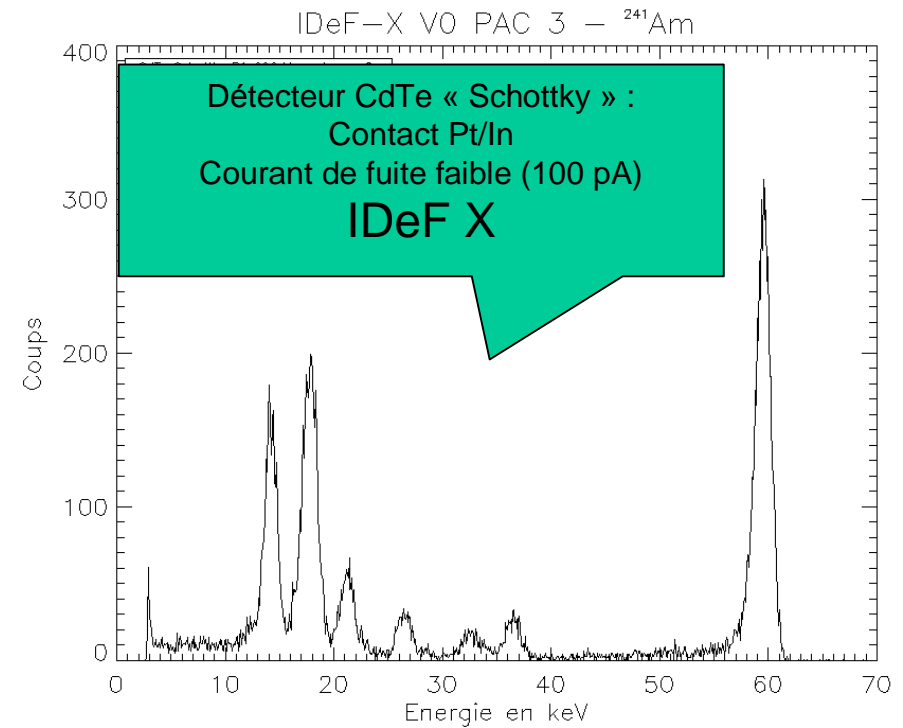
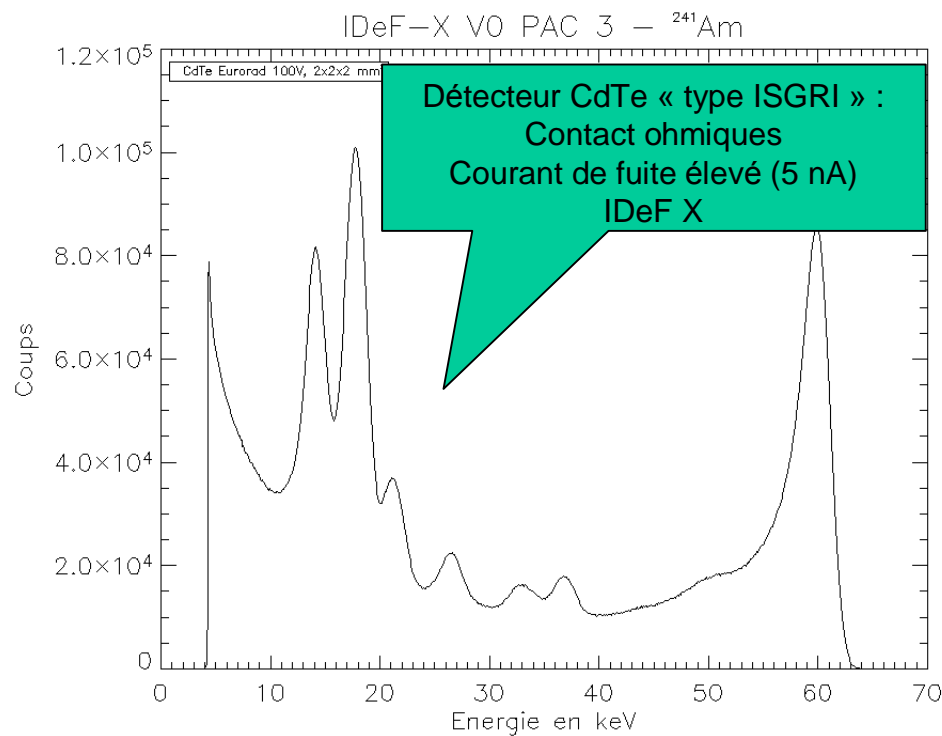


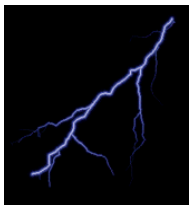


- ASIC ISGRI + CdTe ISGRI : 5.6 keV à 60 keV
- IDeF-X V0 + CdTe ISGRI : 3.5 keV à 60 keV
- IDeF-X V0 + CdTe Schottky : 1.4 keV à 60 keV

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- IDeF-X V2 + Schottky/matrice : <1 keV à 60 keV
- IDeF-X V2 + Schottky/matrice : 0.6 keV à 60 keV



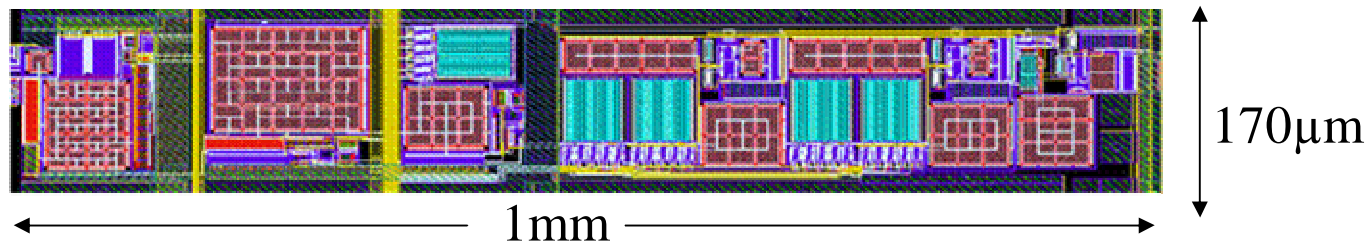
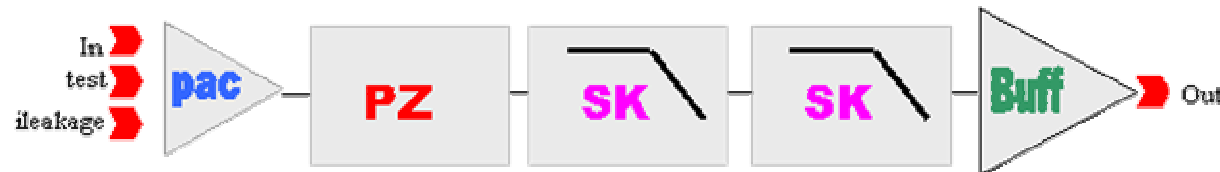


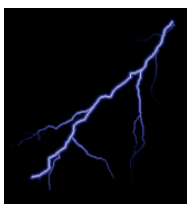
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- IDeF-X V1.0 ASIC : 16 complete spectrometry channels

Each channel is made of :

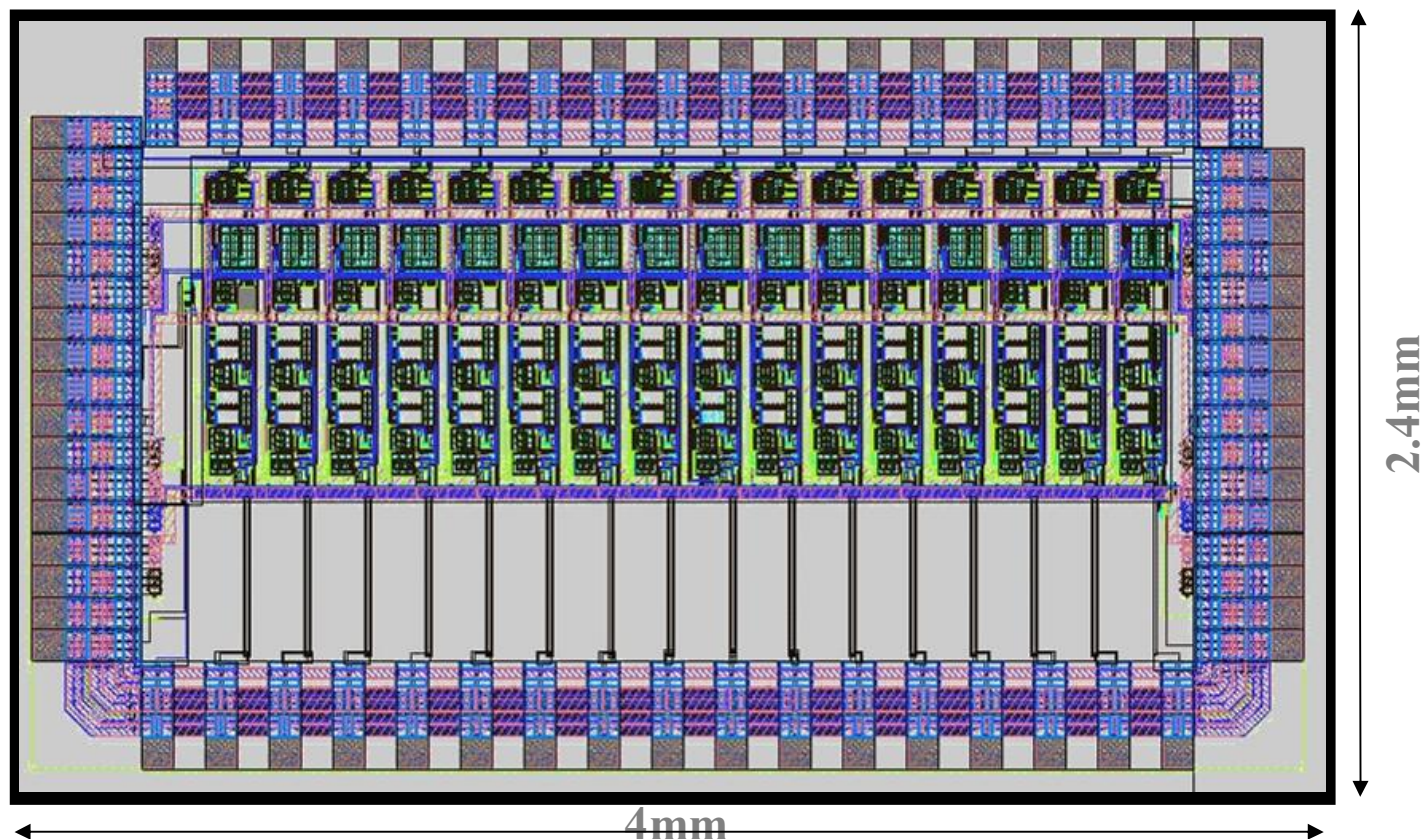
- A charge sensitive preamplifier
- A pole-zero cancelation stage
- Filtering stages (tunable peaking time Sallen & Key)
- An Output buffer



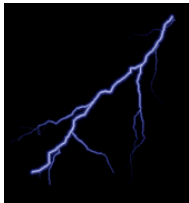


ECLAIRS

- IDeF-X V1.0 ASIC layout :

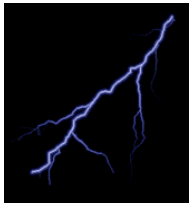


*IDeF-X V1.1 : april 2004*



*ECLAIRS*

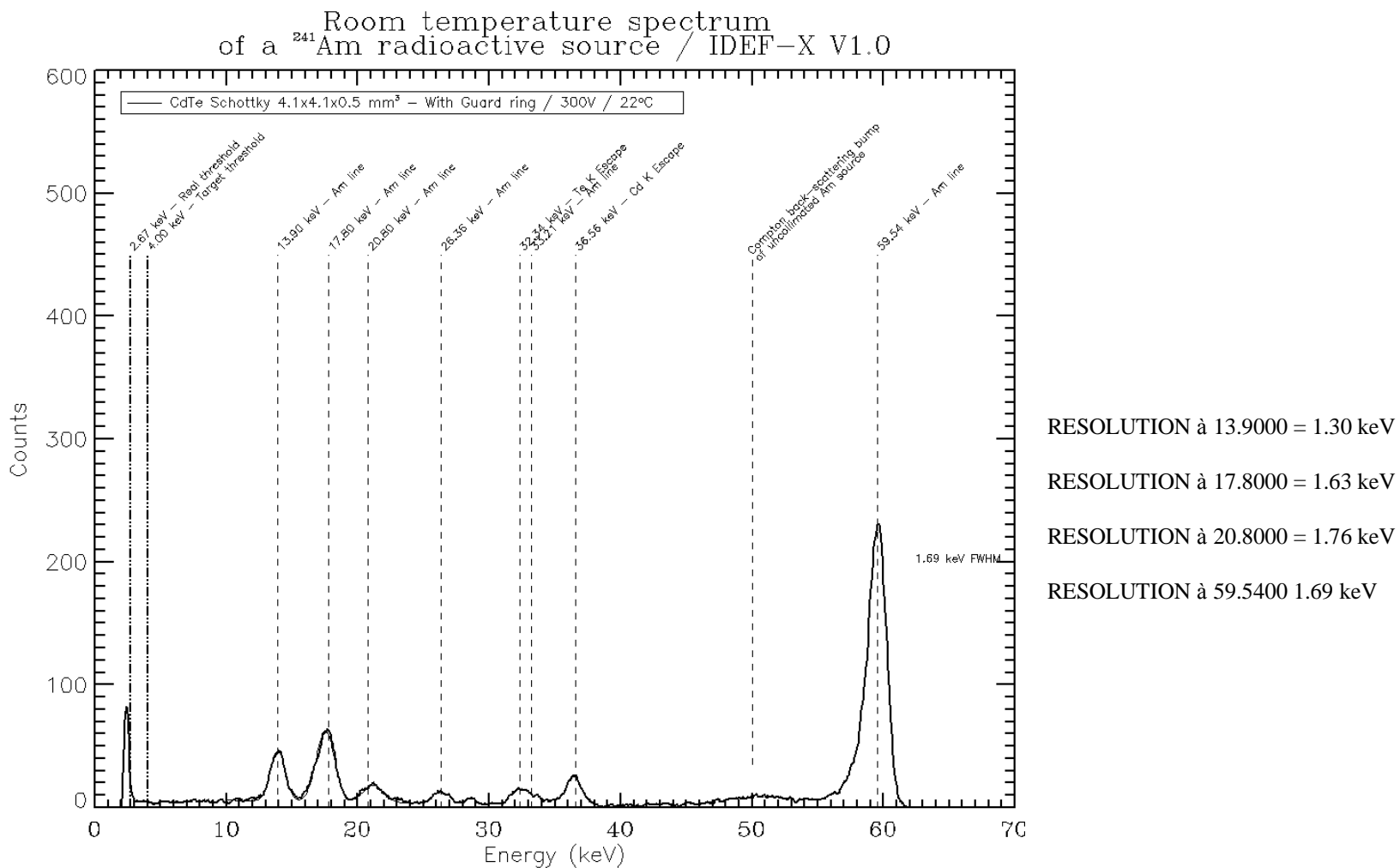
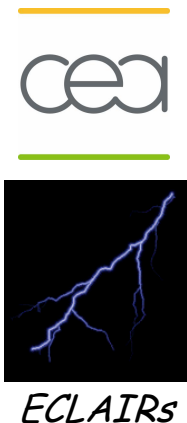
- Optimised for  $C_{det}=2-5pF$
- DC coupling (working up to 1nA detector current)
- Two polarity signals (best when connected to the anode)
- 16 input pads + 1 multiplexed test input (4 config)
- 16 outputs
- CSA current, peaking time, test configurations are tunable
- Fixed Gain



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<b>Chip size</b>	4040 $\mu\text{m}$ x 2355 $\mu\text{m}$
<b>Packaging</b>	JLCC68
<b>Packaging size</b>	2.5cm x 2.5cm
<b>Number of channels</b>	16
<b>Power supply</b>	3.3V
<b>Typical power consumption</b>	2,26mW/channel 36,16mW/chip
<b>Gain</b>	210mV/fC (33mV/ke <sup>-</sup> ) at 9,6 $\mu\text{s}$
<b>Dynamic</b>	-40ke <sup>-</sup> $\rightarrow$ 40ke <sup>-</sup>
<b>Peaking time (<math>\mu\text{s}</math>)</b>	0,3 0,6 1,2 2,4 3,6 4,8 6 7,2 9,6
<b>ENC (9.6<math>\mu\text{s}</math> <math>i_{\text{leakage}}=10\text{pA}</math>)</b>	20e <sup>-</sup> + 3.25e <sup>-</sup> /pF (floor at 35 e <sup>-</sup> )

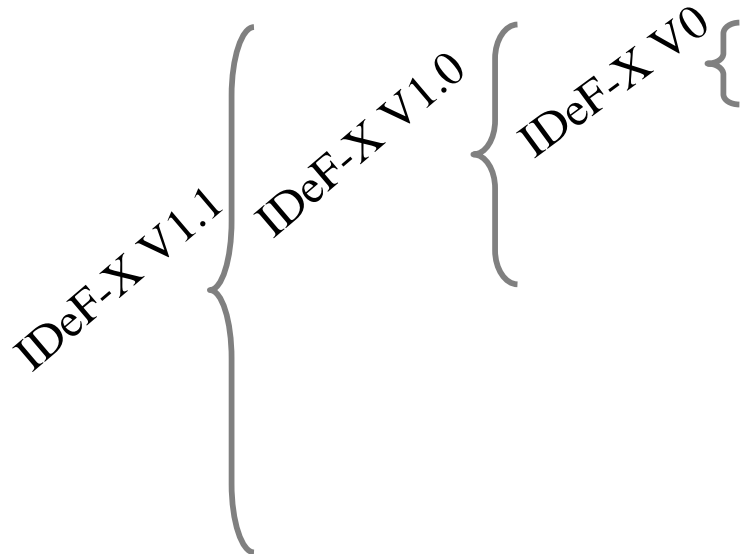
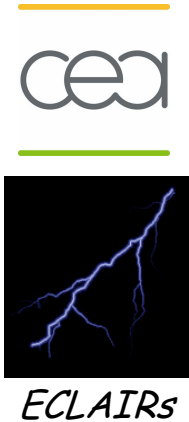
## Spectrum with CdTe Schottky $^{241}\text{Am}$ (line at 59.5keV) at 24°C





# IDeF-X V1.1

16 channels circuit, multiplexed output, peak detector, discriminator



Charge sensitive amplifiers

PZC

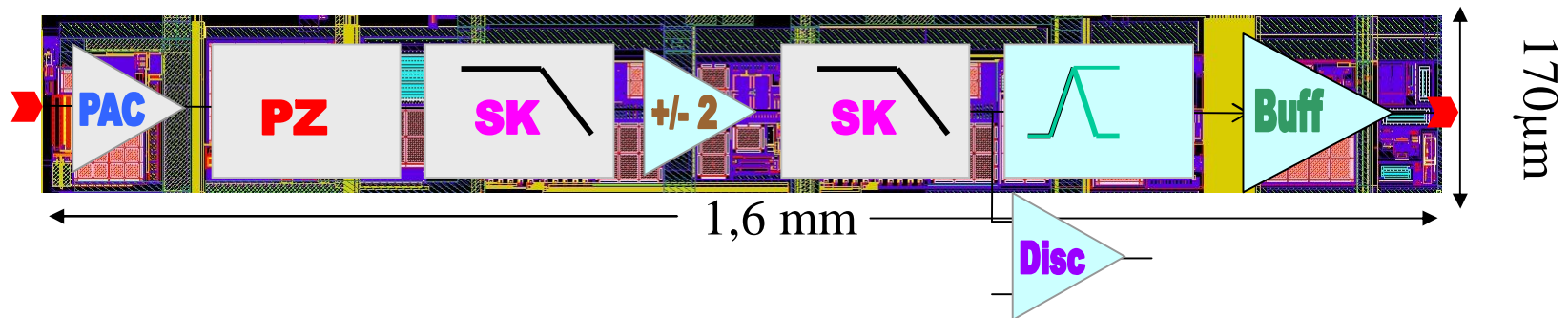
Filtering stages

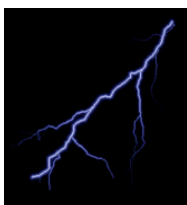
Offset removal and inverting stage

Peak detector

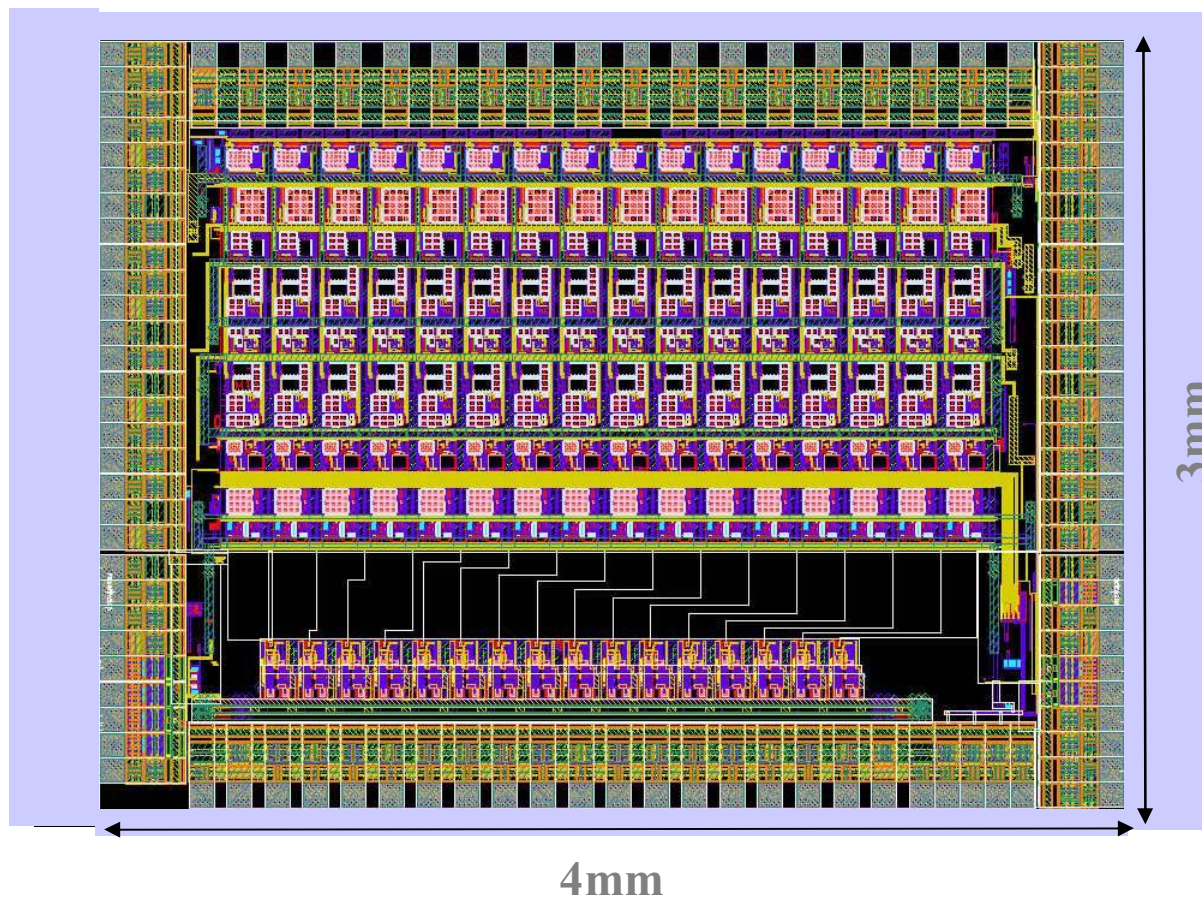
Discriminator

Buffer



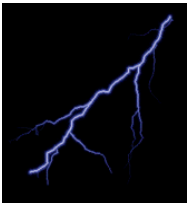


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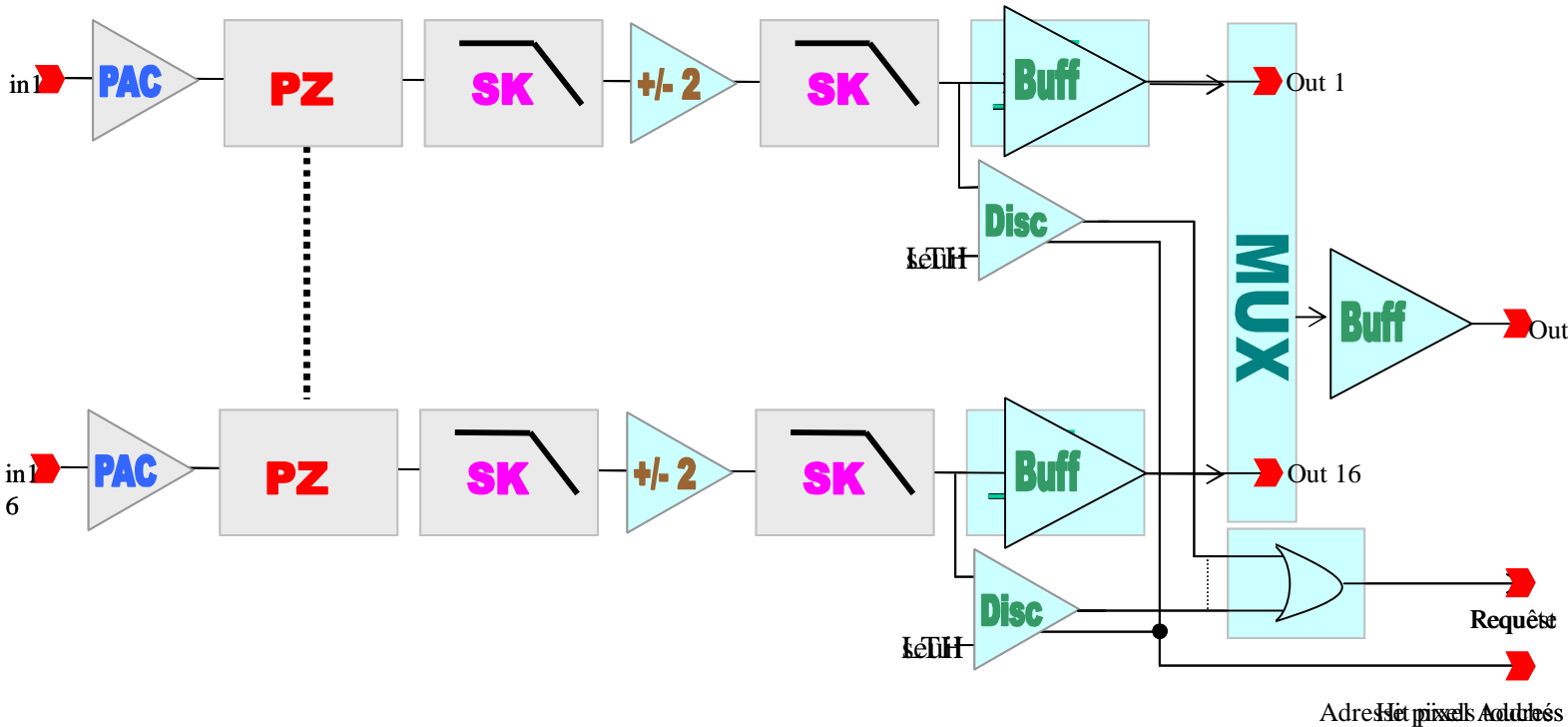
*IDeF-X V1.1 : layout march 2005*

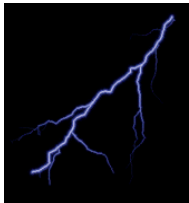
Two operating modes :



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Multiplexed outputs: (IDeF-X V1.0) :





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<b>Chip size</b>	4060 $\mu$ m x 3050 $\mu$ m
<b>Number of channels</b>	16
<b>Power supply</b>	3.3V
<b>Typical power consumption</b>	2,8 to 4mW/channel
<b>Gain</b>	200mV/fC (33mV/ke <sup>-</sup> ) à 9,6 $\mu$ s
<b>Dynamic range</b>	-50ke <sup>-</sup> → 50ke <sup>-</sup>
<b>Peaking time (<math>\mu</math>s)</b>	0,3 0,6 1,2 2,4 3,6 4,8 6 7,2 9,6

Tests will begin this summer