Infrared ROIC for very low flux and very low noise applications

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ABSTRACT

Sofradir is involved in the manufacturing of detectors which cover a large range of wavelengths in the infrared domain from SWIR up to VLWIR for different kind of applications. Thus, different types of ROIC architectures are needed to cover these various kind of applications and operating conditions.

As a major player of the infrared market, Sofradir has developed numerous ROIC with architectures enabling to answer most of the infrared applications in tactical, commercial and space domains. Sofradir is now able to present a new detector (384x288 with a 15 µm pitch) especially designed for very low flux applications in the SWIR domain (as astronomy for example). This new ROIC has been developed with CNES support and includes a SFD (Source Follower per Detectors) input stage enabling to achieve a high gain as well as a low readout noise and a vey low power consumption.

In this paper, we will describe the architecture and functionalities of this new detector. Then, electro-optical characterizations and results will be described. Finally, main applications of this kind of detectors will be presented.

KEYWORDS

Sofradir, Infrared detectors, MCT, Source Follower per Detector, Focal plane arrays, low noise, low flux

1. Introduction

For more than 15 years 2nd generation IR Focal Plane Arrays have been produced widely and in particular in France who has a leading position in this area. For about 30 years, thanks to research carried on at CEA-LETI and whose successful results are regularly transferred to Sofradir, Sofradir produces thousands of cooled IR detectors. Sofradir is continuously developing new products for all IR applications. These applications include military, security, process control, environment monitoring, science and space. Combined with the research capacity existing at CEA-LETI, this force represents more than 500 people, which constitutes one of the largest area worldwide dedicated to R&D and production of IR detector dewar assemblies.

Sofradir has been involved in space applications since the beginning of the nineties, in particular with the development of the detector for the French military satellite Helios II. Today, Sofradir is the only European manufacturer of infrared detectors of 2nd and 3rd generation detectors which is able to show a large experience in the space field with this type of detectors. In particular, several satellites with infrared channels currently operating are made with Sofradir infrared detectors: the most famous one is the French military satellite Helios II but one can quote also Venus Express mission which is in orbit around Venus planet for more than 3 years, and more recently the French military satellite SPIRALE.

Very low flux applications, especially astronomy, need dedicated Readout Circuit (ROIC) with improved circuit architecture. In the frame of a R&D Study supported by CNES, Sofradir has designed and produce a new ROIC with 15µm pixel pitch. The CNES specification is to develop a ROIC which minimizes the ROIC noise to the detection noise for very low infrared flux in the SWIR domain.

In this paper, we will present this new ROIC. The architecture and functionalities of this 384x288 array with 15µm pixel pitch will be presented, main general required performances and electro-optical characterizations will be also described.

2. ROIC Specifications and Design overview

The challenge of the development of such ROIC for very low noise applications is the choice of the input stage. For years Sofradir has developed ROIC with different input stages adapted to various applications with different wavelength ranges (from visible to VLWIR). Two main input stages are commonly used:

- Direct Injection: this architecture is well adapted to high diode current applications. It is usually integrated in ROIC for high flux applications, in LWIR spectral domain for example

- CTIA (Charge Trans Impedance Amplifier): this architecture provides a very good linearity along the whole electrical dynamic but the complexity of this architecture need more space available in the pixel only possible with recent CMOS technologies. The ROIC noise is low and the gain might be high but the main drawback is that the CTIA needs some power during all integration phase. In fact, very low flux applications mean long integration time, so the problem with CTIA input stage is that amplifier generates some glow which is much higher than the dark current of the PV diodes. Integrating this glow during a long time generate noise uncompatible with very low flux application.

As these two input stages are not well adapted for very low noise and low flux applications, another type of input stage is needed. Sofradir has decided to use a Source Follower per Detector (SFD) input stage to reach the specifications. It is commonly used for this kind of detector.

The principle of operation of SFD input stage is to integrate the charge directly onto the capacitance of the photodiode. As this capacitance is very low, the gain is very high. The diode is connected to a MOS in follower mode to achieve high impedance. During integration time, the capacitance of the diode is slowly discharged as the photo electrons are collected. At the end of the integration, the diodes are read out through the follower MOS.

This type of design allows to achieve a very high sensitivity and a very low leakage current compatible to dark current in order of magnitude close to 0,01 e-/s/pixel. It also allows integrating charges for several hours in order to extract the dark current and the photonic current.

SFD is smart and very simple design architecture but the difficulty is to manage with high impedance design and the low integration capacitance which is needed to achieve a high gain without being disturbed by the parasitic capacitances. Actually, the pixel performance in terms of sensitivity and noise level directly depends on the integration capacitance. This integration capacitance consists of the intrinsic capacitance of the detector and the input pixel capacitance including parasitic capacitances. The performance optimization needs to decrease the overall capacitance of the integration node which will increase this node sensitivity for the useful signal but also for the parasitic coupling.

The main specifications given by CNES for this ROIC were: develop an array with 15µm pixel. The electrical consumption should be lower than 1mW and the ROIC noise have to be lower than 10 to 15 e-, in order to measure expected dark current lower than 0.01e-/s (0.1e-/s for maximum value). The format chosen for this prototype has been 384x288.

The other technical difficulty for this kind of design is to obtain a very low and stable electrical consumption in time in order to reduce glow phenomena and not to disturb the electrical and thermal balance of the ROIC. For example the warming generated by analogical or logical part of the ROIC could induce biasing fluctuation. We need to keep these phenomena as small as possible.

3. Design details and expected performances

This ROIC is the first Sofradir release designed with SFD input stage. Typical dark current specification can be 0.01 é-/s/pixel for astronomy applications for example and need thousands of seconds integration time to extract signal from background level. This order of magnitude is several decades away from usual applications of IR-FPA detectors.

This ROIC is design to fit the high gain, low noise and low Idark requirement, it could also be used as a tool to measure and understand specific high impedance characteristics of CMOS technology, HgCdTe technology, hybrid FPA technology and unpredictable second order effect.

This first ROIC takes advantage of choices and feedback experience from other products already available on the market . Some specific improvements have been also introduced to give some answers to user requirements noise reduction, low glow and low power consumption. An original <4 fF input capacitance pixel has been designed within 15µm pitch to improve state of the art performance and increase S/N ratio.

At design level, testing has been taken into account in order to facilitate the characterizations and analysis. For example different types of tests pixels have been implemented on the array.

3.1 Overall characteristics

The next table presents the overall characteristics of the ROIC.

Pixel pitch	15µm
Array size	384x288
Frame frequency	100kHz nominal value
Operating temperature	77K to 200K
Electrical consumption	< 1mW
Readout Noise	<10e-
Testing features	2 test lines for PV diode capacity measurement, hybrid leakage measurement, and operating check
CMOS Technology	0.35µm
Input stage	Very low input capacitance and low leakage pixel
Diode compatibility	N/P and P/N
Scanning	Zero-power lines and columns shift register
Output	2 outputs, buffered or un-buffered modes
Reference output	Optional reference output for pseudo-differential mode
Design optimization	Optimized glow-free design

Figure 1 :Overall ROIC characteristics

3.2 Block diagram

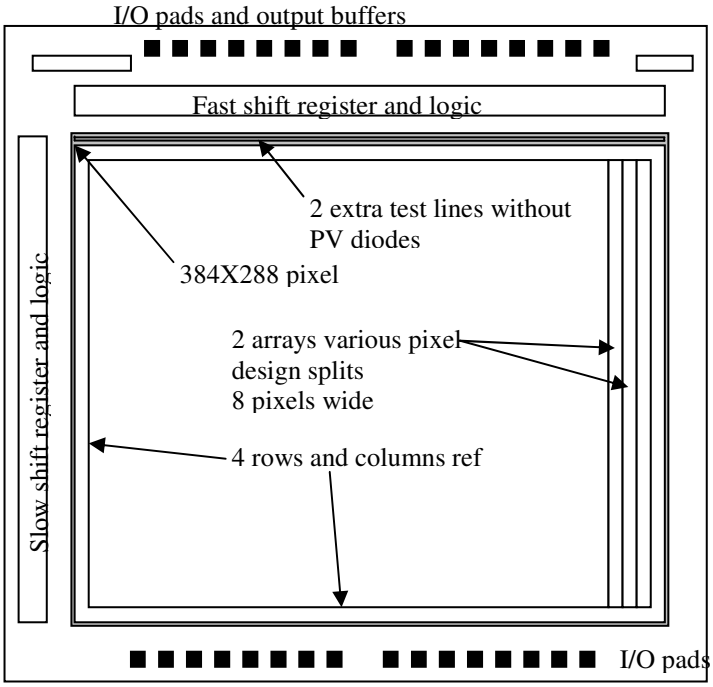

Figure 2 : ROIC Block Diagram

The 384X288 pixel array includes an outer ring of reference pixel without any contact with PV diodes and 40 fF integration capacitance. These pixels can be used for second order compensation and CMOS dark current control.

Various pixel design splits are implemented for low leakage design and higher parasitic capacitance design.

Extra test lines are separated from pixel array but scanned by shift registers; they include several test pixels to evaluate parasitic capacitance and noise measurement, to test leakage origin from CMOS technology, hybrid technology and PV technology. They also include DC voltage follower to check ROIC linearity and shift register behaviour.

3.3 Very low input capacitance pixel

Pixel architecture is SFD, simplified schematic is shown bellow

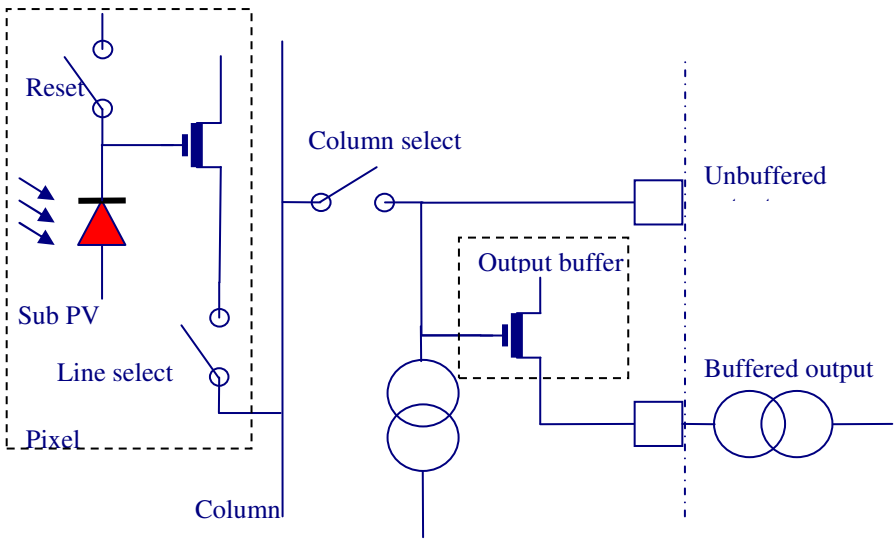

Figure 3 : Pixel architecture

The main characteristic of this pixel is the conversion gain that depends on nodal capacitance C_0 of each pixel. This nodal capacitance is the sum of pixel input capacitance C_G and the voltage dependent junction capacitance of the detector C_D.

As the conversion gain increase, the ROIC noise decrease in terms of electrons. This conversion gain is the main parameter to improve for high performance ROIC.

Nodal capacitance has been measured on Hawaii-2RG array [1] using Capacitance Comparison method. Typical values for HgCdTe diodes (λc=2,5µm) and 18 µm pitch pixels are C_G = 17,8 fF, C_D = 9,5 fF and C_0 = 27,3 fF.

Gert Finger explains that the pixel input capacitance is quite large for a nodal capacitance of C_0=27.3 fF. Since the junction capacitance of the detector diode is only C_D =9.5 fF it may be considered in future multiplexer designs to reduce the gate capacitance C_G to ~ 10 fF to increase the overall conversion gain and improve the noise performance of the detector at the expense of somewhat reduced linearity [1].

Sofradir has reduced this capacitance as much as possible by an innovative pixel design based on SFD architecture that leads to an input pixel capacitance C_G =3,5 fF (15µm pitch, 0,35 µm CMOS technology). Simulation results are 3.5fF for this C_G capacitance. §4 presents experimental results very close to these expectations.

3.4 Zero-power lines and columns shift register

Analysis of previous detector results showed that shift registers could generate glow effect that increases the dark current near the edge of matrix and limit the efficiency of N order Fowler's noise reduction techniques. Power consumption variation also induces self heating that disturb thermal balance [6].

In order to reduce this glow effect and self eating, we designed a specific high-impedance dynamic shift register that reduces the consumption on chip to zero by principle. All commands and clocks are externally driven to facilitate evaluation and test of this new shift register. Simulations showed less than 1 µA consumption at 100 kHz.

3.5 Addressing mode

Several addressing mode are available by external driving. Standard addressing mode is rolling frame starting with a reset frame, followed by several read frames for fowler averaging, a standby state during integration, then several read frame to end fowler averaging. As the glow is very low, we use mainly a continuous reading mode called “follow up the ramp” (FUR) to maintain thermal and electrical balance.

3.6 Detector bias

Detector bias is set during reset phase and maintained constant by diode and parasitics capacitances on integration node. The node voltage changes slowly during integration phase depending on IR flux. There are also several parasitic coupling during reset or read transition that put some small charge on integration node.

As we had reduced drastically the pixel input capacitance, it is now possible to hybrid this ROIC with specific low capacitance PV diodes and reach a new state of the art for the gain and low capacitance node.

3.7 Constant current consumption

During the read phase, consumption remains constant in the ROIC to avoid thermal and electrical fluctuation by self heating. Using this concept, the reset anomaly [6] is only present at the beginning of the multi-read phase. This constant consumption helps also to keep internal electric nodes stable between two lines or two frames, and decrease the settling time of first column pixel without using an horizontal double bus structure that would require more consumption.

4. ROIC characterizations

4.1 Test Setup

Tests were performed using two different set-ups. At Sofradir, measurements have been performed in a first step to find the electrical interface and to assess the main characteristics of the ROIC, in that case a liquid nitrogen bath cryostat have been used.

CEA Service d’Astrophysique de Paris (SAp) has a great experience in very low flux and low noise detectors testing and has also all the facilities to measure Sofradir SFD ROIC. Thus, accurate tests have been done at SAp (Figure 4). For these specific tests, ROIC is integrated into a cots LCC package (Figure 5). This LCC packaged circuit is inserted in a thermally controlled environment allowing very low thermal background on the detector. The thermal stability obtained is around 1.7 mK rms in the 70-200K range. The two stage cryo cooler is light tight and the inside infrared diffused illumination system is also temperature controlled.

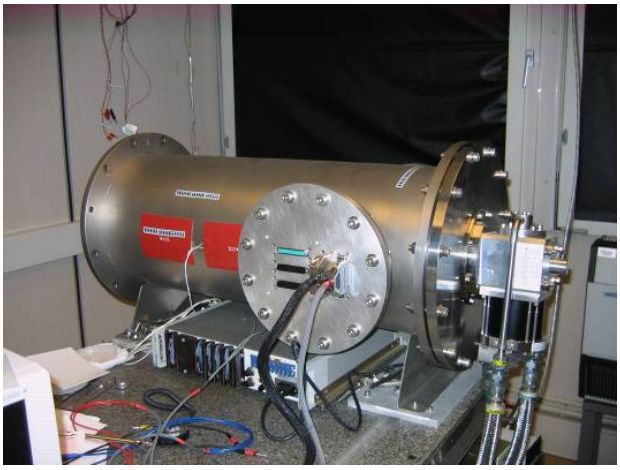

Figure 4: Test system: Read out electronics and test cryostat

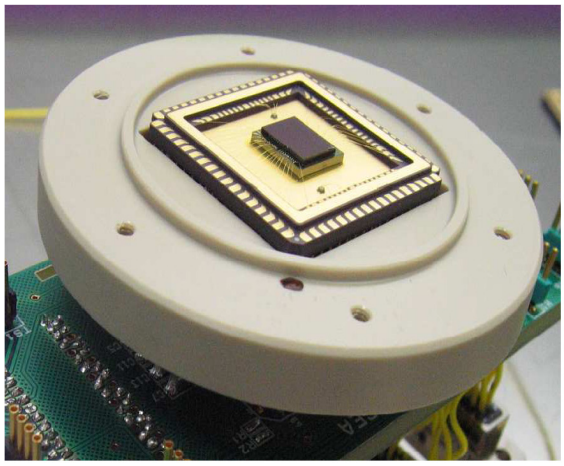

Figure 5: DUT in its LCC packaging

A dedicated ReadOut Electronics and associated supervision software has been also developed. This ROE must be targeted for low noise, adequate bandwidth and ADC resolution for the expected performances of the ROIC. The warm electronics acquisition board is composed of two channels one for each detector output. The gain of 2 at the entrance of the ADC, with a 5V input range and 18 bits digitization, allowed to reduce the acquisition chain noise to 21 µV rms (Figure 6). The warm electronics shows also linearity better than few 0.01% over the input range. Most of the measurements were performed at 50 kHz pixel readout rate of or 1 Hz frame rate of and focal plan temperature at 100K

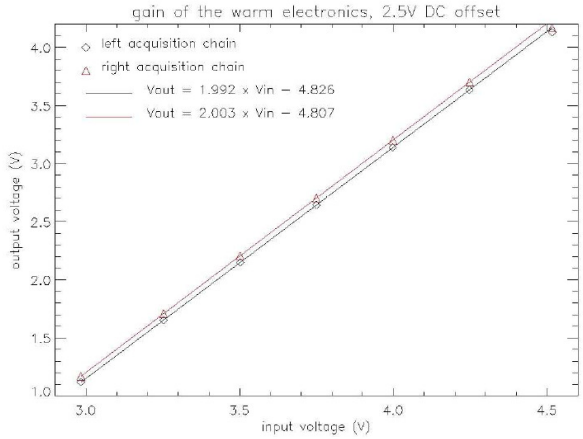

Figure 6: Gain of the warm electronics

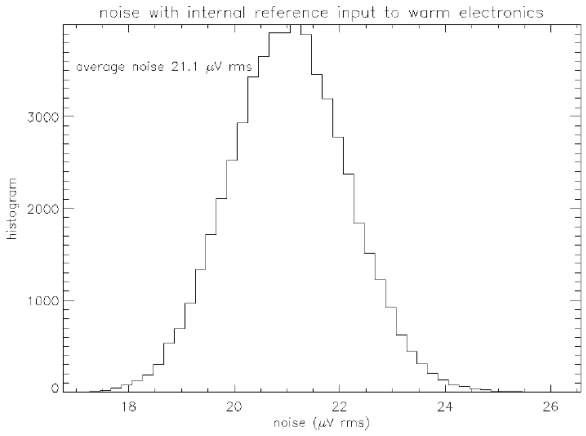

Figure 7 : Noise distribution of the acquisition chain

4.2 Conversion gain

One of the most important parameter of the detector is its pixel capacitance or conversion gain, as explained in §3.2. In order to quantify the different elements of the pixel capacitance in this SFD architecture, test pixels with known capacitances (10, 20 and 40fF) have been implemented on the ROIC matrix. The output voltage difference of these pixels when varying the polarization voltage gave the pixel capacitance part related to the ROIC or parasitic pixel capacitance. In the figure below, we plotted the polarization voltage and the test pixel output level versus frame number.

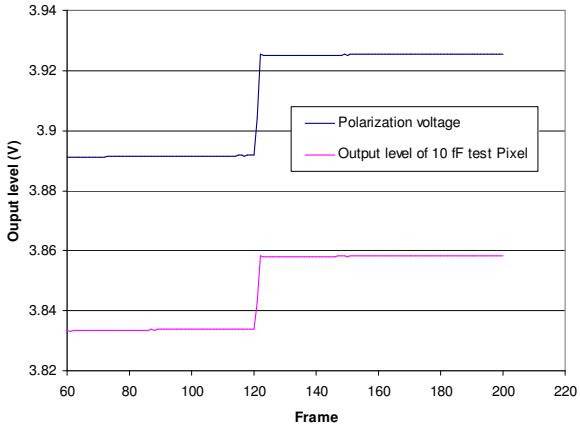

Figure 8 : Measurement of the parasitic capacitance

Measurements gave a parasitic capacitance C_G of about 4 fF for all test pixels. The overall pixel capacitance C_0 has not been calculated using the photon shot noise method. Indeed, for small pixels the coupling capacitance tends to overestimate the pixel capacitance [1]. Instead we evaluated the pixel capacitance based on direct measurement of the diode capacitance and by interpolating the reset noise, mainly due to kT/C noise [2], versus the known test pixel capacitance (including parasitic capacitance). In Figure 9, we plotted the pixel capacitance of test pixels versus the inverse of the squared reset noise. The active pixel capacitance (connected to the diode) is obtained from the linear least-squares fit law on test pixels. The estimated active pixel capacitances are then added to the graph for different polarization voltages for comparison.

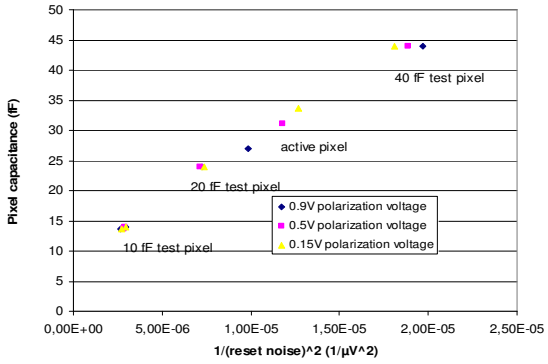

Figure 9 : Pixel capacitance versus inverse squared reset noise

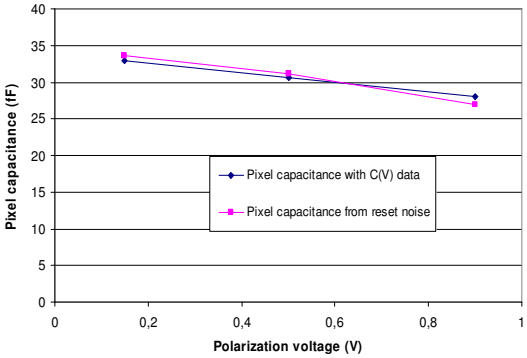

Figure 10 : comparison between pixel capacitance reset noise method and C(V) method

The interpolated pixel capacitance is compared to the measured diode capacitance on Figure 10. Diode capacitance of the detection circuit has been measured with a precise capacitance meter bench at CEA LETI [7] for a group of diodes. The correlation between the two methods shows good agreement. The interpolation method seems promising. However the validity range needs to be assessed with more measurements. The conversion gain derived from those data were summarized in the underneath table. Active pixel capacitance values are higher than expected but are close to the goal value (5 µV/e-).

Polarization voltage (V)	0.15	0.5	0.9
Pixel capacitance (fF) with C(V) method	33	30.5	28
CVF (µV/e-)	4.9	5.3	5.8

Figure 11 : Pixel capacitance and Conversion factor for various voltage polarization

4.3 ROIC noise and leakage current

Another crucial feature of the ROIC is the ROIC intrinsic noise. Unlike reset noise, the ROIC intrinsic noise could not be subtracted from the signal using CDS. Obviously it has to be minimized. In order to evaluate this parameter, we quantified the current integrated by the test pixels. As they are not connected to a diode, this measured current is in fact the ROIC leakage current. A long integration time allows a precise measurement of the leakage current. On the following graph, and as an example, the voltage drift is about 1.01 µV/s for 15000 s integration time and at 100K for this "10 fF test pixel" (Figure 12). This measured value is in fact a worst case. Actually, ROIC current leakage has been measured using "10 fF test pixel" without hybrid contact and with 14 fF node capacitance and for a continuous reading during several hours. A continuous reading represents a worst case concerning parasitic current produced by shift register that seems to be the main source, test pixels are on the side of the matrix very close to the fast shift register.
Latest results are still under analysis and present different current leakage values depending on the considered zone of the array. Leakage current has been measured using reference pixel without hybrid contact and with 44 fF node capacitance far away from shift registers. The best result is obtained for an array zone on the right or bottom side, far away from shift registers. The median leakage current has been measured at 0,002 e-/s.

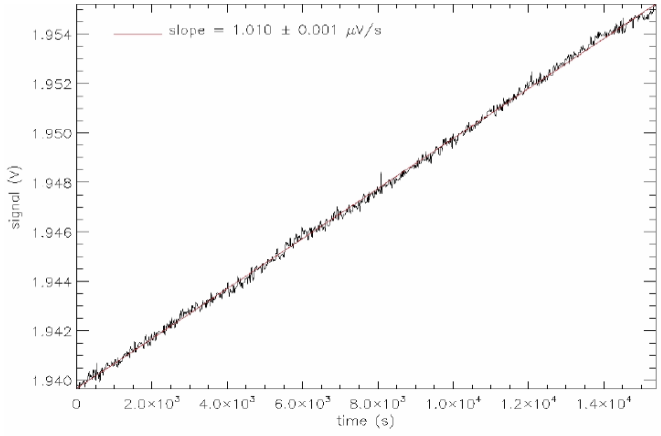

Figure 12: Measurement of the ROIC leakage current

We subtracted then the linear regression obtained by the linear least-squares fit from the drift of the measured output level. We calculated the standard deviation from the resulting signal to give the total noise. As the acquisition chain noise is not negligible with respect to the ROIC intrinsic noise, one had to subtract quadratically the electronics noise from the total noise to obtain the ROIC noise. The average noise on 10fF test pixels corresponds to 97 µV rms of total noise and 94 µV rms of ROIC noise. With the 14 fF pixel capacitance of the 10 fF test pixel, we computed the ROIC noise distribution of the 10 fF test pixels in e- (Figure 13). The average noise measured on 10 fF test pixel was around 4-8 e- rms or 6-12 e- in CDS mode.

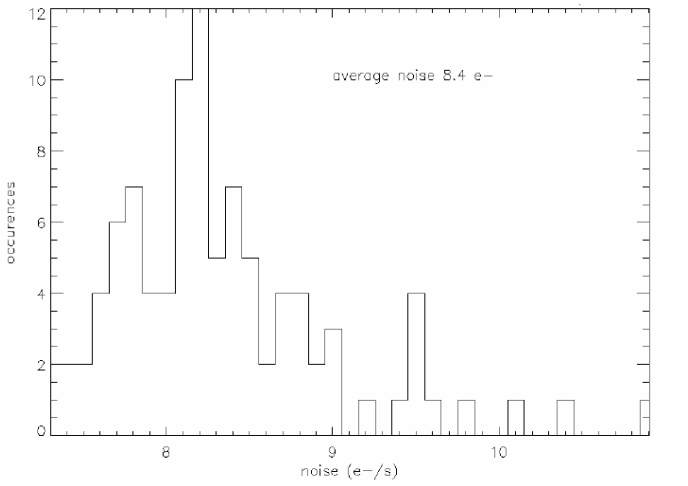

Figure 13: ROIC noise distribution on the 10 fF test pixel

4.4 Glow leakage

Light shielding, careful biasing and others techniques are used to reduce glow consequences on PV diodes. We measured the glow with N/P diodes to separate current leakage (positive drift) and glow (negative drift):

- The main glow source was the unshielded external temperature diodes lighting the entire matrix.
- The next one is about 1 e-/s visible on edges, it came from the extra consumption of slow and fast register that we need to improve.
- No glow effect from analog buffers has been evidenced. Glow current in the matrix is less than 0.06 e-/s/pixel, investigations are still in progress.

Specific internal thermal sensor without glow is present in the ROIC. This internal thermal sensor replaces the typical external temperature diode that generate glow, around 1 e-/s/pixel for 10 µW bias.

Low glow enables noise reduction by Fowler reading.

4.5 ROIC linearity and well capacity

To evaluate this feature, the diffused illumination source is pulsed before each reading with a constant duration after an initial reset and a settling time. In the resultant curve in Figure 14 with a 0.1V bias, we plotted the average output level versus frame number. The electrical dynamic in the SFD architecture is defined by the polarization voltage minus the capacitance reset voltage. This maximum value is however altered by the coupling after the capacitance reset and the roll-off near the full well. The linearity range corresponds to a linear least-squares fit from 6% to 82% of the full well. For the 0.1V bias, the non linearity error is lower than 1% over that range and the useful dynamic is equal to 0.11V.

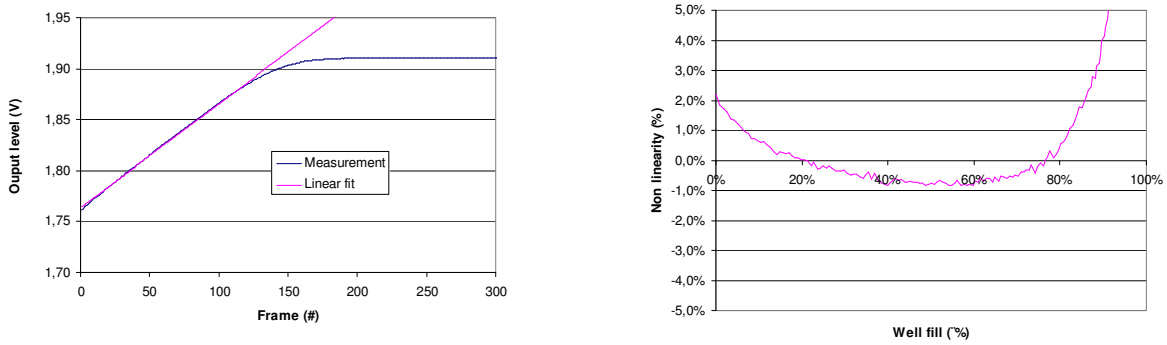

Figure 14 : Detector linearity with a 0.1V bias

In a SFD design, ROIC linearity is inherently linked to the diode linearity, because the device debiases with increasing flux. This effect is more noticeable when the bias is increased. The curve on Figure 15 is obtained for 0.9V bias.

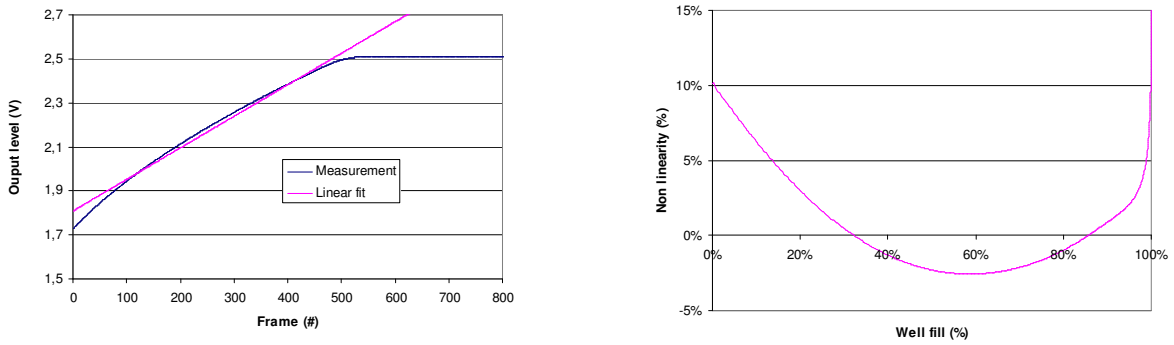

Figure 15 : Detector linearity with 0.9V bias

In that case, the linearity range corresponds to a linear least-squares fit from 7.5% to 99% of the full well. The non linearity error is inferior to 5% and the useful dynamic is equal to 0.7V.

Full well capacity for this kind of detector depends on polarization voltage and conversion gain. The charge handling capacity is calculated from the linearity range and the conversion factor from §4.2. The following table summarizes the results.

Polarization voltage (V)	**0.1**	**0.9**
Charge handling capacity(ke-)	22	120

Figure 16 : Charge handling capacity for different diode bias

4.6 Frame rate and consumption

To evaluate the detector power consumption, we measured all the voltage supply currents with a picoammeter. The pixel rate or the frame rate influences the ROIC consumption because the amplifier current has to be optimized to achieve the

pixel convergence criteria to be attained. We measured then the ROIC consumption in a worst case at a pixel readout rate of 100 kHz (frame rate of 2 Hz) with buffered video outputs. The total power dissipation is lower than 360 µW. This result is lower than the specification; moreover it could be improved by removing the excess of consumption of the logic part.

5. Main applications

This type of detector is well suited for very low fluxes and combines low readout noise and low consumption (which is particularly suitable for instruments mounted on microsatellites). Another driving requirement concerns the photovoltaic diodes coupled to the ROIC for which a low level dark current is needed.

The MicroCarb mission is designed to measure the carbon dioxide (CO_2) column to within 1 ppm from a microsatellite in low Earth orbit (LEO) in order to locate and characterize CO2 sinks and better understand the carbon cycle and predict its evolution. The instrument concept is based on dispersive spectrometer, for which this type of ROIC is a good candidate.

SFD input stage is also widely used for Astronomy applications requiring deep imaging and surveying capabilities. In this case, large IRFPA (format typically higher than 1kx1k) is another driving requirement. As an example, Euclid mission require SFD input stage and large format FPA. Euclid main scientific goals are to map the geometry of the Dark Universe by investigating dark matter distributions, the distance-redshift relationship, and the evolution of cosmic structures.

6. Performances summary and Conclusions

The main characteristics and performances of the detector are summarized in the next table. Most of the specifications have been reached ROIC noise is lower than 6e- which is a very good result for this first SFD input stage detector developed by Sofradir. The other important result is the leakage current best result that is 0.002e-/s and which opens the way for very low dark current measurement, as needed by the applications (#0.01e-/s)

Sofradir SFD ROIC	
Size	384x288
Pixel Pitch	15 µm
spectral range compatibility	SWIR
FPA temperature	between 80K and 140K
Typical Performances (1)	#6e- ROIC Noise, Leakage current # 0.002e-/s , without CDS
Type	CMOS
Number of outputs	2
Output mode	buffered video output
Maximum frame frequency	2 Hz
Pixel readout clock (max value)	100 kHz
Input stage	SFD : Source Follower per Detector
Conversion Factor	# 5 µV/e-
Well capacity @ 0,9V bias	120ke-
Consumption	<0,4mW
Integration mode	rolling frame
(1) @ 50kHz	

Acknowledgments

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