Ultra low dark current CdHgTe FPAs in the SWIR range at CEA and Sofradir

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ABSTRACT

We report here first results carried out at CEA and Sofradir to build ultra low dark current focal plane arrays (FPA) in the short wave infrared range (SWIR) for space applications. Those FPAs are dedicated to very low flux detection in the 2µm wavelength range. In this purpose, Sofradir has designed a source follower per detector readout circuit (ROIC), 384x288, 15µm pitch. This ROIC has been hybridized on different HgCdTe diode configurations processed at CEA-LETI and low flux characterisations have been carried out at CEA-SAp at low temperature (from 60 to 160K). Both p/n and n/p structures have been evaluated. The metallurgical nature of the absorbing layer is also examined and both molecular beam epitaxy (MBE) and liquid phase epitaxy (LPE) have been processed. Dark current measurements are discussed in comparison with previous results from the literature. State of the art dark currents are recorded for temperatures higher than 120K. At temperatures lower than 100K, the decrease in dark current saturates for both technologies. In this regime, currents between 0.4 and 0.06 e/s/pixel are reported.

Keywords : IR detector, MCT, SFD, FPA, SWIR, dark current, low flux

1. Introduction

Space based observatories for astrophysics are very demanding in ultra low flux detection in the IR spectrum. Such low flux levels represent the detection of a few photons only during long integration times (typically 1e-/s during several minutes) and therefore require ultra low dark current photodiodes coupled to a very high performance ROIC stage in terms of noise and leakage. To meet these requirements, a very attractive structure is a source follower per detector (SFD) where the charge integration is carried out on the diode capacitance itself, minimizing the integration capacitance thus optimizing the charge conversion factor, without any injection efficiency issue. Another advantage of such a structure is the fact that it usually allows non destructive readings, enabling different sampling strategies to minimise read out noise such as correlated double sampling, Fowler sampling or follow up the ramp. Up to now, this type of architecture has been mostly developed by US companies leading to very large format focal plane arrays (FPA) involving p/n Mercury Cadmium Telluride (MCT) diodes, InSb diodes and Si:As diodes [1, 2, 3]. In the case of the MCT material system, the choice of p/n polarity is generally driven by dark current considerations. n/p diodes lead usually to larger dark currents because of the presence of Hg vacancies in the p base layer degrading the minority carrier lifetime. However, this is only true in the case of a diffusion limited diode. Nevertheless, to meet ultra low dark current requirements, diodes have to be cooled down to very low temperatures. The thermal evolution of these data suggests that in these conditions [4], the diode limiting mechanisms are not diffusion current from the absorbing layer but more likely generation-recombination (GR) from the diode depletion region. This GR phenomenon being material and technology dependant, it appeared instructive to explore both polarities in low flux and low temperature conditions.
Recently, a modest format SFD ROIC has been developed by Sofradir within the frame of a CNES contract. This ROIC design allows the use of both diode polarities. Within an ESA contract, and CEA internal funding, this new ROIC has then been hybridized on different MCT diode structures (p/n and n/p) processed at CEA LETI and tested in low flux conditions at CEA SAp. The aim of this work was double: characterization of the ROIC performance in use and study of MCT diode limitations in such low flux conditions.

2. Detection chip technology

Detection circuits were fabricated in CEA-LETI's MCT facilities. The targeted cutoff wavelengths were in the SWIR range (2 and 2.5µm) leading to cadmium compositions around x=0.5. Two different growth techniques have been evaluated: molecular beam epitaxy (MBE) and liquid phase epitaxy (LPE). Both growth batches were carried out on lattice matched CdZnTe with an approximate 2.5% Zn concentration in order to ensure a low dislocation density (in the range of the mid 10^4/cm²). MCT layers have then been processed using two different photodiode technologies available at LETI and Sofradir. Both technologies are planar technologies, passivated by CdTe and ZnSe layers.

The first configuration was p/n As implanted diodes on In doped MBE material [5] (N_D~0.5 to 1e16cm^{-3}, 5µm thick). This configuration was applied to 2.5 and 2 µm cut off layers.

A second configuration has also been explored, composed of n/p ion implanted diodes processed on vacancy doped LPE grown material [6], called LETI standard technology (N_A~3 to 5e16cm^{-3}, 8µm thick). This configuration has been applied to 2µm cut off layer exclusively.

At last, 15µm pitch diode arrays were flip chip interconnected to the SFD ROIC (briefly described in the next paragraph) for low flux characterizations. Test chips containing variable diode geometries (from 10x10µm to 120x120µm) were also hybridized on silicon fan outs for standard "high-flux" characterizations in backside illuminated configuration.
Hence both the technology (n/p, p/n) and the metallurgical nature of the absorbing layer have been compared in terms of dark current. Two different cut-off wavelengths are also studied (2.5 and 2µm).

layer	epitaxy	Doping level	MCT thickness	Measured cut off	Total capacitance
PV3080 (p/n)	MBE:In	0.5-1e16 cm^{-3}	4.0µm	2.45µm	38fF
PV3081 (p/n)	MBE:In	0.5-1e16 cm^{-3}	4.2µm	2.03µm	33fF
PV3140 (n/p)	LPE:VHg	3-5e16 cm^{-3}	6.8µm	1.95µm	20fF
PV3141 (n/p)	LPE:VHg	3-5e16 cm^{-3}	6.4µm	1.96µm	20fF

Table 1 : Summary of tested configurations

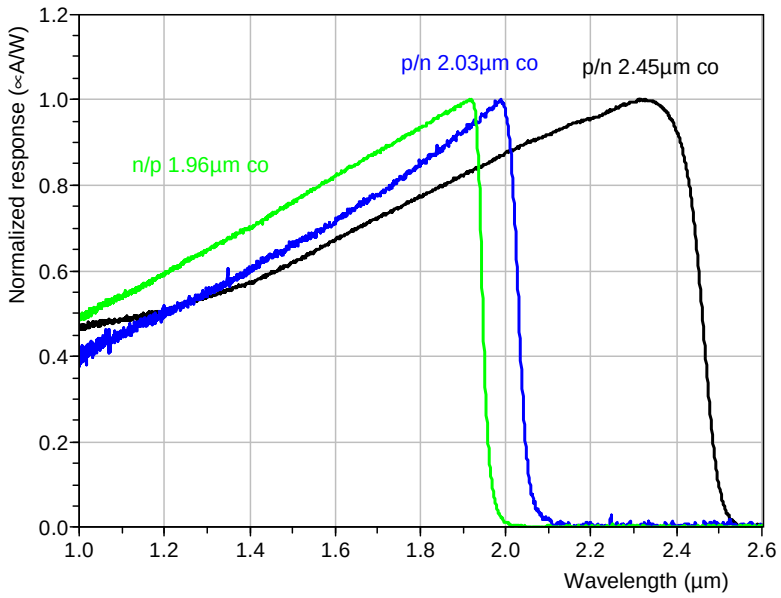

Figure 1 : Example of spectral responses measured under high flux conditions using FTIR spectrometer at 110K

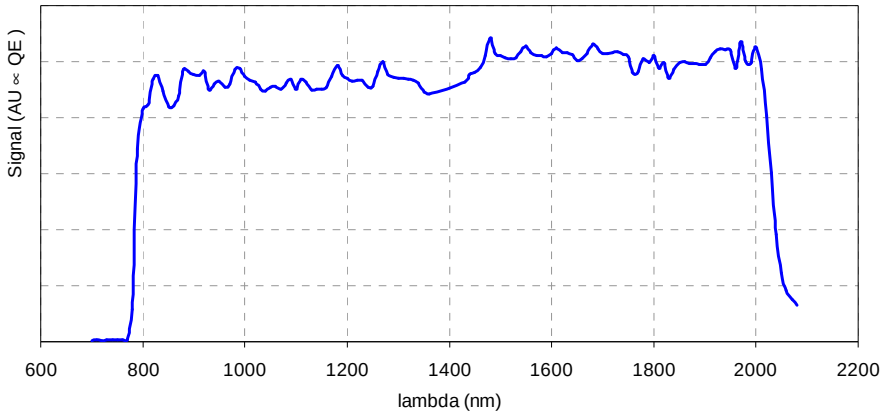

Figure 2 : Example of spectral QE curve measured with a monochromator on layer PV3081 at 77K

First electro-optical tests have been performed under high flux conditions on test chips containing 15µm pitch diodes in array arrangement, hybridized on silicon fan outs. Such diodes are representative of FPA pixels in terms of geometrical and electrical configuration but also in terms of illumination conditions. Spectral responses have been performed using a Fourier Transform IR spectrometer (FTIR) equipped with a DTGS calibrated reference [7]. Typical normalized spectral responses (current relative to incident power) are shown on Figure 1 for three different layers. Half maximum response cutoff wavelengths were estimated at 1.96µm, 2.03µmand 2.45 for those 3 layers, corresponding to n/p on LPE for the first one and p/n on MPE for the two others. Spectral response measurements for different temperatures showed that these cutoff wavelength do not vary with temperature as expected from the typical evolution of the MCT gap [8]. The observed triangular shapes suggests nearly constant quantum efficiency from cuton (0.8µm, limited by CdZnTe substrate transmittance) to peak wavelength, which has been confirmed for the 2.03 cutoff component by another measurement using a diffraction grating monochromator and a calibrated InGaAs photodiode (Figure 2).

Quantum efficiency (QE) measurements have been carried out on the same test chips using a calibrated 1200°C black body cavity. QE at peak response have been estimated larger 70% at 140K both p/n and n/p configurations, taking into account the pixel area $(15\mu m)^2=225\mu m^2$.

Typical I(V) curves measured on isolated 10µm width squared implantation diodes are shown on Figure 3 for temperatures higher than 200K. Such measurements have been carried out in a double shielded helium laboratory Dewar at LETI using a Keithley 6430 femtoamp sourcemeter.
The 2 different diode polarities (p/n and n/p) for cutoff around 2µm are shown and exhibit low leakage current up to polarization larger than 1V.

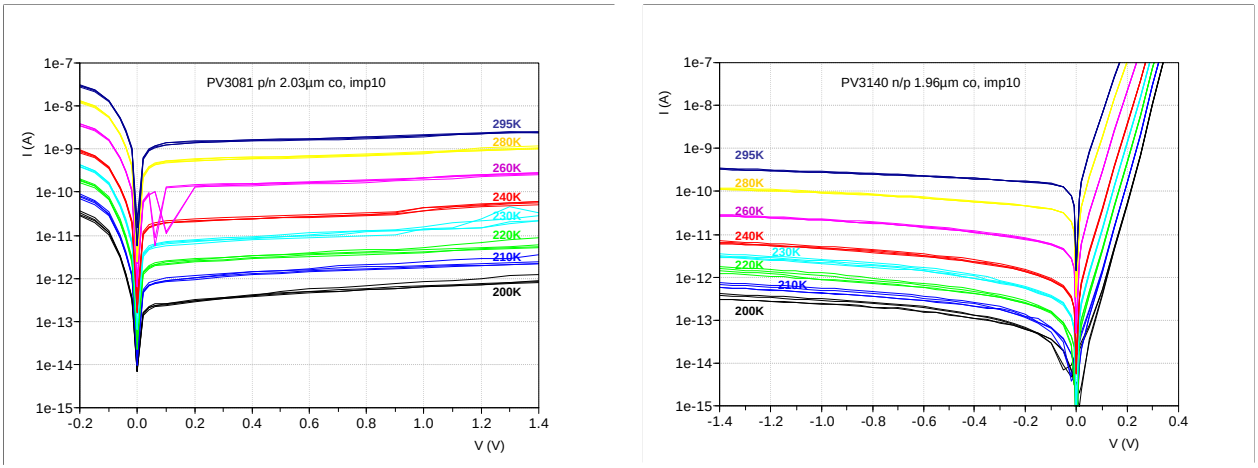

Figure 3 : I(V) curves obtained at darkness between 200 and 300K for ~2µm co p/n and n/p diodes with 10µm width squared implantation

3. Read out circuit design

The ROIC design is detailed in a dedicated paper from Sofradir within the same conference [9]. Briefly, it is a 384x288 array with a 15µm pitch. The input stage is a 3 transistor design source follower per detector (SFD), schematically represented in Figure 4. Two transistors are used as switches (one for the diode reset and the other for the sampling at the output of the follower). Basically, such a structure appears very simple: The diode is reset at the beginning of the integration cycle. Then, during all the integration time, the reset MOS remains open and the diode output only sees the follower transistor grid, which exhibits very high impedance. The photodiode is therefore isolated from the rest of the circuitry and collected charges are unbiasing the diode toward zero. In other words, the collected charges (photo or dark charges) are integrated in the diode capacitance itself, resulting in a variation of the diode node polarization drift toward lower bias values. Actually, the follower transistor has also a non negligible contribution to the integration capacitance that we have to take into account. This input transistor is in fact in follower configuration, ie where crossed by an adapted current Ipolar, it "copies" the base bias onto its collector branch, without any current flow from the photodiode. Non destructive multi-readings are therefore possible using the last transistor as a line switch.

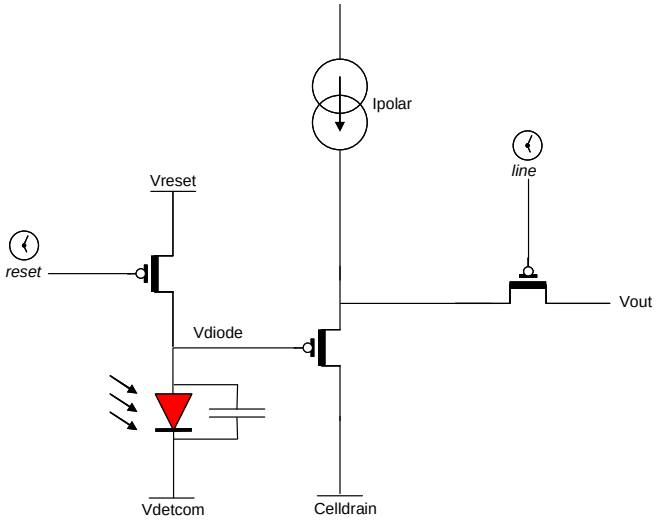

Figure 4 : SFD pixel principle containing 3 MOS per pixel

This structure is compatible with both diode polarities (n/p an p/n) just playing with the detector common contact bias Vdetcom. Moreover, as opposed to direct injection stages, it doesn't suffer from injection efficiency issues as no current is extracted from the diode during integration. Such a structure may appear very simple on the paper, but looking into its details is a hard task: diode bias varies during the integration time and so does the diode capacitance (ie the charge conversion factor). Therefore, the SFD structure is usually not very linear, especially when increasing photodiode current. Moreover, the charge conversion gain highly depends on the detector itself and the way the detector is operated and has to be accurately characterized.

The ROIC design chosen by Sofradir minimizes the ROIC contribution to the integration capacitance. Values as low as 4fF have been achieved, based on test pixel measurements. Efforts have also been made in order to minimize the ROIC noise to reach very low signal levels. Noise values of 4 to 8e- rms have been measured. ROIC current leakage is also very low, as values of 0.002e-/s/node are reported (see [9] for details on ROIC performances).

4. Low flux measurement bench

The bench has been implemented in an existing CEA cryostat (cf. Figure 5), which has been used previously to characterize a NASA/JPL SiAs SB305 BIB detector that has been loaned for the MIRIM development (4- 28µm MIR detector working at 5K) [10, 11]. By construction, this cryostat is light tight; it uses a 2 stage cryocooler, delivering 40W of cooling power at 35K on its first stage, and 1W of cooling power on its second stage. Two thermal shield enclosures are directly attached to the cold heads, and multi layer insulation is wrapping each enclosure to limit the thermal radiation leaks between stages. All the signal harness wires are made of manganin twisted pairs to reduce heat losses between 4K and 300K, and are thermally anchored to the cold heads to avoid unpredictable thermal gradient in the cryostat. The tested device is mounted onto a ceramic leadless chip carrier (LCC), which is a convenient way to assemble and operate such a detector for test and operations means. Such ceramic package provides a very good thermal behaviour and all the electrical connections are taken from the rear face of the chip carrier, thus eliminating any potential parasitic light coming from/thru the wires.

Altogether, the cryostat provides an inner experiment chamber completely light tight, with a surrounding temperature of 4 to 10K (cold screen shield temperature). Thermal stability of 1.7mK rms has been recorded on the detector over 8 hours of experiment.

Reference pixels are available on the ROIC side in order to correct any low frequency fluctuations, which is a common procedure in such a detector. However, the long term stability of the test bench (cryostat and associated electronics) was so good that such a correction was not necessary for integration time up to 5 hours.

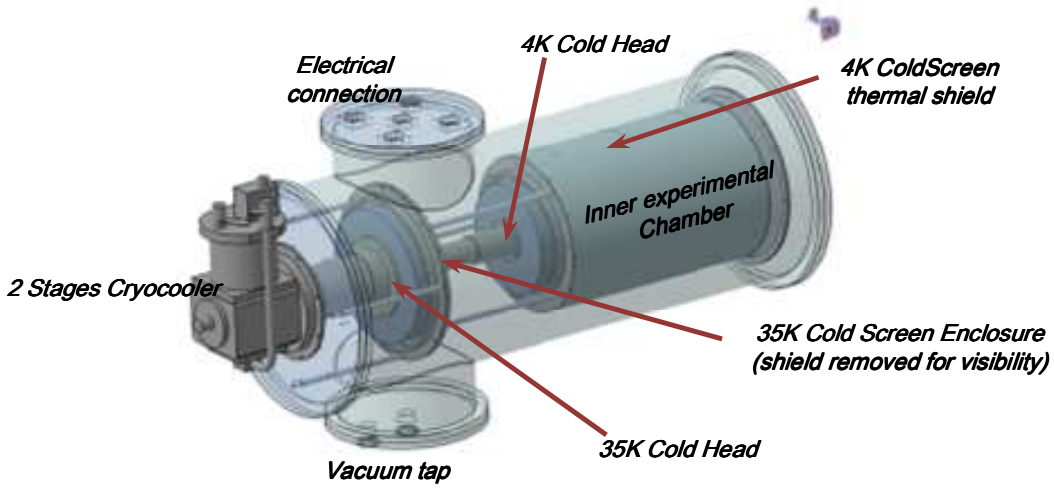

Figure 5: Light tight cryostat used with two stage cryo cooler.

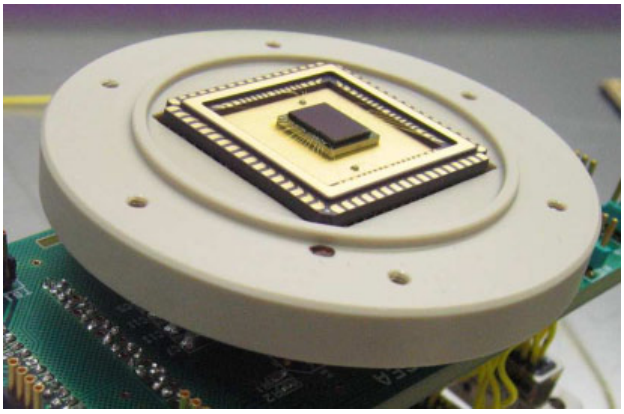

Figure 6 : Real device assembly

5. Conversion gain issue

As mentioned previously (§3), the charge conversion factor has to be determined in order to convert output bias in current. This parameter has two contributions: the diode capacitance and the ROIC parasitic capacitance.

Concerning the ROIC contribution, typical value is estimated around 4fF using an impedance bridge approach on test pixels with known load capacitances of 10, 20 and 40 fF.

Regarding the diode capacitance, direct measurements have been carried out at LETI. These measurements were performed on representative test diodes cooled at 77K in a cryo tip test bench using a LCR meter HP4275A. No particular precaution have been done to lower the flux level: the diodes were front side illuminated by ambient IR radiation. Measured C(V) curves are shown in Figure 7 for both p/n and n/p configurations and both cut off wavelength. For the 2µm cut off, typical values at low bias are in the range of 16fF for n/p diodes and a little higher for p/n diodes (25fF).

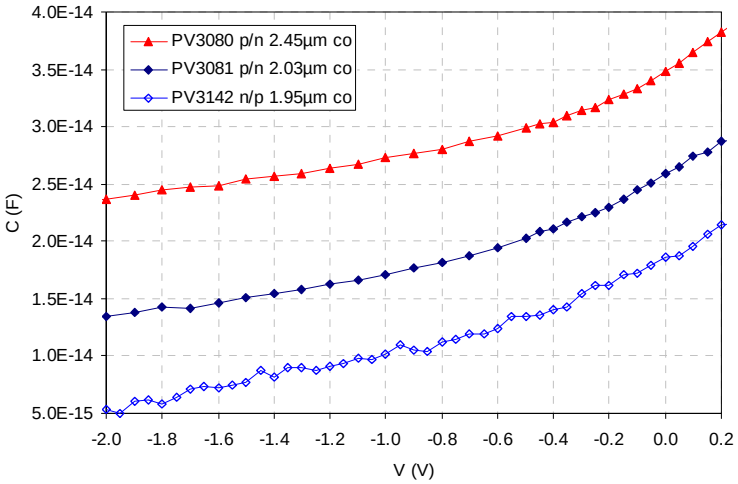

Figure 7 : C(V) measurements at 77K carried out on test diodes.

Direct estimation of the FPA charge conversion factor has been also tested. The usual way to make this estimation is by correlating diode noise and diode signal using FPAs under different illuminations. However, as mentioned by previous authors [12], values obtained using this method were clearly overestimated by a factor close to 50%, probably due to

parasitic capacitances coupling neighboring diodes in the array. An alternative method has also been investigated, namely the « integrated autocorrelation », where integral of autocorrelation function of difference image is plotted against mean signal. For the moment, this method did not give satisfactory result and is still under active investigation.

Given the diodes capacitance measurements and parasitic capacitance estimation, the total capacitance used in the following dark current calculations are:

- 38fF for PV3080 (λc=2.45µm, p/n)
- 33fF for PV3081 (λc=2.03µm, p/n)
- 20fF for PV3140-3141 (λc=1.96-1.95µm, n/p)

These values are very well correlated with kT/C noise measured during reset, which slope is perfectly consistent with reset noise performed on 10, 20 and 40fF test pixels (see [9] for more details).

6. Low dark current estimation

Very low dark current measurements were carried out on FPAs mounted in the CEA-SAp light tight cryostat. The sampling strategy was a "follow up the ramp" scheme (FUR) where the integration ramp is integrally sampled: at low temperature (60-90K), a full image is acquired every 10 to 20s until saturation. The sampling is then faster (0.5s) at higher temperature (>140K), in order to get a full description of the integration ramp with at least 900 readings. The resulting curve presents three different regimes. The first images seem affected by a reset anomaly where charge/discharge of various trap levels in the narrow gap material and/or the passivation may disturb the integration ramp. This phenomenon has been observed by other groups on other SFD ROICs [13, 14]. This reset anomaly is then followed by a linear regime, ended by a saturation regime. Typical curve is shown in Figure 8 for PV3081 FPA cooled down at 80K. The dark current estimation is then given by the slope of this linear regime obtained by linear regression.

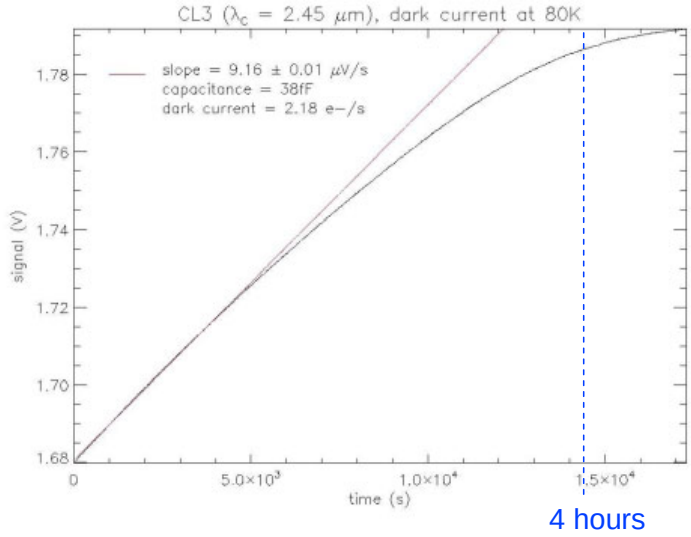

Figure 8 : Typical integration ramp obtained at low temperatures

First measurements gave unfortunately high background dark currents, even for very low temperatures. Besides, the thermal evolution of these currents was not physically relevant for a photodiode dark current. Measured currents were increasing from 3e/s up to 10 e/s, cooling down the FPA from 90K down to 60K, see Figure 9. This effect was observed identically for 2 different FPAs with different cutoff (2.45µm and 1.95µm) and different diode structure (p/n and n/p). Actually, the chip carrier was equipped with two additional temperature probes (2N2222) not properly shielded. Once those probes turned off, the measured dark current felt down to fractions of e/s, without any increase at low temperatures (see Figure 9). This puts in evidence electroluminescence glow from the silicon temperature probes as a potential parasitic flux detected by the FPA photodiodes.

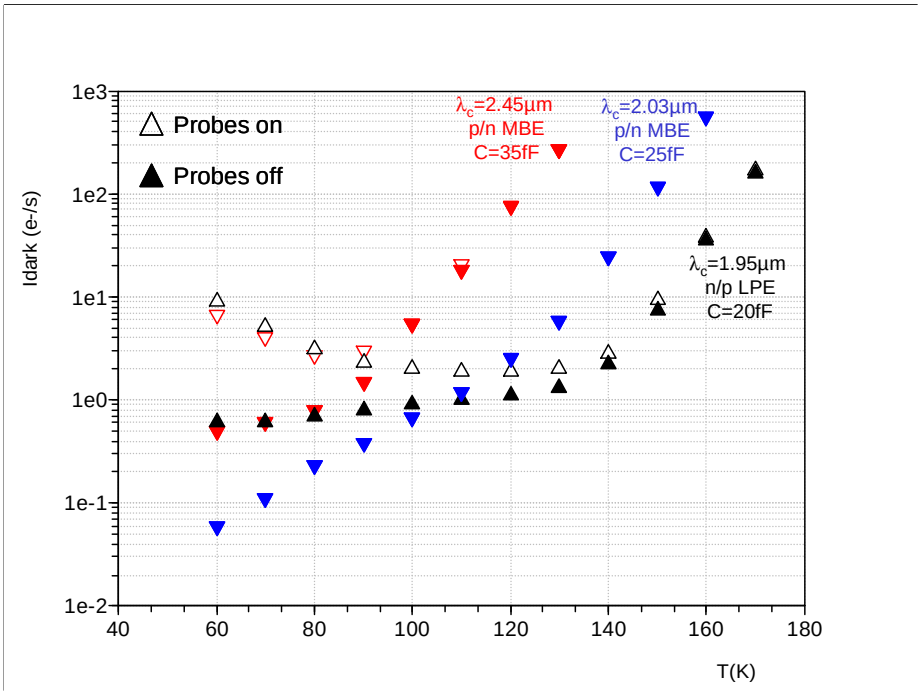

Figure 9 : effect of additional temperature probes (2N2222) on the recorded dark current

At last, very low dark current values are observed at low temperatures (60K). Two components exhibit a dark current floor around 0.4-0.5 e-/s. A last FPA shows an even lover dark current 0.06e-/s at the same temperature.

7. Dark current measurement at higher temperatures

The SFD ROIC gives access to very low current values but is very limited for higher currents: the saturation regime is so rapidly obtained that the slope becomes difficult to estimate for values above 1000 e/s≈0.1fA. In order to investigate the diode behavior at higher temperatures, dark current measurements have also been done at LETI, using the standard IR EO characterization setup (cf §2). Currents have been measured on large diodes (120µm width square implantation) taken from the same wafers, hybridized on Si fan outs, for temperatures between 160 and 300K. Lowest currents reachable in this configuration are in the range of 10fA.

8. Discussion

Figure 10 gathers all dark current densities measured on the three different layers, for both large diodes and 15µm pitch SFD FPAs. Measured currents on FPAs where normalized by pixel area, ie (15µm)². An area of (120µm+L_d)² was taken for large diodes, where L_d stands for lateral diffusion length (5-6µm for n/p and 10-15µm for p/n). Diffusion trend line is also plotted for the three MCT compositions in plain line

Measured data follows this diffusion trend line down to relatively low temperatures (around 170K). At lower temperature however, the decrease in dark current is not so effective, consistent with generation-recombination (GR) limiting currents. At last, two detectors have exhibited a common dark current floor lower than 1e-/s at very low temperatures, whereas the last one kept on going down to ultra low current values, lower than.0.1e-/s. The real nature of the ultimate limiting mechanisms is not really clear today, and remains under investigation. However, the first floor around 0.4e-/s is common to two very different FPAs: Cut off wavelengths (2.45µm vs 1.96µm), diode technologies (p/n vs n/p) and epitaxial methods are different, which suggests that this limiting phenomenon may not be related to the photodiode itself. Moreover, the fact that we were able to measure even lower values on the last detector suggests also that this 0.4e/s floor is not related to any optical pollution or leakage in the measurement bench. A last remaining contribution to this excess currents could be related to non negligible glow from the ROIC, which may vary for unknown reasons from one ROIC to another.

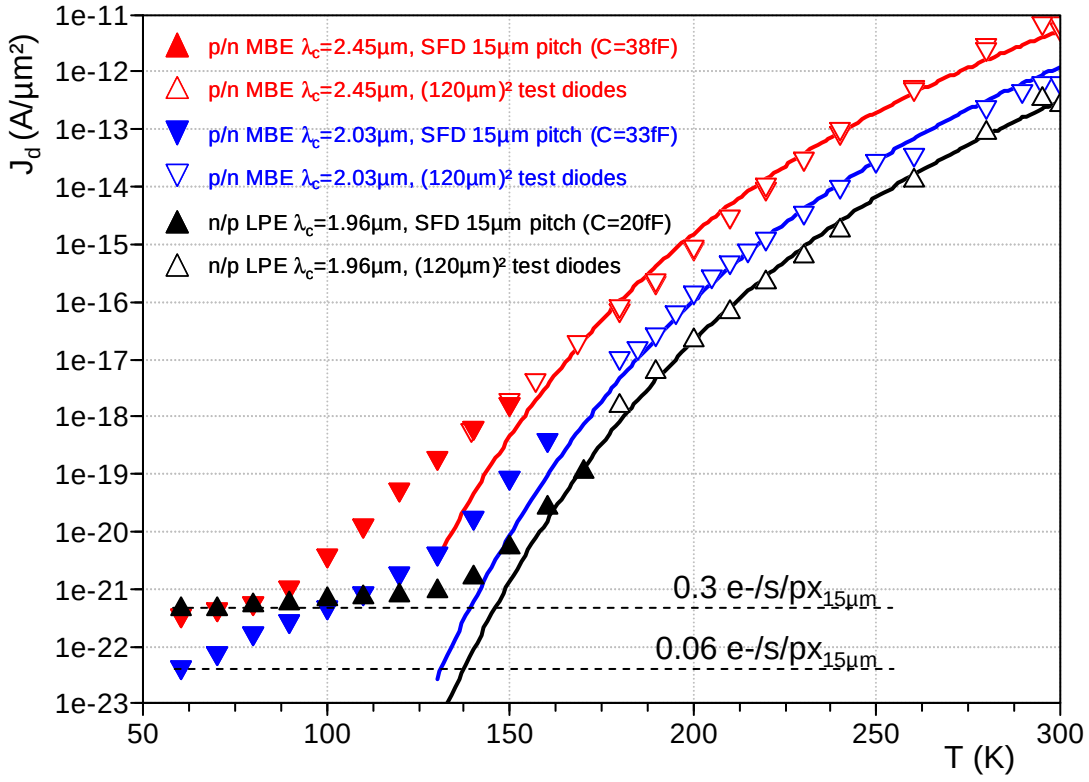

Figure 10 : Dark current measurements carried out on PV3080 (red), PV3081 (blue), and PV3140 (black) using both SFD FPA and large test diodes.

The last figure (Figure 11) is a comparison of dark current densities between our recent data and data taken from the literature at 2.5µm cut off. MBE p/n data from layer PV3080 is represented together with 2.5µm co dark currents measured on standard LPE n/p 15µm pitch CTIA FPA from Sofradir. Also represented is VIRGO data [15] corresponding to dark current measured on a 20µm pitch SFD FPA where diodes are fabricated using MBE grown p/n heterojunction reticulated by a mesa etch. Two representative diodes of a Hawai2RG FPA [16] are also plotted, corresponding to a p/n ion implantation technology on MBE material, similar to our p/n technology. At last, a plain line stands for the Rule07 [17] which is a widely used empirical rule given by Teledyne to estimate the optimum dark current reachable by a diffusion limited p/n diode. Dotted line gives a trend for a GR limited diodes starting at 110K, given the intrinsic carrier concentration ni from Hansen law [18].

A first comment is that our first attempt to reach very low dark current seems successful: state of the art dark currents are measured on a large range of temperature. However, the floor level measured on our FPAs may be improved as it remains one to two orders of magnitude higher than ultimate limits observed on VIRGO and Hawai.

A second comment is that, given the technological parameters used here, both MBE p/n and LPE n/p configurations gave the same level of dark currents for temperatures higher than 160K. Furthermore, p/n dark currents measured on our diodes at high temperatures (where it should be diffusion limited) remain one order of magnitude higher than rule07. Moreover, data taken at lower cut off in Figure 10 show n/p diodes even better than p/n by a factor of 5, for a cut off difference of just 0.07µm. In fact, this rule 07 holds only for low doping level diodes (lower than 1e15 cm^{-3}). The fact

that we were working with a factor of 10 higher doping levels (1e16 cm^{-3}) is supposed to increase the dark current significantly. Actually, for such diffusion limited diodes, dark current is related to minority carrier lifetime, which is inversely proportional to the doping squared:

$$J_{dark} \propto \frac{1}{\tau} \propto N_{Dop}^2$$

Hence, lowering this doping by a factor of 5 to10 should decrease this dark current by a factor up to 25 to100. Therefore, at high temperature p/n data should exhibit lower dark currents than n/p as suggested by rule07.

However, at low temperatures, diodes are usually not limited by diffusion current from the absorbing layer. Limitations are more expected to be related to GR phenomenon occurring in the depletion layer, and improvement may not be expected lowering the doping level. In this regime, the material quality but also the surface passivation should be key parameters for dark current optimization.
Therefore, it is interesting to watch carefully the difference between the two wafers at 2µm cut off in Figure 10. LPE n/p diodes remained very close to the diffusion line down to 160K, corresponding to currents densities in the mid 10^{-20}A/µm², whereas MBE p/n diodes left the diffusion lines earlier around 180K for current density two orders of magnitude higher, in the 10^{-18}A/µm² range. It should be very interesting now to investigate other configuration such as MBE n/p or LPE p/n in order to see whether the determining parameter in limiting GR currents is related to the layer nature or the technology itself (passivation and depletion region extension).

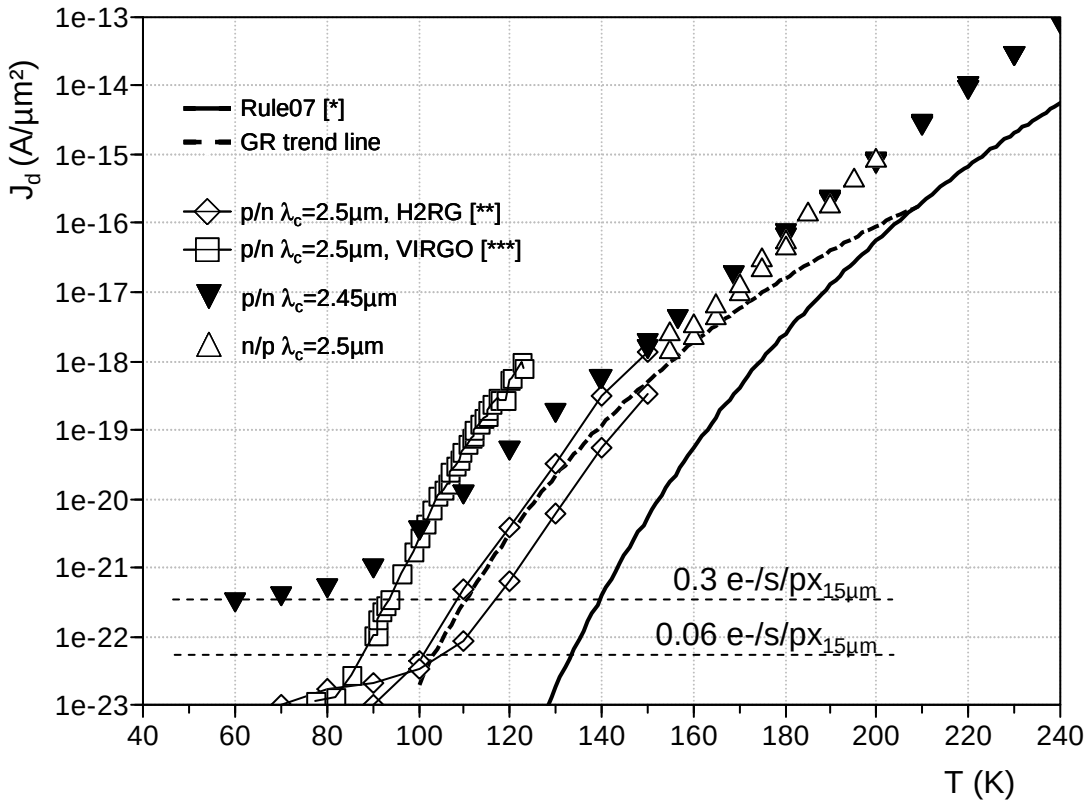

Figure 11 : measured dark currents and comparison with literature data at 2.5µm cut-off [14, 16, 17]

9. Conclusion

In conclusion, low flux detection in SWIR range (2.5 to 2 µm cut off) has been investigated at CEA using a new SFD ROIC designed by Sofradir. Two different diode configurations have been investigated: p/n ion implanted diodes on MBE grown MCT layers and n/p diodes made by ion implantation on VHg doped LPE grown layers. At high temperatures, diodes follow a diffusion trend line for both technologies. This diffusion regime holds down to relatively low temperatures, between 160 and 180K. Dark currents recorded at lower temperatures with the SFD ROIC show as expected an inflexion in the decreasing rate of the dark current, usually attributed to G-R current limitation. However, measured dark currents keep on decreasing for even lower temperatures. Two detectors showed a minimum dark current floor of 0.3e/s/pixel, independent from cut off or diode configuration. The third one showed even lower dark currents, as values as low as 0.06 e/s/pixel have been recorded at 60K. Therefore, state of the art currents have been measured with the first version of this ROIC, using non optimized diodes. Both configurations (MBE p/n and LPE n/p) gave similar dark currents, but optimization remains possible in the p/n case.

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REFERENCES

[1] A. M. Fowler, "*Performance of the current 256x256 SBRC InSb array and status of the next generation 1024x1024 InSb array*", Experimental Astronomy 3 p243 (1994)
[2] J. Wu, "*Development of IR detectors for space astronomy*", Thesis Univ of Rochester (1997)
[3] G. Finger, "*Review of the state of infrared detectors for astronomy in retrospect of the June 2002 Workshop on Scientific Detectors for Astronomy*", proceedings of the "SPIE's International Symposium on Astronomical Telescopes and Instrumentation", 2002
[4] R.E. Dewames, "*Dark current generating mechanisms in short wavelength IR photovoltaic detectors*", JEM27(6) p722 (1998)
[5] L. Mollard, "*HgCdTe FPAs made by Arsenic-ion implantation*", SPIE 6940 p0F (2008)
[6] G. Destefanis, "*MCT IR diode arrays*", SemiCondSciTech 6 pC88 (1991)
[7] O. Gravrand, "*HgCdTe Quantum Detection: from Long-Wave IR down to UV*", JEM 40(8) 1781 (2011)
[8] G. L. Hansen, "*Energy gap vs alloy composition and temperature in CdHgTe*", JApplPhys. 53(10) p7100 (1982)
[9] B. Fieque, "*IR ROIC for very low flux and very low noise applications*", SPIE8176-55 (2011)
[10] S Ronayette, "*Performance verification of the MIRI imager flight model at CEA*", Proceedings of 2010 SPIE Space Telescopes and Instrumentation Conference, Vol. 7731, San Diego, (2010)
[11] J. Amiaux; "*Development approach and first infrared test results of JWST/Mid Infra Red Imager Optical Bench*", Proceedings of 2008 SPIE Space Telescopes and Instrumentation Conference, Vol. 7010, Marseille, (2008)
[12]G. Finger, "*Interpixel capacitance in large format CMOS hybrid arrays*", SPIE6276-0F (2006)
[13] R. Smith, "*Noise and zero point drift in 1.7um cutoff detectors for SNAP*", SPIE 6276-0R (2006)
[14] R. Smith, "*VIRGO-2K 2.5um HgCdTe Dark Current*", SPIE 5499 (2004)
[15] Mc Mutry, "*Characterization of 2.5µm HgCdTe VIRGO/VISTA detector array*", SPIE San Diego (2005)
[16] G. Finger, "*Performance evaluation, readout modes and calibration techniques of HgCdTe HAWAII-2RG mosaic arrays*", SPIE 7021-28, (2008)
[17] W. E. Tennant, "*MBE HgCdTe Technology: A Very General Solution to IR Detection, Described by ''Rule 07'', a Very Convenient Heuristic*", JEM 37(9) 1406 (2008)
[18] G. L. Hansen, "*Calculation of intrinsic carrier concentration in HgCdTe*", JApplPhys. 54(3) p1639 (1983)