Le développement des circuits intégrés
Une introduction

- Histoire simplifiée des technologies de circuits intégrés : induite par la science des semiconducteurs plus qu'a la radio
- Au début : utilisation empirique de solides comme le sulfure de plomb (galène comme ce n'était pas compris on s'est tourné vers les tubes a vide) (fin du XIX siècle)
- Tubes a vide (Lee de Forest)
- Ensuite retour vers les dispositifs état solide (1940-50)
- La voie est ouverte pour l'intégration monolithique (1960 ---…)

- Simple history of Integrated Circuit Technology : semiconductor science rather than radio techniques (RF Integrated Circuits are one of the last step)
- Semiconductor (early empirical) : PbS (Lead Sulfide) point contact not well understood then replaced with vacuum tubes
- Vacuum tubes
- And then back to Solid State devices
- It's then the step forward towards monolithic integration

OUTLINE

- Introduction à la technologie et la conception des circuits intégrés
- Progrès dans la fabrication et des matériaux solides: quelques exemples
- Premières avances dans la théorie quantique du solide
- Bases de la technologie des Circuits Intégrés
- Integrated Circuits technology and design : an introduction
- Progress in solid material processing : some examples
- Early progress in quantum solid state theory
- Integrated Circuits Basic Devices

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IC TECHNOLOGY AND DESIGN : AN INTRODUCTION

- The birth of semiconductors : material processing, physics and devices (first step Lilienfeld patents ,1920)
- Physics of active devices, monolithic integration, how it was a possibility and a requirement
- Progress in circuit theory and information processing, analog and digital electronics and hence microelectronics
- Signal and circuit theory, mainly Radio pre-1940 (heterodyne, negative feedback …)
- Specific circuits and devices in integrated circuits
- One exception : power devices
- Radiation hardening issues

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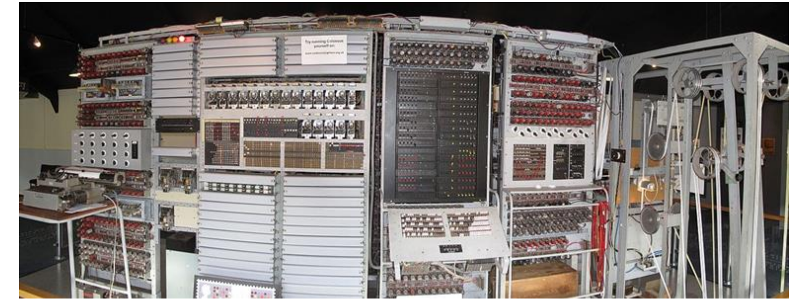
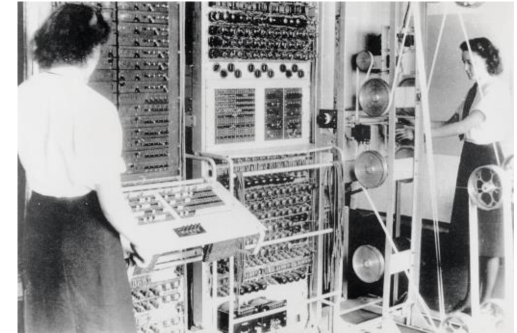
IC TECHNOLOGY AND DESIGN:AN INTRODUCTION





- Implication in circuit theory and practice
- Monolithic integration
- Huge number of nodes and branches
- Analytical calculations outpaced by numeric simulations
- Large and complex digital functions
- Power reduction : from the Colossus to the microprocessor
- Vacuum tubes : 10-1 mA 100 V : 1 W per gate and one heating filament (10 W) a few tens of KHz
- Old CMOS : 30 mW-3mW per gate in the MHz range
- Now : 1 µW @ 1GHz

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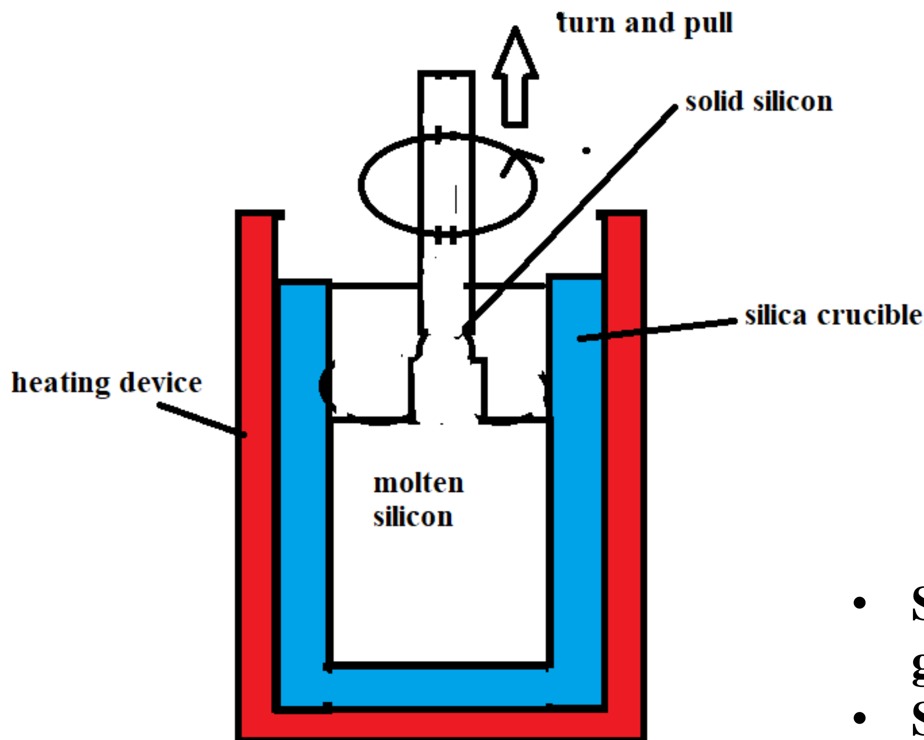
PROGRESS IN MATERIAL PROCESSING : CRISTAL GROWTH

- **Czrochralski growth, needs a seed**



- Because of the silica high oxygen content Si is not the problem
- Cz also used for III-V (encapsulated)
- Magnetic Cz (reduced convection)
- Needs initial purified material
- Travelling heater method (Pfann method)
- Zone melting where impurities diffuse
- FZ wafers Vacancy-Oxygen complexes widely characterized
- Impurity gettering such as transition metal at oxygen clusters, precipitates

- **Silicon wafers are mechanically resistant , not as brittle as germanium wafers, so large diameter can be fabricated**
- **Self passivation by native 2 nm oxide.**
- **Initial Silicon material is produced by the reduction of silica by carbon**

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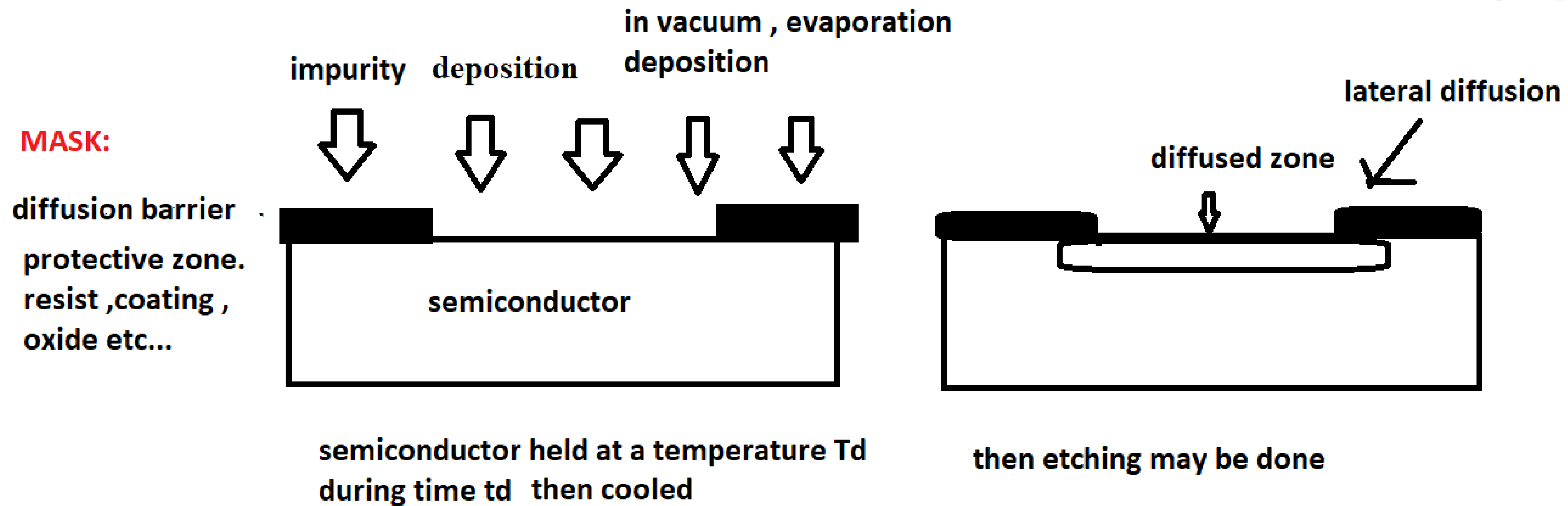
PROGRESS IN MATERIAL PROCESSING : DOPING BY DIFFUSION

- **Impurity doping by diffusion :**



other techniques exists such as gaseous cracking (for impurities such as P, As ,B)
modern processing needs high temperature reduecd time : RTD,RTP

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PROGRESS IN MATERIAL PROCESSING : DOPING BY DIFFUSION

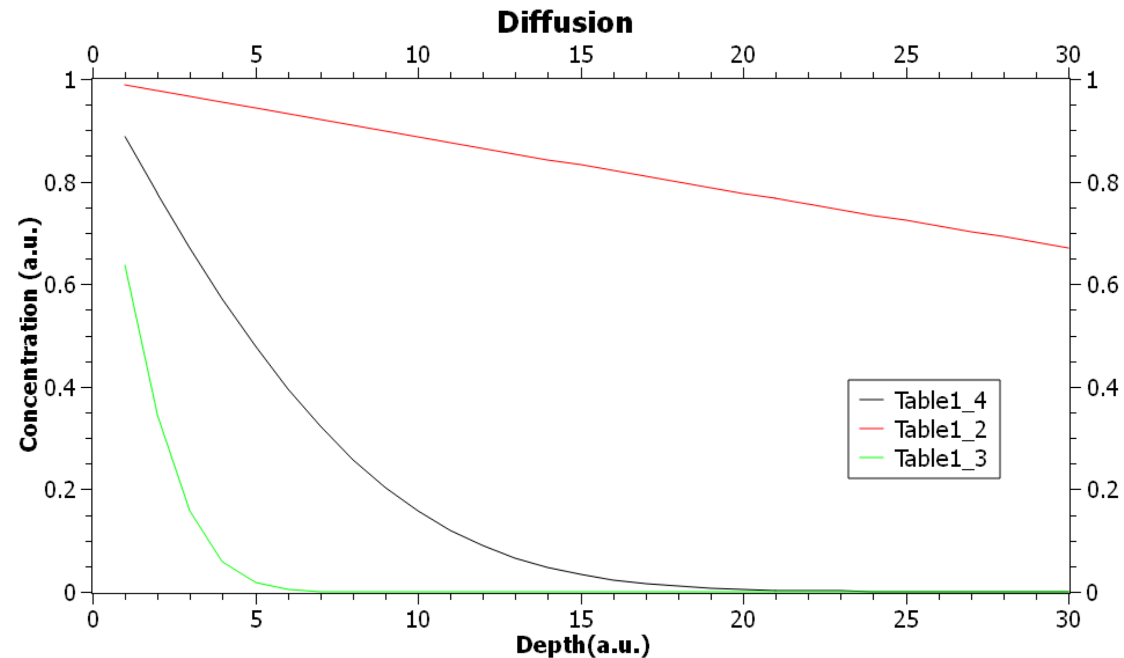
Problems with diffusion:

Diffusion constant depends on the properties of the material (defect, dislocations)

It is a high temperature process

Poisenous impurity exist: for both Ge and Si , such as Copper, Gold and transition metal

Aluminum is a shallow p-dopant , so it has been used in priority for metal lines



$$\frac{\partial \rho}{\partial t} + \vec{\nabla} \cdot \vec{j} = 0$$

$$\frac{\partial \rho}{\partial t} - \Delta D\rho = +M_i$$

$$M_i = M\delta(x)$$

$$\rho(x,t) = \rho_0 \ erfc\left(\frac{x}{\sqrt{Dt}}\right)$$

$$\text{erf(x)} = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} \mathrm{d}t \ \text{ here } \ \mathrm{erfc}(x) = 1 - \mathrm{erf}(x)$$

CLASSIC THERMAL DIFFUSION IS NOT ACCURATE (DEPTH CONTROL)
FIRST SOLID STATE DEVICES , SINGLE TRANSISTORS OR DIODES
This technique triggered diffusion of impurities and defects in semiconductors studies (ten thousands of papers , thesis)
Renewed interest with laser processing and RTD

PROGRESS IN MATERIAL PROCESSING : DOPING BY ION IMPLANTATION

ION IMPLANTATION

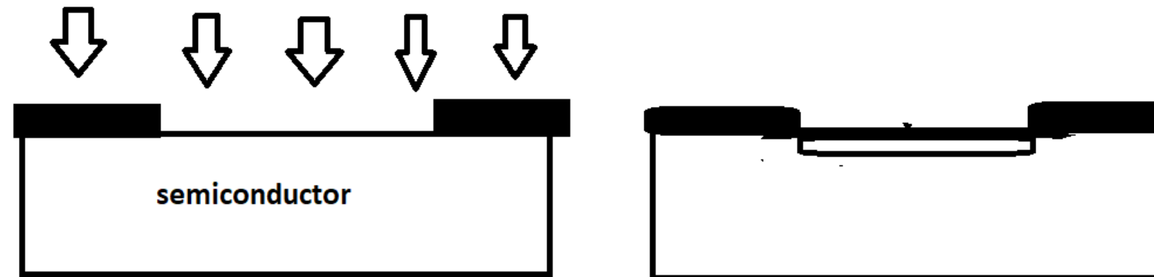
- Theoretical advances : LINDHARD ,SHARFF, et SCHIOTT (1950's) , ion transport in matter at low energy
- Accelerator techniques : up to 500 keV (higher energies are used too (SIMOX))

Ion Implantation : energy of a few keV , flux of 10^{12} cm-2s-1

Ion sources gases , cracking and mass separation

MASK:

protective zone.
resist ,coating ,
oxide etc...



substrate held at room temperature or below , thermal treatment sometimes necessary to repair implantation (irradiation) defects always ⇧

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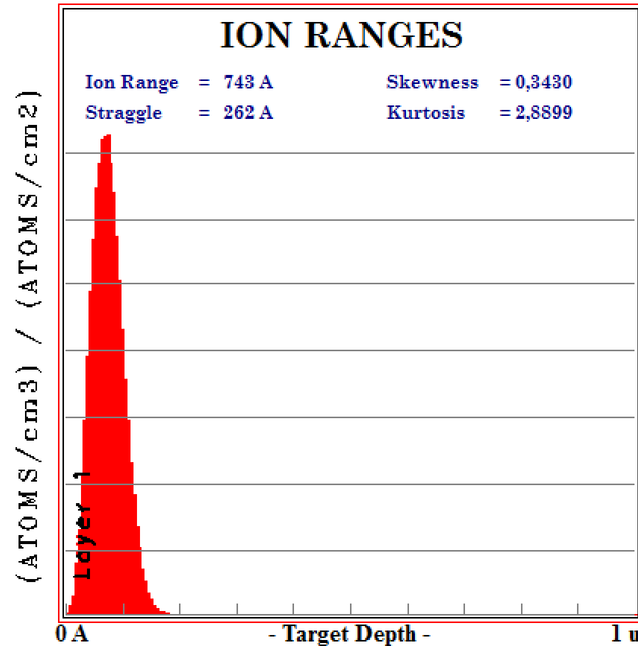
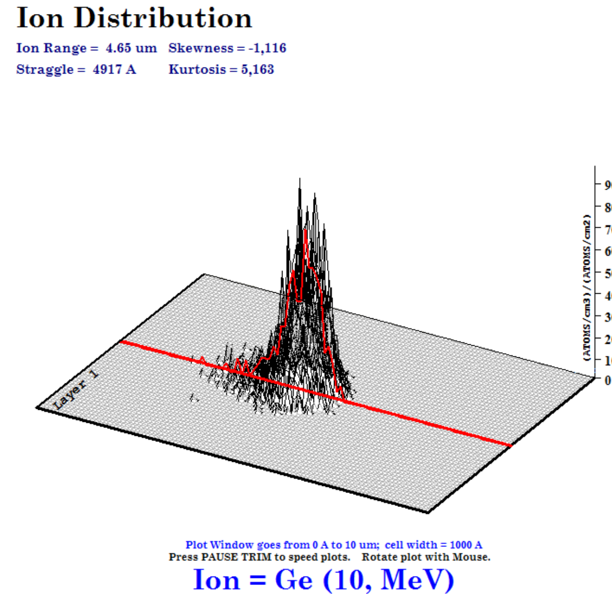
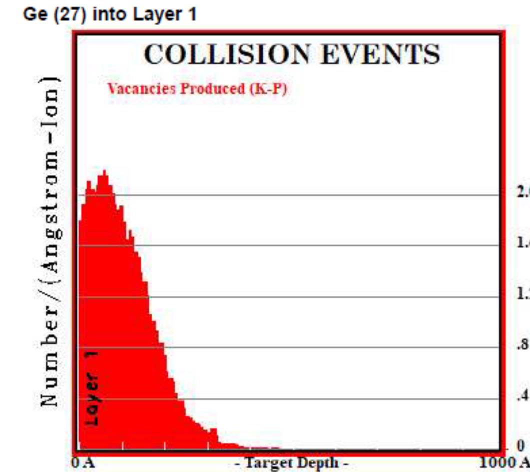
PROGRESS IN MATERIAL PROCESSING : DOPING BY ION IMPLANTATION SIMULATION







1821 Ions Calculated
Ion Type = Ge
Ion Energy = 27 keV
Ion Angle = 0

Calculation Parameters:

Backscattered Ions	17
Transmitted Ions	0
Vacancies/Ion	405.2

ION STATS	Range	Straggle
Longitudinal	162 A	83 A
Lateral Proj.	57 A	75 A
Radial	90 A	56 A

Type of Damage Calculation
Quick: Kinchin-Pease

Stopping Power Version
SRIM-2008

% ENERGY LOSS	Ions	Recoils
Ionization	5.13	19.47
Vacancies	0.21	2.77
Phonons	0.71	71.72

SRIM-2013.00
July 19, 2018
www.SRIM.org

SPUTTERING YIELD

	Atoms/Ion	eV/Atom
TOTAL		
Ge	0.000000	0.00

Target layers:

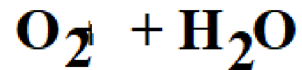
	Layer Name	Width (A)	Density	Ge (72.61)	Solid/Gas	Stop Corr.
1	Layer 1	1000	5.350	1.00000	Sold	1
	Lattice Binding Energy			2		
	Surface Binding Energy			3.88		
	Displacement Energy			20		

High energy in this case 1 MeV , used for SIMOX technology (Separation by Implanted Oxygen)

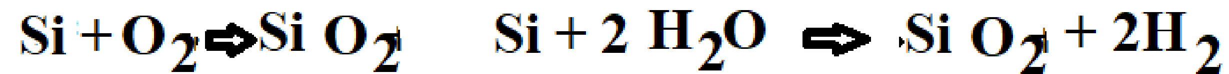
Many implantation induced defects that need to be removed , point defects and dislocations , many studies were devoted to this topic (thousands of papers, theses)

PROGRESS IN MATERIAL PROCESSING : INSULATORS BY THERMAL OXIDIZATION

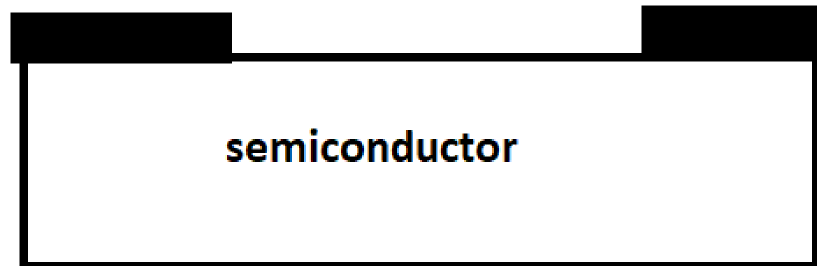
Thermal Oxide

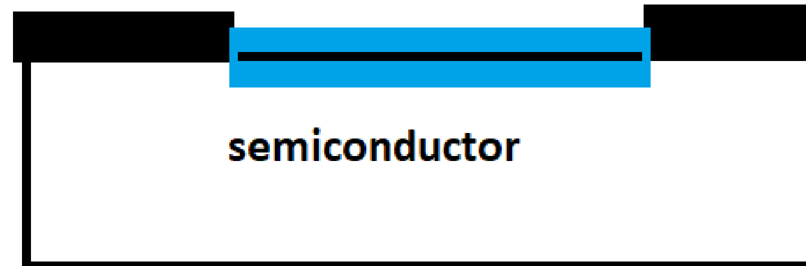


Thickness : 3 nm to 25 nm
wet oxide , faster oxidization than dry oxide



limited by oxygen diffusion





high temperature : > 700 °C

Oxygen vacancies : E' centers

- E' centers tend to charge positively under ionizing irradiation , low hole mobility in the oxide
- (100) substrate orientation to reduce interface state density and to enhance mobility

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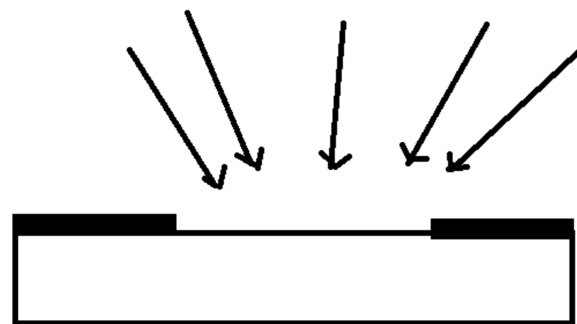
PROGRESS IN MATERIAL PROCESSING : DEPOSITION EPITAXY

- **Material deposition :**
- **Amorphous materials : Silicon Dioxides, Nitrides, Glasses**
- **Crystalline layers, should be epitaxial grown layer on a substrate or another layer**
- **Crystal structure and lattice constant**
- **Strained layers lattices examples : SiGe on Silicon, GaInAs on InP**



molecules react with the surface and an epitaxial layer is formed , different molecules give way to a chemically different layers

MBE : molecular beam epitaxy a beam of molecules with a velocity
homoepitaxy : identical chemical as the substrate
heteroepitaxy : chemically different

MBE : Solid source, sublime , need Ultra High Vacuum 10-8 Torr or less used for IIIV (1958-1960)

In UHV CVD (Chemical vapour Deposition)
chemical gas act as precursors and react
with the surface , these reactions can be enhanced by a
Plasma using RF (PECVD)
For silicon SiH4 (silane) and germanium GeH4(germane)
In LPE liquid phase epitaxy a liquid reacts with the
Substrate (thick layers, III-V)
Substrate may need high temperature heating to set chemical reaction

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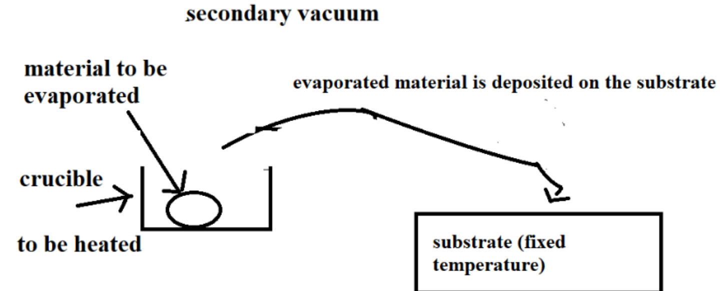
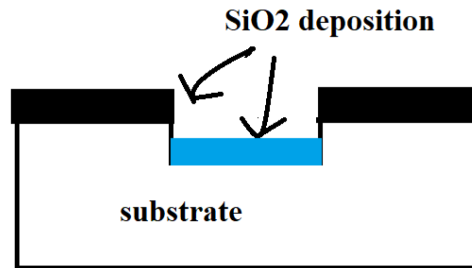
PROGRESS IN MATERIAL PROCESSING : SPUTTERING AND DEPOSITION

- Material deposition :
- Non crystalline : amorphous of polycrystalline
- No need for a substrate with lattice matching, fast deposition rate but low crystalline quality
- Use of Sputtering in vacuum , a target of the material is bombarded with ions, the sputtered ions are accelerated by an electric field (substrate put at a voltage bias and heated if necessary) , and a coating occurs
- Use of a silicon dioxide as a target for field oxides , no need to have a good interface with Silicon
- Use as a magnetron (RF) for ionization and a plasma source (atomic ion low temperature plasma)
- The interface substrate/film is not well defined
- The same apparatus can be used for plasma etching





- Problems : oxides may get charged because of the ions used
- Many impurities can be deposited
- But better than Vacuum Evaporation (lower temperatures and reduced contamination)

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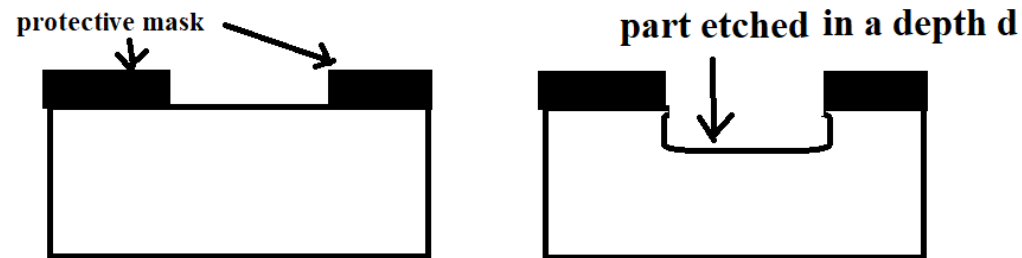
PROGRESS IN MATERIAL PROCESSING : ETCHING

Etching:

- Is defined by the way for a given area in a (solid) material we remove some material of thickness in a predefined way (isotropically or anisotropically)
- Selective etching (etching silicon dioxide and not silicon)
- Three techniques : wet etching , gaseous etching and dry etching



- Wet etching the oldest : corrosive liquid bath reacting with and removing material using a chemical reaction
- Needs liquid processing and rinsing (pure liquids)
- Not very adapted for automation
- Examples : HF acid used for SiO2 (glass) removing
- Redox 'blend' CPn oxidizing and dissolving silicon or germanium
- Reaction rate depends on the bath temperature (control)

- One alternative, chemical gaseous etching, better controlled in a reactor
- Example XeF2 vapour etching used for silicon processing
- The newest : dry etching with ions(plasma, physical)) or reactive (chemically) ion etching
- Better controlled but slower (example etching with Ar ions in a sputtering apparatus). May be used at low temperature . Well controlled, time , pressure allows measurements during processing

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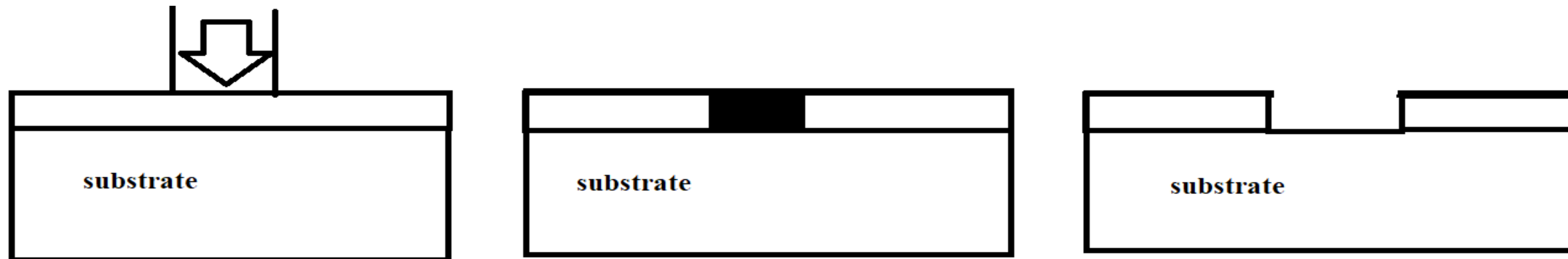
PROGRESS IN MATERIAL PROCESSING : PATTERNING/RESISTS

- Processing: Masking and photoresists
- Visible light towards lower wavelength (electron beam lithography, shorter wavelength)) feature length of the order of the wavelength problem can be solved by adequate light source positioning and the use of UV
- Main principle :
- Positive resist : part exposed is soluble into a solvent (developer), limits in line feature
- Negative resist the part non-exposed is soluble in the solvent (developer)

- POSITIVE RESIST



New resists , multipaterning , with specific masks the rescue.
Today; needs high doses of UV light (Extreme Ultra Violet) >>> Soft X rays ???
Wavelength is of the order of 10 nm, Problems next to ionizing irradiation effects during fabrication
Radiation tolerance during fabrication is needed for nanoscale processes !!!

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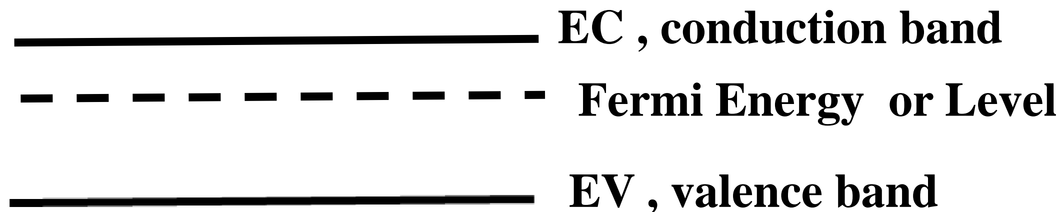
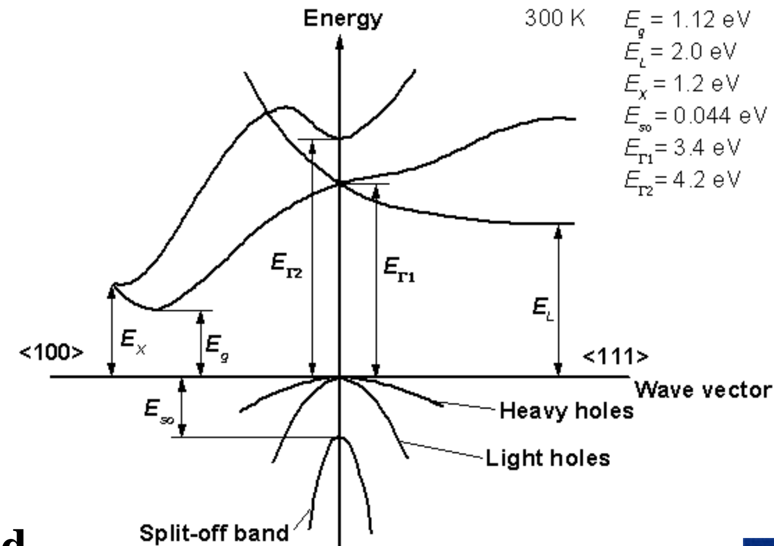
PROGRESS IN SOLID STATE PHYSICS THEORY

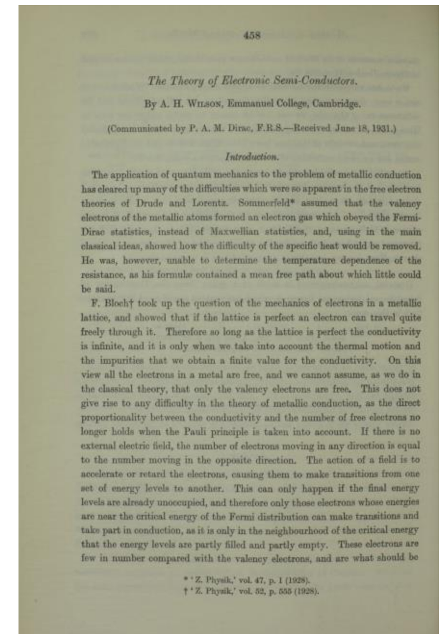
- Once pure enough semiconductors :
- p type with holes in the valence band
- n type with electrons
- Intrinsic : Fermi level roughly in the middle of the bandgap (holes + electrons)
- Mobility depends on the effective masses of the electron and holes (electronic structure of the soli effective mass tensor anisotropic effective mass) < free electron mass >>> speed
- Quantum theory of solids : 1920's-1940's onward
- Band structure of solids (Calculation , more recei numeric technique (Density Functional Theory)

  - Distinction between direct bandgap and indirect band gap semiconductors
  - Optical properties



Ioffe Institute (Russia) band structure of silicon





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The Theory of Electronic Semi-Conductors.

By A. H. Wilson, Emmanuel College, Cambridge.

(Communicated by P. A. M. Dirac, F.R.S.—Received June 18, 1931.)

Introduction.

The application of quantum mechanics to the problem of metallic conduction has cleared up many of the difficulties which were so apparent in the free electron theories of Drude and Lorentz. Sommerfeld* assumed that the valency electrons of the metallic atoms formed an electron gas which obeyed the Fermi-Dirac statistics, instead of Maxwellian statistics, and, using in the main classical ideas, showed how the difficulty of the specific heat would be removed. He was, however, unable to determine the temperature dependence of the resistance, as his formulæ contained a mean free path about which little could be said.

F. Bloch† took up the question of the mechanics of electrons in a metallic lattice, and showed that if the lattice is perfect an electron can travel quite freely through it. Therefore so long as the lattice is perfect the conductivity is infinite, and it is only when we take into account the thermal motion and the impurities that we obtain a finite value for the conductivity. On this view all the electrons in a metal are free, and we cannot assume, as we do in the classical theory, that only the valency electrons are free. This does not give rise to any difficulty in the theory of metallic conduction, as the direct proportionality between the conductivity and the number of free electrons no longer holds when the Pauli principle is taken into account. If there is no external electric field, the number of electrons moving in any direction is equal to the number moving in the opposite direction. The action of a field is to accelerate or retard the electrons, causing them to make transitions from one set of energy levels to another. This can only happen if the final energy levels are already unoccupied, and therefore only those electrons whose energies are near the critical energy of the Fermi distribution can make transitions and take part in conduction, as it is only in the neighbourhood of the critical energy that the energy levels are partly filled and partly empty. These electrons are few in number compared with the valency electrons, and are what should be

* 'Z. Physik,' vol. 47, p. 1 (1928).
† 'Z. Physik,' vol. 52, p. 555 (1928).

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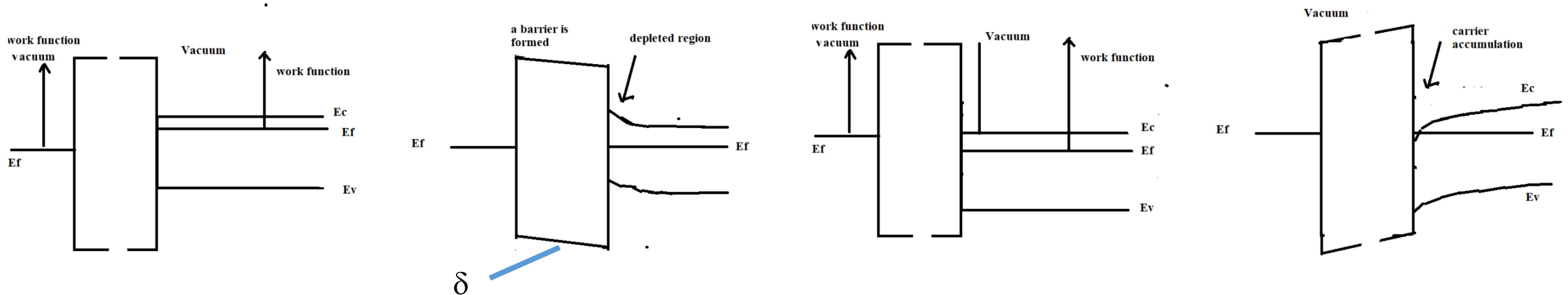
IC BASIC DEVICES : the rectifier and ohmic contacts

- First proposed by Schottky (field effect barrier lowering) : metal semiconductor contacts
- Photoemission for barrier characterization



- Interface is very important, a MIS is similar with the thickness of the middle region tending to 0
- The Schottky theory is only valid for clean interfaces (no intermediate layer, δ =0)
- Carriers can tunnel through the structure, at equilibrium the Fermi Energy are equal
- The best for a ohmic contact is to use a degenerate SC (highly doped) (Fermi level in the CB or VB)
- Schottky contacts are used on GaAs MESFETS but not on silicon (Smaller Gap)

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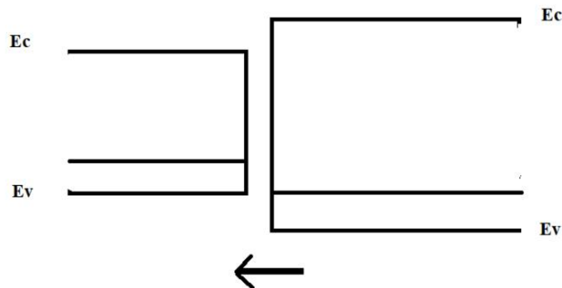
IC BASIC DEVICES : the junctions

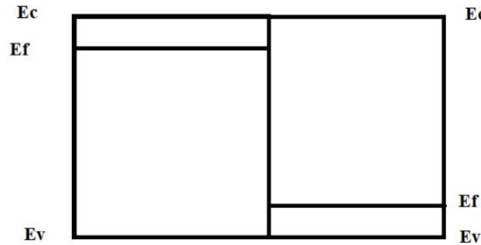
- **Heterojunction and Homojunction**



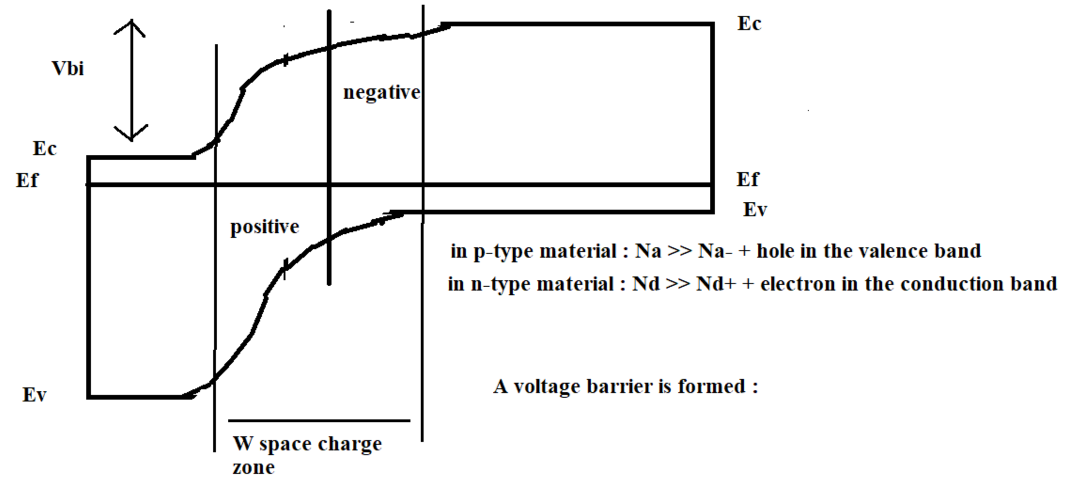
Heterojunction , metalurgical junction of different semiconductors

can be p p or np or nn juctions

Here a p-p junction



Homojunction, with same semiconductor



$$V_{b_i} = \frac{k_T}{q} ln\left(\frac{N_a N_d}{n_i^2}\right)$$

Eqf is the quasi fermi level

positive on the p side means a current flow in the junction : forward mode

$$J = -q\, p\mu_p \vec{\nabla} E_{F.p}$$

For an abrupt asymmetric p+n junction
Most of the current is due to diffusion

At reverse bias the space charge zone is given by:

$$W = \sqrt{\frac{2\varepsilon(V+Vb)}{q(Na-Nd)}}$$

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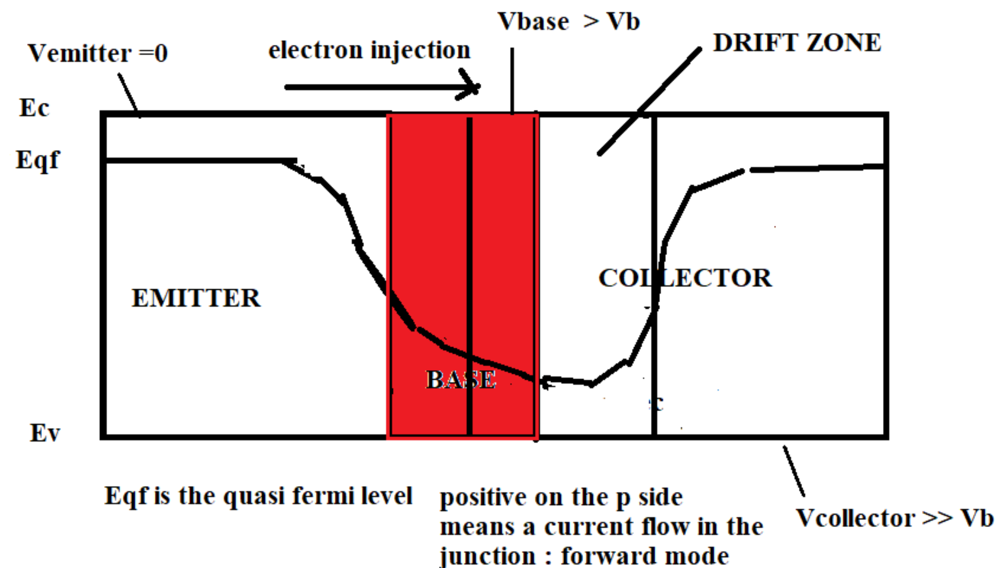
IC BASIC DEVICES : the bipolar transistor (transfer resistor)

- First IC made with bipolar devices , first amplifying semiconductor device
- Based on the junction properties three terminal device
- Homojunction or heterojunction (even proposed by W. Shockley)
- Doped emitter, thin base (opposite doping) , large collector, slightly doped to make a drift region



- In npn device . Base is p type biased positively
- Electron injection from the emitter >> hole injection from base
- As it is a diffusion process ,most electron do not recombine in the base region and reach the collector were they drift towards to the higher potential
- The base current is due to electrons that recombine with holes in the base and is proportional to:
- Base thickness, inverse of the lifetime

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OUTLINE

- Bases de la technologie des Circuits Intégrés

1. Dispositifs intégrés de base
2. Bases des procédés de fabrication

- Integrated Circuits Basic Technology

1. Operation of IC Basic Devices
2. IC Basic Processes

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OPERATION OF IC BASIC DEVICES : the bipolar transistor

- $\frac{n-n_0}{\tau_n}+\frac{\partial^2 n}{\partial x^2}D_n=0.0$ in the base region
- Ebers Moll model and Gummel model
- Transfert characteristics (base and collector current versus base voltage) and beta versus collector current and Output characteristics
- Linear (triode mode) and saturation mode :

Irradiation induced effects

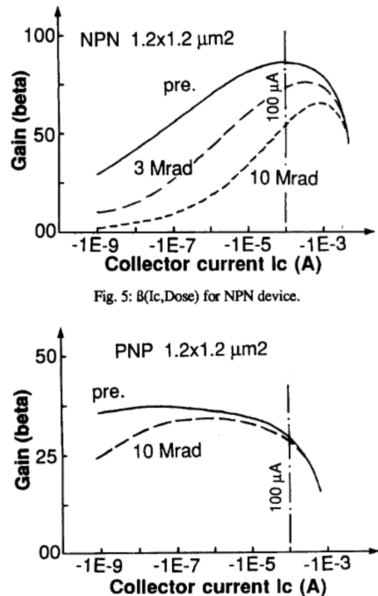
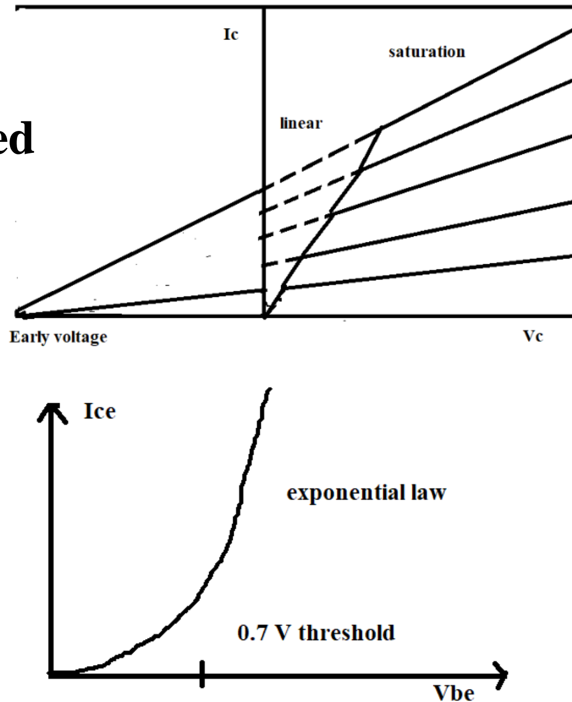


Fig. 5: ß(Ic,Dose) for NPN device.



$J_{bc}=qD_n\frac{\partial n}{\partial x}$ at the Base Collector junction , x= Wbc

$J_{eb}=qD_n\frac{\partial n}{\partial x}$ at the Emitter Base junction , x=Web=0

$\frac{n-n_0}{\tau_n}+\frac{\partial^2 n}{\partial x^2}D_n=0.0$ in the base region , $n-n_0=n_0\mathrm{e}\left(-\frac{x}{L_n}\right)$

with : $L_n=\sqrt{\tau_n D_n}$ then $\frac{\partial n}{\partial x}\cong -{}^{n}/{}_{L_n}$

$\mathrm{J}=\sqrt{\frac{D_n}{t_n}}q\,exp\left[-\frac{x}{L_n}\right]$ $\beta\approx\frac{L_n}{W_{cb}}$

Transfer bipolar characteristic , near ideality , does not depend on the doping level as for MOS

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OPERATION OF IC BASIC DEVICES : injection theory

- $qV = E_{F_n} - E_{F_p}$ these are the quasi fermi levels and V the applied potential, we can write , in the transition region :
- The Quasi fermi levels are defined by (from Fermi-Dirac to Boltzmann): $n = n_i\, exp\left(\frac{E_{F_n} - E_i}{kT}\right)$ $np = n_i^2 exp\left(\frac{qV}{kT}\right)$ p= $n_i\ exp\left(\frac{E_i - E_{F_p}}{kT}\right)$
- We consider the limit of transition zone in the p-type region of a n+p abrupt structure x=W , the injection curent is asymetric , more diffusion current from n+ to p than the opposite , charge in the p region = $-qN_A - n_p q + qp_p = Q_p$ with charge neutrality Q_p =0
- Poisson equation : $\frac{\partial E}{\partial x} = q(p_p - n_p - N_A)/\varepsilon$ when x > W , or x <0 outside the transition region $\frac{\partial E}{\partial x} = 0$ because $np = n_i^2$ we have got : x =W
- $n_p \approx \frac{n_i^2}{N_A}$ and $p_{p_0} \approx N_A$ x > W with this inside the transition region , which is close to x =0 $n_p \approx \frac{n_i^2}{p_p}\ exp\left(\frac{qV}{kT}\right)$in fact if we take $n_p = 10^{19} cm^{-3}$
- Continuity equations for electrons: $-U_n + \mu_n n_p \frac{\partial E}{\partial x} + \mu_n E \frac{\partial n_p}{\partial x} + D_n \frac{\partial^2 n_p}{\partial x^2}$ =0 and for holes : $-U_p - \mu_p p_p \frac{\partial E}{\partial x} - \mu_p E \frac{\partial p_p}{\partial x} + D_p \frac{\partial^2 p_p}{\partial x^2}$ =0
- Un/p are the recombination rates ,we have identical recombination rates for electrons and holes U and : $\frac{p_p - p_{po}}{\tau_p} = \frac{n_p - n_{po}}{\tau_n}$ =U for the excess carrier concentrations.
- Combining the two equations with the expression of p and n in the p-type region, in the p-type region n << p at x=W
- Because $p_p = p_{p0} exp\left(\frac{qV}{kT}\right)$ with $n_{p_0} = \frac{n_i^2}{p_p}$ for x= W on the p side. At the x=0.0 for the electrons $J_T \approx J_n$ and p << n we can say that the injection efficiency : J_n / J_T is close to one. If we combine the two continuity equations by multiplying by $\mu_n n_n$ and $\mu_p n_p$ respectively and summing we obtain a equation for which the second term with field derivative cancels and the equation reduces to three terms .We have :
- $n_p \frac{\partial p_p}{\partial x} + p_p \frac{\partial n_p}{\partial x}$ =0 if we consider that $\frac{\partial p_p}{\partial x} = -\frac{\partial n_p}{\partial x}$ this gives a second term , the equation reads : $-U\ (\mu_n n_p + \mu_p p_p\ ) + \mu_p \mu_n E\ (p_p - n_p) \frac{\partial n_p}{\partial x} + s_a \frac{\partial^2 n_p}{\partial x^2}$ =0 then :- $\frac{n_p - n_{po}}{\tau_n} + \frac{E\ (p_p - n_p)}{(p_p/\mu_n - n_p/\mu_p)} \frac{\partial n_p}{\partial x} + +D_n \frac{\partial^2 n_p}{\partial x^2}$=0

- $-\mu_n n_p E^2 \left(\frac{q}{kT}\right) = E\mu_n \frac{\partial n_p}{\partial x}$ and $D_n \frac{\partial^2 n^p}{\partial^2 x} = \mu_n n_p E^2 \left(\frac{q}{kT}\right) + \frac{q}{\varepsilon} \mu_n n_p$ numerrically the second is dominant so that we can neglect the field term

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OPERATION OF IC BASIC DEVICES : injection theory

- In the case of low injection we can make the hypothesis that : $E \approx 0$ the equation reduces to :- $\frac{n_p - n_{po}}{\tau_n} + +D_n \frac{\partial^2 n_p}{\partial x^2}$=0
- The general solution for this equation is : $n_p - n_{po} = \alpha_1 \exp\left(\frac{x}{L_n}\right) + \alpha_2 \exp\left(-\frac{x}{L_n}\right)$ where the α_1, α_2 should be determined with the boundary conditions. $L_n = \sqrt{D_n \cdot \tau_n}$ the injected current is determined by the electron concentration at x=0.0 and $np = n_i^2 exp\left(\frac{qV}{kT}\right)$ in this case at x=0.0 the electron concentration is given by : $n_p(0) = n_{p0} exp\left(\frac{qV}{kT}\right)$ where n_{p0} is the reference concentration in the p-type region.
- Henceforth we may rewrite: $n_p(0)\, p_p(0) = n_{p0} exp\left(\frac{qV}{kT}\right) n_i^2/n_{po} = n_i^2 exp\left(\frac{qV}{kT}\right)$ which gives the first condition :
- $\alpha_1 + \alpha_2 = n_{p0}\ (exp\left(\frac{qV}{kT}\right)$-1) and the second condition : $n_p - n_{po} = \alpha_1 \exp\left(\frac{W}{L_n}\right) + \alpha_2 \exp\left(-\frac{W}{L_n}\right) = 0.0$ for a diode , $n_p(W) = n_{p0}$
- For a bipolar transistor the equations are then : $n_p(0) = n_{p0} exp\left(\frac{qVbe}{kT}\right)$ and $n_p(W) = n_{p0} exp\left(\frac{qVbc}{kT}\right)$ there are two junctions !!!
- Let us consider the general solution, all calculations made : I= det (A) =2sh $\left(\frac{W}{L_n}\right)$ with $A = \left(\frac{exp\left(-\frac{W}{L_n}\right)}{1} \middle| \frac{exp\left(\frac{W}{L_n}\right)}{1}\right)$, we may write
- $A\begin{pmatrix}\alpha_1\\ \alpha_2\end{pmatrix} = \begin{bmatrix} n_p(W) - & n_{p_0} \\ n_p(0) - & n_{p_0} \end{bmatrix}$ we can solve and we obtain the values of the α_1, α_2

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OPERATION OF IC BASIC DEVICES : injection theory

- **For a diode we obtain** : $\alpha_2 = -\alpha_1 exp\left|-\frac{2w}{L_n}\right|$ hence we can determine the current density: $J_n = -qD_n(\alpha_1 - \alpha_2)/\, L_n$
- $\frac{\partial n_p}{\partial x} = \frac{\alpha_1 - \alpha_2}{L_n} = \frac{-\alpha_2}{L_n}$ which reduces to $-n_{\frac{p-\eta_p}{L_n}\cdot 0}$ for x=0 for a diode we consider that α_2 is the only term remaining
- Then : $\alpha_2 = n_{p0}\,(exp\left(\frac{qV}{kT}\right)$-1) $J_n = -D_n\, q\frac{\partial n_p}{\partial x}$ $J_t = n_{p0}D_n/\, L_n(exp\left(\frac{qV}{kT}\right)$-1) q
- Charge neutrality condition in the p type region: $n_{p0} - p_{p0} + N_a = 0.0$ as x=W we have got $n_{p_0} = \frac{n_i^2}{p_p}$ hence $n_{p_0} = \frac{n_i^2}{N_A}$
- $J_s = \frac{n_i^2}{N_A}\frac{D_n}{L_n}q$ and for a symetric junction we can can add the p injection with a other term.
- **For a bipolar transistor we have :** $n_p(0) = n_{p0}exp\left(\frac{qV_{be}}{kT}\right)$ and $n_p(0) = n_{p0}exp\left(\frac{qV_{bc}}{kT}\right)$
- $J_{en} = \coth(\frac{W}{L_n})n_{p0}D_n/\, L_n(exp\left(\frac{qV_{be}}{kT}\right)$-1) q and then $J_{cn} = \frac{1}{\mathrm{sh}(\frac{W}{L_n})}n_{p0}D_n/\, L_n(exp\left(\frac{qV_{be}}{kT}\right)$-1) q
- These are the emitter and collector currents : $\frac{J_{cn}}{J_{en}} = \frac{1}{\mathrm{ch}(\frac{W}{L_n})} \approx 1 - \frac{W^2}{2L_n^2}$ $J_B = J_E - J_C$ and $\beta = \frac{2L_n^2}{W^2}$

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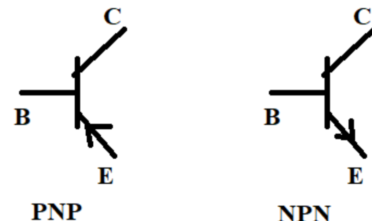
OPERATION OF IC BASIC DEVICES : injection theory, consequences

- Commenting the different results : The current gain reduces when the diffusion length reduces, this means that the carrier lifetime must not be reduced or the base length must be reduced.
- The lifetime is extrinsically dependent on the defect and deep impurities (Shockley-Hall-Read) , Auger and direct recombination(photon emission) contribute but and high injection and for direct band-gap semiconductors
- There may be some surface recombination that contribute to kill lifetime
- Radiation effects can reduce lifetime (surface and bulk) : surface (interface Si/SiO2, ionizing irradiation) and bulk (basically NIEL, Non Ionizing Energy Loss), such as neutrons and hadrons, heavy ions)
- Semiconductor empirical law : $\frac{1}{\tau} = \frac{1}{\tau_0} + K\boldsymbol{\Phi}$ where K is determined empirically and $\boldsymbol{\Phi}$ is a neutron fluence
- No need to get into microscopic details , simplified defect model can be taken , but K must be determined by measurements
- The neutron fluence corresponds to the equivalent neutron integrated flux of a 1 MeV neutrons (for the same 'damage')
- The surface of silicon can be the source of leakage currents and then to increase the Collector Emitter current independent of the base emitter voltage
- Electric symbol of a bipolar :



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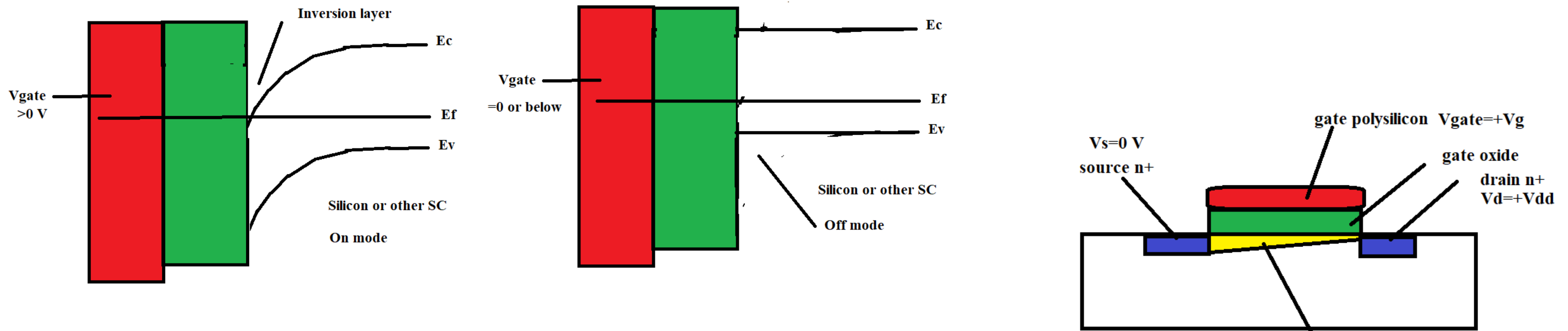
OPERATION OF IC BASIC DEVICES : MOS structures



- The Poisson equation holds for the metal, dielectric and semiconductor
- In the metal y= -tox , we have : $\frac{\partial E}{\partial y} = 0$ and hence $V(x) = V_A + V_s$ for x< 0 , tox is the dielectric thickness and
- No charge is supposed to be present in the oxide $-\frac{\partial^2 V}{\partial y^2} = 0$
- When no bias is applied the surface potential at the SIO2/Si interface depends on the surface states and the work functions;
- $V_s = f\ (W_{Fg}, W_{Fox}, W_{Fsc})$ let's calculate the equilibrium carrier densities at the interface , no current flow along x :
- $n_{Si}(y) = n_0\ exp\left(\frac{qV}{kT}\right)$ and $p_{Si}(y) = p_0\ exp\left(\frac{-qV}{kT}\right)$ Quasi Fermi Levels are constant and can be considered equal
- At $x = \infty\ p_{Si} = N_A$ neutrality conditions, and then $n_{Si}(\infty) = n_i^2\ /N_A$ we can also write when a voltage is applied :
- $n_{Si}(0) = n_0\ exp\left(\frac{qV}{kT}\right)$ where $V_a + V_s \ = V$ the hole concentration is much lower, this is called the field effect
- The electron and hole concentrations near the interface can be controlled by the gate(metal or polysilicon).
- On mode $n_{Si}(0) >> p_{Si}(0)$ in p-type material n-channel MOSFET , tis is called inversion (weak and strong)
- Off mode $n_{Si}(0) >> p_{Si}(0) \approx Na$ background doping.
- If we adjunct two electrodes beside the channel , we obtain a MOS transistor as described above :
- The source can inject electrons in the channel to the drain. The device is four terminal because the bulk (p-type) is grounded

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OPERATION OF IC BASIC DEVICES : MOS structures

- **Calculation of the current in the inversion layer :** Let x be the coordinate in the vertical dircetion and y the coordinate along the channel from source to drain, n (x,y) is the electron density at the interface (inversion layer) , the mobile charge Q is given by : $x_x Q_n = q\int_0^{x_n} n(x,y)\,dx$, where we define xn by the point at which the Quasi Fermi Level for electrons crosses the Intrinsic level. The value of the resitivity w.r.t the the coordinate y is then : $\rho_n(y) = \frac{x_n}{\mu_n Q_n(y)}$, the value of the differential resistance dR(y) is then , taken into account the area :
- $S = Zx_n$ this is : $\mathrm{dR} = \frac{dx}{\mu_n W Q_n(y)}$ subsequently the incremental and differential voltage is : $dV = I_D\, dR$
- The channel current is normally constant through the channel so we can integrate the previous equation along the voltage from source to drain :
- $V_D - V_S = \frac{I_D}{\mu_n Z}\int_0^L \frac{dy}{Q_n(y)}$ now we have to determine the value of the integral by solving Poisson equation in the structure.
- First the solution , in the silicon depletion layer with not considering the inversion layer that does contribute greatly to the space charge zone is then :
- $\mathrm{W} = \sqrt{\frac{2\varepsilon V_s}{qN_a}}$ W is the extension of the depletion layer verticaly below the point at the interface potential V_s (y) then the bulk charge reads
- $Q_B(y) = -\sqrt{2\varepsilon q V_s N_A}$ now we have to determine the interface potential !!!

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OPERATION OF IC BASIC DEVICES : MOS structures

- We shall assume flat band conditions the CB and VB are flat and no space charge zone exists
- First no charge is considered in the oxide (thickness=tox) or at the interface : Nox=0 and Nss=0
- From the gate electrode (metal or polysilicon), the structure is that of a capacitor:
- We can write : $C_{ox} = {}^{\varepsilon_{ox}}/_{t_{ox}}$ the oxide thickness is t_{ox} and this is the expression of the capacitance per unit area.
- The charge on the capacitor is equal to the inversion layer charge + the depletion charge
- It is the image charge on the gate electrode.
- So : $Q_C = Q_n + Q_B$ this being true for each point along y.
- We can write : $Q_n(y) = C_{0x}V_c(y) - \sqrt{2\varepsilon q V_s(y) N_A}$ this is true at each y along the channel
- What are V_c and V_s ???

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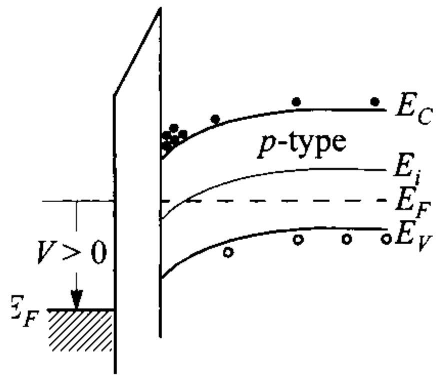
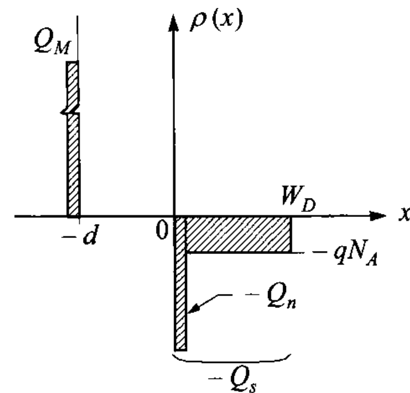
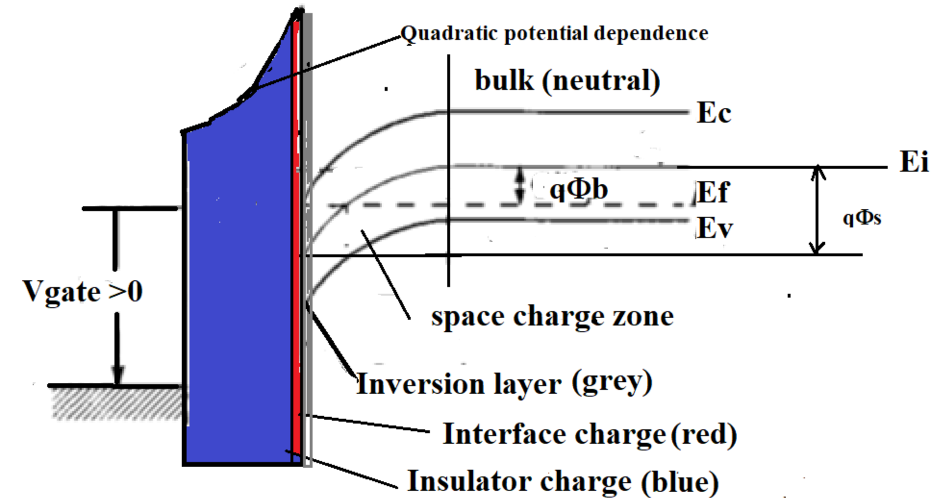
OPERATION OF IC BASIC DEVICES : MOS structures







Out of Sze et al., above figures

Structure with charged zones

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OPERATION OF IC BASIC DEVICES : MOS structures

We define : $qV_B = E_i - E_F$ and an extension of the depletion W given by the interface potential: $V_s(y)$

The interface potential is given by : $V_s(y) = \varphi(y) + V_B$

The potential across the oxide capacitor is given in high inversion by :

$$V_c(y) = V_{gate} - V_s(y)$$

Hence the inversion charge is given by :

$$Q_n(y) = C_{0x}(V_{gate} - \varphi(y) + V_B) - \sqrt{2\varepsilon q(\varphi(y) + V_B)N_A}$$

If we take into consideration that the flat band conditions are satisfied with a certain voltage on the gate and that there is a charge in the oxide, then we introduce a term $V_T(N_{ox})$ in the first term of the second member.

$$Q_n(y) = C_{0x}(V_{gate} - V_T\,(N_{ox}) - \varphi(y) + V_B) - \sqrt{2\varepsilon q(\varphi(y) + V_B)N_A}$$

- The drain current is given by :$I_D = \frac{dV}{dR}$
- With the definition of 1/dR we have : $d\varphi Z\mu_n Q_n(y) = I_D \mathrm{dy}$
- We can integrate it and average it, the first term is : $I_D = \mu_n \frac{Z}{L} C_{0x} V_D\left(V_g - V_T - V_D\ /2\right)$
- Which hold when : $V_D \leq V_g - V_T$

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OPERATION OF IC BASIC DEVICES : MOS structures

- When $V_D > V_g - V_T$ the second term corrects the first one this means that the density of electrons does not increase and is set to zero at the drain voltage hence we can write :
- $Q_n(L) = C_{0x}(V_{gate} - V_T\,(N_{ox}) - \varphi(L) + V_B) - \sqrt{2\varepsilon q(\varphi(L) + V_B)N_A} = 0$
- In other terms : $Q_n(y) = C_{0x}(V_{gate} - V_T\,(N_{ox}) - V_{DSAT} + V_B) - \sqrt{2\varepsilon q(V_{DSAT} + V_B)N_A} = 0$
- We find approximately : $V_{DSAT} = V_{gate} - V_{th}(N_{ox}) + V_B/2$
- The approximate expression of the drain current in saturation is then: $I_D = \mu_n \frac{Z}{2L} C_{0x}\left(V_g - V_T\right)^2$
- This is valid for long channel devices, in nanoscale devices , with constant mobility , for short channel devices velocity saturation can occur or ballistic transport be important
- We see that the threshold voltage depends on the charge in the oxide, we set a positive charge density of N_{ox} the threshold voltage shift is then : $\Delta V_{ox} = \frac{qN_{ox}}{2} t_{ox}^2$

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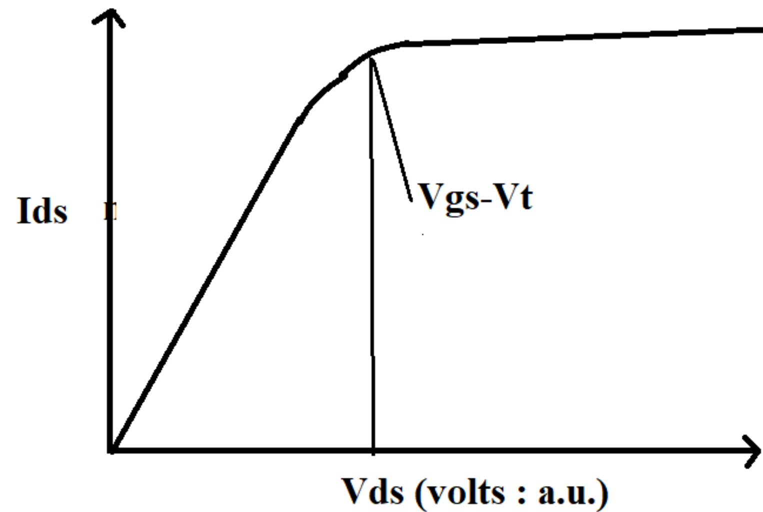
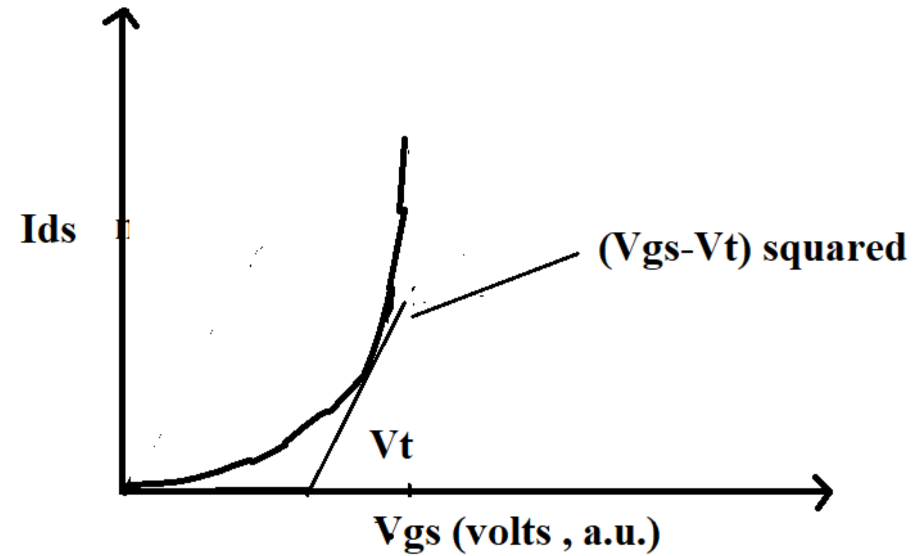
OPERATION OF IC BASIC DEVICES : MOS structures



Output charactersitics



Transfer characterstics

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OPERATION OF IC BASIC DEVICES : SUMMARY

- We understand now the basic theory of the two important devices
- We are able to see where most of their weaknesses are located
- For the bipolar : the gate length and the minority carrier lifetime
- For the MOS the gate oxide and its charge
- Other effects such as leakage and surface current remain to be studied

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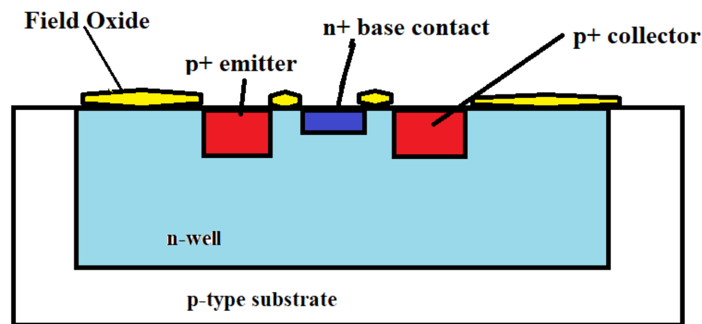
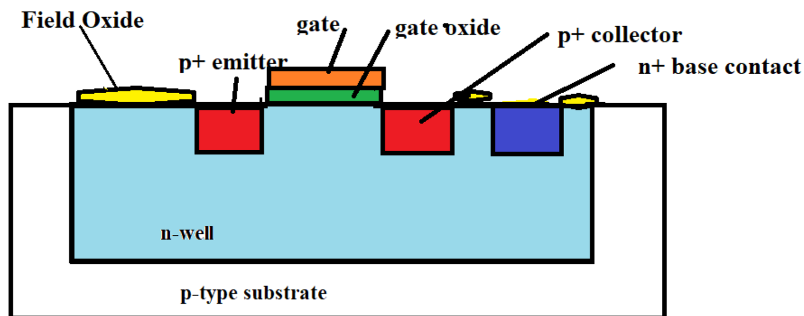
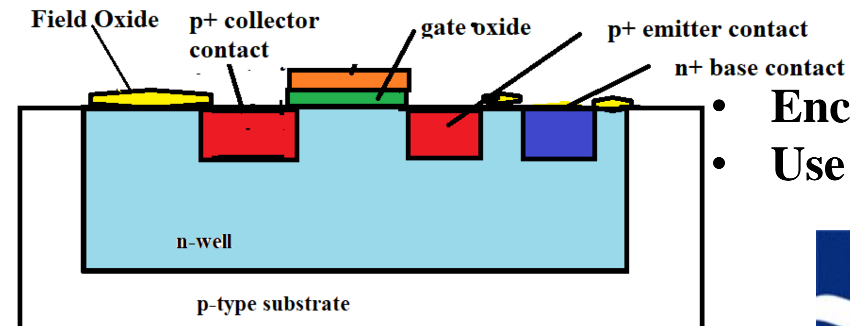
IC BASIC PROCESSES : pn junction and transistors

- Integrated Bipolar : lateral structures



- The lateral transistor is a parasitic structure of the CMOS technology
- pnp only in p-substrates use a p-channel MOS with no gate oxide
- The p-substrate can be a parasitic collector
- Field oxides can charge and induce leakage currents
- Collector does not enclose the base : low gain current defocusing
- and spreading
- Thick base at least for standard technologies





- Enclosed geometry
- Use the gate to control leakage

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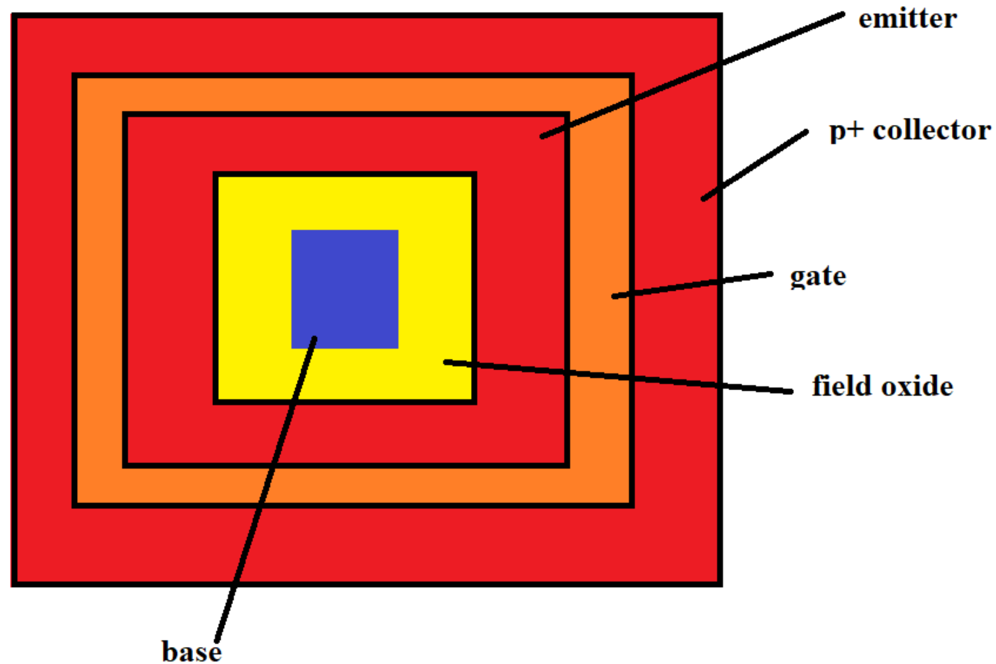
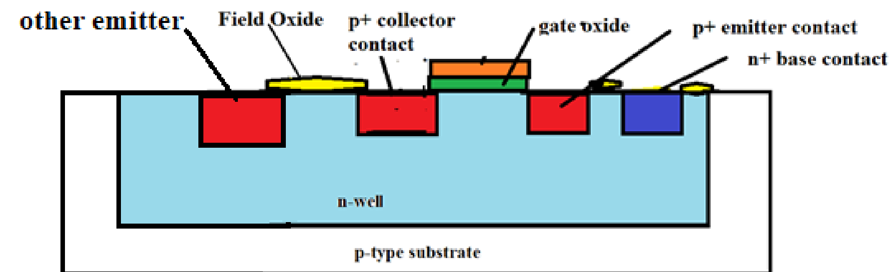
IC BASIC PROCESSES : pn junctions and transistors

- Enclosed structure : lateral structure, planar



- The gate voltage can reduce the parasitic channel from emitter to collector
- The emitter base can be low because of the presence of the junction
- Beware of other parasitic devices, this is a p-channel enclosed MOS transistor !!!
- This is very sensitive to neutrons however



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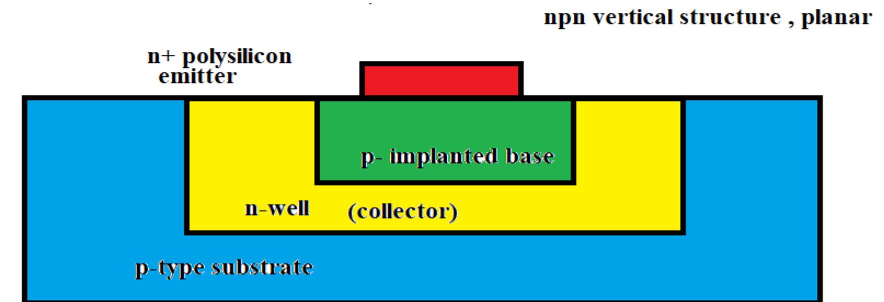
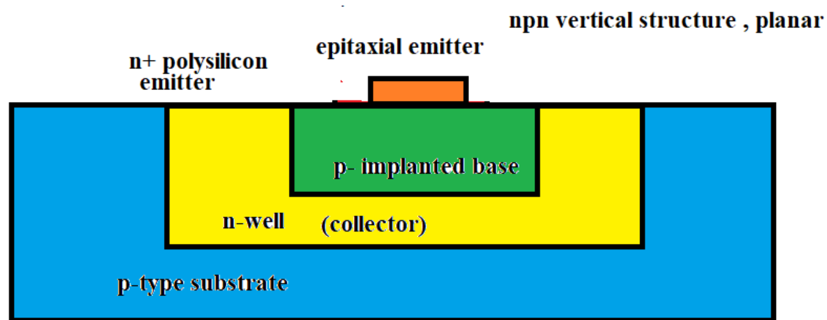
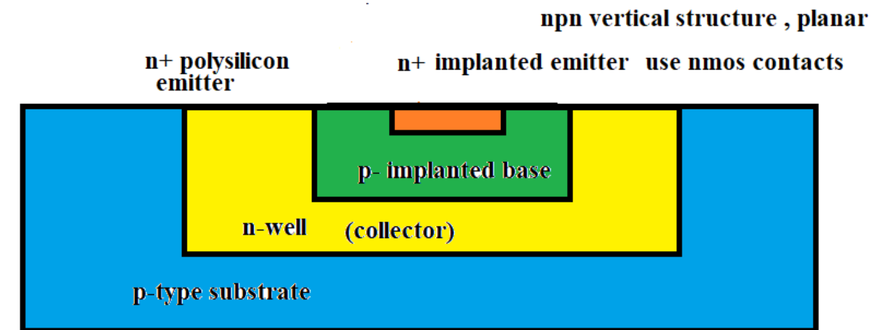
IC BASIC PROCESSES : pn junctions and transistors

- Integrated Bipolar : vertical structures
- Structures obtained by design
- Use a n-well and a p-implant
- Other architecture using implants or epi-layers







- Use p lightly doped substrate , needs a p-well and an n-well step
- Polysilicon emitters are often used
- Parasitic pnp transistor

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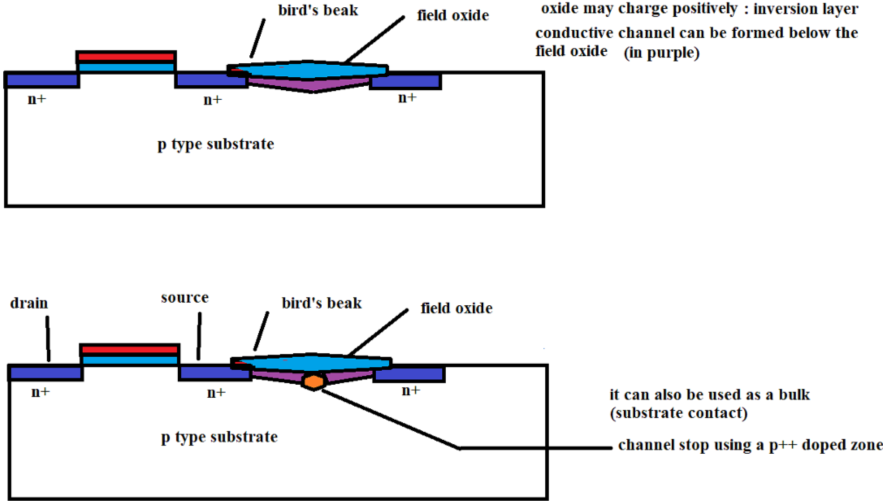
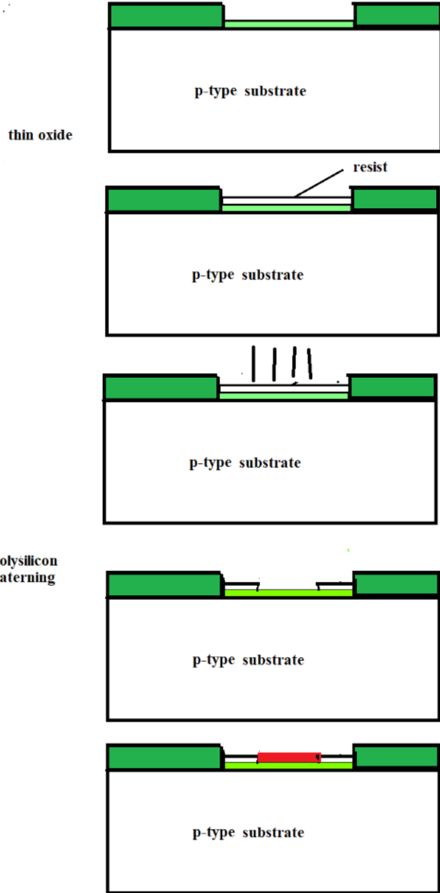
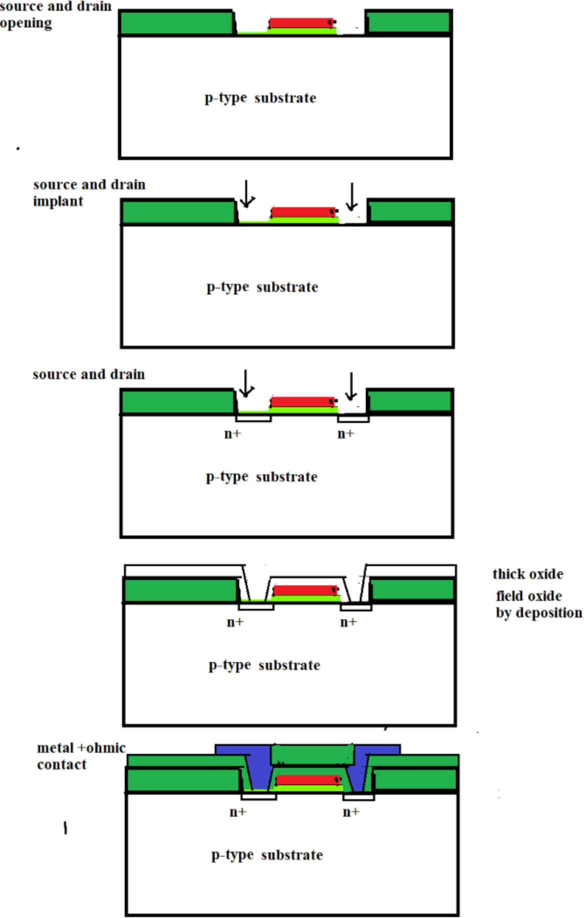
IC BASIC PROCESSES : self aligned MOS structures

- Monolithic integration : diffused, implanted, epitaxial, mesa
- Initial substrates : mainly p-type sometimes n-type
- Standard CMOS usually p-type (easier to control)
- Notice the field oxide is present everywhere between the devices







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IC BASIC PROCESSES : then, now and the near future

- **Monolithic integration : diffused, implanted, epitaxial, mesa**
- **Initial substrates : mainly p-type sometimes n-type**
- **Standard CMOS usually p-type (easier to control)**
- **Down to the nm scale**
- **Other new MOS structures design for nanoscale integration:**
- **FDSOI: Fully Depleted Silicon On Insulator**
- **GAA: Gate All Around**
- **FinFet (Use Fins)**
- **Two great families : BULK (Silicon substrate) and SOI (Silicon On Insulator)**
- **Recent technologies : Use of SiGe to strain the Silicon channel tensively improve carrier mobility**
- **BiCMOS with Heterojunction Field Effect bipolar transistor (High Injection Efficiency)**

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IC BASIC PROCESSES : process simulation

- Strong need to model the different process steps
- Numerical methods instead of analytical specific models
- Need to develop a process including all process steps to have the cumulative effects , such as thermal treatments for all the devices.
- Every effect should be taken into consideration, in a finite element framework , for many different starting materials (silicon , IIIV etc..)
- For silicon and GaAs: SUPREM is the starting program , but vendors have more performing codes (Stanford University Process Modelling program)
- These codes are referred to as TCAD (Technological Computing Aided Design)
- Diffusion of impurities, defects, ion implantation , oxidization are usually included

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IC BASIC PROCESSES : device simulation

- There is a need for device simulation :
  - To make and effective process offering devices with adequate characteristics
  - To study side-effects in device operation
  - To evaluate new or improved devices without the need to fabricate a prototype
  - To shorten device development timescale
- PISCES one of the first silicon device simulator : PISCES II: Poisson and continuity equation solver MR Pinto, CS Rafferty, RW Dutton - 1984
  - The MOS transistor , and bipolar silicon (1D simulation for a bipolar, Gummel early 1960)
  - 1 D and 2 D simulation , 3D is now available from vendors
  - Note that 3D needs very advanced hardware, typical for a new type of photodetector 48 hours simulation with an 8 processor workstation
  - https://books.google.fr/books?id=PlX0BwAAQBAJ&pg=PA8&lpg=PA8&dq=pisces+device+simulation+program&source=bl&ots=YYKLtvZ8Dn&sig=VVHf8sNTZbCB1VyedeARJ2FXCc8&hl=fr&sa=X&ved=2ahUKEwjJr57ejIzfAhWqxYUKHfMtAbUQ6AEwDHoECAgQAQ#v=onepage&q=pisces%20device%20simulation%20program&f=false
- Vendors have developed power device simulation (quantum, photo,many materials, engineered bandgap, deep defects, interfaces, charged insulators)

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IC BASIC PROCESSES : SUMMARY

- We know how the mainstream processes work and the weak points concerning effect of radiation
- We have focused on standard CMOS
- Leakage current at the interface (silicon/oxide) are the main source of malfunction (at Total Ionizing Dose)
- Change of oxide (chemical) is on its way

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IC : IRRADIATION EFFECTS

- IRRADIATION : Single Event (one particle) and cumulative effects
- Cumulative effects : Total Ionizing Dose
- Cumulative effects : Non Ionizing Energy Loss , Some of this in crystalline defects
- Dose in Grays(Gy)= One Joule per Kg
- Defects (NIEL) : 1 MeV equivalent neutron for the damage (n/cm2)
- Other effects such as neutron capture at boron :
- n + 10B >>> 7Li+alpha(He) eliminate boron in protective coatings

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OUTLINE

- Bases de la conception de circuits intégrés CMOS

1. Circuits de base : logique et analogiques
2. Méthodes de base: simulation, dessin des masques par mise a plat etc. ..

- Integrated Circuits Basic Design MOS

1. IC Basic circuits : digital and analog
2. IC Basic methods: simulation, layout

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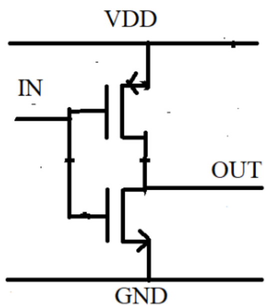
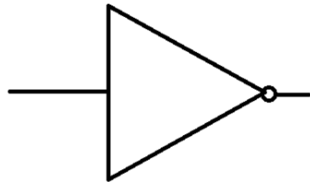
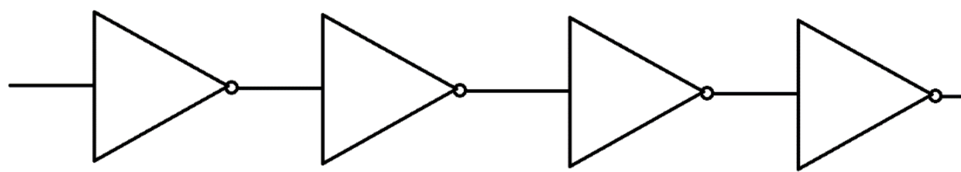
IC Basic circuits : digital

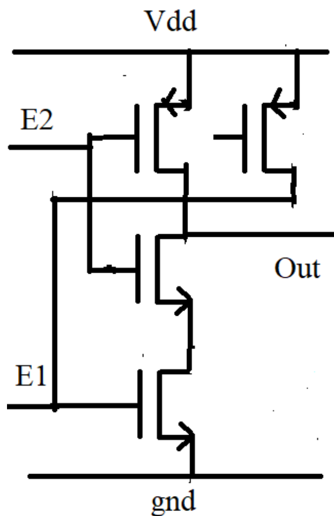
- The CMOS inverter and NAND gate, the buffer/driver

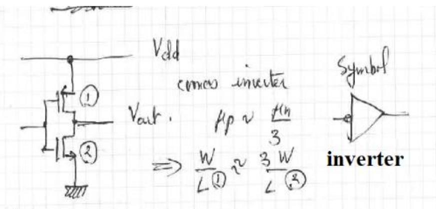


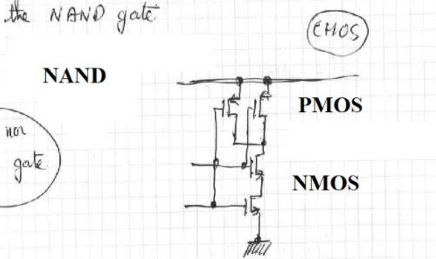


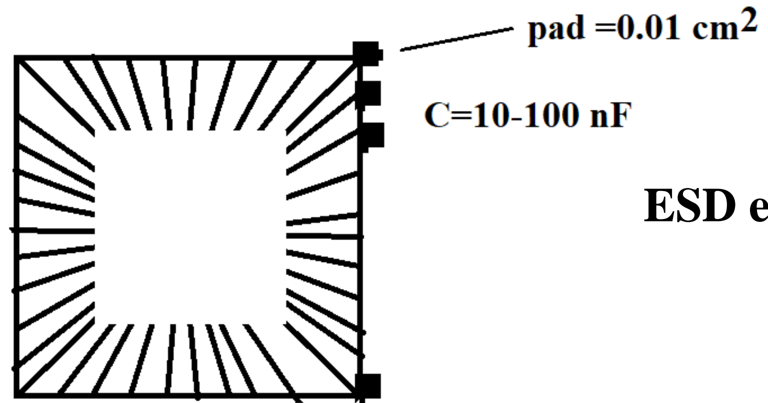


- W/L <<< W/L <<< W/L
- Aspect ratio has progressing values to drive output Pads
- + protecting diodes









pad =0.01 cm2

C=10-100 nF

The transmission gate : for synchronous logic

ESD electrostatic discharge, use of diodes

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IC Basic circuits : digital

$$i = C_L \frac{dV}{dt}$$

$$\frac{dV}{dt} = V_{DD} f_t$$

$$I_{max} = C_L \frac{V_{DD}}{\tau_D}$$

$$I_{max} \approx \frac{W}{L}$$

$$P = i \frac{V_{DD}}{2} C_L$$

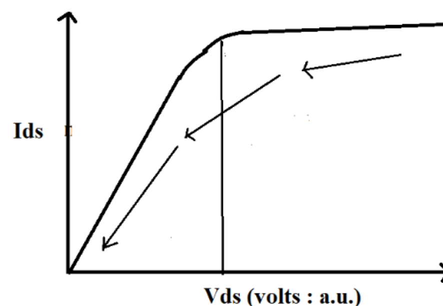
$$P = C_L \frac{V_{DD}^2}{2} f_t$$

$$C_L \sim WL$$

$$\tau_D \sim L^2 V_{DD}$$

f_t= is the frequency of operation of the gate

- The capacitive load and stray should be limited to avoid power dissipation
- The frequency is limited by the power dissipation



The propagation delay reduces as the feature size reduces and the supply voltage reduces.
To have a accurate calculation of the delay then
Id=f(Vg,Vd) characteristic and then the dynamic operation point is determined
Both in saturation and linear .

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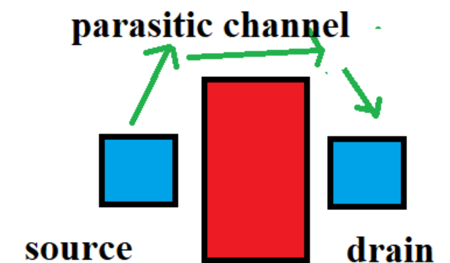
IC Basic circuits : digital

- The leakage current problem : ionizing irradiation
- Figure needed : source to drain current due to positive charges in the oxide
- Parasitic MOS n-channel structures for the nMOS



- If the gate oxide is thin no real problem Vth does not vary considerably
- The elementary gate leaks with excess power consumption

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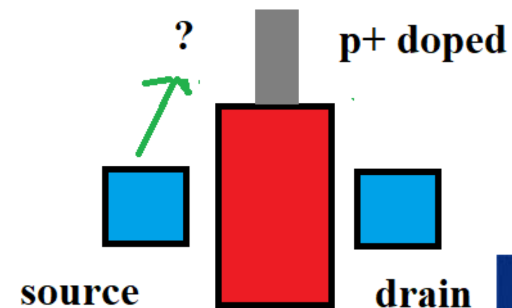
IC Basic circuits : digital

- How to reduce this :
- Closed shape transistors : but a lot of area is needed
- Introduce a highly doped n+ layer below the field oxide (whether STI shallow trench insulation or else) This is a spray when in a large area or a channel stop p+ in a limited area)
- In the past guard rings were used too.
-



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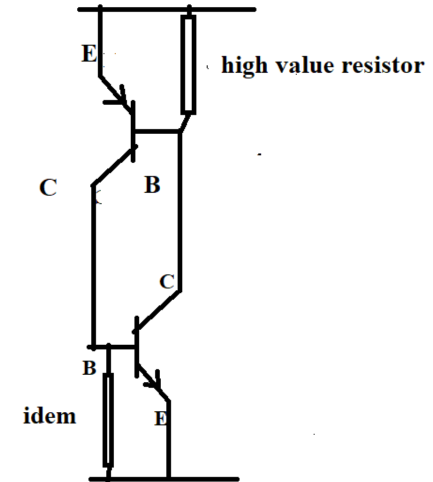
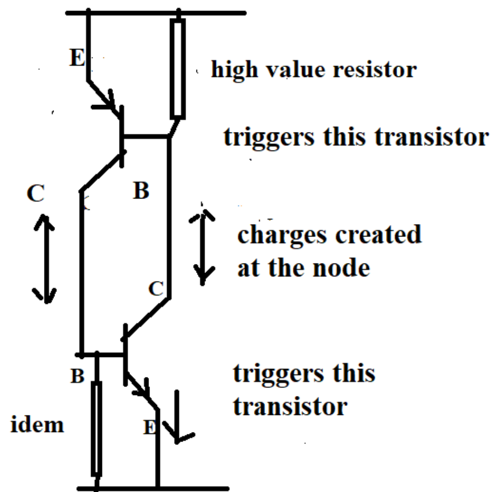
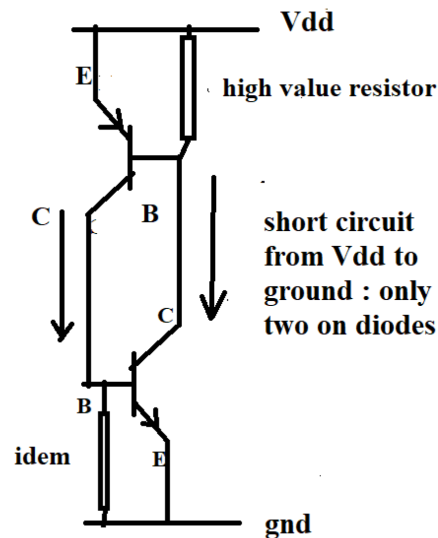
IC Basic circuits : digital

- The latchup problem :
- What is latchup : two c-bipolar, thyristor like (SCR)
- Simple inverter see the parasitic bipolar
- Figure of the two bipolars, parasitic
- Off (figure) and On (figure)







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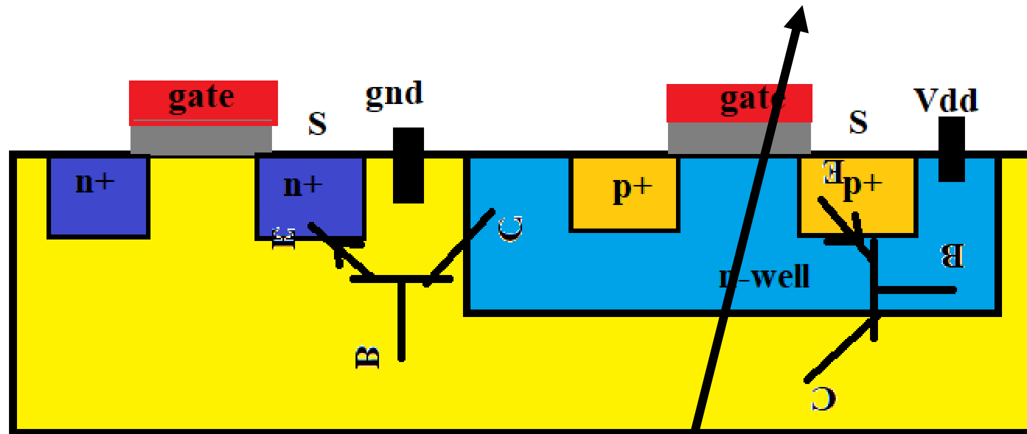
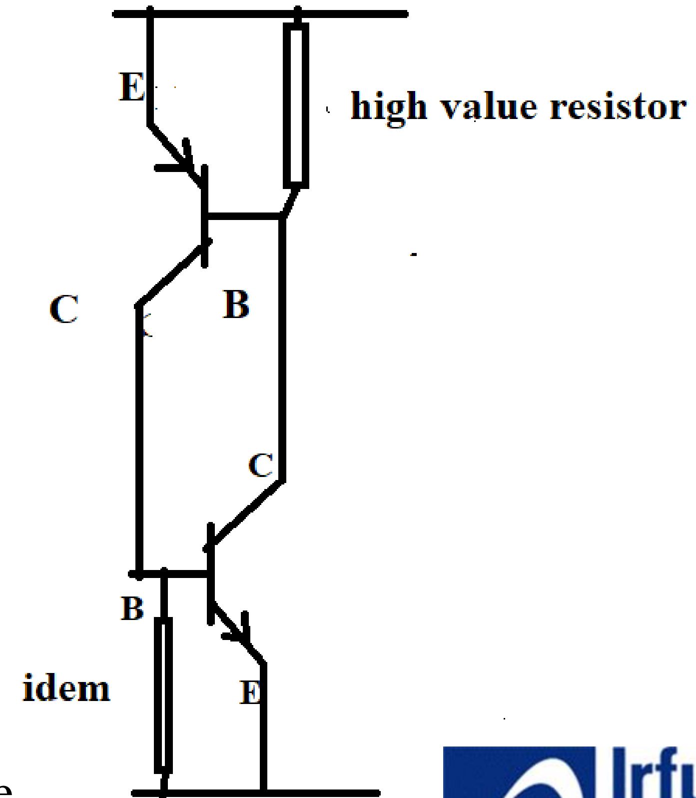
IC Basic circuits : digital





if n-well or the substrate is resistive

S is the source of the two transistors

Charges are generated by the traversing particle
Electron and holes are separated by the electric field

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IC Basic circuits : digital

- How to reduce this ?
- Adequate structures should be better (usually charge generation is proportional to length , LET = linear energy transfer) through spacing rules
- Guard ring to control potential, and direct charges to ground and voltage supply well connected to p and n wells.
- Reduce resistance between parasitic bipolars (the voltage drop will reduce) by adequately doped substrates
- Analyse all the circuit for parasitics npnp structures
- SEE will not be totally eliminated but destructive latch up yes
- Silicon On Insulator is the solution (no parasitic structure, no inter device leakage)

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IC Basic circuits : digital

- New devices for the nanometer scale : More Than Moore
- FinFet : Depleted Lean-channel TrAnsistor or DELTA transistor
- Very low operation voltage < 1 V Vdd , very low gate delay < ps
- FDSOI is the alternative
- Non planar technology, no leakage other than the channel leakage vertical structure
- Many gate structure useful for logic gates (NAND)
- Metal interconnect : copper with a diffusion barrier
- GAA (Gate All Around device) with III-V materials GaInAs

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IC Basic circuits : digital

- Digital functions do not need to have a model down to the MOS transistor
- Simulations can be made with a cell model (gate/ flip-flop etc…)
- Layout can be automatized with a cell library (parametrized)
- High level simulation tools can be used : VHDL, VERiLOG
- Simulation at transistor level , tedious and limited to small mixel-signal circuits

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IC Basic circuits : analog

- Specific circuits in IC design: limit to the MOS
- Neighbouring transistors operate at the same temperature (one circuit)
- Neighbouring transistors have very similar geometry
- Analog processes do not have precise high value resistances
- Capacitor OK , but inductances only in RF oriented technology
- Specific circuits : switches (the Transmission Gates), the problem of charge injection on the analog signal
- Current Mirror not possible with discrete circuits
- Differential amplifier with low offset

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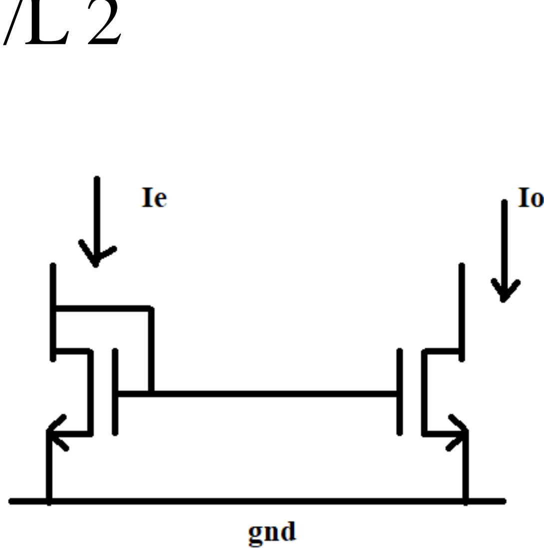
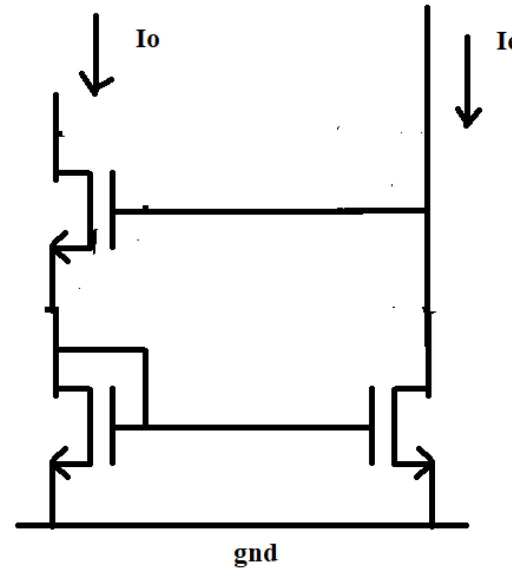
IC Basic circuits : analog

- The basic current mirror , with Wilson and cascoded versions
- Figure :
- To enhance similarity use of the interdigited device
- W/L 1 =W/L 2





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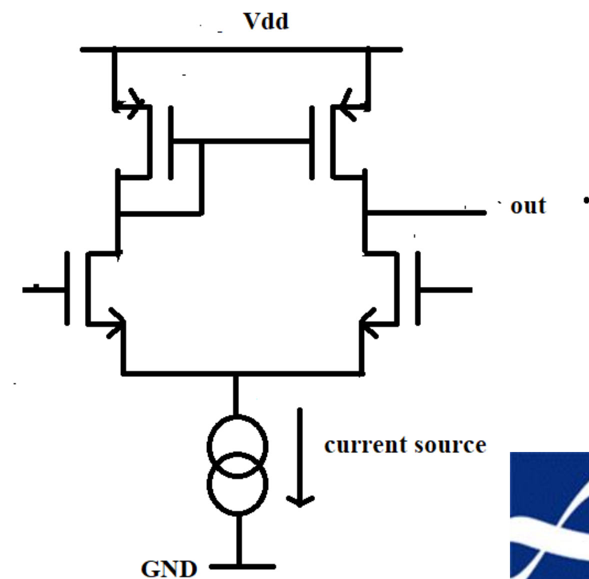
IC Basic circuits : analog

- A basic one side design:
- A p-mos upper current mirror with same aspect ratio (load resistor)
- A differential a pair interdigited
- A bias current source



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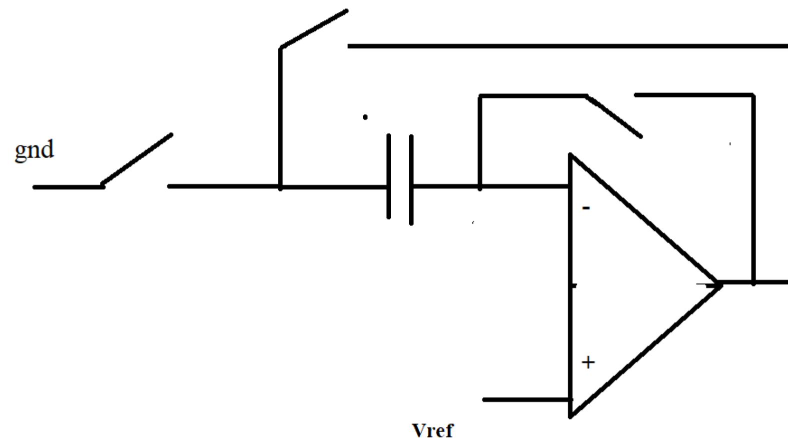
IC Basic circuits : analog

- Use of capacitor and amps to make signal processing
- Switch capacitor circuits
- Examples : offset compensation for comparators



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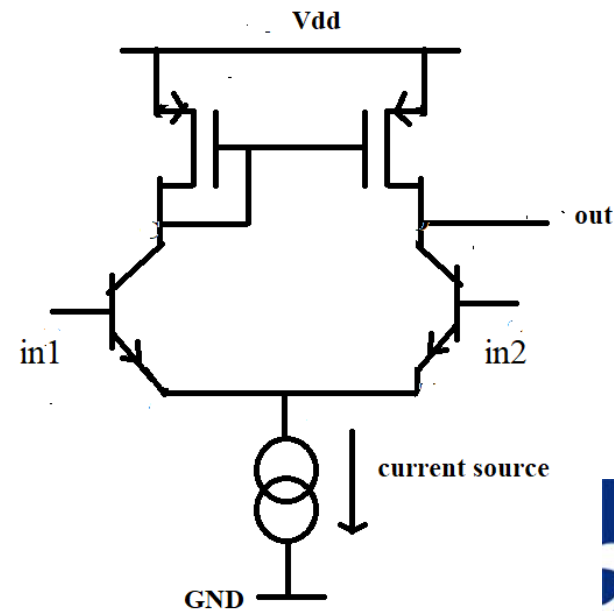
IC Basic circuits : analog

- Use of npn bipolars for low offset differential pairs
- Higher transconductance for same quiescent current bias
- High speed (reduced capacitances



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IC Basic circuits : analog

- Noise : as in discrete circuits but can be simulated
- Low frequency Flicker Noise (flicker: low variations with time), basically depend on the defects in the material
- $v_n^2/df = A_f/f^{\alpha}$ $\alpha \approx 1$ when f > 0 the prefactor is device dependent
- Johnson or thermal noise, related to the conductance or the transconductance : $v_n^2 = 4kT\frac{\Delta f}{g}$
- Schottky noise or shot noise related to the current I trough the device (needs a potential drop in devices such as diodes or contacts)
- $i_n^2 = 2qI\Delta f$
- Leakage current can cause noise (interface current , due to excess interface states, charging and recharging)
- Extended defects induce Flicker noise (Lorentzian PSD, power spectral density)

IC Basic methods: simulation, layout

- High number of devices : intractable analytic calculations
- First software in the 1970’s : SPICE (Specific Program for Integrated Circuit Emulation)
- For transistor level simulation : DC (operating point) , AC (harmonic simulation), and transient.
- These codes were improved and some were written. Good for analog medium number of devices simulations
- Node and branches with capacitors and analytic model for n-channel MOS devices
- Use of a custom drawn schematic to simulate the circuit

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IC Basic methods: simulation, layout

- Layout : It's just drawing , respecting design rules
- All the layers needed for the detector technology are available
- You can draw devices and circuits according to your need
- DRC is run : design rule checker if errors then corrections
- ERC is sometimes needed (Electric Rule Checker), (branch with no node…)
- Then run the extract code to obtain a schematic from the layout usually with the capacitance and the resistances extracted from the layout
- Compare with initial schematic
- If OK then may run the schematic with the parasitics if not OK change the layout accordingly

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SUMMARY AND HARDENING ISSUES

- Hardening by design was introduced here. Be careful of conductive channels, parasitic bipolars and thick bipolar bases.
- ESD is a problem, needs to be careful with metallization
- Modern technology : trend to use SOI which is the path towards hardening by process, thin insulators (different from SiO_2, use of Al_2O_3, which behaves differently no positive charge)and HfO_2 for the gate insulator high strength
- Use of spray and channel stop because of Extreme Ultra Violet processing, very ionizing (comparable to soft X rays)
- Ultrathin gate insulator : no threshold voltage shift
- HBT : higher injection efficiency then improved performance at low carrier lifetime.

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SUMMARY AND HARDENING ISSUES

- Material and their characteristic with respect to ionizing irradiation

Material	Si	Ge	CdTe	GaAs	SiC β	(diamond) C
Density in gcm^{-3}	2.33	5.33	5.85	5.32	3.21	3.5
Bandgap	1.1 eV	0.67 eV	1.44 eV (dir)	1.4 eV (dir)	2.3 eV	5.47 eV
Breakdown field (MV/cm)	0.3	0.1	0.4	0.4	2	20
ε or Eth	3.6 eV	2.98 eV	~4.5 eV	~4.5 eV	8.8 eV	12 eV

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SUMMARY AND HARDENING ISSUES

- Some figures and graphs with hardened IC processes and circuits
- Neutrons (hadrons) cascades of atomic displacements , leading to extended defects at room temperature, and point defects (NIEL: Non Ionizing Energy Loss)
- Ionizing effects: photons and Compton electrons, leading to positively charging oxygen vacancies in silicon dioxide E' paramagnetic centres (TID :Total Ionizing dose) effects are different in HfO2 dielectrics and with thin dielectrics
- Oxygen vacancies may become negative in HfO2
- There are still interface states : Pb (amphoteric)

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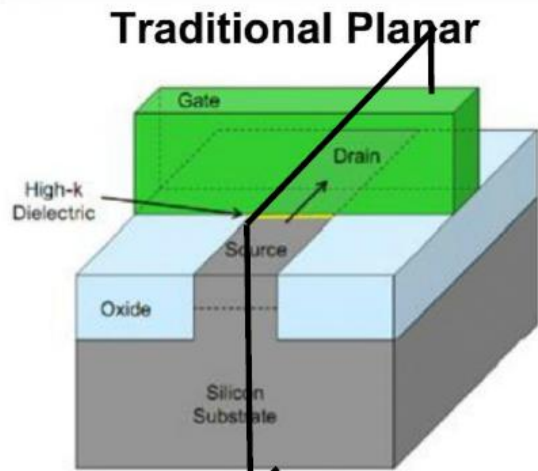
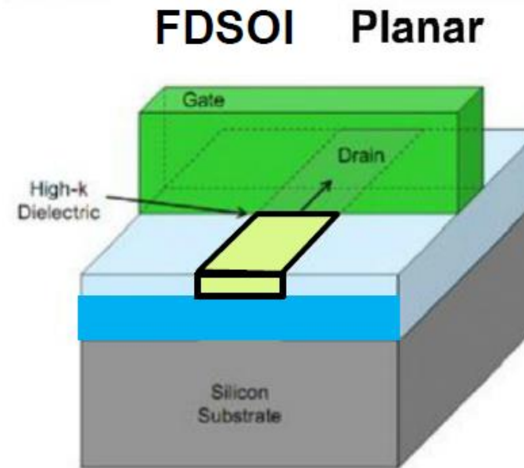
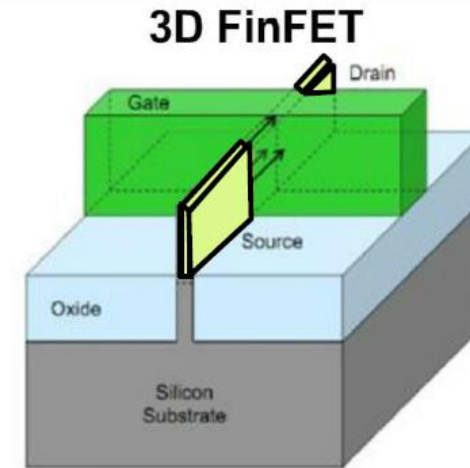
IC Basic circuits : digital

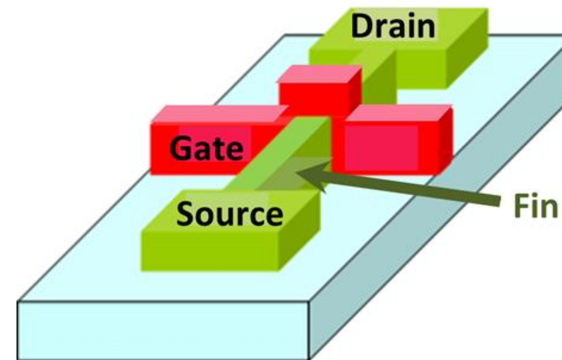
Evolution : 10 nm node





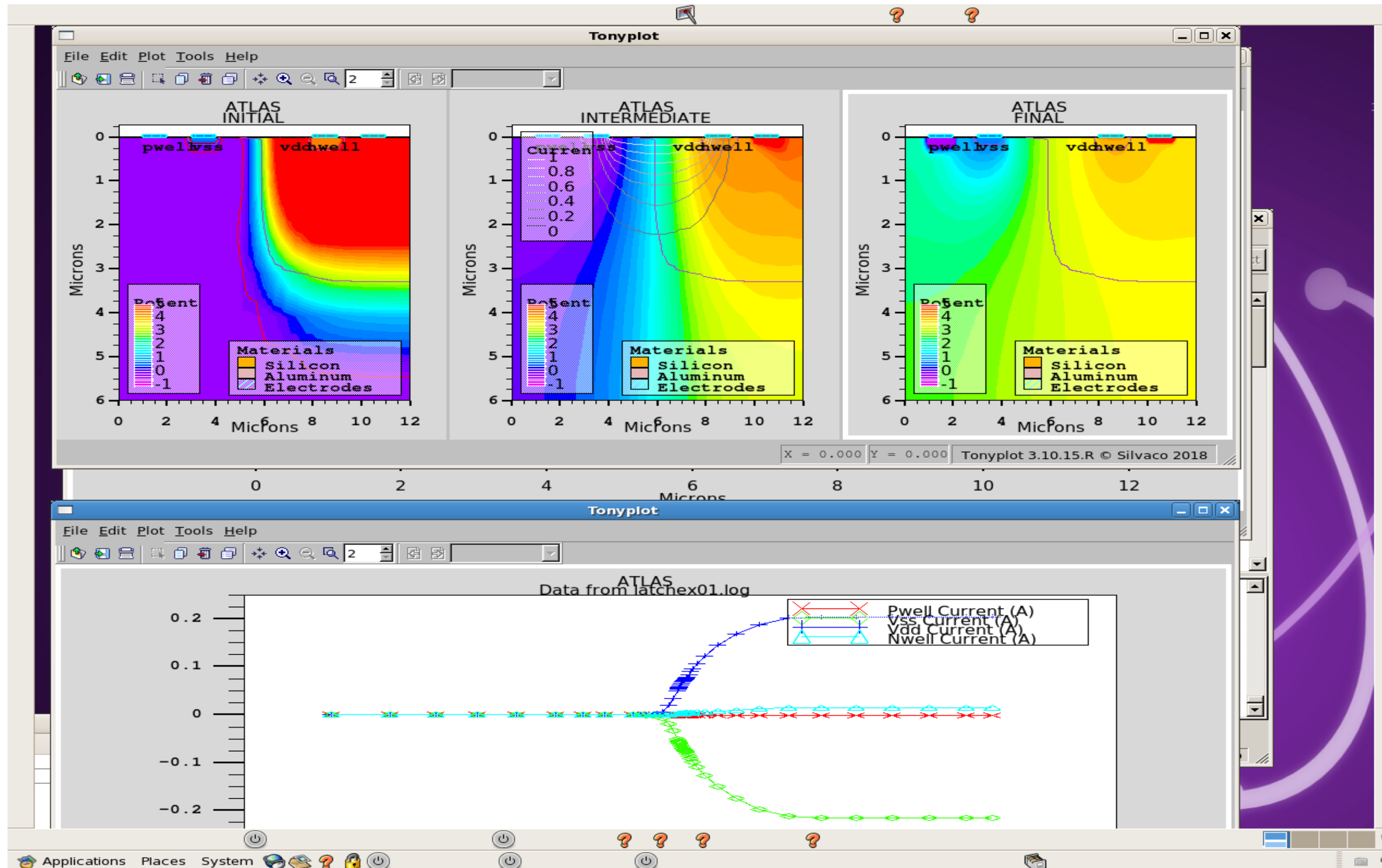


Out of Thomas Ernst and Francois Andrieu presentation (2017)

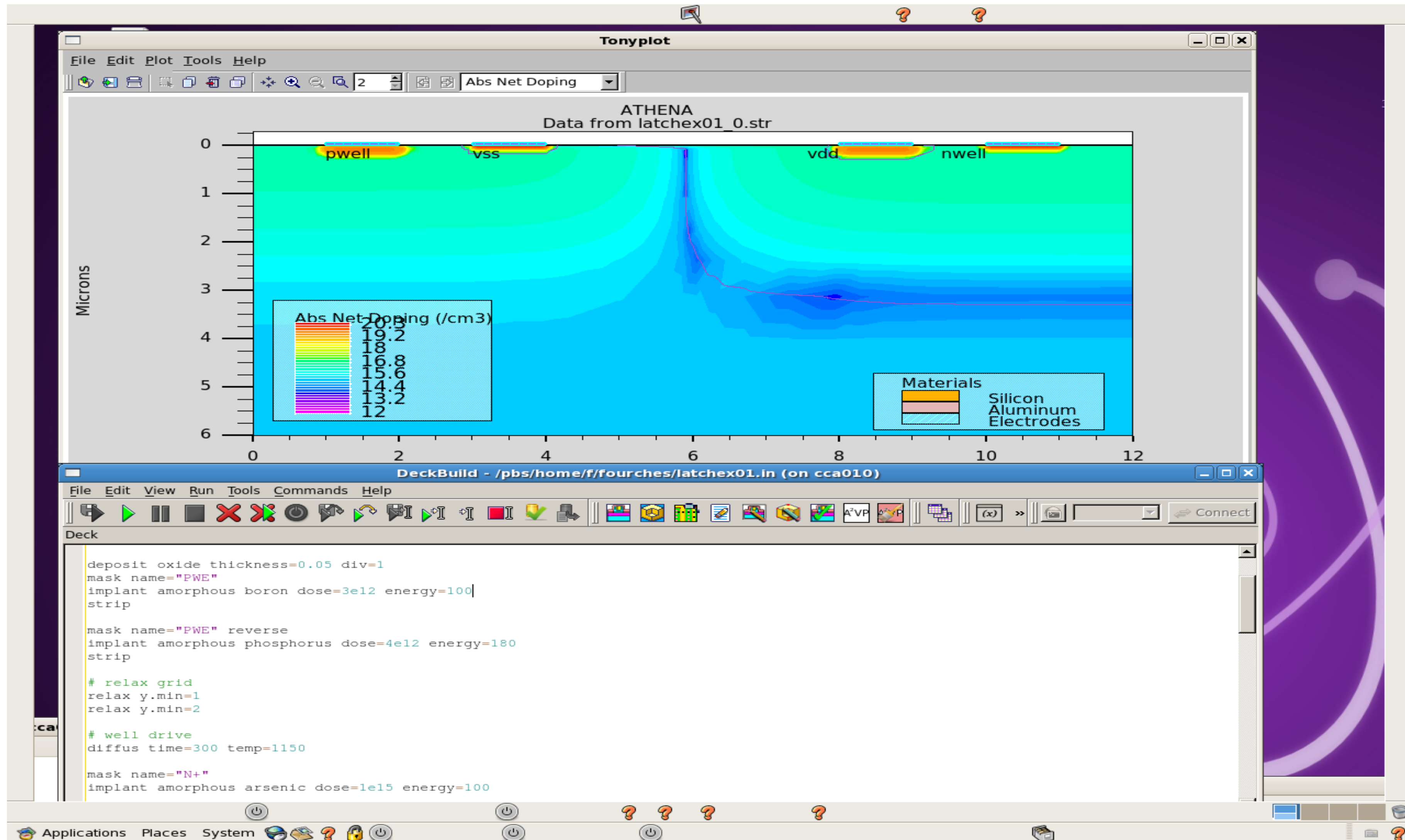


Backside substrate biasing in to eliminate
Carriers in undoped substrate

IC BASIC PROCESSES : device simulation



IC BASIC PROCESSES : process simulation



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