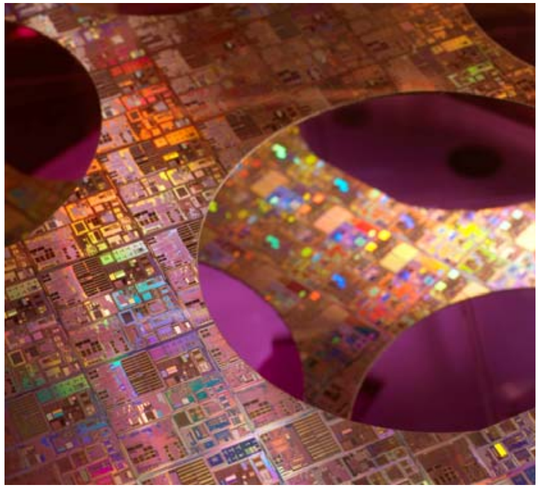
# Spintronic phenomena and components for memory, logic and RF applications



Giant MagnetoResistance

Benefit in magnetic recording technology

Tunnel Magnetoresistance

Spin-transfer

Magnetic Random Access Memories (MRAM)

Hybrid CMOS/magnetic components for non-volatile and reprogrammable logic

Radio Frequency oscillators based on spin-transfer

Conclusion

# Acknowledgements

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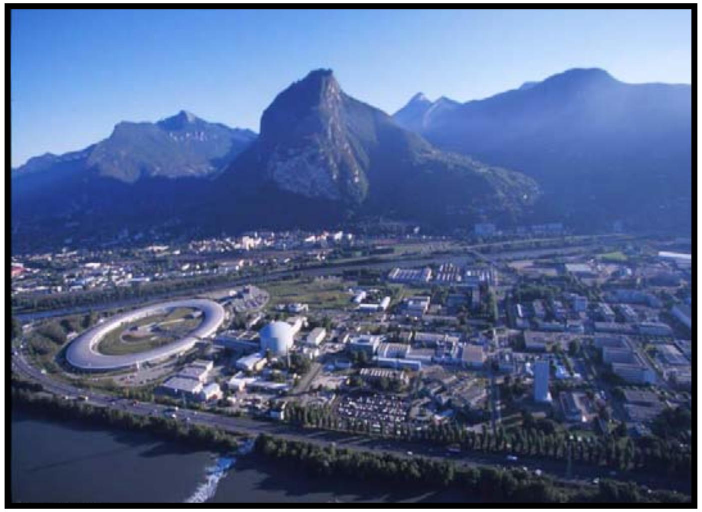

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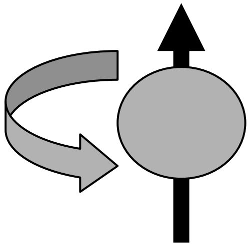
# Spin electronics

**Spin electronics or spintronics** :

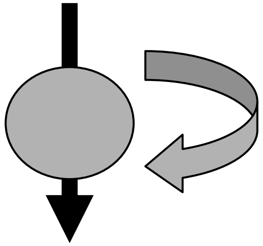
⇨ electrons = electrical charge + spin ↑ or ↓

<u>Purpose of spin-electronics</u> : Use spin as a new degree of freedom
⇒ New phenomena ⇒ new components (MRAM, Logic gates, RF components)

Classical image of spin :



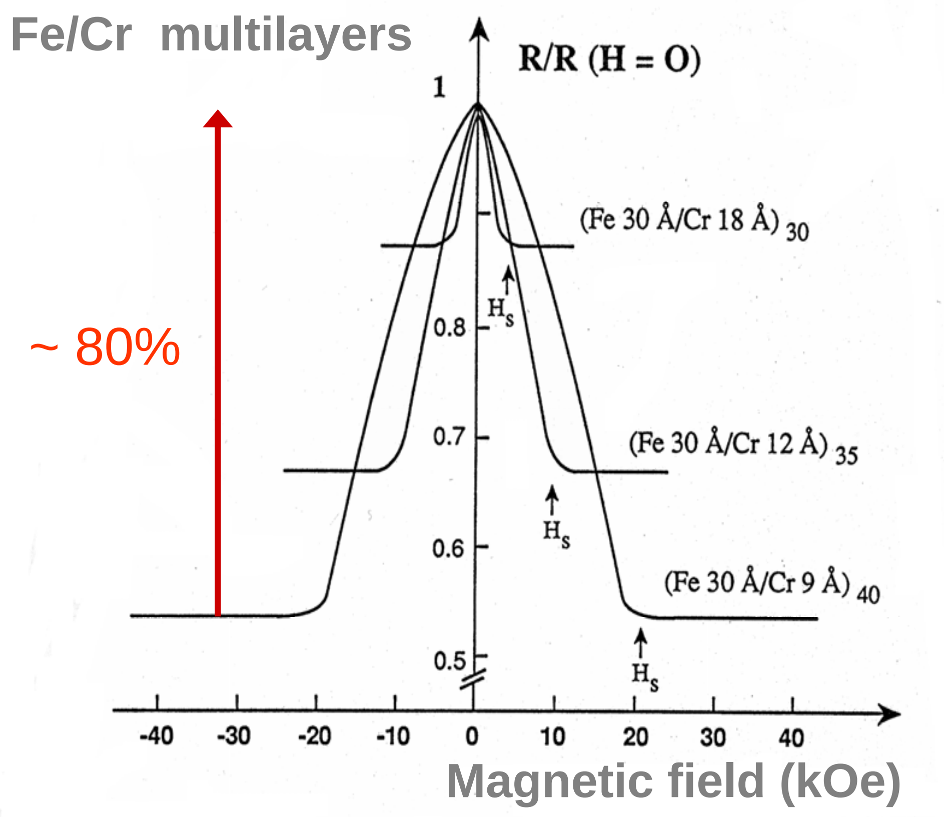
Spin up



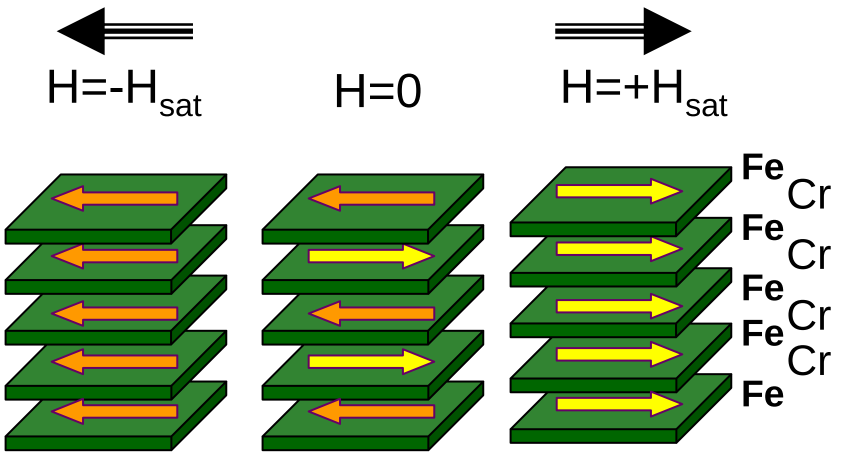
Spin down

All electrons have a spin: wave function described with « up » and « down » components.
In non-magnetic material : « up » and « down » spin populations are equal
In magnetic material : net spin polarization parallel to magnetization (~50% in Co).

# Birth of spin electronics : Giant magnetoresistance discovery (1988)



*A.Fert et al, PRL (1988);*
*P.Grunberg et al, patent (1988)+PRB (1989)*



Antiferromagnetically coupled multilayers

$$GMR = \frac{R_{AP} - R_P}{R_P}$$

*Nobel Prize 2007*

# Spin dependent transport in magnetic metals

Current carried in parallel by “spin up” and by “spin down” electrons

Scattering of electrons determined by DOS at $E_F$ :

Fermi Golden rule : $P^{\sigma} \propto <i|W|f>^2 D_f(E_F)$

Different density of states at Fermi energy for spin-up and spin-down electrons

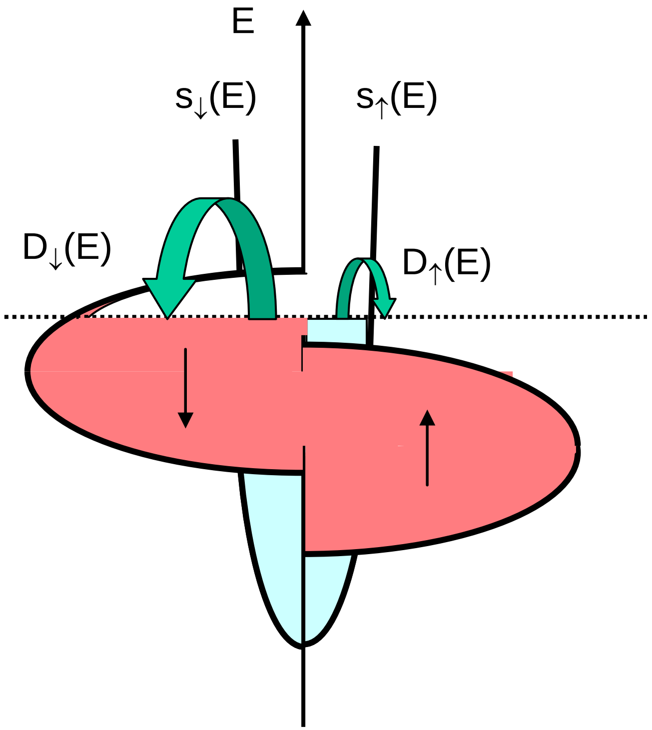
⇨

Different mean free paths and different resistivities for spin-up and spin-down electrons

Example: $\lambda_{\uparrow Co} = 10nm; \lambda_{\downarrow Co} = 1nm$

$\rho_{\uparrow Co} = 18\mu\Omega.cm \quad \rho_{\downarrow Co} = 180\mu\Omega.cm$

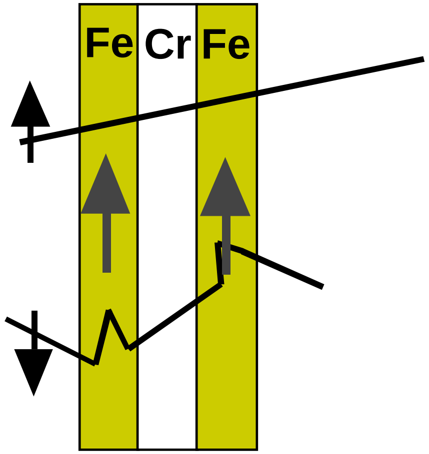
*Schematic electronic structure of magnetic metals*



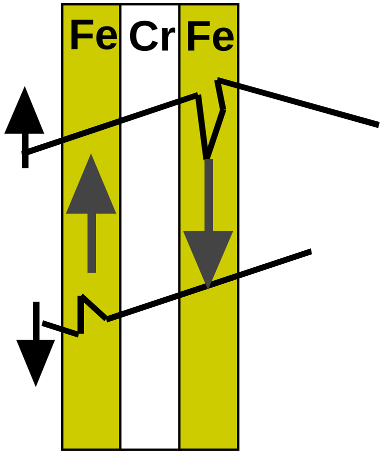
$$\rho_{Co} = \frac{\rho_{\uparrow Co}\rho_{\downarrow Co}}{\rho_{\uparrow Co} + \rho_{\downarrow Co}} = 16.4\mu\Omega.cm$$

# Simple model of Giant Magnetoresistance

**Parallel config**

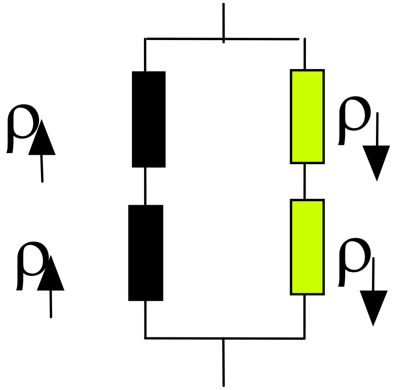


**Antiparallel config**

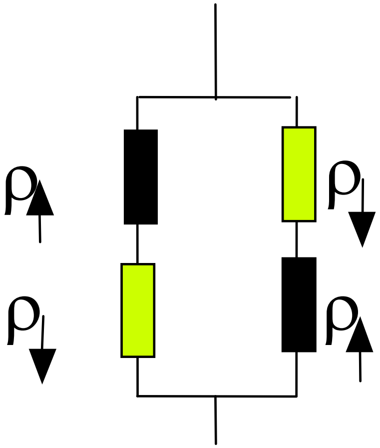


$$\frac{\Delta\rho}{\rho_{ap}} = \left(\frac{\rho_{\uparrow} - \rho_{\downarrow}}{\rho_{\uparrow} + \rho_{\downarrow}}\right)^2 = \left(\frac{\alpha - 1}{\alpha + 1}\right)^2$$

Equivalent resistances :



$$\rho_P = \frac{2\rho_{\uparrow}\rho_{\downarrow}}{(\rho_{\uparrow} + \rho_{\downarrow})}$$

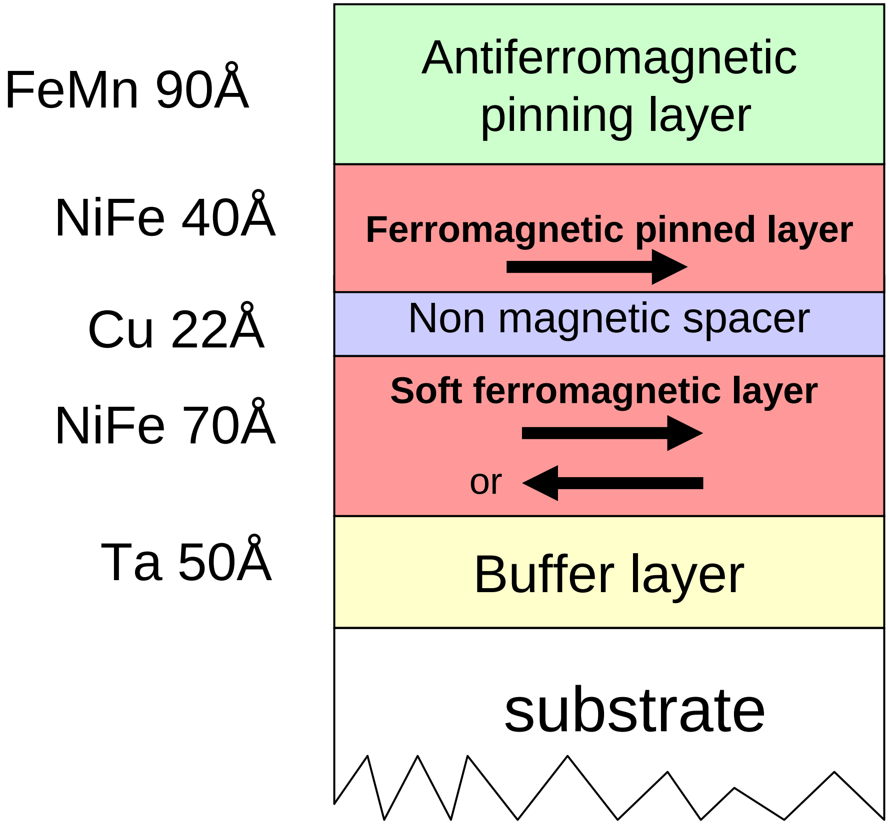


$$\rho_{AP} = \frac{(\rho_{\uparrow} + \rho_{\downarrow})}{2}$$

$$\alpha = \frac{\rho_{\uparrow}}{\rho_{\downarrow}}$$

Key role of
scattering contrast $\alpha$

# Low field GMR: Spin-valves



FeMn 90Å

NiFe 40Å

Cu 22Å

NiFe 70Å

Ta 50Å

Antiferromagnetic pinning layer

**Ferromagnetic pinned layer**

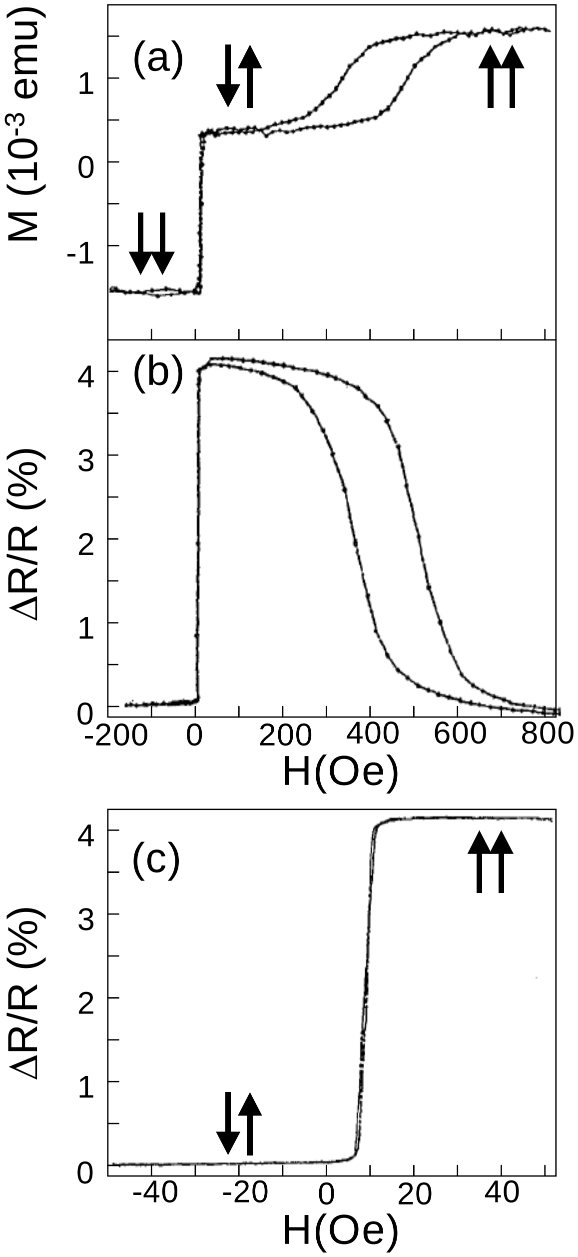
Non magnetic spacer

**Soft ferromagnetic layer**

or

Buffer layer

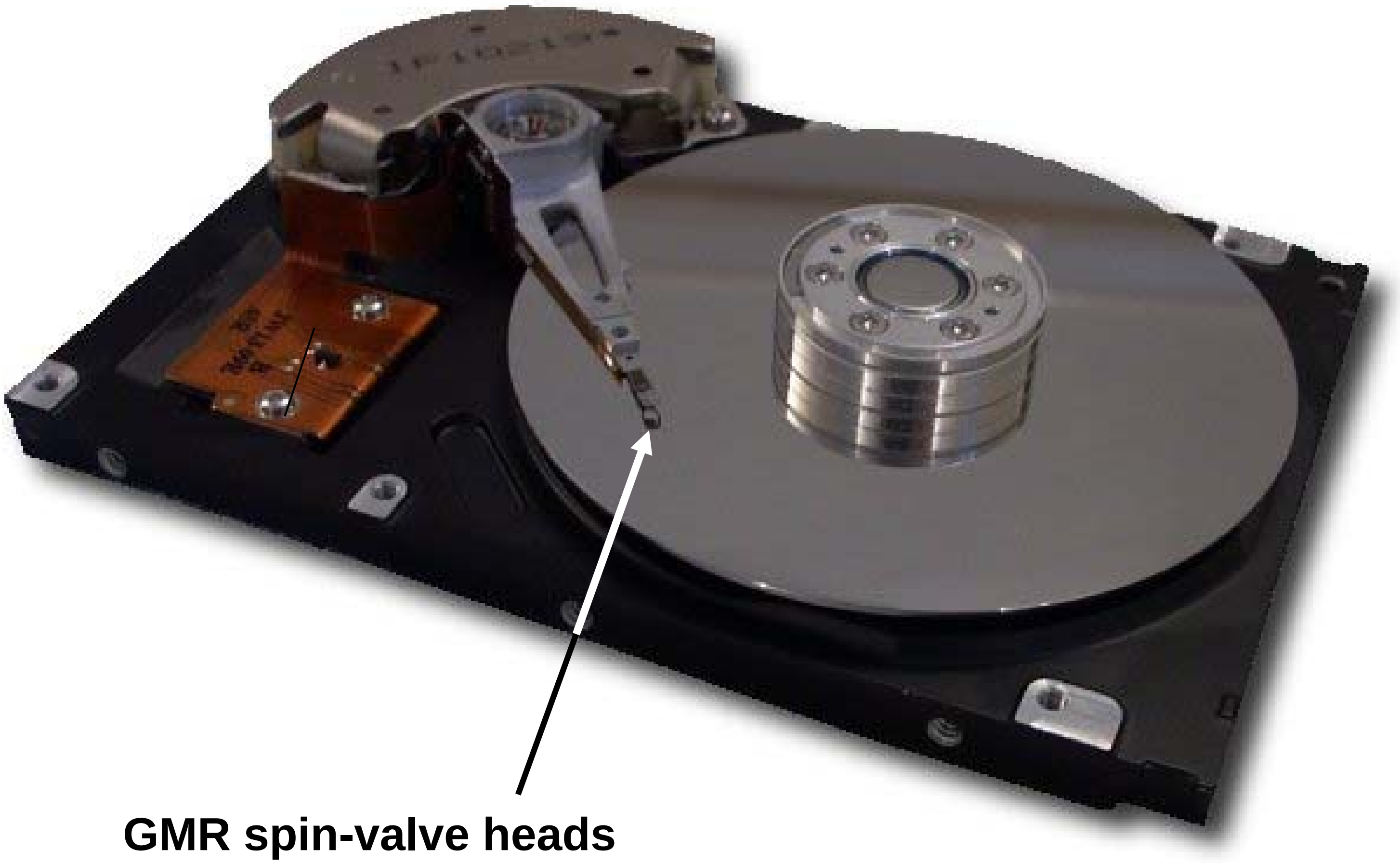
substrate



- •Ultrasensitive magnetic field sensors (MR heads)
- •Spin engineering of magnetic multilayers

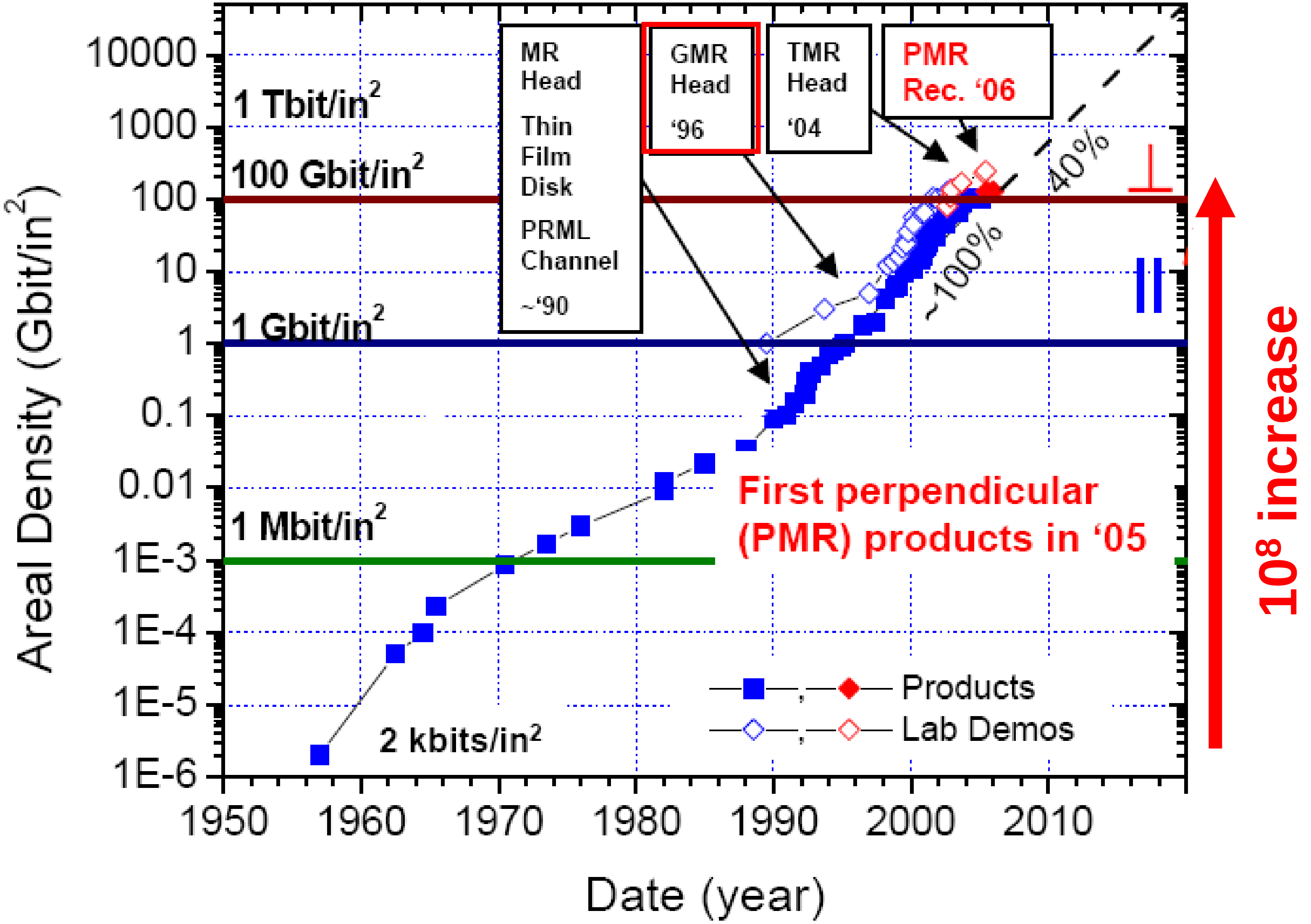
B.Dieny et al, Phys.Rev.B.(1991)+patent US5206590 (1991).

# Benefit of GMR in magnetic recording



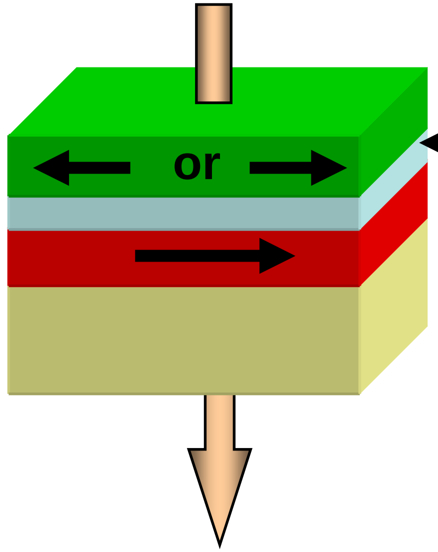
**GMR spin-valve heads from 1998 to 2004**

# Dramatic increase in areal storage density over the past 50 years



# Magnetic tunnel junctions – Tunnel magnetoresistance

**Structure of a magnetic tunnel junction**



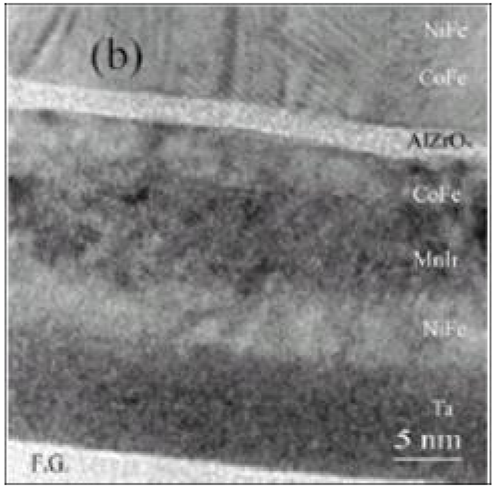
**Storage layer: CoFe 4 nm**

**$Al_2O_3$ barrier 1.5nm**

**Reference layer :CoFe 3nm**

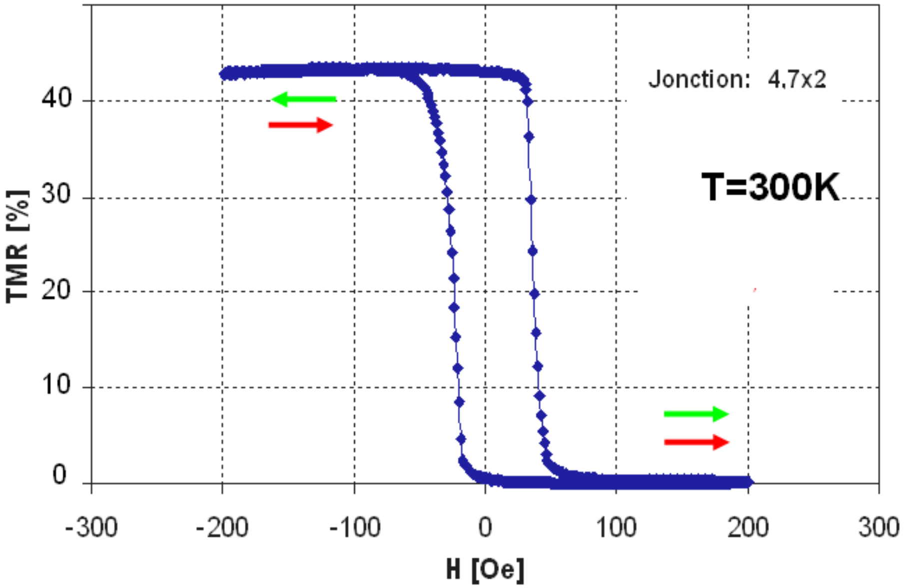
**IrMn 7nm**

**Acts as a couple polarizer/analyzer with the spin of the electrons.**



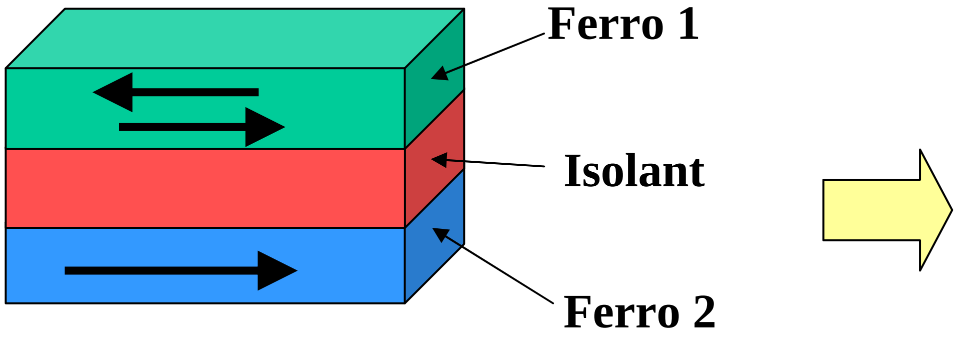
**$Al(Zr)O_x$**

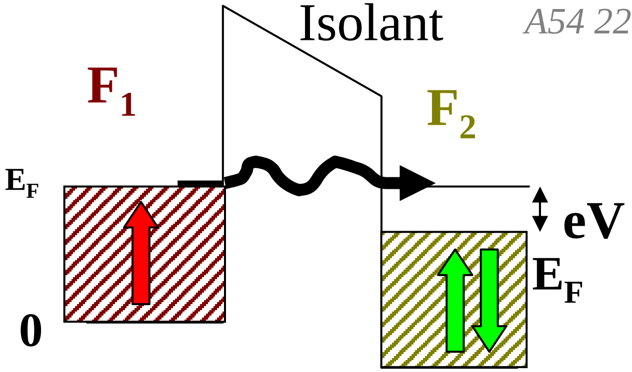
- First observation of TMR at low T in MTJ: Julliere (1975) (Fe/Ge/Co)
- TMR at 300K : *Moodera et al, PRL (1995); Myazaki et al, JMMM(1995).* $\Delta R/R \sim 50\%$ in $AlO_x$ based junctions



# Julliere model of TMR

*Jullière,Phys. Lett. A54 225 (1975)*





Fermi Golden rule: proba of tunneling $P^\sigma \propto <i|W|f>^2 D_f(E_F)$

Nb of electrons candidate for tunneling $\propto D_i(E_F)$

$\Rightarrow$ tunneling current in each spin channel $J^\sigma \propto D_1^\sigma(E_F) \times D_2^\sigma(E_F)$

<u>Parallel configuration</u>

$$J^{parallel} \propto D_1^\uparrow D_2^\uparrow + D_1^\downarrow D_2^\downarrow$$

<u>Antiparallel configuration</u>

$$J^{antiparallel} \propto D_1^\uparrow D_2^\downarrow + D_1^\downarrow D_2^\uparrow$$

$$\boxed{P = \frac{D^\uparrow(E_F) - D^\downarrow(E_F)}{D^\uparrow(E_F) + D^\downarrow(E_F)}}$$

$$\boxed{TMR = \frac{\Delta R}{R_P} = \frac{2\,P_1 P_2}{1 - P_1 P_2}}$$

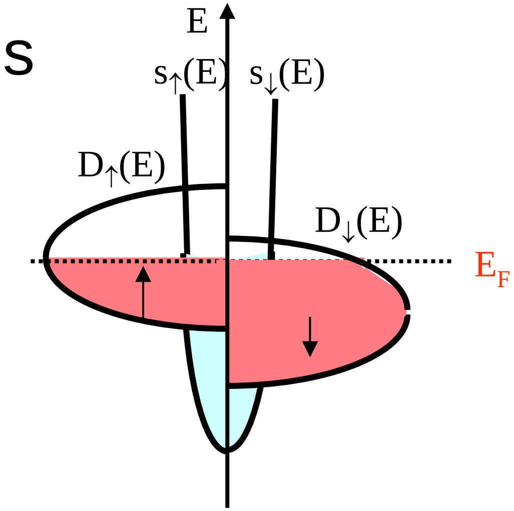
$$TMR = \frac{\Delta R}{R_{AP}} = \frac{2\,P_1 P_2}{1 + P_1 P_2}$$

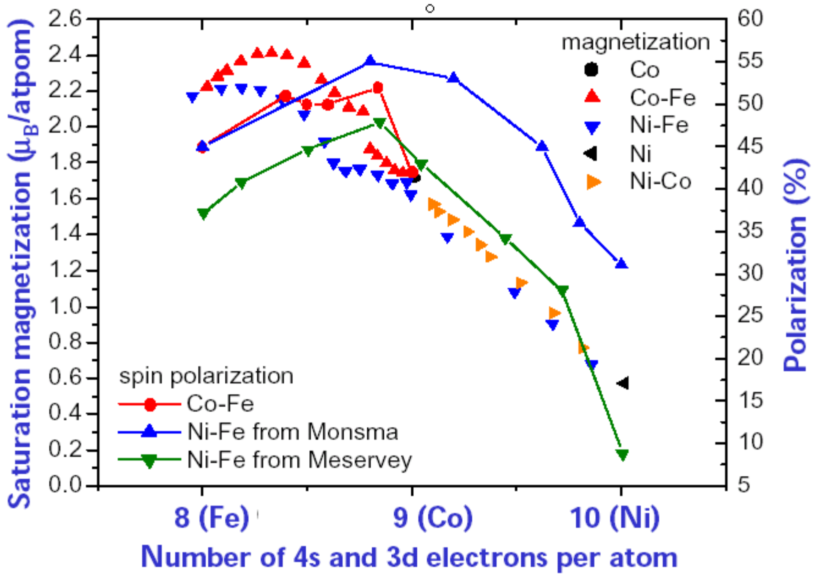
P~50% in Fe, Co

ΔR/R~40 - 70% with alumina barriers

# Spin polarization of 3d metals

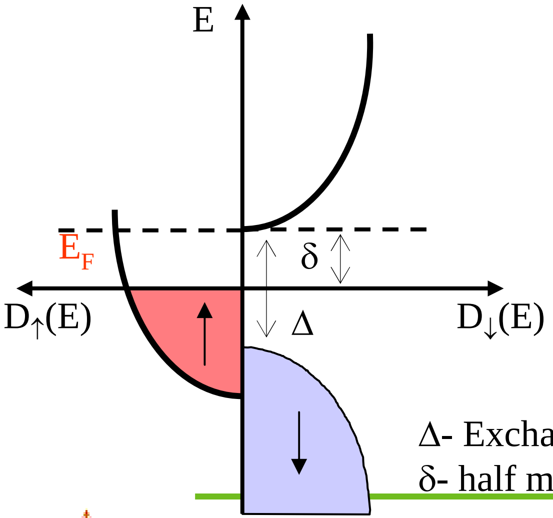
Metals





Parkin
et al

Half metals



Δ- Exchange splitting
δ- half metallic gap

Half metals are
100% spin polarized !

Heusler alloys

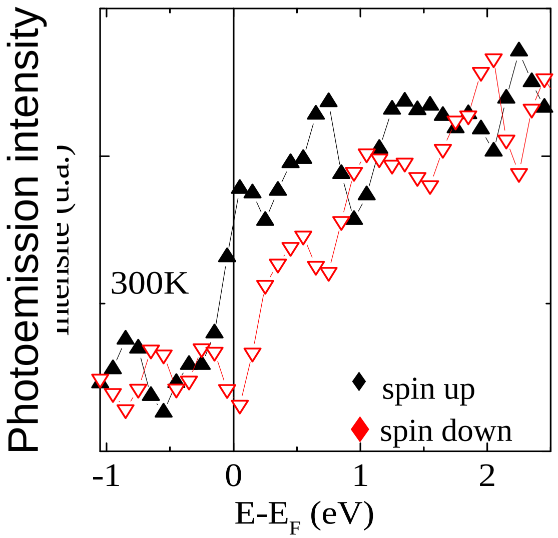
$LaSrMnO_3$

$Fe_3O_4$

$CrO_2$

…

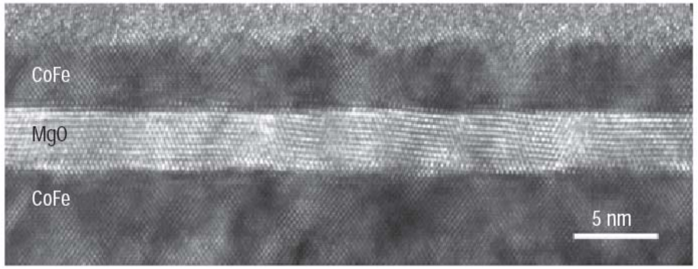
NiMnSb *(Ristoiu et al.)*



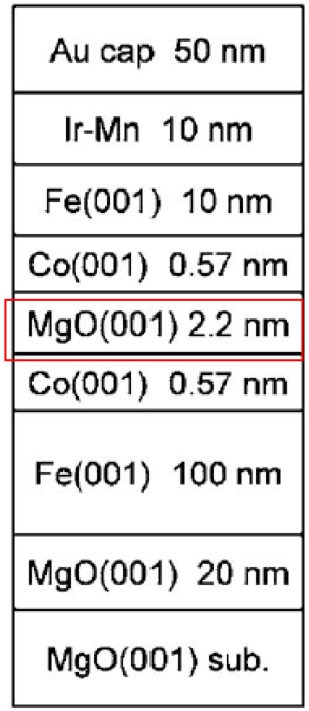
# Giant TMR of MgO tunnel barriers

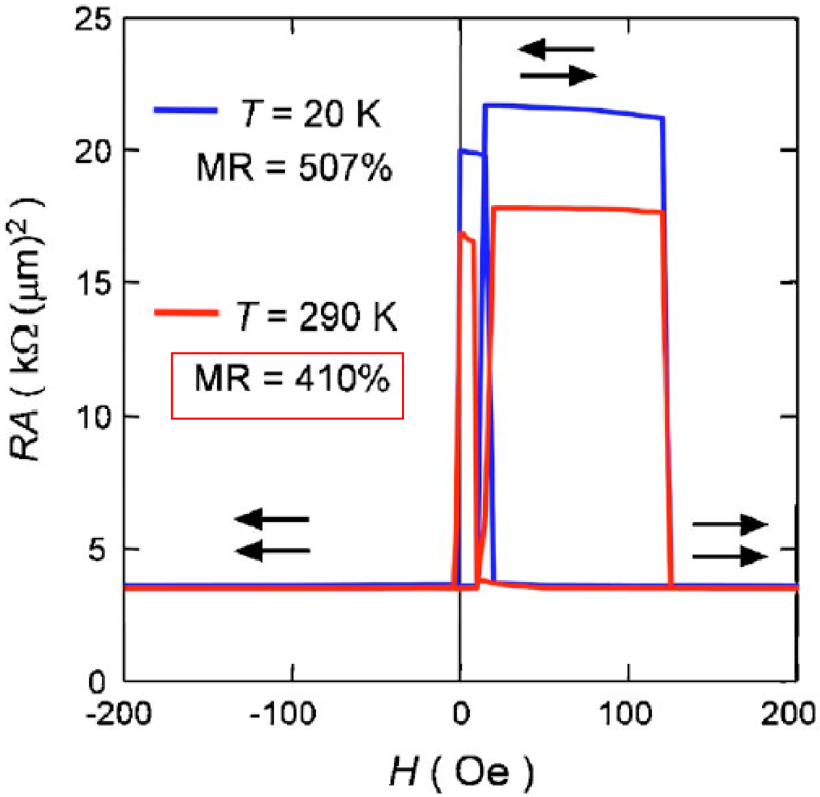
*S.S.P.Parkin et al, Nature Mat. (2004), nmat1256.*
*S.Yuasa et al, Nature Mat. (2004), nmat 1257.*

Very well textured MgO barriers grown by sputtering or MBE on bcc CoFe or Fe magnetic electrodes, or on amorphous CoFeB electrodes followed by annealing to recrystallize the electrode.



*Yuasa et al, APL89, 042505(2006)*





# Tunneling through crystalline MgO barriers (cont'd)

Co|MgO|Co and CoFe|MgO|CoFe were predicted to show extremely high TMR for well ordered interfaces (W.Butler, Phys.Rev.B.(2000)).
New mechanism of spin-filtering during tunneling through MgO according to symmetry of wave functions.

| Spin alignment | up-up | down-down | up-down or down=up | $G_P/G_{AP}$ |
|---|---|---|---|---|
| Fe\|MgO\|Fe | 2.55 x$10^9$ | 7.08 x$10^7$ | 2.41 x$10^7$ | **54.3** |
| Co\|MgO\|Co | 8.62 x$10^8$ | 7.51 x$10^7$ | 3.60 x$10^6$ | **147.2** |
| FeCo\|MgO\|FeCo | 1.19 x$10^9$ | 2.55 x$10^6$ | 1.74 x$10^6$ | **353.5** |

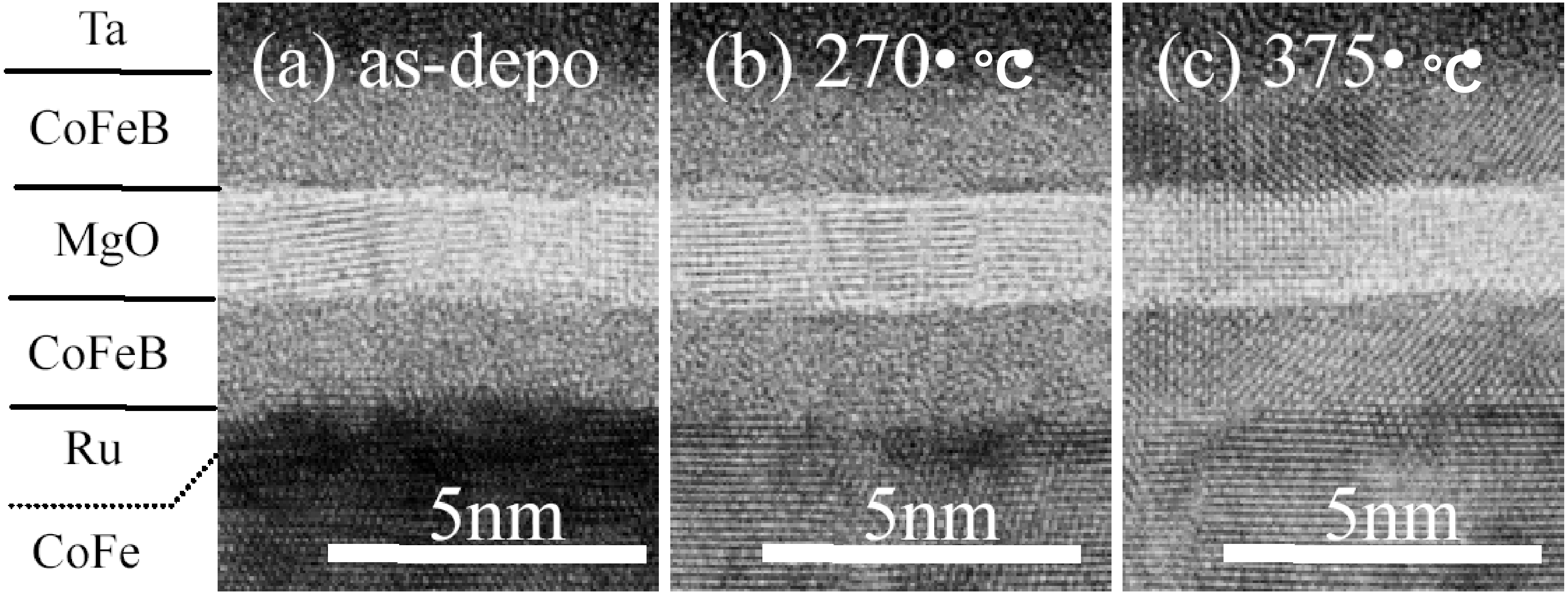
The conductances above were calculated by integrating over the entire Fermi surface. They assumed 8 layers of MgO.

*W.Butler, Alabama Univ*

# Magnetic tunnel junctions based on MgO tunnel barriers

- As-deposited, CoFeB amorphous, MgO polycristalline
- Upon annealing, recrystallization of CoFeB from the MgO interfaces and improvement in MgO crystallinity with (100) bcc texture

*J. Hayakawa et al. Jap. J. Appl. Physics 2005*

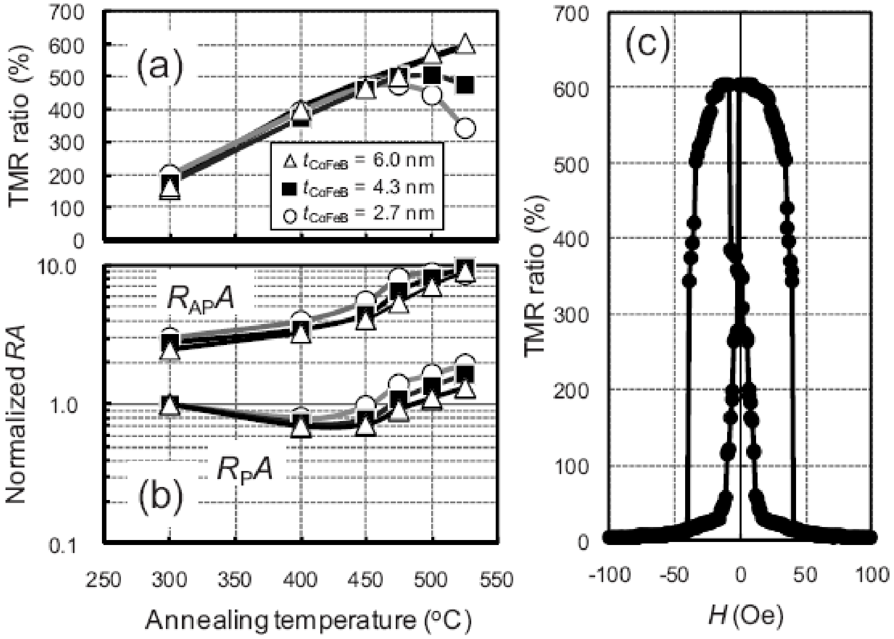


*Also, Yuasa et al. Applied Physics Letters, 2005*

APPLIED PHYSICS LETTERS **93**, 082508 (2008)

# Tunnel magnetoresistance of 604% at 300 K by suppression of Ta diffusion in CoFeB/MgO/CoFeB pseudo-spin-valves annealed at high temperature

S. Ikeda,[1,a)] J. Hayakawa,[2] Y. Ashizawa,[3,b)] Y. M. Lee,[1,c)] K. Miura,[1,2] H. Hasegawa,[1,2]
M. Tsunoda,[3] F. Matsukura,[1] and H. Ohno[1,d)]



Applied Physics Express **2** (2009) 083002

# Large Tunnel Magnetoresistance of 1056% at Room Temperature in MgO Based Double Barrier Magnetic Tunnel Junction

Lixian Jiang, Hiroshi Naganuma*, Mikihiko Oogane, and Yasuo Ando

*Department of Applied Physics, Graduate School of Engineering, Tohoku University, Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan*

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# Magnetic Tunnel Junctions (MTJ): a reliable path for CMOS/magnetic integration

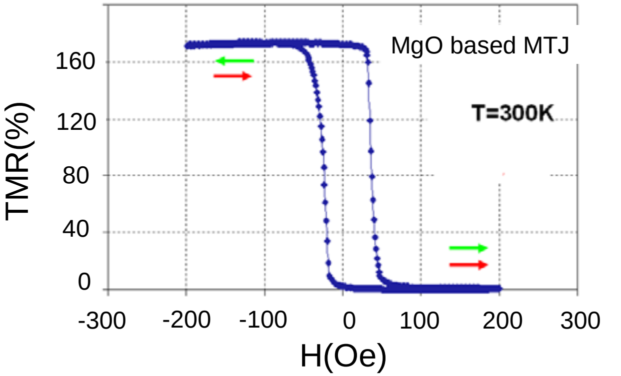
- Resistance of MTJ compatible with resistance of passing FET (few kΩ)

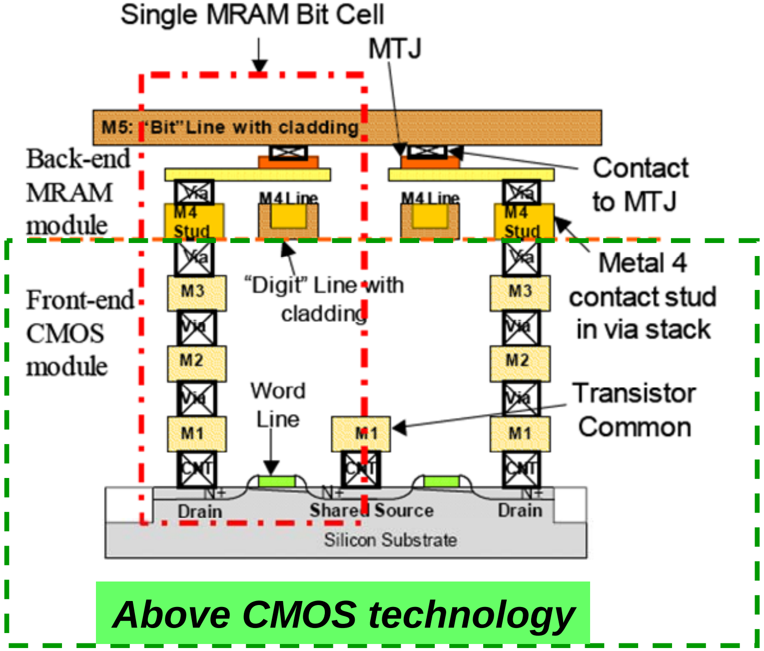
- MTJ can be deposited in magnetic back end process

- No CMOS contamination

- MTJ used as variable resistance controlled by field or current/voltage (Spin-transfer)

- Commercial CMOS/MTJ products available from EVERSPIN since 2006 (4Mbit MRAM)
Implemented in Airbus flight controller





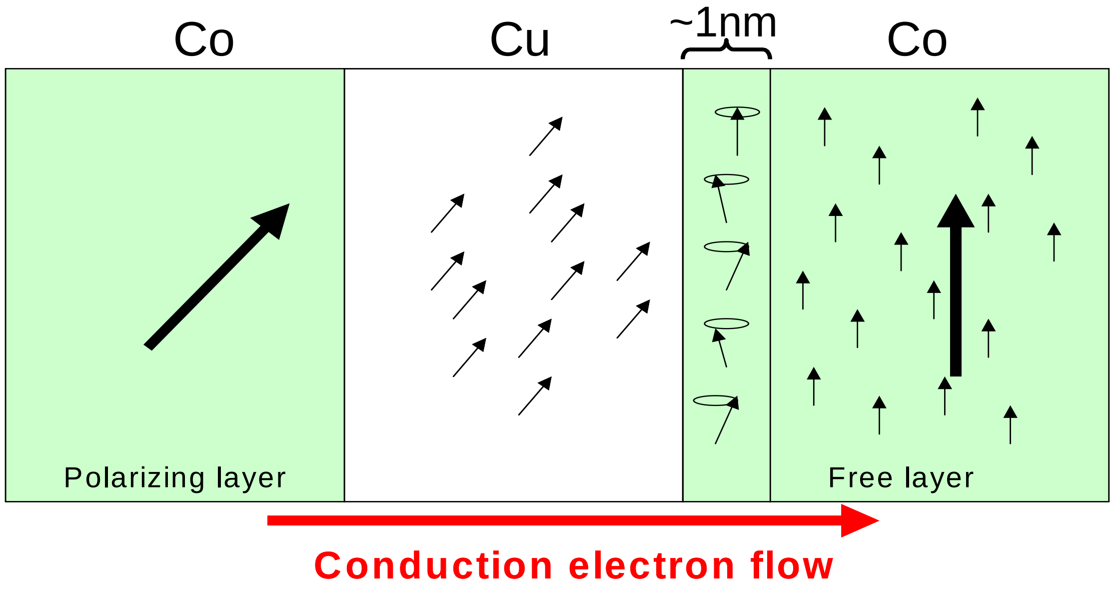
Cross-section of Freescale (Everspin) 4Mbit MRAM based on field switching

# Spin-transfer

Predicted by Slonczewski (JMMM.159, L1(1996)) and Berger (Phys.Rev.B54, 9359 (1996))

**Giant or Tunnel magnetoresistance**:
Acting on electrical current via the magnetization orientation

**Spin transfer is the reciprocal effect**:
Acting on the magnetization via the spin polarized current



*M.D.Stiles et al, Phys.Rev.B.66, 014407 (2002)*

Reorientation of the direction of polarization of current via incoherent precession/relaxation of the electron spin around the local exchange field

⇒ **Torque on the free layer magnetization**

# Magnetization dynamics: Effective field + spin-torque

*Slonczewski (JMMM.159, L1(1996)) and Berger (Phys.Rev.B54, 9359 (1996)), Stiles, Levy, Fert, Barnas, Vedyaev*

*Polarizer M*

$$\frac{dM}{dt} = -\gamma M \times \Big(\underbrace{H_{eff} + \boxed{bI.M_p}}_{\text{Effective field term (conserves energy)}}\Big) + \boxed{\underbrace{\gamma a I.M \times \big(M \times M_p\big)}_{\text{Spin-torque term: damping (or antidamping) term}}} + \underbrace{\alpha M \times \frac{dM}{dt}}_{\text{Gilbert Damping term}}$$

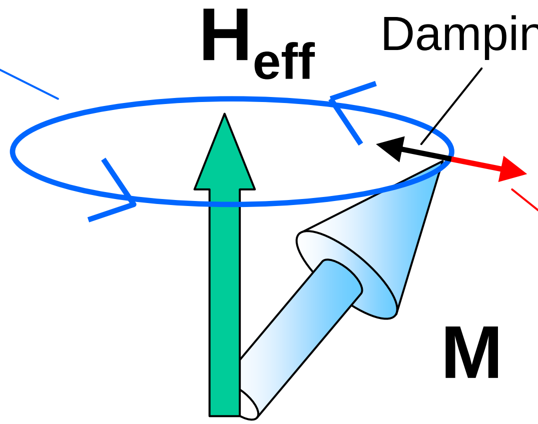
( Modified LLG)

Non conservative

a and b are coefficients proportional to the spin polarization of the current

Precession from effective field

Damping torque (intrinsic Gilbert damping α)



Current-induced torque (Spin-torque)

Effective field term is relatively weak in metallic pillars (<10% of spin-torque term) but more important in MTJ (~30% of spin-torque term)

# Energy dissipation and energy pumping due to spin transfer torque

Without spin torque (standard LLG) $$\frac{dE}{dt} = -\frac{\alpha\gamma}{1+\alpha^2}\frac{1}{M_s}\left|\mathbf{H}_{eff}\times\mathbf{M}\right|^2. \quad <0$$

Dissipation, leading to relaxation towards effective field

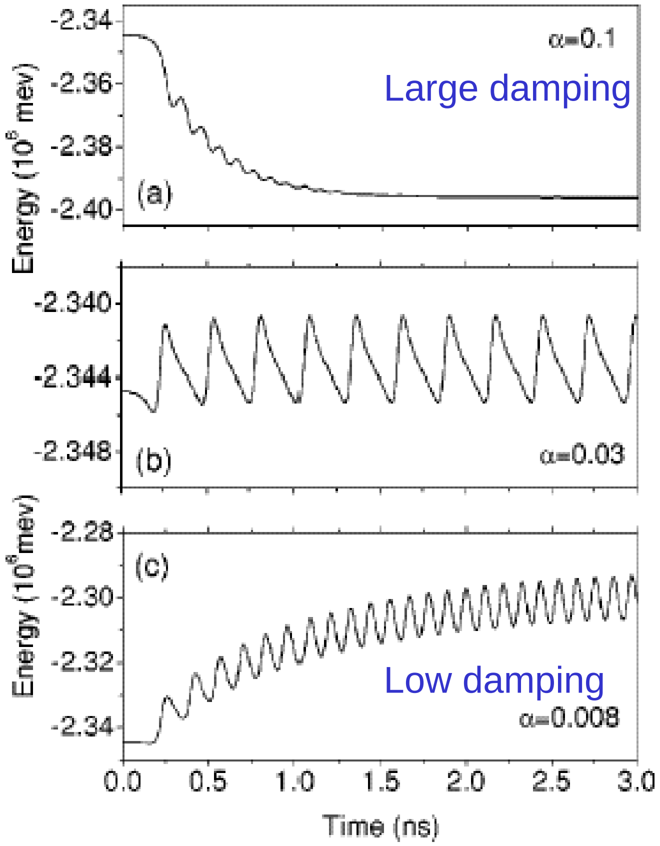
With spin torque term :

Proportional to current

$$\frac{dE}{dt} = -\frac{\gamma}{1+\alpha^2}\frac{1}{M_s}\Big[\alpha\left|\mathbf{H}_{eff}\times\mathbf{M}\right|^2 - \overset{\downarrow}{a}_J(\alpha M_s\hat{\mathbf{M}}_p - \mathbf{M}\times\hat{\mathbf{M}}_p)$$
$$\times(\mathbf{H}_{eff}\times\mathbf{M})\Big],$$

dE/dt can be either >0 or <0

*Z.Li and S.Zhang, Phys.Rev.B68, 024404 (2003)*



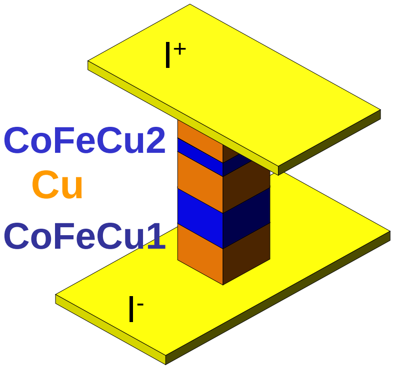
With large damping: standard dynamical behavior,

With low damping: New dynamical effects such as spin current induced steady excitations.

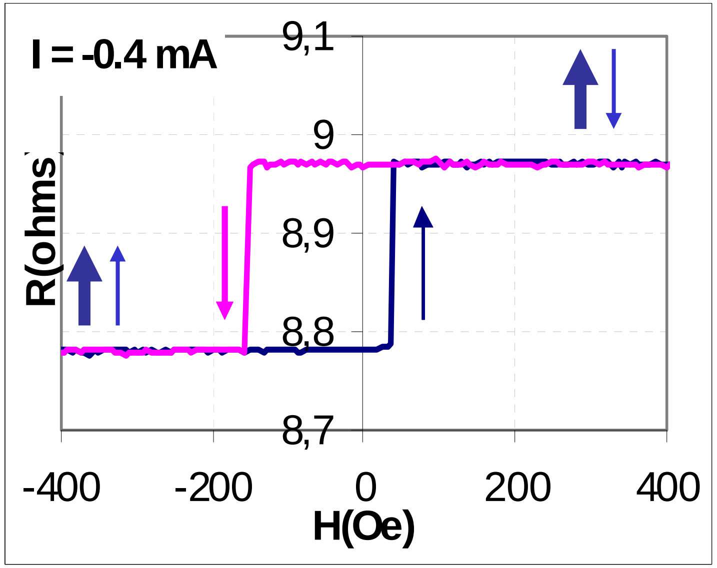
**The magnetization pumps energy from the spin-current.**

# Magnetization switching induced by a polarized current

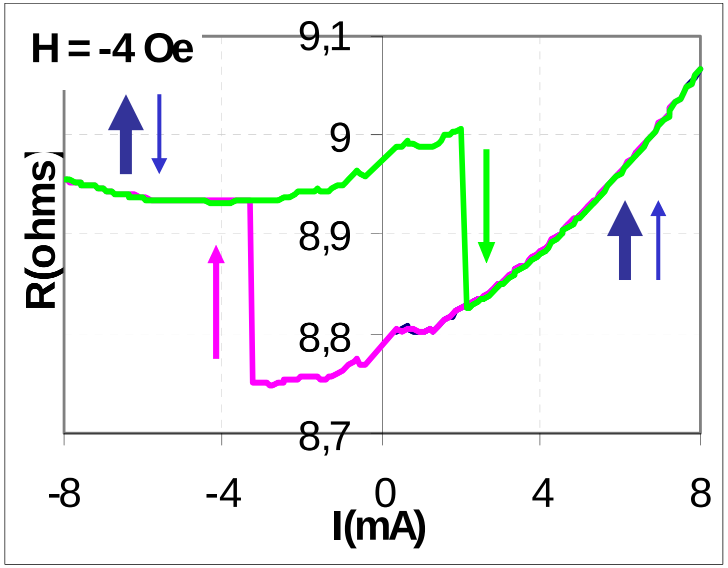
*Katine et al, Phys.Rev.Lett.84, 3149 (2000) on Co/Cu/Co sandwiches (Jc ~2-4.107A/cm²)*



## Field scan



## Current scan



$j_c^{P\text{-}AP}=1.9.10^7 A/cm^2$

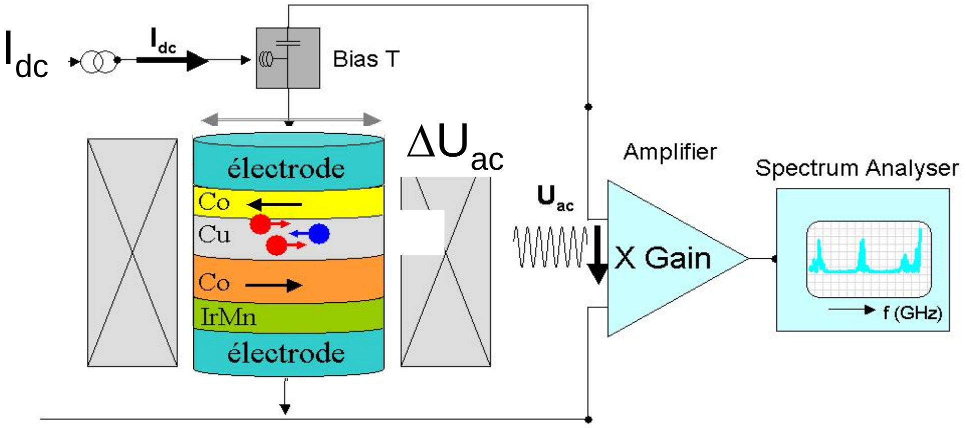
$j_c^{AP\text{-}P}=1.2.10^7 A/cm^2$

By spin transfer, a spin-polarized current can be used to manipulate the magnetization of magnetic nanostructures instead of by magnetic field.

⇒Can be used as a **new write scheme in MRAM**

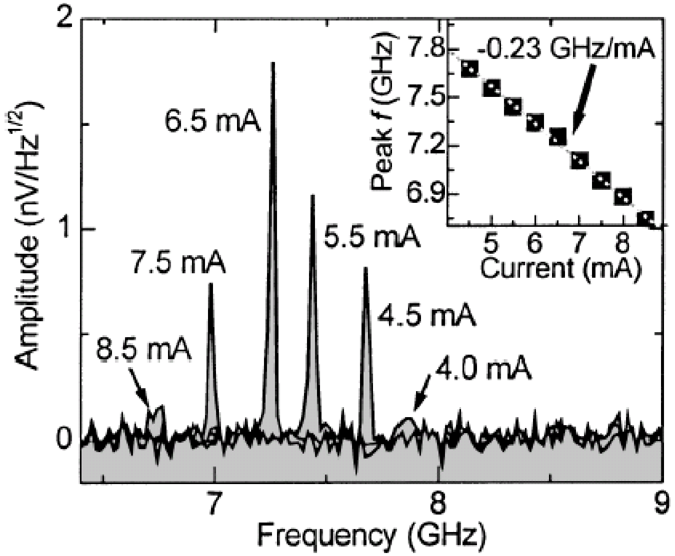
⇒Or to generate steady state oscillations leading to **RF oscillators**

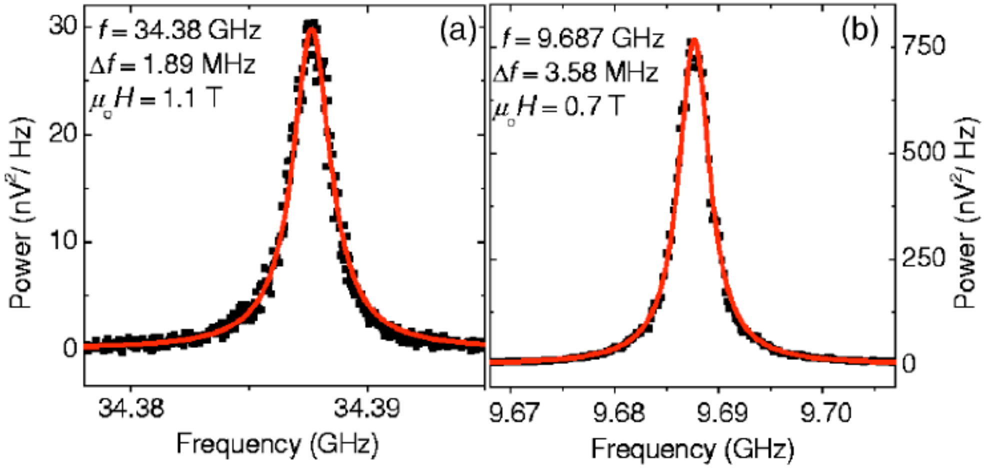
# Steady magnetic excitations induced by a polarized current



Kiselev et. al.,
*Nature* **425,**
p. 380 (2003)

Rippard et. al.,
*Phys. Rev. Lett*. **92**,
p. 27201 (2004)

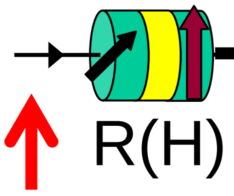


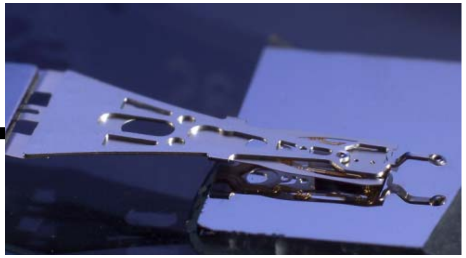


*Q=18200* *Q=2700*

Interesting for RF components

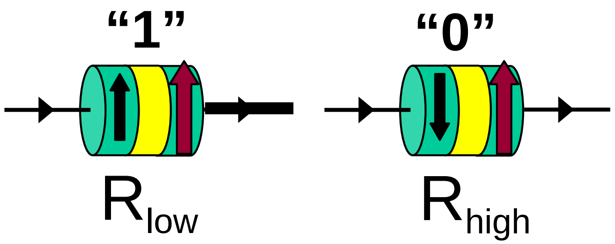
# Spintronic components

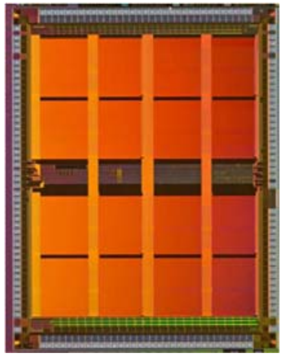




Write/read heads

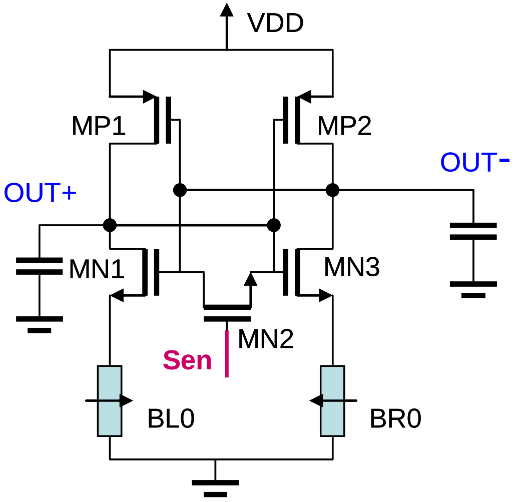
## Magnetic field sensors



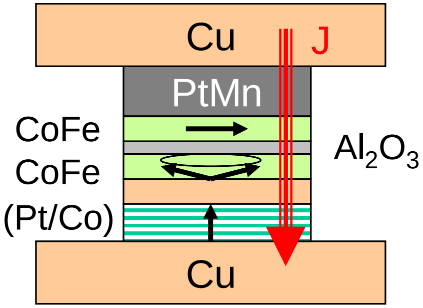


Freescale 4Mbit

## Memories



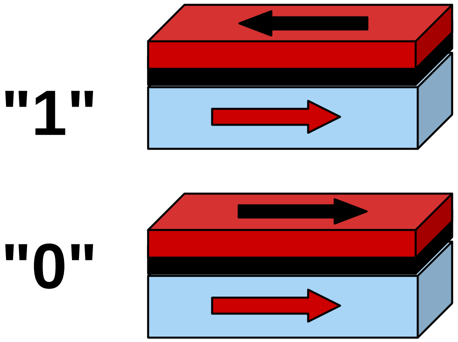
## Logic circuits

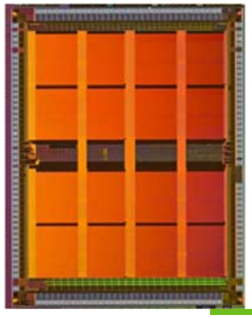


## RF components

# Field induced magnetic switching (FIMS) MRAM

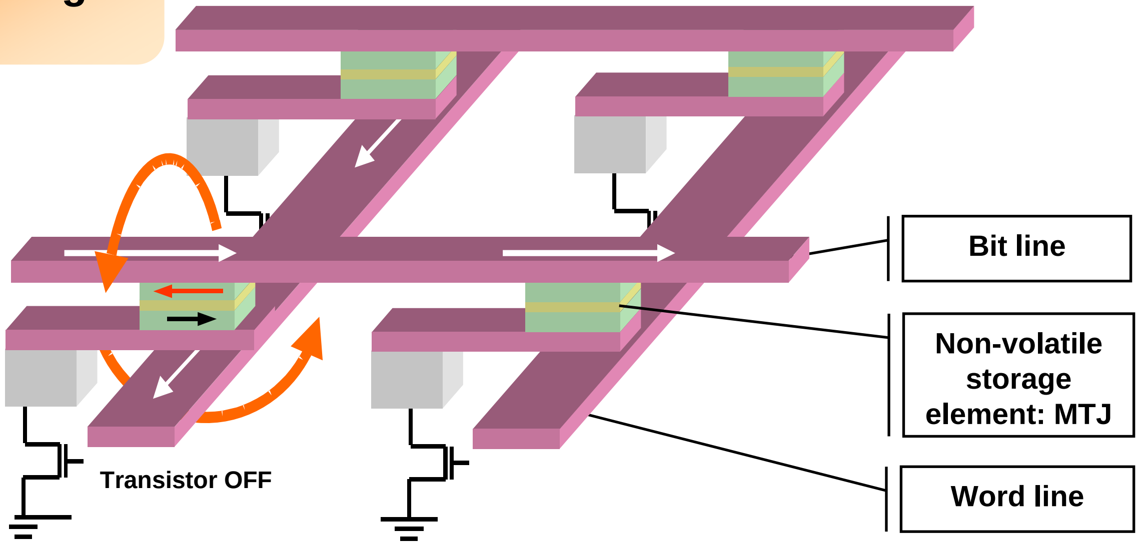
Principle :
Store data by the direction (parallel or antiparallel) of magnetic layers in MTJ





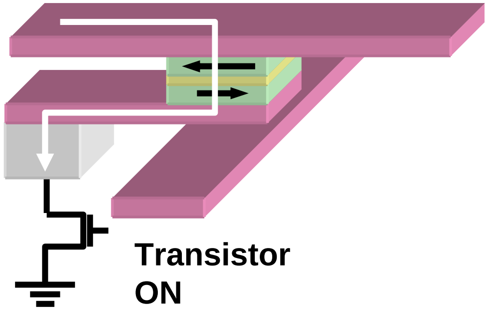
Freescale
4Mbit
(2006)

## Writing

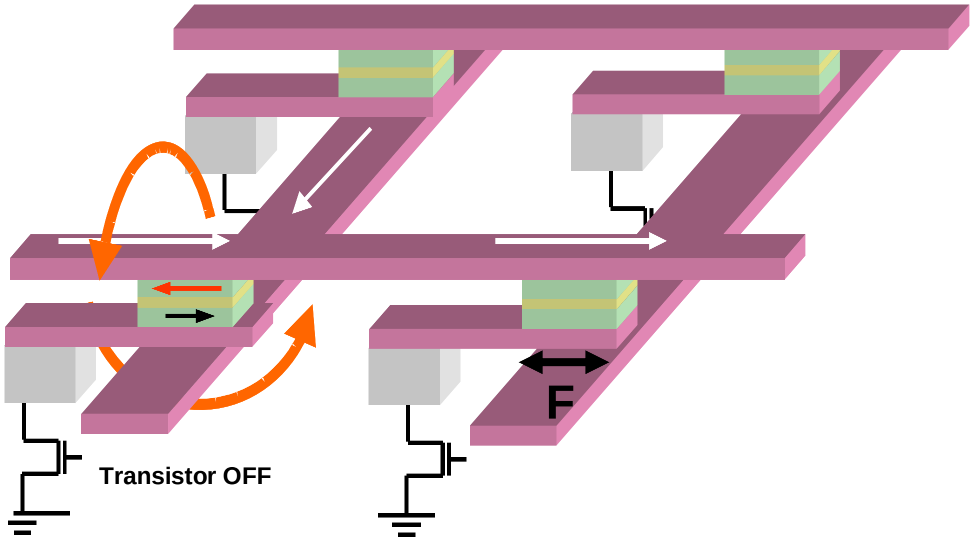


**Selectivity achieved by combination of two perpendicular magnetic fields**

## Reading



# Poor scalability of field induced switching MRAM



Limited scalability due to electromigration in bit/word lines

Energy barrier $KV > 40k_BT$ required for thermal stability of the information,

if V ↘ ~ $F^2$, then K and $H_{write}$ ↗ ~ $1/F^2$

$H_{write}$ in the range 5mT-10mT requiring write current ~ 5-10mA

As a result, $I_{write}$ ↗ ~ $1/F^2$ so that current density $j_{write}$ ↗ > $1/F^3$

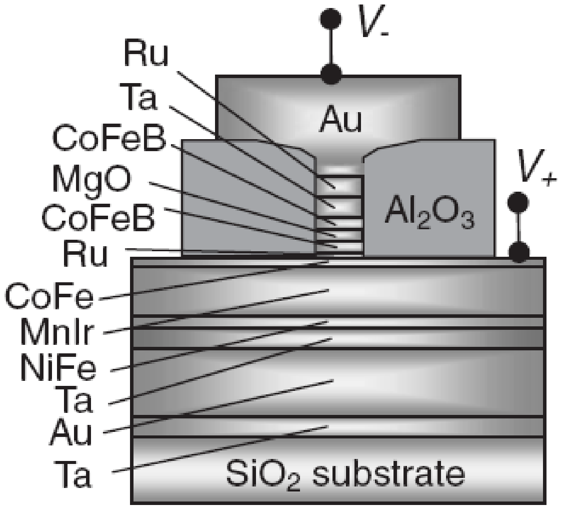
Electromigration limit: $j_{max} \sim 10^7 A/cm^2$ reached around F=60nm

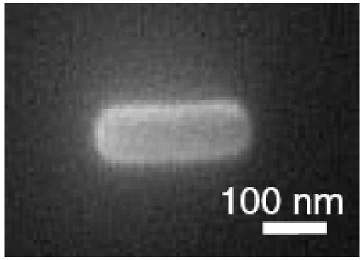
# Solution 1: Spin-Transfer Torque MRAM

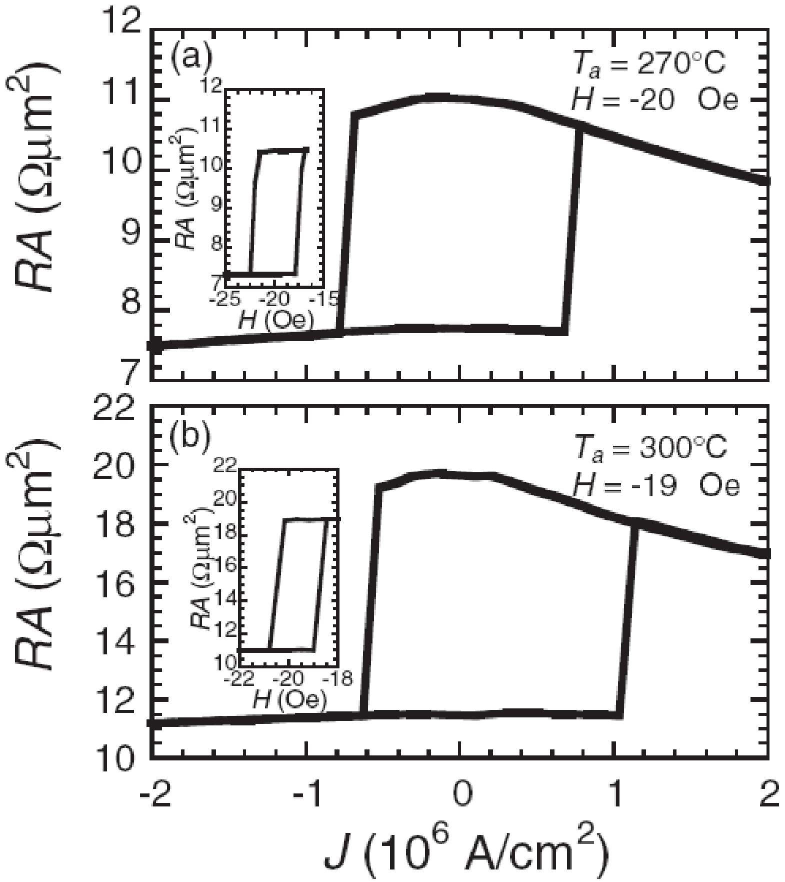
Slonczewski, Berger (1996); STT in MTJ: Huai et al, APL (2004); Fuchs et al, APL (2004)

The bipolar current flowing through the MRAM cell is used to switch the magnetization of the storage layer.

Reading at lower current density then writing so as to not perturb the written information while reading.



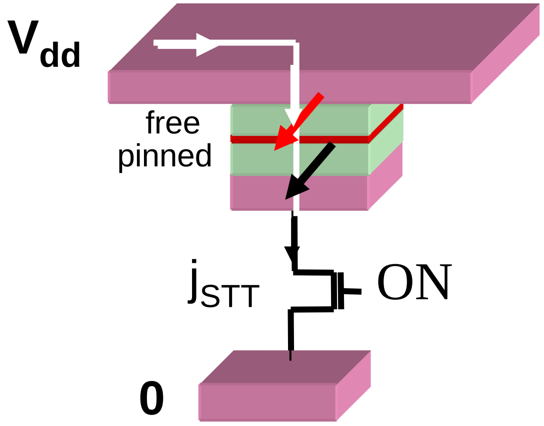




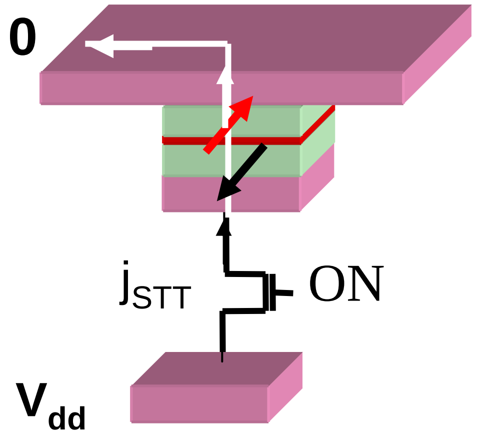
*Hayakawa et al,*
*Japanese Journal of Applied Physics*
*44, (2005),L 1267*

# STT MRAM scalability

**Writing “0”**



**Writing “1”**



- **Writing determined by a current density :**

$$j_{WR\ in-plane} = \left(\frac{2e}{\hbar}\right)\frac{\alpha\, t_F}{P}\left(\frac{\mu_0 M_S^{\ 2}}{2} + 2K\right)$$

**•Current through cell proportional to MTJ area**

**•$j_{write\ \ SST\ in\text{-}plane}$ ~ $8.10^5$A/cm² quasistatic ⇒ $3.10^6$A/cm² @10ns**

*Huai et al, Appl.phys.Lett.87, 222510 (2005) ; Hayakawa, Jap.Journ.Appl.Phys.44 (2005) L1246*

**•Still need to reduce critical current for switching by factor ~4 to minimize electrical stress on the barrier.**

- **Concern with thermal stability of the cell below 45nm (superparamagnetic limit)**

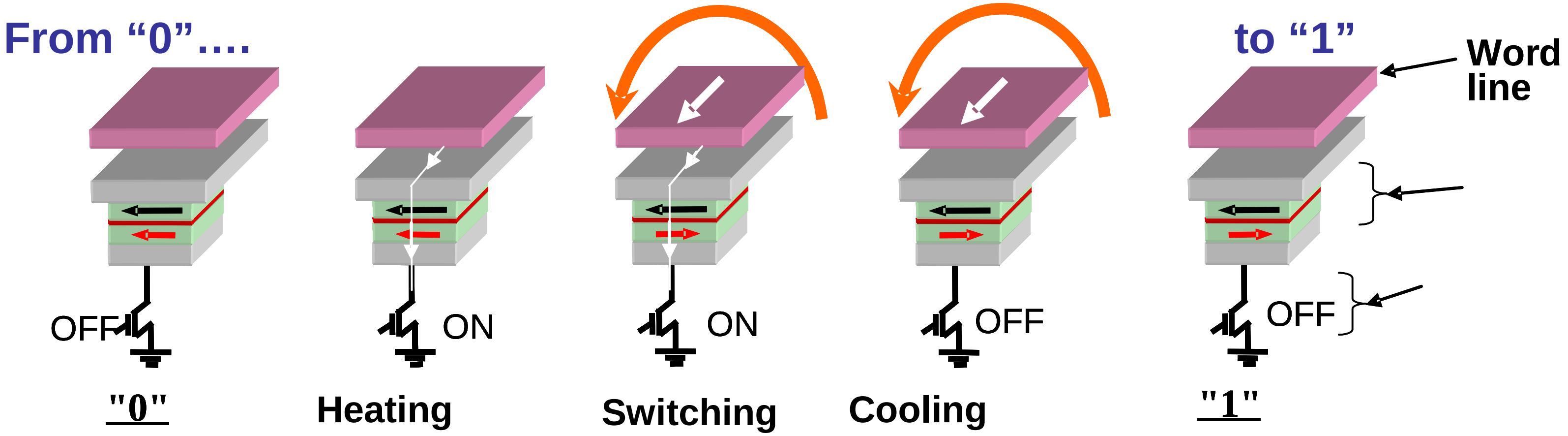
# Solution 2 : Thermally assisted MRAM

Very similar to Heat Assisted Magnetic Recording (HAMR)

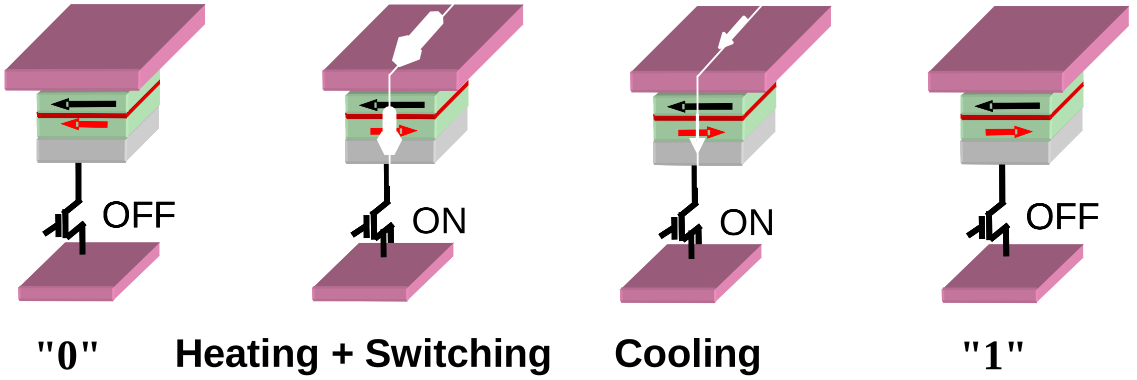
Write at elevated temperature (switching easier) – Store at room temperature

**In TA-MRAM: Heating by current flowing through the cell**

## Heating+ pulse of magnetic field:



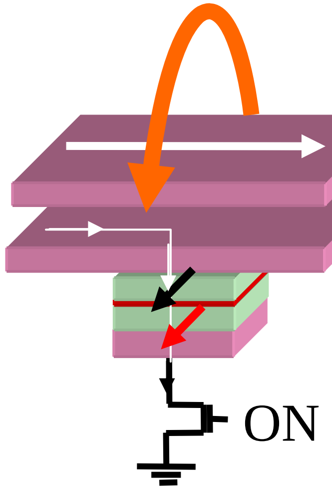
## Heating + STT:

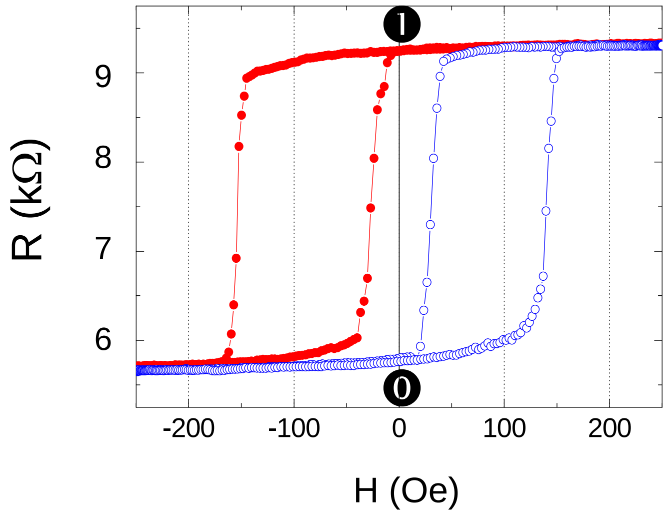


FR2832542 filed 16th Nov.2001, US6385082

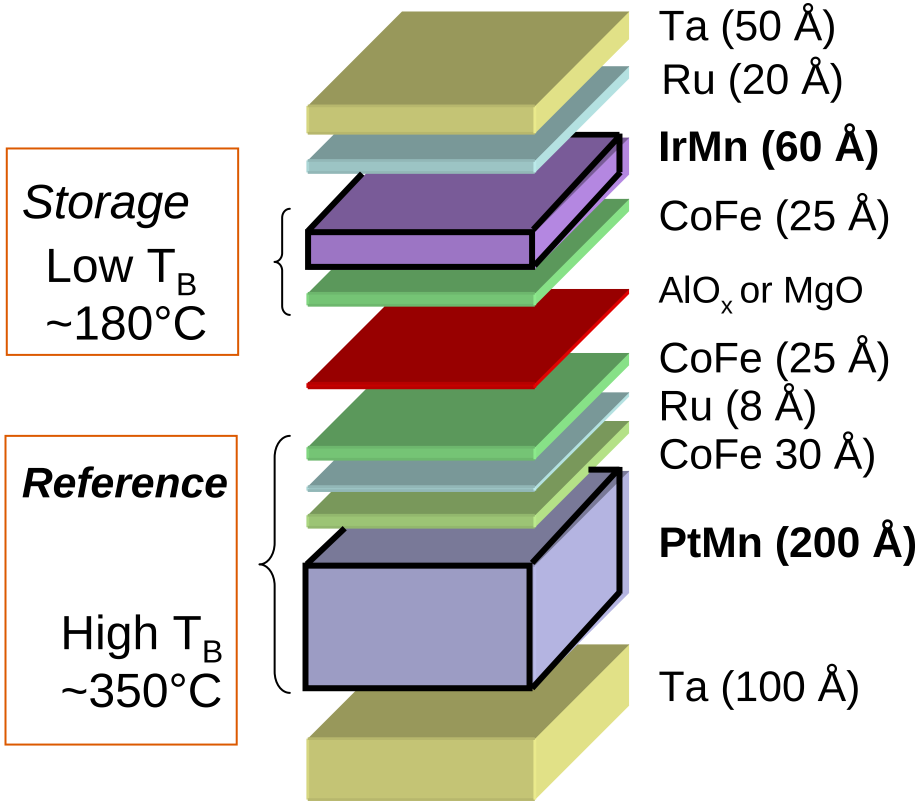
# Thermally assisted writing in TA-MRAM

**Heating**
**+**
**Field~2.5mT**



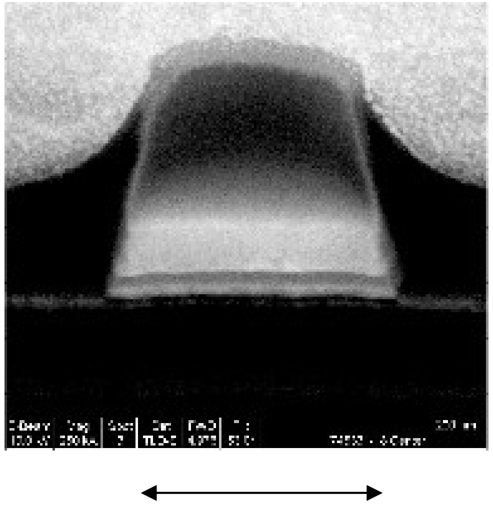


## Exchange biased storage layer



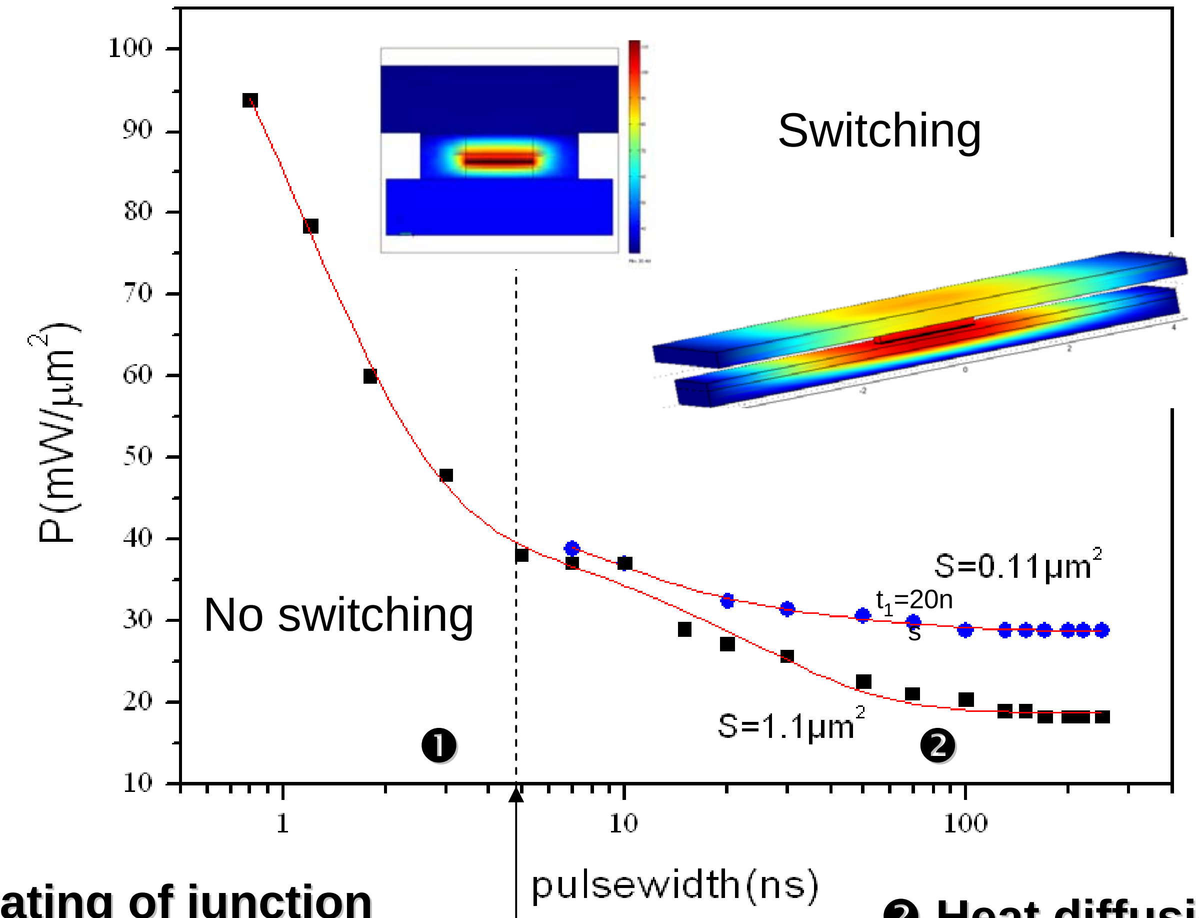
- heat the storage layer above the **low $T_B$**

# Heating Dynamics in TA-MRAM



MTJ pillar etched by RIE

CROCUS Technology
Blossoming Future



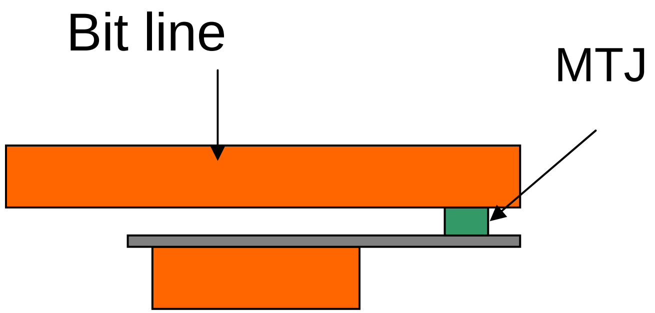
❶ **Adiabatic heating of junction**

$E_{write}=C\Delta T \Rightarrow P_{write}=C\Delta T/t$

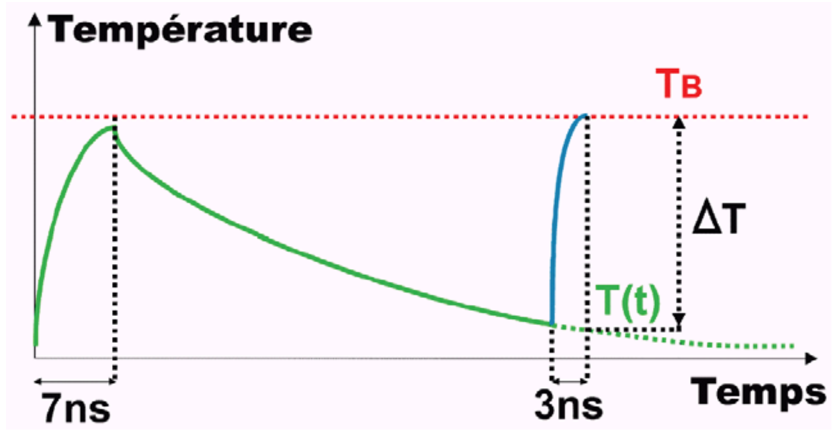
Best operating region
$J_{heating}\sim10^6 A/cm^2$

❷ **Heat diffusion towards the leads**

# Cooling dynamics in TA-MRAM

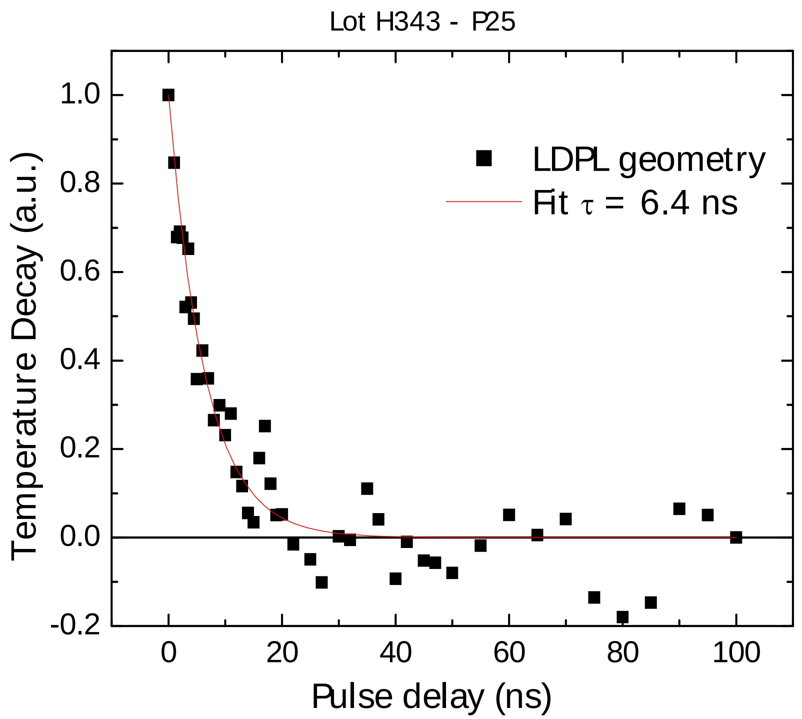


Double-pulse method for measuring cooling dynamics *(C.Papusoi, J.Hérault):*



**Pre-heating pulse**

**Probing pulse**

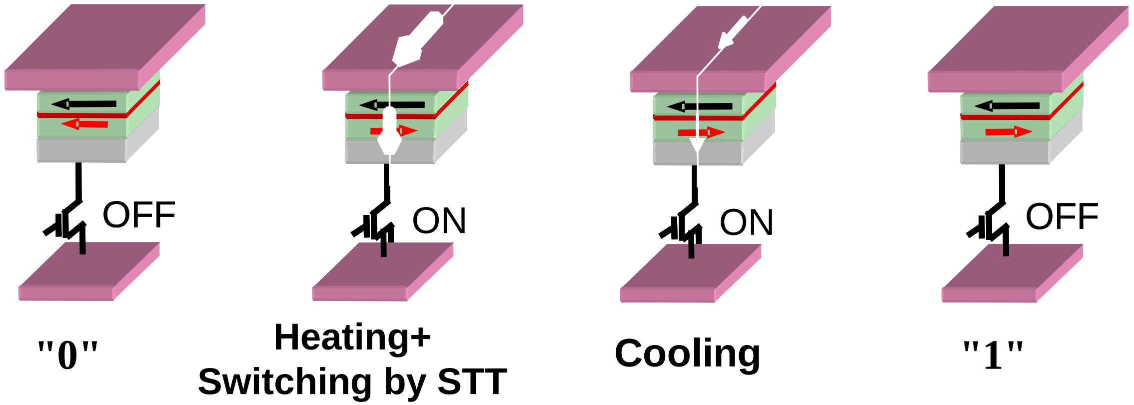


**Characteristic cooling time~15ns.**

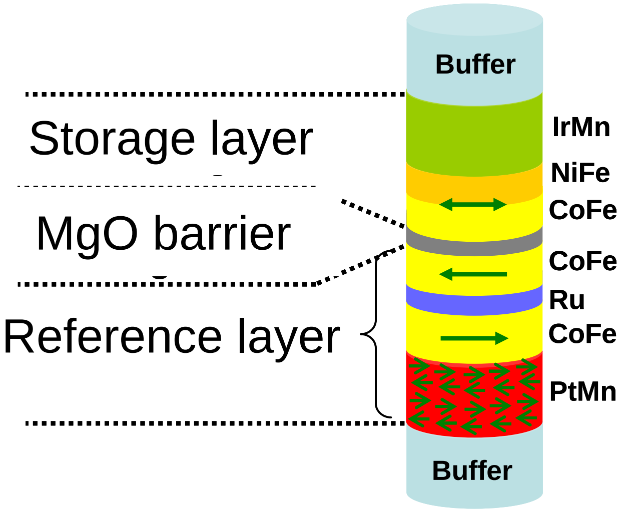
**TA-MRAM cycle time ~30ns**

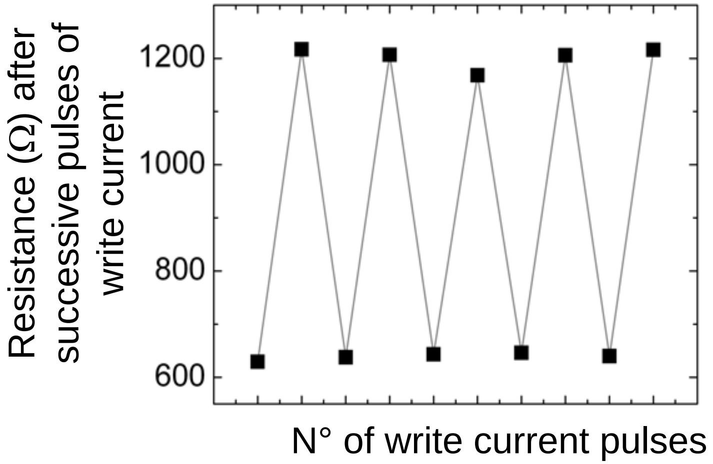
# Combining spin-transfer with thermally assisted writing

The same bipolar current flowing through the cell is used to both temporarily heat the cell and apply a spin transfer torque to switch the magnetization of the storage layer.



Experimental demonstration:





**Approach offering the ultimate scalability (sub-15nm cell-size possible) with stability of information over 10 years.**

# Scalability of TA-MRAM

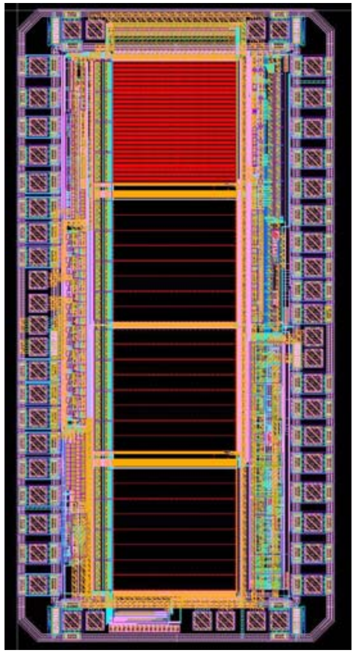
**Heating+ pulse of magnetic field~2.5mT:**

Scalability limited by electromigration in bit line (field generation) @ 40nm

**Heating+ STT:**

Same bipolar CPP current used to heat and switch;
No Physical limit in downscaling from magnetic point of view down to a few nm;

Can be implemented with :
-in-plane magnetized material (exchange biased storage layer)
-perpendicular-to-plane magnetized material (variation of $M_s$ or K with T)



*Layout of 1Mbit TA-MRAM demonstrator from Crocus Technology*

# Hybrid Magnetic/CMOS Integrated Electronics

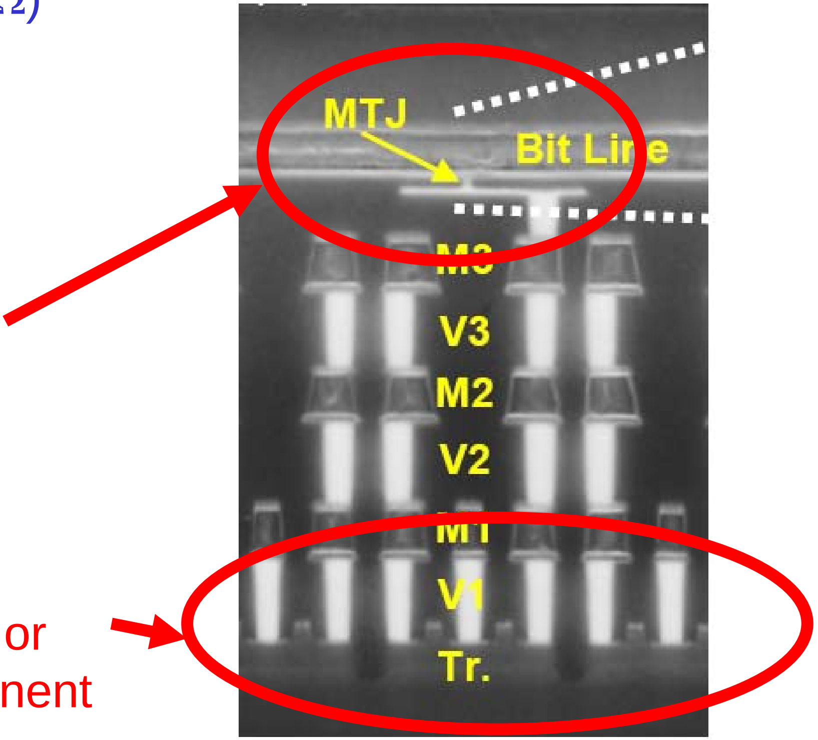
ERD-ITRS 2007:

> “*Nanodevices that implement* ***both logic and memory in the same device*** *would* ***revolutionize*** *circuit and nanoarchitecture implementation*”

Possible with CMOS/MTJ integration thanks to the unique set of qualities of MTJs:

- -Resistance compatible with CMOS (a few kΩ)
- -Above IC technology possible
- -Cyclability (>$10^{16}$ cycles for field writing)
- -Switching speed (~200ps-30ns)
- -High density possible
- -Thermal stability
- -Radiation hardness

**« Janus logic/memory components »**



Non-volatile MTJ memory element

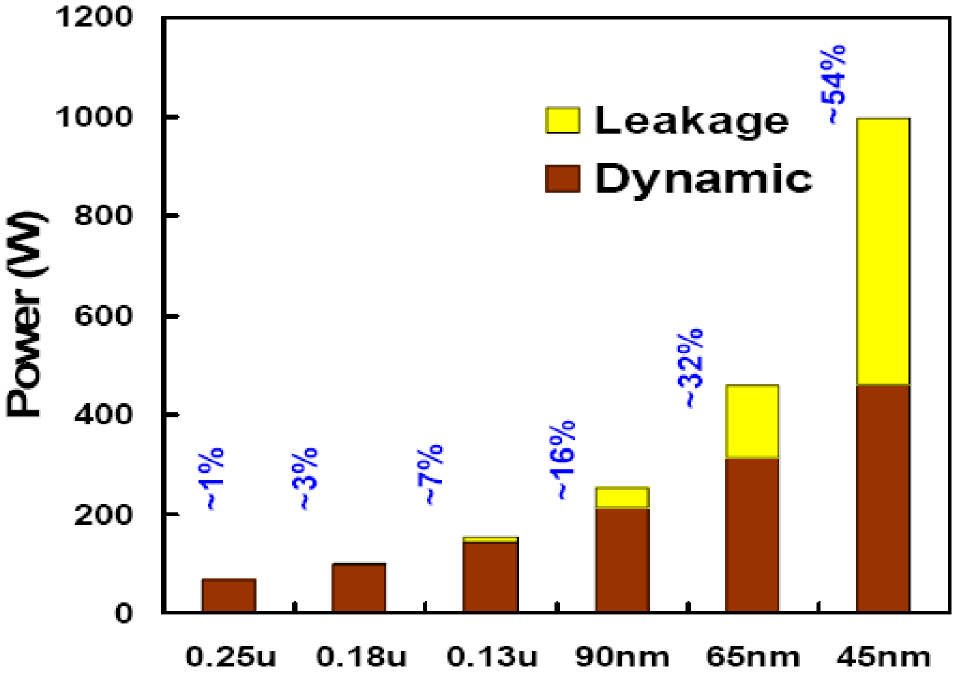
Simple MOSFET or CMOS logic component

# New hybrid CMOS/MTJ architectures for non-volatile logic

DRAM, SRAM: volatile. Cannot be switched off without loosing information.

However, increasing leakage current with downsizing (thinner gate oxide).

**Power consumption in CMOS electronic circuit per inch²**



Major benefit in introducing non-volatility in CMOS devices in terms of **energy savings**

# Non-volatile logic with ferroelectric RAM

Prototype of **non-volatile 8-bits CPU** developed by Rohm.

**Embedded FeRAM registers** to temporarily store the information;

Possibility to turn off power on the temporarily inactive parts of the processor => **50% gain in power consumption**

**Instant on restart**

However FeRam not fast enough and limited cyclability.

⇒Advantage of MTJ’s:
- Speed
- Cyclability (magnetic non-volatile flip-flops)

# Magnetic Full Adder (Hitachi, Tohoku University)

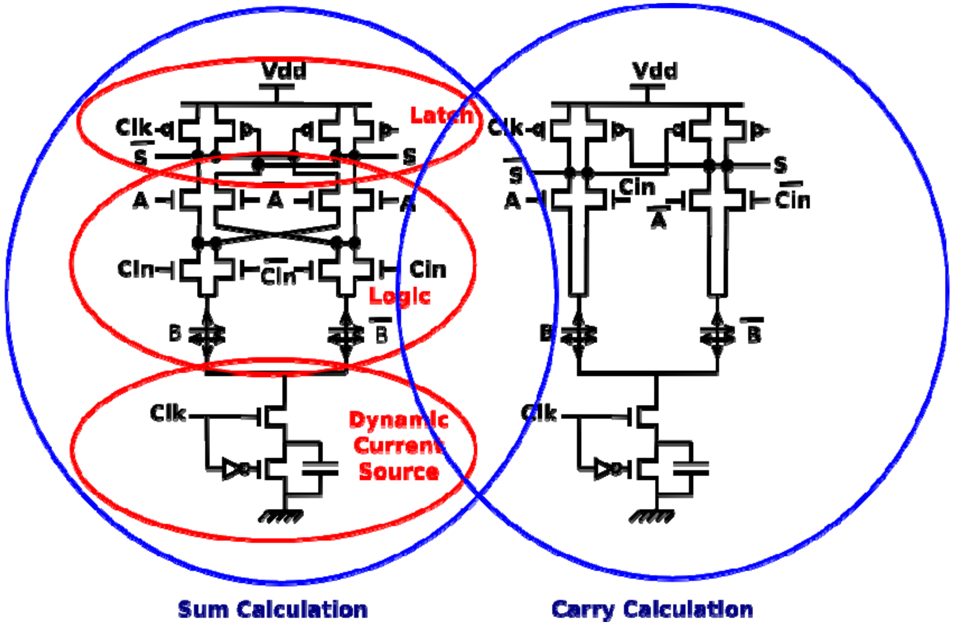
S.Matsunaga et al, *Applied Physics Express*, vol. 1, 2008.

- Based on

  Dynamic Current Mode Logic
    - Dynamic consumption reduction
    - Footprint reduction

  MTJs
    - One input is made non-volatile (instant startup, security)
    - Drastic static consumption reduction
    - Footprint reduction
- Demonstrator : CMOS 0.18µm,
- MTJs size: 200X100nm²

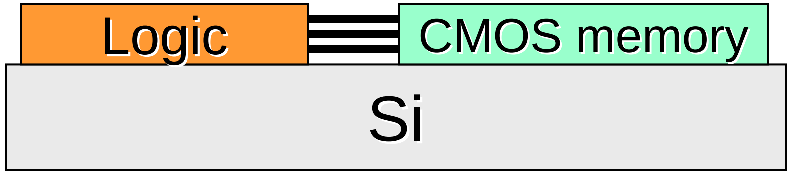
| | CMOS | Hybrid |
|---|---|---|
| Delay | 224 ps | 219 ps |
| Dynamic Power | 71.1 µW | 16.3 µW |
| Writing Time | 2 ns/bit | 10 (2) ns/bit |
| Writing Energy | 4 pJ/bit | 20.9 (6.8) pJ/bit |
| Standby Power | 0,9 nW | 0 nW |
| Surface | 333 µm² | 315 µm² |

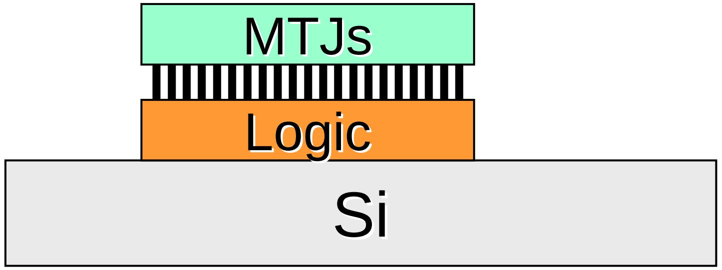


# Tighter integration between logic and memory

**Same technology as for MRAM**

**Benefit from "Above IC" technology**





**With CMOS technology only:**

-Slow communication between logic and memory
-few long interconnections
-complexity of interconnecting paths
-larger occupancy on wafer

**With hybrid CMOS/magnetic:**

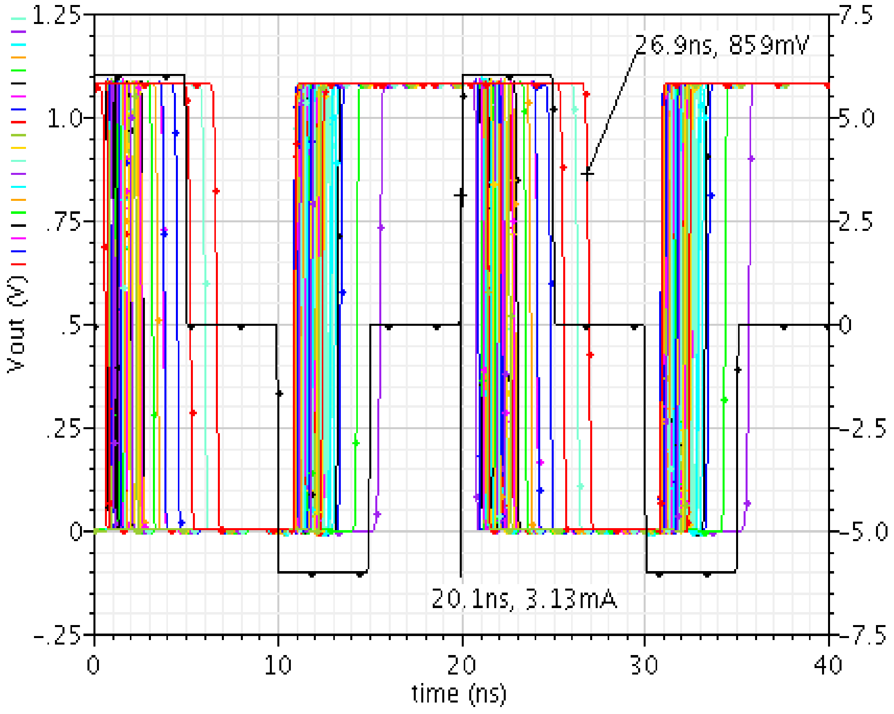
-Non-volatility in logic
-Large energy saving
-Fast communication between logic and memory
-Numerous short vias
-Simpler interconnection paths
-Smaller occupancy on wafer

**New paradigm for architecture of complex electronic circuit (microprocessors...)**

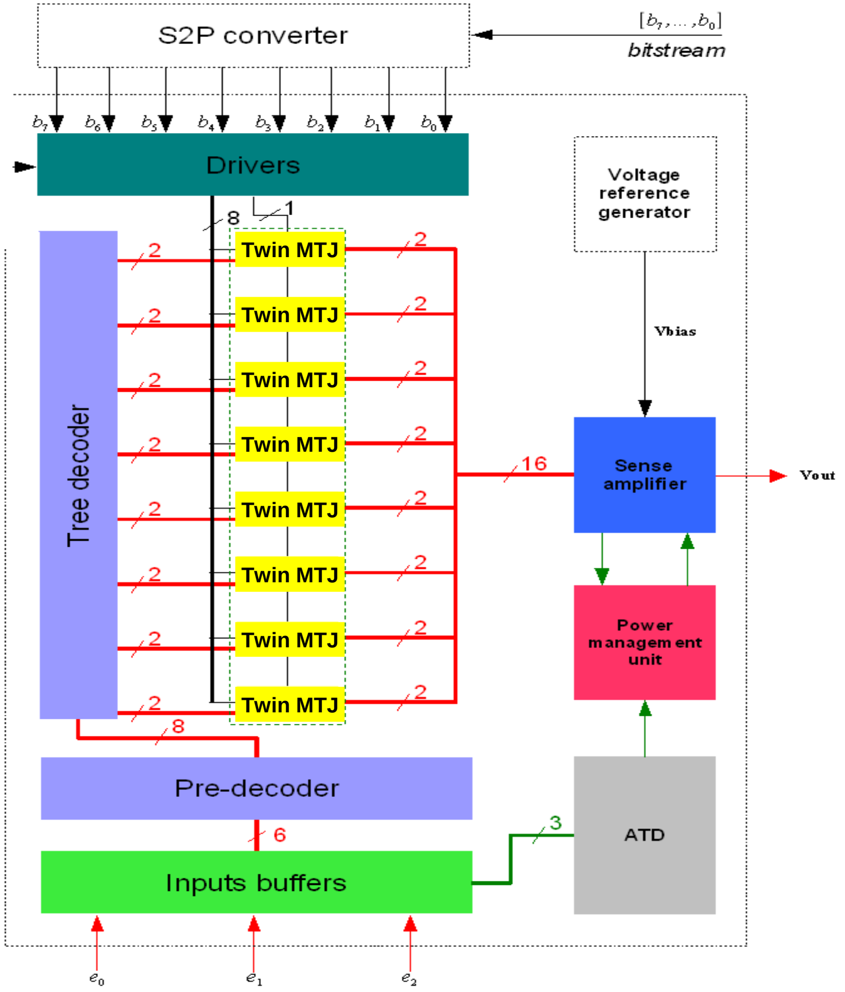
# Reprogrammable hybrid CMOS/MTJ logic gates

MTJ used as variable resistances to change the switching threshold of CMOS components

## Simulations of reprogrammability taking into account CMOS and magnetic process variations

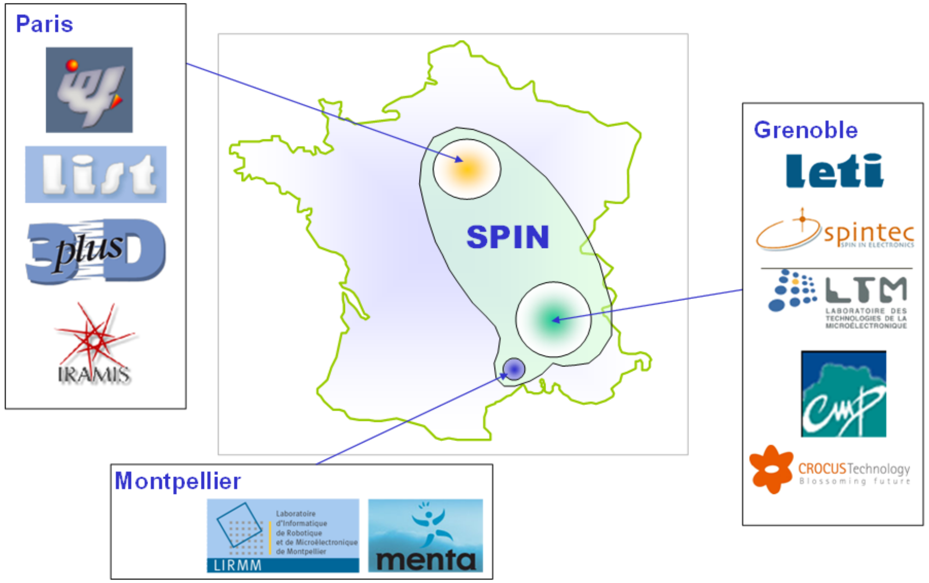


Extremelly fast reprogrammation

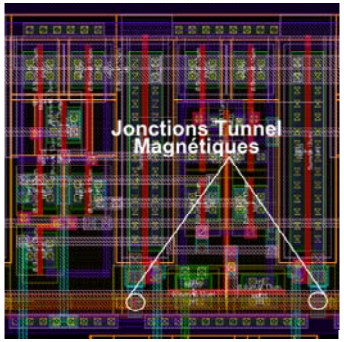


# Examples of CMOS/magnetic integrated circuits

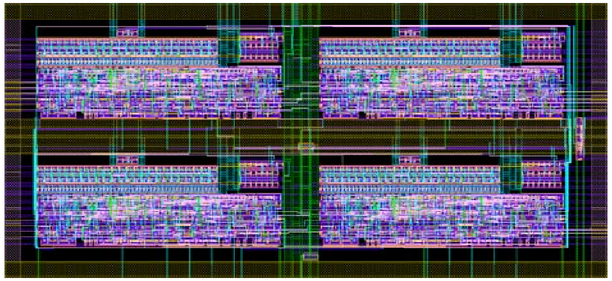
French consortium:



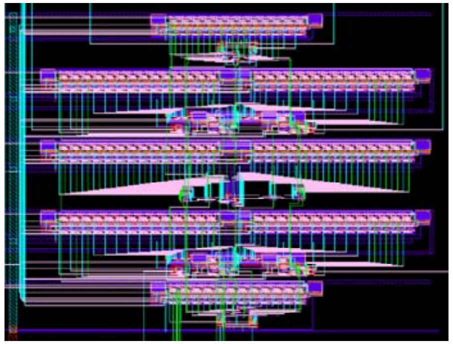
Non-volatile flip-flop



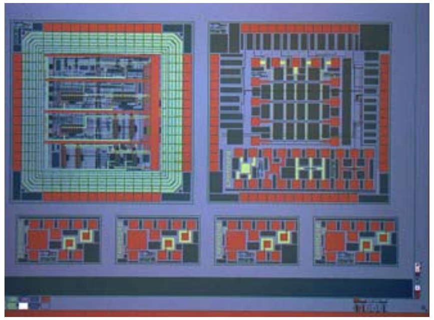
Magnetic FPGA

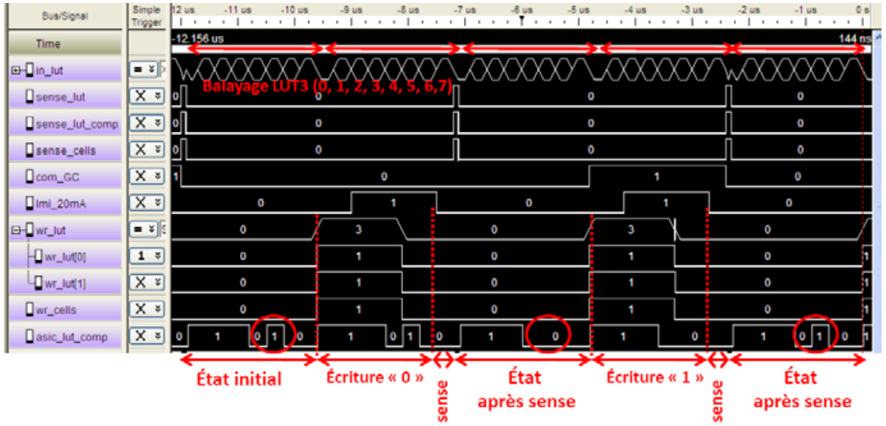


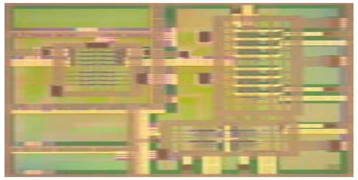
Arithmetic Logic Units

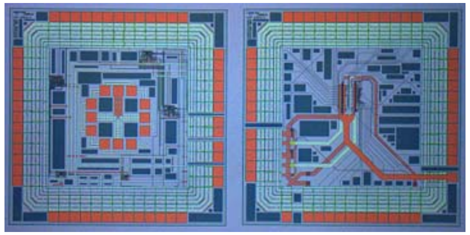


Magnetic look up table



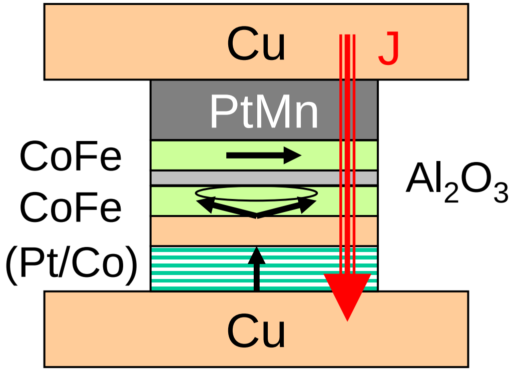


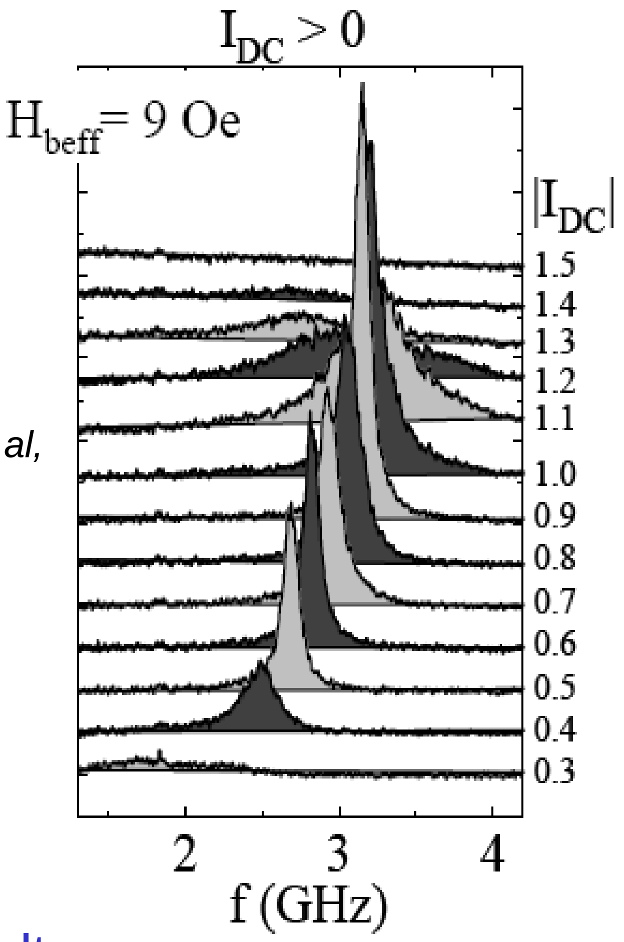




# RF components based on spin transfer

RF oscillator with perpendicular polarizer:





*D.Houssamedine et al, Nat.Mat 2007*

Injection of electrons with out-of-plane spins;
Steady precession of the magnetization
of the soft layer adjacent to the tunnel barrier.

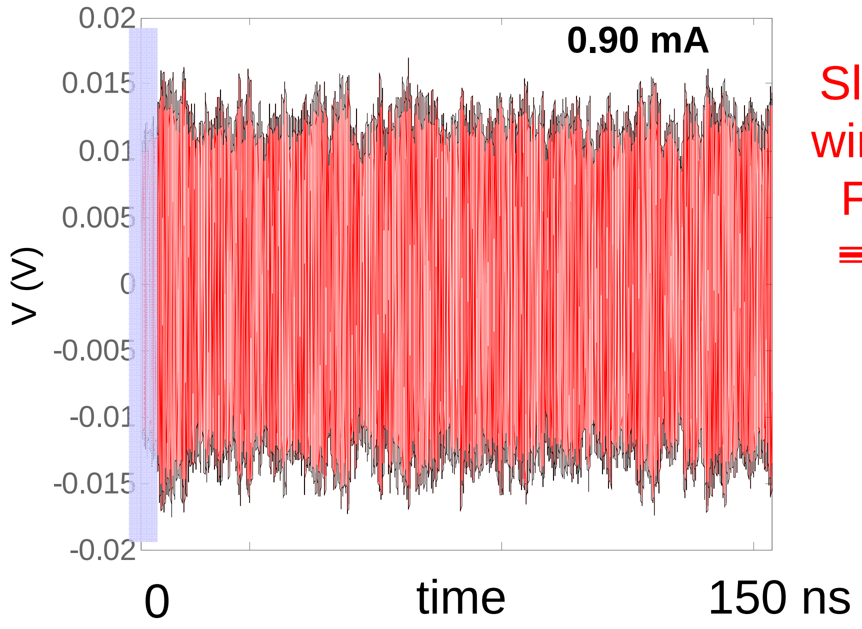
Precession (2GHz-40GHz) + Tunnel MR ⇒ RF voltage
Interesting for frequency tunable RF oscillators ⇒ Radio opportunism

(SPINTEC patent + Lee et al, Appl.Phys.Lett.86, 022505 (2005) )

# Spin-transfer RF oscillators: linewidth and phase noise

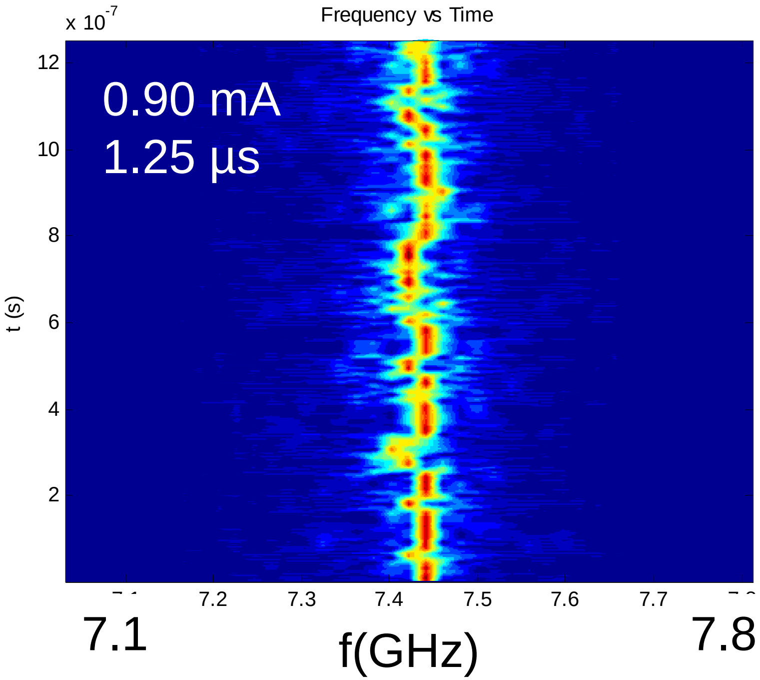
Still too large for practical applications but steady progress thanks to optimization of stack composition and shape

*Time domain measurement*



Sliding window FFT

*Time evolution of spectrum*



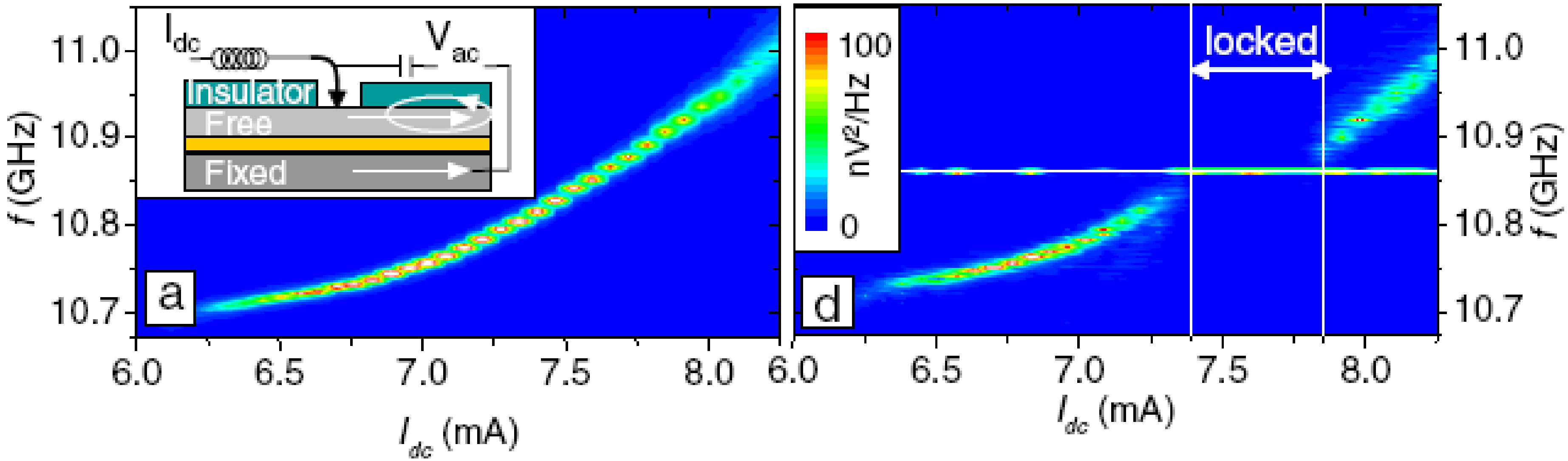
Influence of thermal fluctuations on magnetization dynamics and pillar edge modes

Increasing magnetic volume of oscillator, locking of several oscillators, locking on external source, feedback with PLL…

# RF components based on spin transfer (cont'd)

Phase locking phenomenon: **<u>Locking on an external source</u>**

CoFe 20nm (fixed)/Cu 4nm/NiFe 5nm (free)



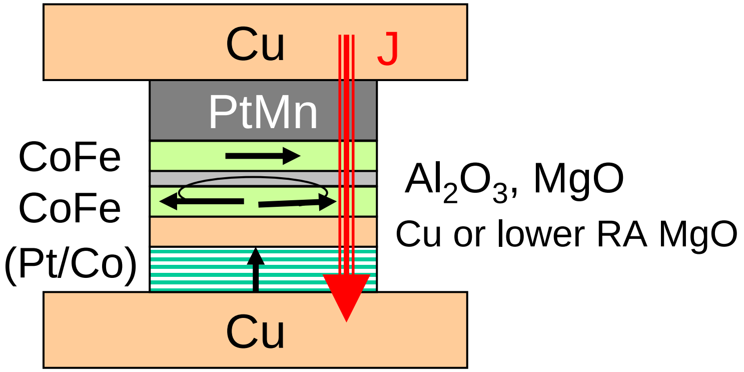
DC current, no AC drive

$I_{DC}+I_{AC}$ 10.86GHz 410μA RMS

*Rippard et al, PRB70, 100406 (2004)*

# Precessional switching in MRAM cell with perpendicular polarizer

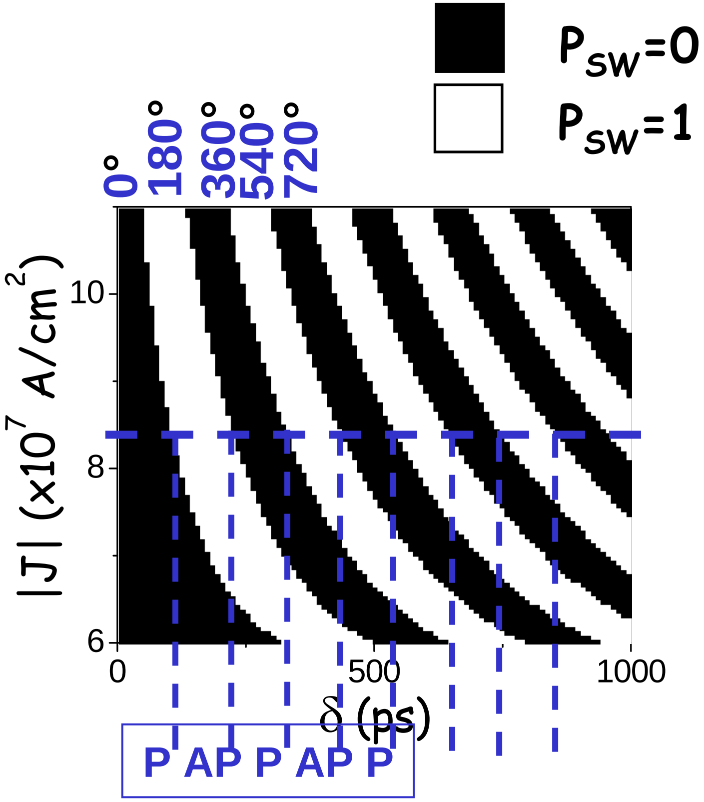
**MRAM cell:**
**planar MTJ+perpendicular polarizer**



**Switching by monopolar pulse of current of duration ~half precession period (30ps-300ps)**

Macrospin LLG calculation at 0K assuming STT from perpendicular polarizer only.

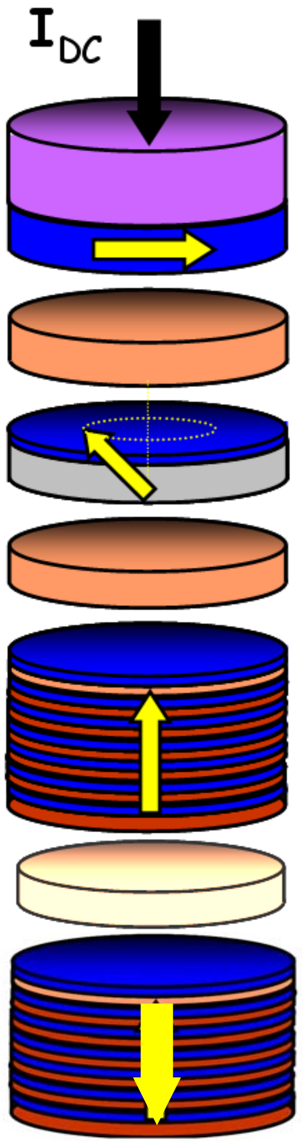
*70nm*140nm elliptical , CoFe 3nm*



**Same pulse duration for P⇒AP and AP⇒ P**

# Precessional STT-switching

After stack optimization:



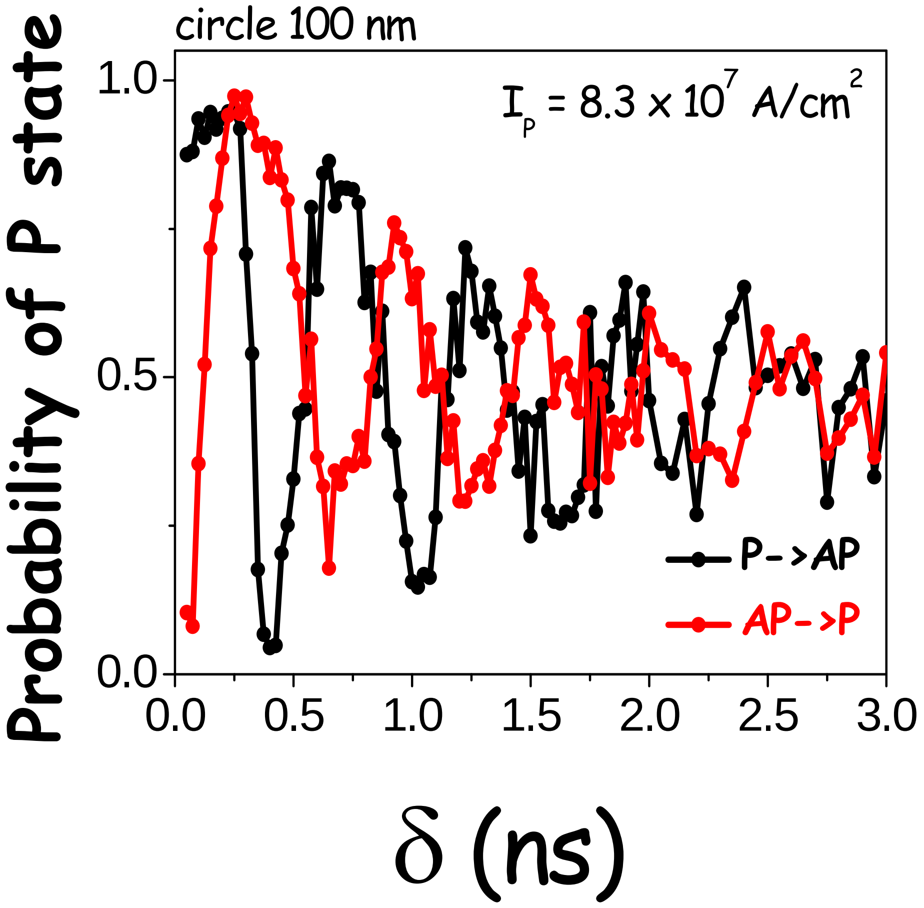
In-plane analyzer
(Co/IrMn)

Metallic spacer (Cu)

Free layer (NiFe
3/Co0.5nm)

Metallic spacer (Cu)

Perpendicular polarizer
(Pt/[Co/Pt]$_n$/Co/Cu/Co)



Ultrafast deterministic switching.

Interesting for MRAM or logic

# Conclusion

- GMR discovery has triggered the development of spin-electronics.

  Played a key role in magnetic recording and other sensor applications;
- Spin-valve magnetic concept (free/pinned by exchange anisotropy) also used in MTJ ⇒ Spin engineering;
- Spin-transfer offers a new way to manipulate the magnetization of magnetic nanostructures (switching, steady excitations);
- For CMOS/magnetic integration, MTJ offers more suitable impedance ~ few kΩ and larger magnetoresistance than GMR;
- Increasing interest for MRAM in microelectronics industry;
- Besides MRAM, CMOS/MTJ integration quite interesting for logic, reprogrammable logic, innovative architecture;
- Frequency tunable RF oscillators interesting for wireless communications, RF interconnects, microwave assisted magnetic recording.

# Conclusion (cont'd)

Other more basic areas of spinelectronics are being investigated not covered in this presentation:

- Domain wall manipulation by current;
- Spin currents without charge current;
- Spin Hall effect, inverse Spin Hall effect;
- Spincaloritronics;
- Magnetic semiconductors, spintronics with semiconductors;
- Half metallic materials
- Multiferroïcs
- Spin-injection in semiconductors, spin-collect, spin-manipulation by Rashba effect;
- Graphene and Carbone nanotube spintronics;
- Spintronics with topological insulators

Certainly more to come…

# Thank you !