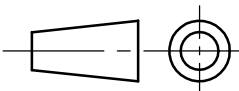


<b>Matière:</b> PCB		<b>Epais</b> 3,2	<b>Traitement:</b>	H:11 js:13 h:11 lrg:3,2	<b>Date :</b> 30/01/2008	<b>Dessiné par :</b> RIALLOT	
<b>Ech :</b> 1	<b>Qté :</b> 1	<b>Cote mécanique</b>	X	<b>Face</b>	<b>Modifié le:</b> / /	<b>Etat:</b> R	
		<b>Cote piste</b>		<b>Double</b>			X
		<b>Dessus (Top)</b>		<b>Simple</b>			
		<b>Dessous (bottom)</b>					
 <b>Titre : PCB test</b>							
<b>Solid Edge</b> EDS PLM Solutions		Document <b>LPTPC/2000003</b>				<b>Plan:</b> 1/1	
		<b>C.E.A / SACLAY / DAPNIA / SEDI</b>					

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