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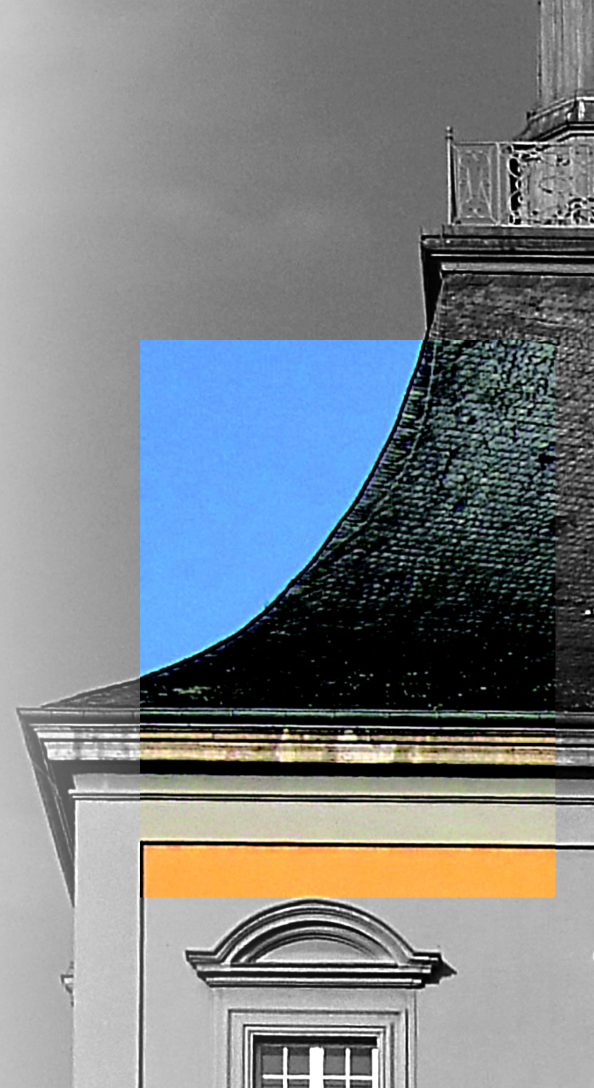
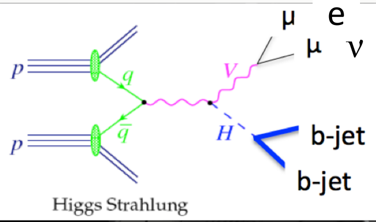
SI LAB Silizium Labor Bonn

MONOLITHIC CMOS PIXELS FOR LHC TRACKERS

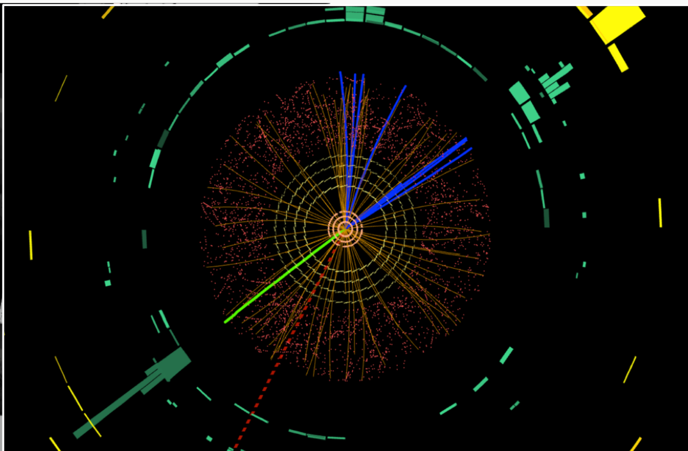


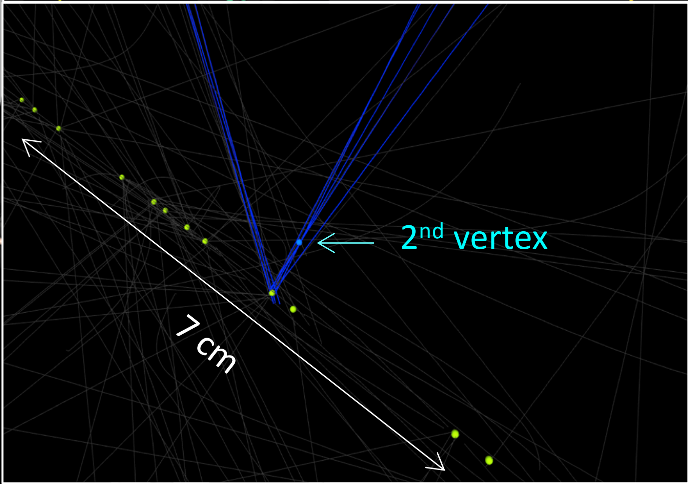
NORBERT WERMES (UNIVERSITY OF BONN)

IRFU, Paris-Sud, 26.11.2018



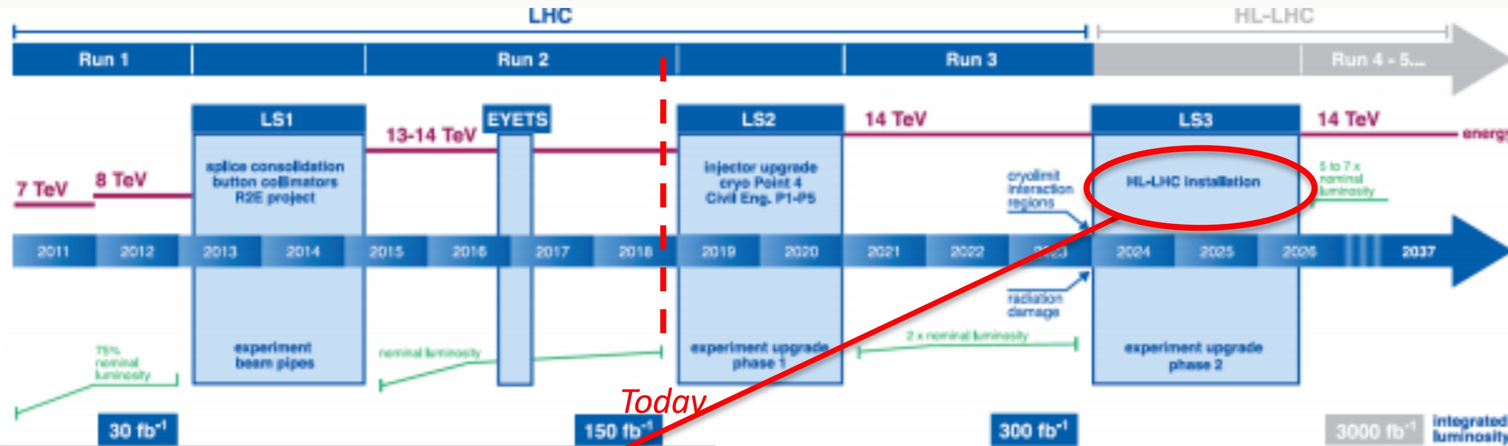
ATLAS EXPERIMENT
Run: 204442
Event: 3121233
2012-06-05 06:52:59 CEST

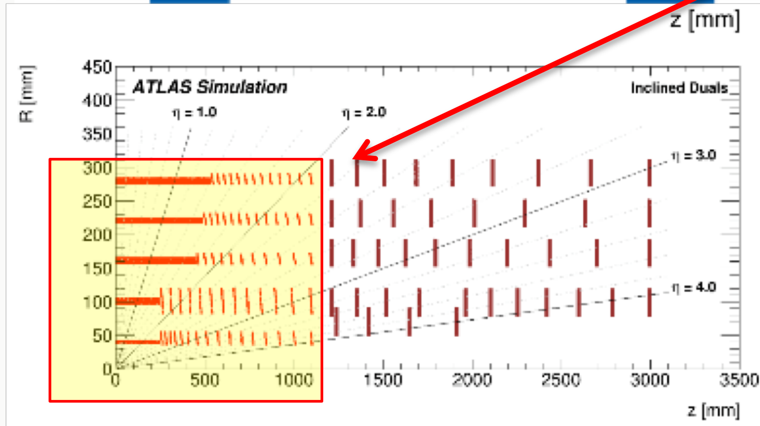




22 collisions piling up

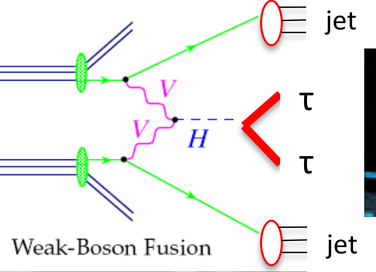
TRACKER UPGRADES @ LHC





- **2024/25: Phase 2 ATLAS** ATLAS completely replaces its trackers
- ~ 160 m^2 silicon strips
- ~10 m^2 silicon pixels (currently $2m^2$)

What does this mean?



200 pile-up events
simulation for 2026

CMS (Run 1) ... real collisions

78 interactions
piling up in
one collision

~9 cm (2σ)

ENVIRONMENT AT THE HL-LHC (PP)

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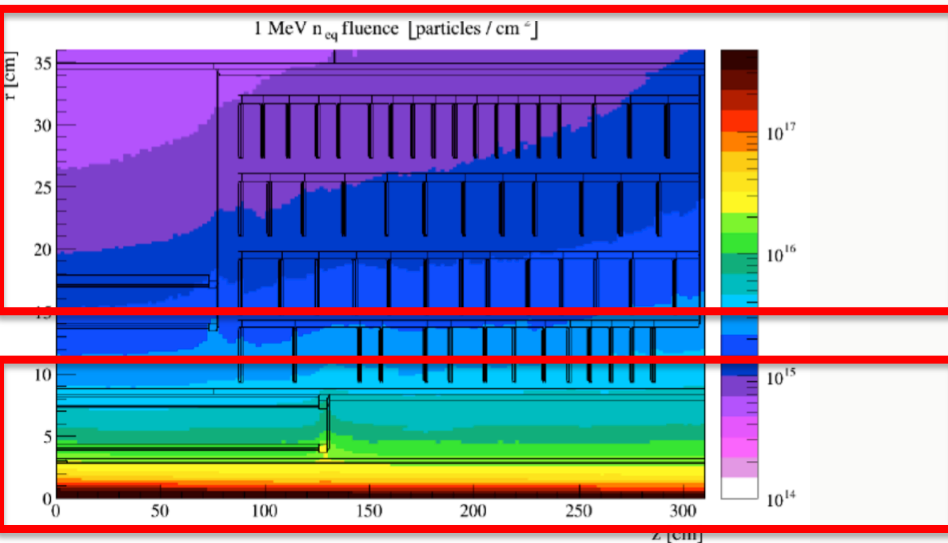
Solution: pixels as much as possible / affordable / buildable in time

Radiation levels, hit rates and bunch structure in the tracker dominate the development of sensors and front-end electronics

25ns bunch crossing

L1 trigger rate (e.g. ATLAS 4 MHz)



Strip layers

- NIEL ≈ 10^{14} n_{eq}/cm^2
- TID ≈ 10Mrad
- rate ≈ 30 MHz / cm^2
- Larger area O(100m^2)

Outer pixel layers

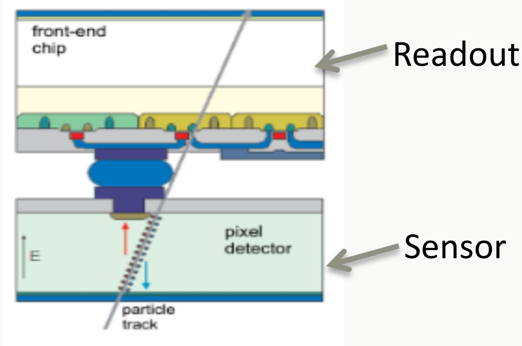
- NIEL ≈ 10^{15} n_{eq}/cm^2
- TID ≈ 100 Mrad
- rate ≈ 300 MHz / cm^2
- Larger area O(10m^2)

Inner layers

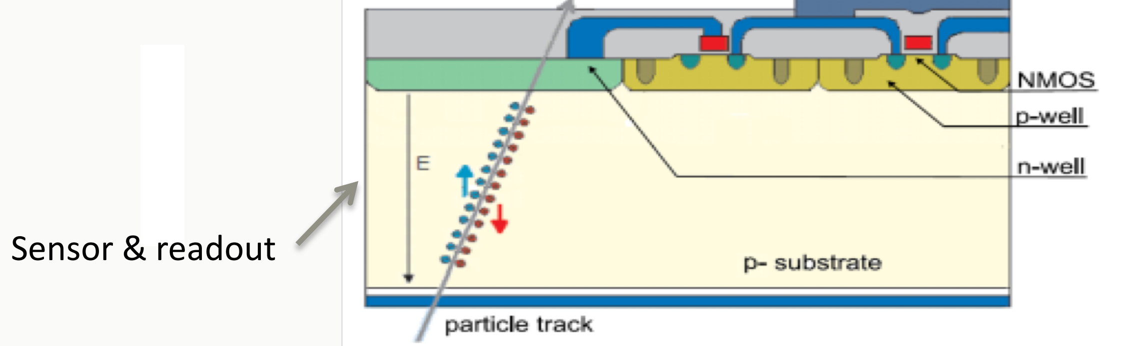
- NIEL ≈ 5x10^{15} to 10^{16} n_{eq}/cm^2
- TID ≈ 1Grad
- rate ≈ 3-4 GHz / cm^2
- Smaller area O(1m^2)

INTRODUCING DMAPS

Hybrid detector



Depleted monolithic active pixel sensor (CMOS)



No need for fine pitch bump bonding between sensor and readout circuitry.

→ **Easier to produce**

→ Large cost reduction (sensor + R/O chip + BB → one chip)

→ Plus all advantages that large CMOS Fabs may offer, including fast turn around, large wafer sizes, large throughput

CMOS PIXEL DETECTORS

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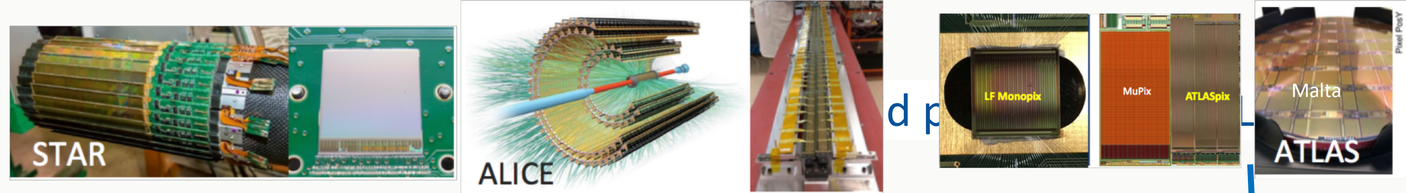

	STAR	ALICE-LHC	ILC	ATLAS-HL-LHC	
				Outer	Inner
Time resolution [ns]	110	20 000	350	25	25
Particle Rate [kHz / mm²]	4	10	250	1000	10 000
Fluence [n_{eq} / cm²]	> 10^{12}	> 10^{13}	10^{12}	10^{15}	2 x 10^{16}
Ion. Dose [MRad]	0.2	0.7	0.4	50	> 1000

MAPS (ALPIDE)

Radiation-hard DMAPS or hybrid (L4)

need: radhard (TID & NIEL) + fast response time + fast readout => Q coll. by drift & full R/O architecture

WHAT IS NEEDED TO REALISE (RADHARD) DEPLETED CMOS PIXELS?

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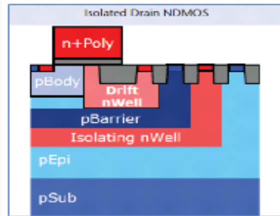
$$d \sim \sqrt{\rho \cdot V}$$

1 **“High” Voltage add-ons to apply 50 – 200 V bias**

I. Peric, DOI: 10.1016/j.nima.2007.07.115

2 **“High” Resistivity Substrate Wafers (100 Ωcm – kΩ cm)**



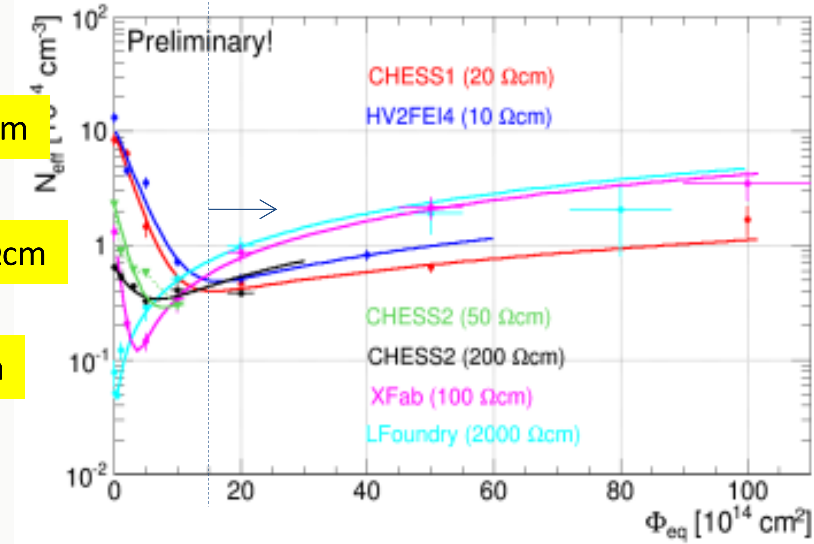
from: www.xfab.com

3 **Multiple (3-4) nested wells (for shielding and full CMOS)**

~10 Ωcm

~100 Ωcm

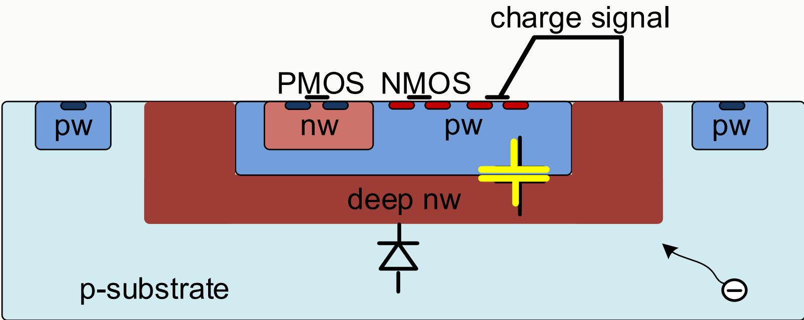
kΩcm

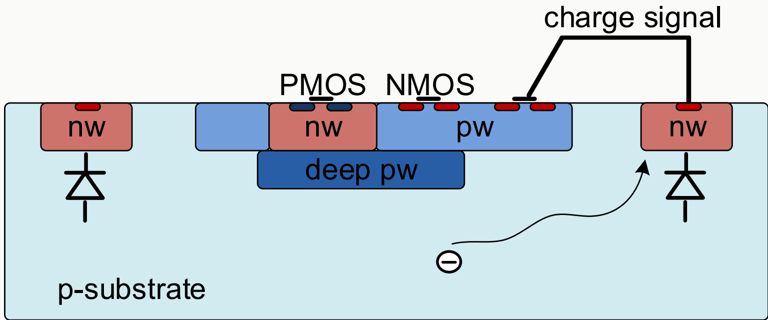


I. Mandic et al., JINST 12 (2017) no.02, P02021

4 **Backside Processing (for thinning and back bias contact)**

LARGE VERSUS SMALL COLLECTION ELECTRODE (FILL FACTOR)





Electronics **inside** charge collection well

- **large fill factor** (better: large collection electrode)
  → no low field regions
  → on average **short(er) drift** distances
  → less trapping -> **radiation hard**
- **Larger (100 fF)** sensor **capacitance**
- **additional well-well capacitance** (~100 fF)
  → noise & speed/power penalties
  → possible x-talk (digital to sensor)

$$\tau_{CSA} \approx \frac{1}{g_m}\frac{C}{C_f}$$

$$ENC^2_{\text{thermal}} \approx \frac{4}{3}\frac{kT}{g_m}\frac{C}{\tau_f}$$

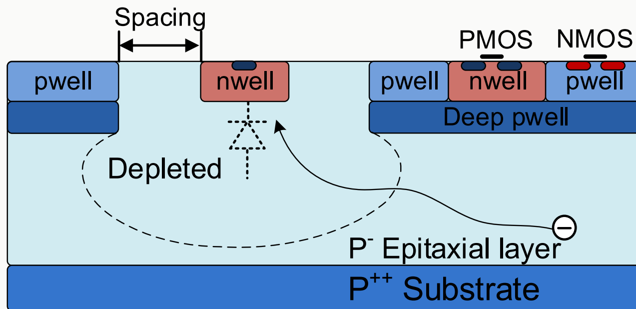
power

Electronics **outside** charge collection well

- **small fill factor**
  → **very small sensor capacitance (< 5fF)**
  → noise low, speed high, power low
- on average longer drift distances and low field regions possible
  → **radhard hardness needs technology "improvements"**

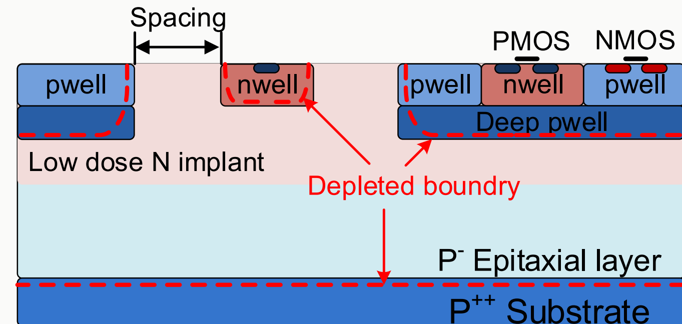
$$\frac{S}{N} \approx \frac{Q/C}{\sqrt{g_m}} \sim \frac{Q/C}{\sqrt[n]{P}} \Rightarrow P \sim \left(\frac{C}{Q}\right)^m$$

E.G. PROCESS MODIFICATION – TOWERJAZZ 180 NM CMOS



Standard process

- **ALICE ITS type**
- **High res.** **p**-type epi. (> 1 kΩ·cm)
  => thickness typ. **25 µm**
- Quadruple-well
  => deep pwell shields nwell => **full CMOS**
- **Reverse bias** typ. -6V
  => enhanced (but not yet full) depletion
  => some charge collected by diffusion only => slow



Modified process

- Additional planar medium dose **N implant**
  => depletion from two junction boundarie
  full volume can be depleted
  better charge collection in lateral direction
- Maintain small capacitance
- No significant circuit/layout changes

W. Snoeys et al. DOI: 10.1016/j.nima.2017.07.046

FOUNDRIES THAT HAVE BEEN CONSIDERED

feature sizes ≥ 130 nm

LARGE INTEREST IN DEPLETED CMOS PIXELS

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design

groups

UNIVERSITÀ DEGLI STUDI DI MILANO

AMS/TSI

- KIT/Heidelberg
- Geneva
- Liverpool IFAE

Large Fill factor

LF	TJ
Bonn CEA/IRFU	CERN CPPM
Large Fill factor	Small Fill factor

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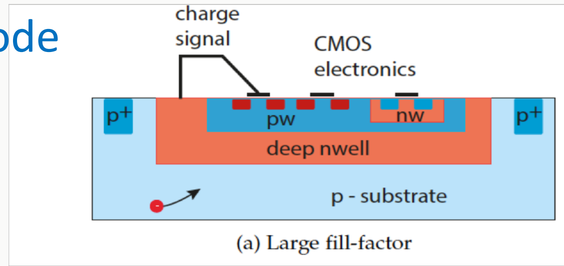
Different electrode (large/small) approaches lead to different

DMAPS

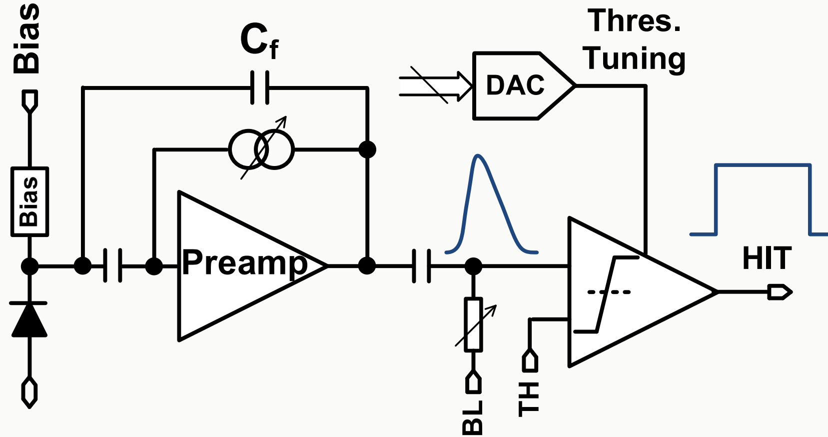
ANALOG FRONT END CHOICES

ANALOG FRONT-ENDS - CSA VS. VOLTAGE AMPLIFIER

- large electrode



(a) Large fill-factor



Charge Sensitive Amplifier

- Used for large electrode design
- Gain (ideally) independent of C_D

  => G ~ $1/C_f$ (typ. C_f ~ fF)

- $\tau_{CSA} \propto \frac{C_D}{g_m \cdot C_f}$, $ENC^2{}_{therm} \propto \frac{kT}{g_m} \frac{C_D^2}{\tau}$

  => need larger g_m (power) for large C_D

  => typ. power 20 – 40 µW per pixel

- In-pixel threshold tuning needed

ANALOG FRONT-ENDS - CSA VS. VOLTAGE AMPLIFIER

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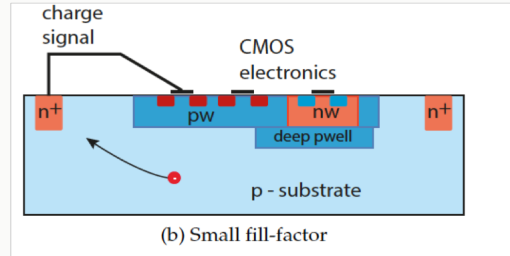
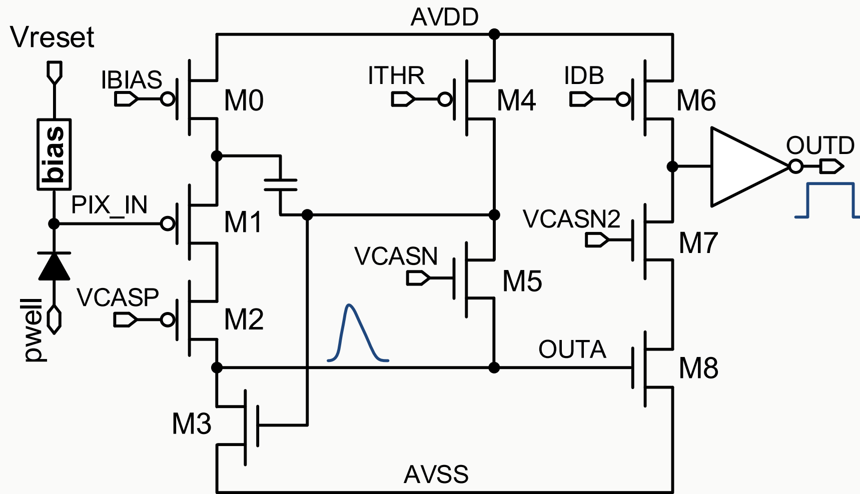
- small electrode



(b) Small fill-factor



D. Kim et al., doi 10.1088/1748-0221/11/02/C02042

Voltage amplifier (ALPIDE like)

- => Profit from small sensor capacitance
  => large voltage signal @ input node
- Very compact design
  => amplification + shaping in one stage
  => simple inverter as discriminator
  => no threshold trimming (in ALPIDE)
- Optimized power for required timing
  => ~1 µW/pixel for 25 ns peaking time

DEVELOPMENT LINES: LARGE ELECTRODE

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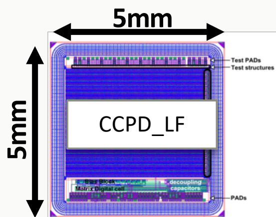
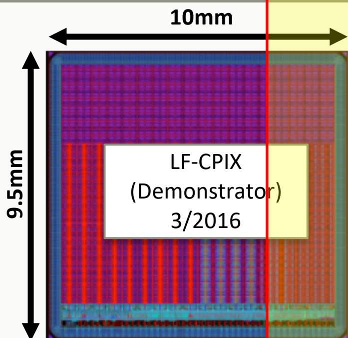
LFoundry

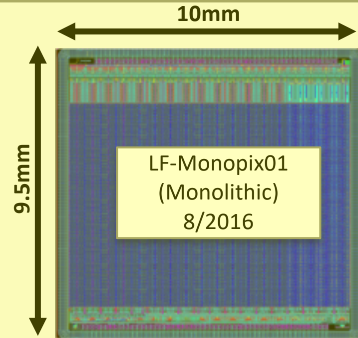


small **prototypes**



full size **demonstrator** bondable to FE-I4

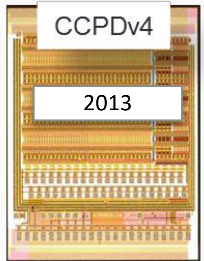
big step

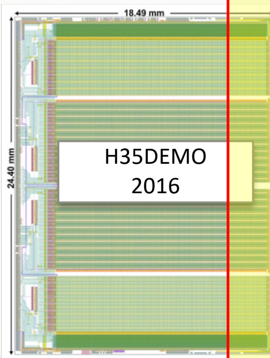


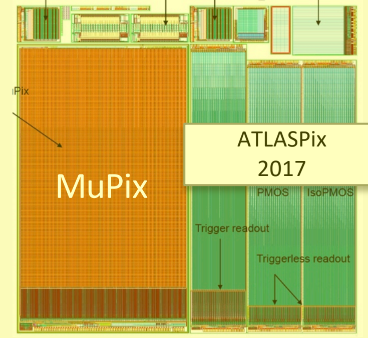
fully monolithic version with R/O architecture

Full RD53B compatible system chip

AMS







DMAPS

READOUT ARCHITECTURE CHOICES

needed

- Small pixels
- High logic (memory) density
- Fast shaping
- High data transmission bandwidth

DMAPS: COLUMN DRAIN ARCHITECTURE

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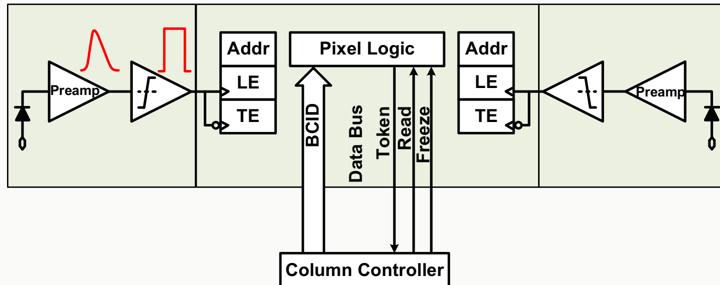
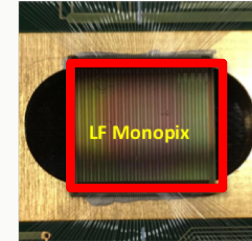
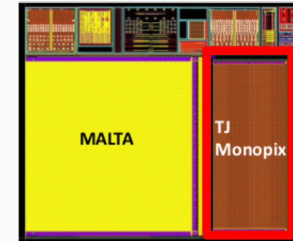
DMAPS with synchronous readout => time stamping in matrix





- Well established scheme in ATLAS – FE-I3 like (current pixel detector)
  => sufficient rate capability for ITk outer pixel layers
- Time reference (BCID) distributed in the matrix (small skew req.)
- ToA & ToT recorded in pixel
- Hits read out following a token passing scheme on shared column bus
- In-pixel memories and digital R/O logic

  challenges: prevent digital cross talk, pixel size, C_D (for large electrode design)

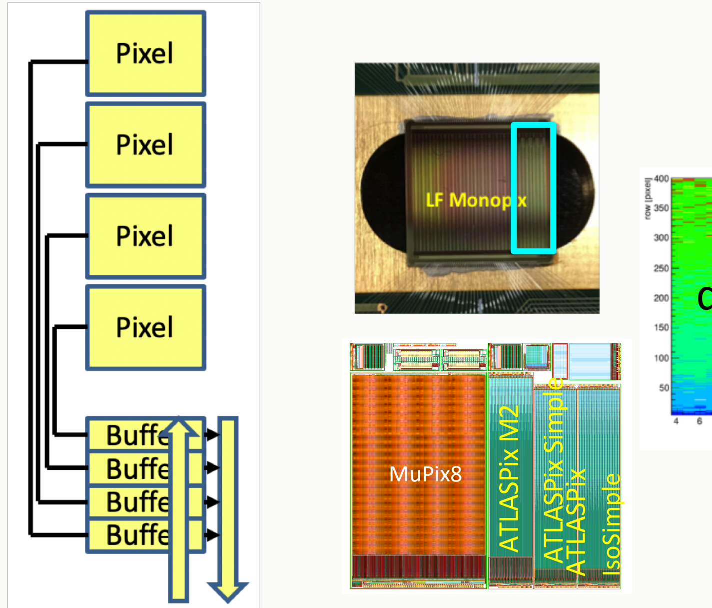


ASYNCHRONOUS READOUT SCHEMES

DMAPS with asynchronous matrix => time stamping at periphery

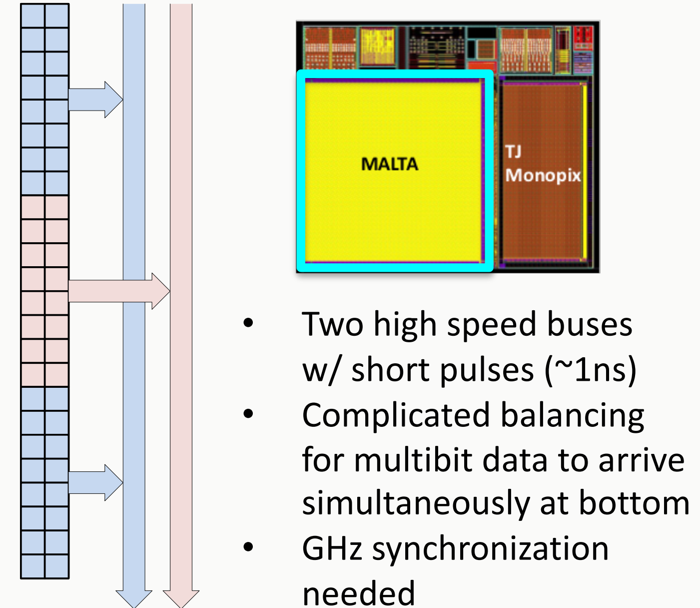
=> Hits transferred to periphery immediately => calls for massive parallelism

A) One to one connection



400 lines in two metal layers; larger periphery

B) Shared bus by pixel groups



- Two high speed buses w/ short pulses (~1ns)
- Complicated balancing for multibit data to arrive simultaneously at bottom
- GHz synchronization needed

- Challenge: avoid data collisions

LARGE (~1 CM^2) FULL CMOS CHIPS (=MODULES) W/ READOUT

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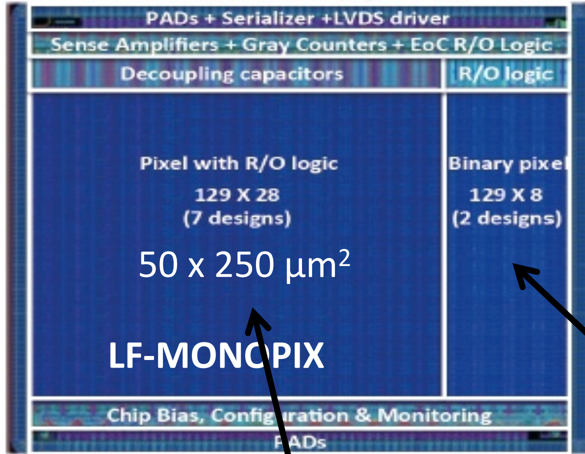
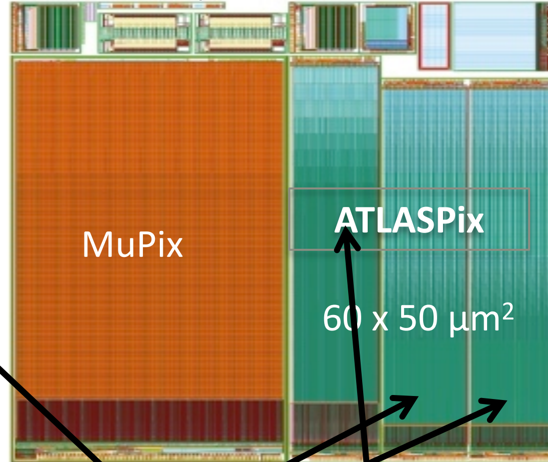
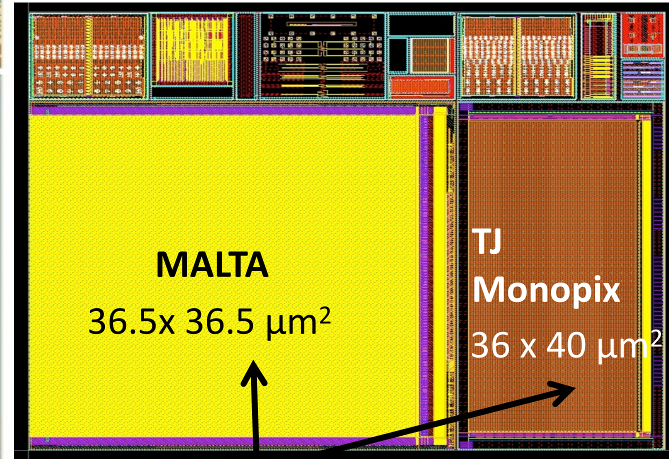
LFoundry 150 nm
substrate ρ > 2 kΩcm

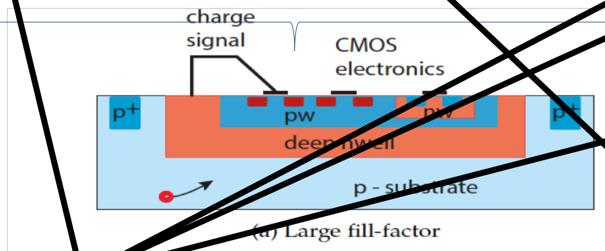
ams 180 nm -> TSI
substrate ρ ~ 0.08 - 1 kΩcm

TowerJazz 180 nm epitaxial (25 μm)
substrate ρ > kΩ cm

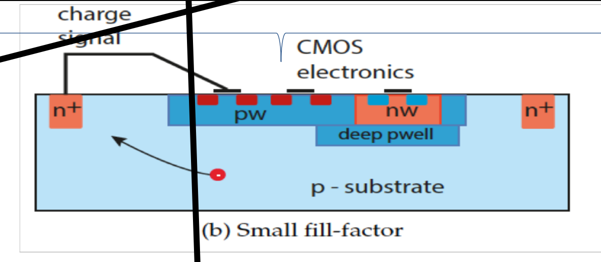








(a) Large fill-factor



(b) Small fill-factor

column drain (conservative) - asynchronous A - asynchronous B

LARGE (~1 CM^2) FULL CMOS CHIPS (=MODULES) W/ READOUT

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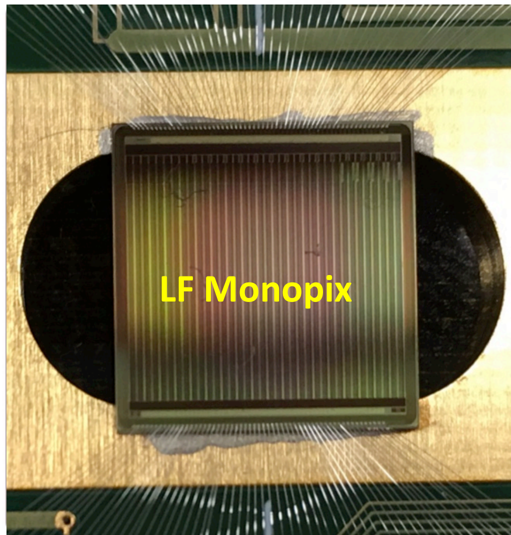

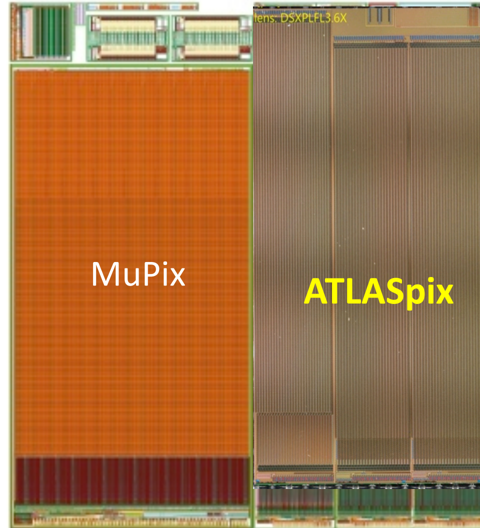

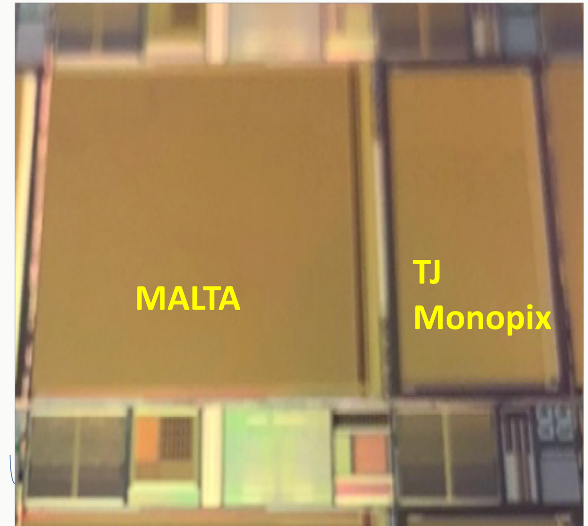

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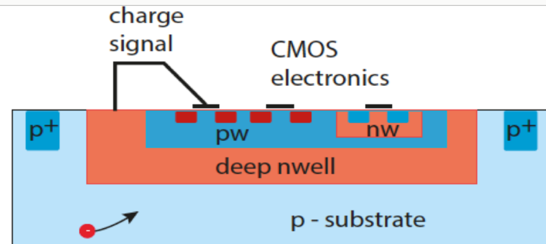
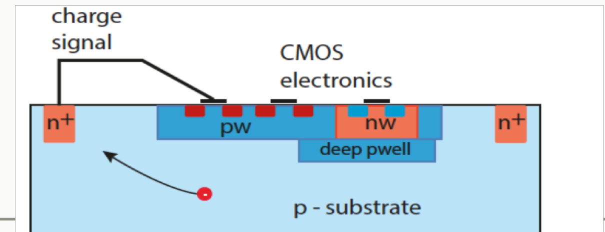


(a) Large fill-factor



(b) Small fill-factor

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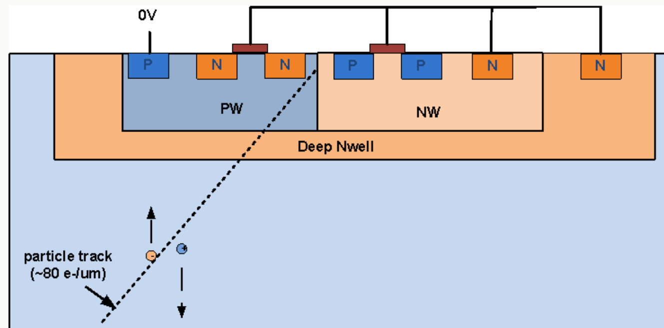
RESULTS ON

AMS/TSI 180 NM DESIGNS

AMS 350/180 NM -> TSI 180 NM LARGE ELECTRODE



- Substrate: **10 (initially) – 2k Ohm-cm**
- Bias: >60 – 100 V
- 180nm/350nm
- 3-6 metal layers
- **No PMOS isolation (3 well process)**

Designs: KIT, Liverpool, Geneva, Heidelberg, IFAE

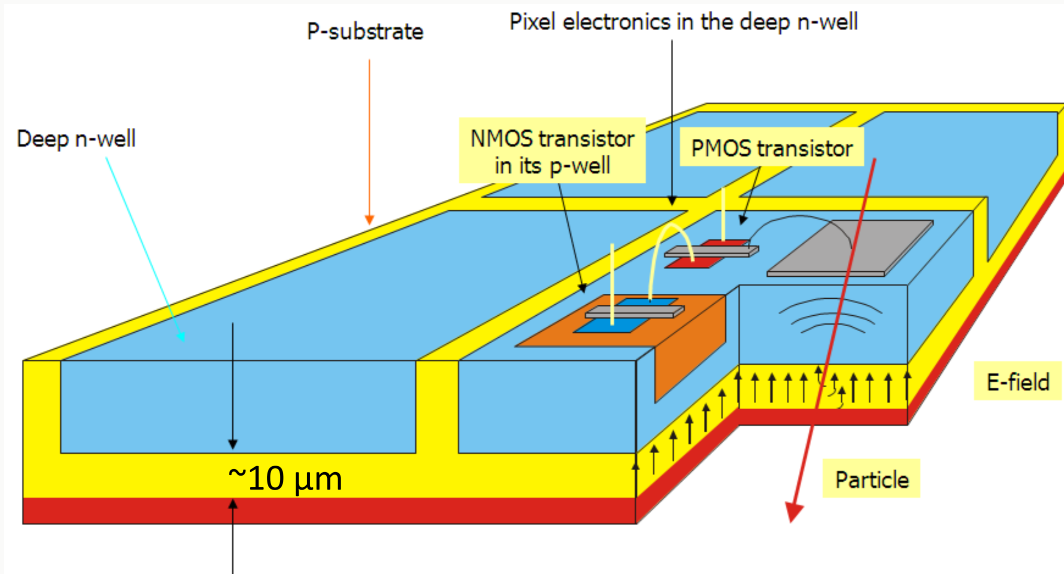
Collaboration: + ANL, Hefei, Liverpool, Bern, BNL, Lancaster, Illinois, Oklahoma, Tsukuba

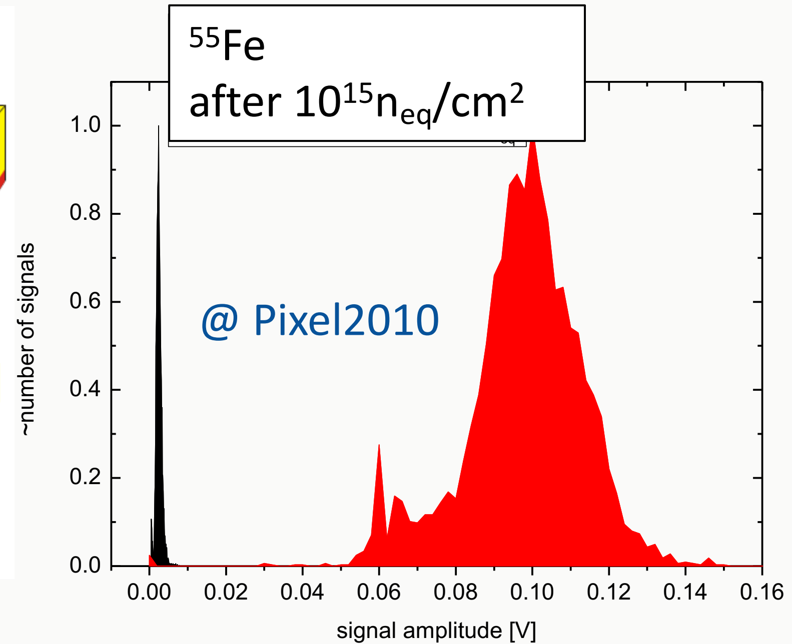
DMAPS IDEA (THEN CALLED "HVCMOS")

I. Peric, NIM A582 (2007) 876-885

HV add-on (AMS H35)

Medium resistivity





AMS 350 DEMONSTRATOR (H35DEMO)

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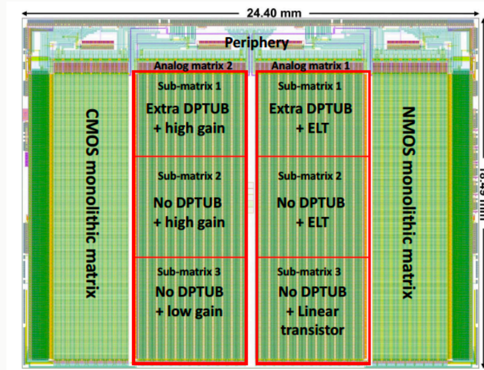
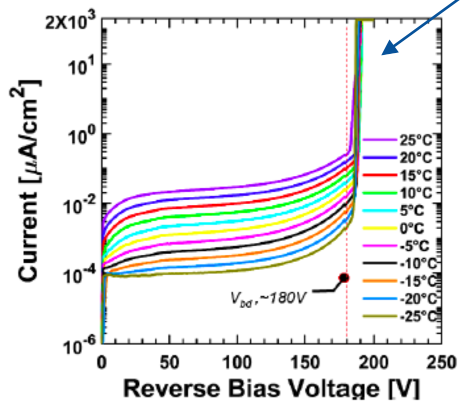
4 resistivities : 20 Ωcm (standard), 80 Ωcm, 200 Ωcm, 1 kΩcm

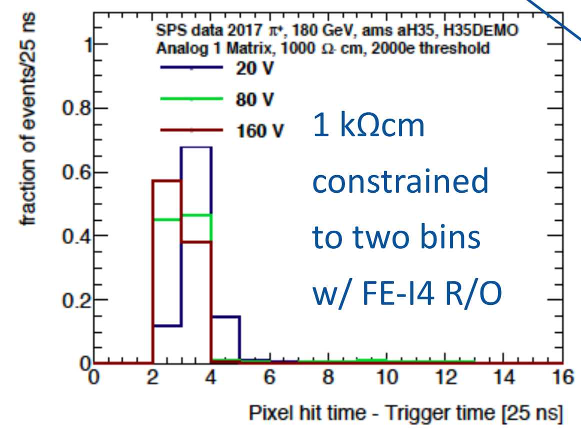
- Standalone matric w/ in-pixel nMOS discriminator
- Analog matrix for coupling to FE-I4
- Standalone matrix w/ off-pixel CMOS discriminator
- Demonstrated Bias up to 180V



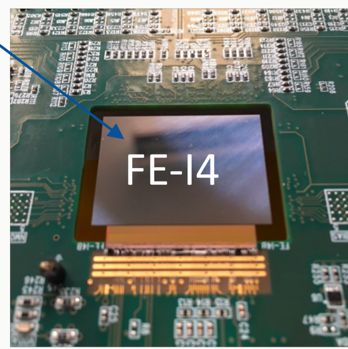
unirradiated

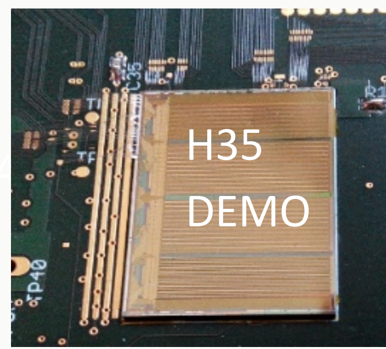


(b) 200 Ω cm



1 kΩcm constrained to two bins w/ FE-I4 R/O





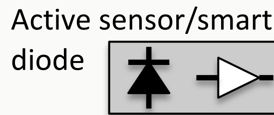
M. Benoit et al. : arXiv 1712.08338v1

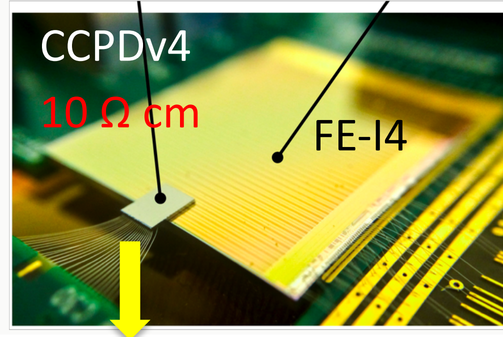
"SENSOR" IRRADIATION PERFORMANCE

- Good radiation hardness of large electrode AMS sensor proven in various prototypes

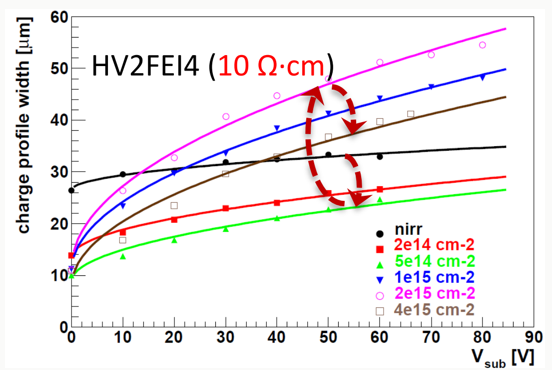
AMS 180 nm CMOS
p-substrate 0.01-2kΩ·cm
Bias 60 - 100 V
6 metal layers

Active sensor/smart diode





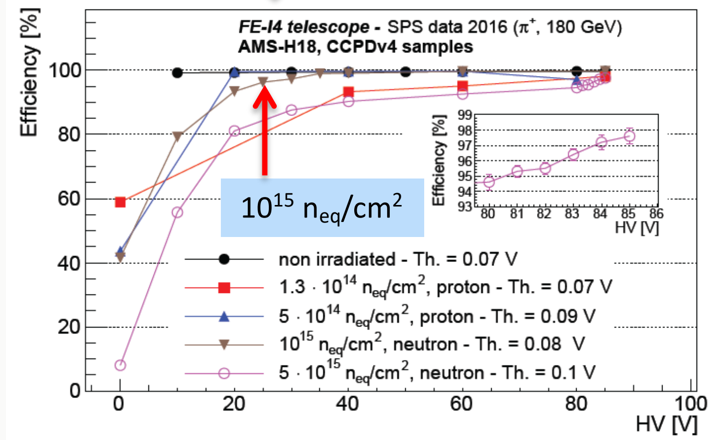
A. Affolder, et al., DOI: 10.1088/1748-0221/11/04/P04007



Benefit from acceptor removal

⇒ However, "valley of tears" exits @ 5×10^{14}

⇒ Higher res. substrate should help



M. Benoit, et al., DOI: 10.1088/1748-0221/13/02/P02011

“FULL” CHIP: ATLASPIX1 (180 NM)

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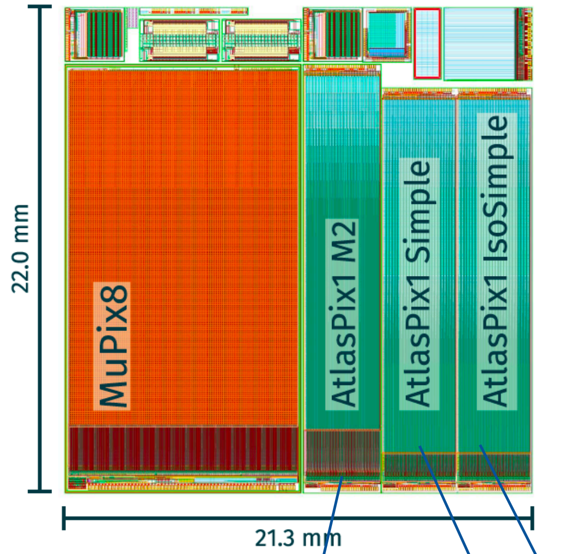
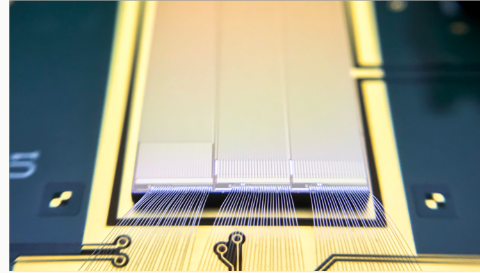




asynchronous scheme A

(60×50 μm²)

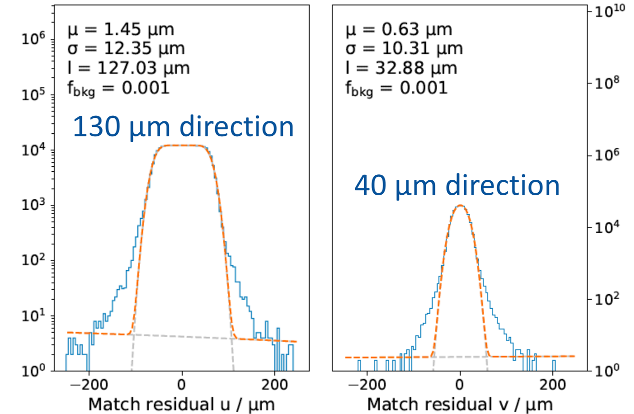
Column drain

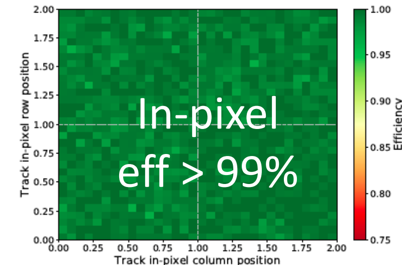
(40×130 μm²)

unirradiated

M. Kiehn
ATLAS UW 4/18

Resistivity 80 Ωcm & 200 Ωcm





RESULTS – ATLASPIX SIMPLE

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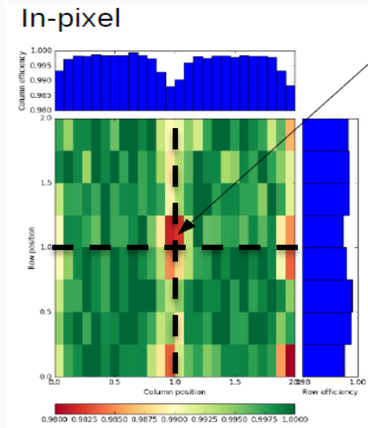
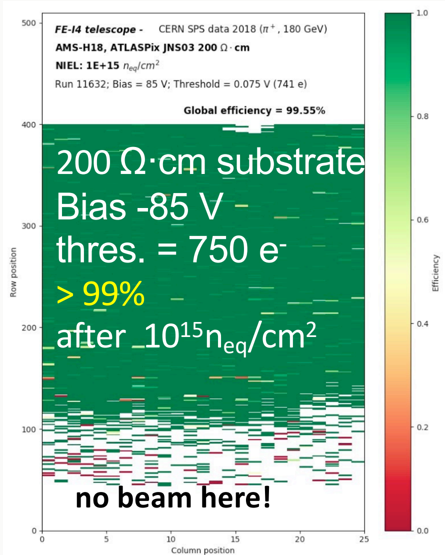
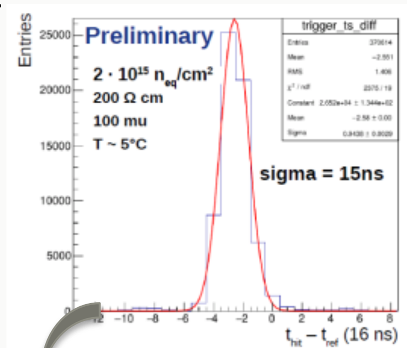
- High efficiency after $10^{15} n_{eq}/cm^2$ (neutron) at a noise rate below 40 Hz (noise occ. < 10^{-6})
- Improved timing expected by correcting time walk based on ToT

200 Ω·cm substrate
Bias -60 V
Before irradiation
Global efficiency > 99%

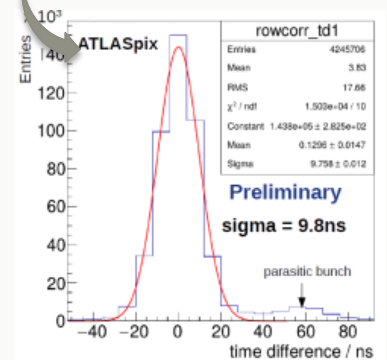


Pixel corner
98%





Off-line column delay correction + lower threshold



in-time efficiency ~ 85%

Geneva-Heidelberg-KIT Collab.
Source: VERTEX 2018

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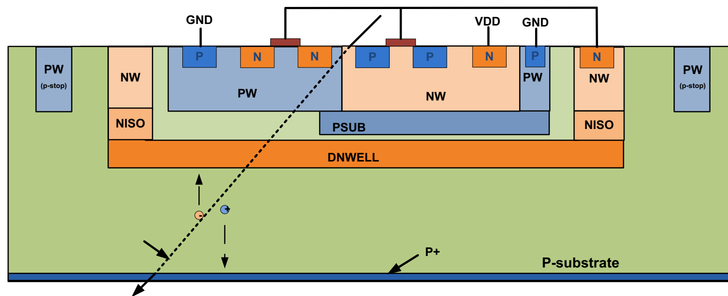
RESULTS ON
LFOUNDRY 150 NM DESIGNS

LFOUNDRY 150 NM LARGE ELECTRODE (55% FF)



LFA150:

- LFoundry **150 nm** process (deep N-well/P-well)
- **Quadrupel** well
- 7 metal layers
- Resistivity **> 2 kΩ·cm**
- Small implant customization possible
- Backside processing
- Voltages > **350 V**

Designs: Bonn, CPPM, IRFU

Collaboration: + CERN, Ljubiljana, Milano, Bologna, Oxford, Glasgow, Birmingham

SENSOR IRRADIATION PERFORMANCE

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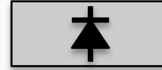
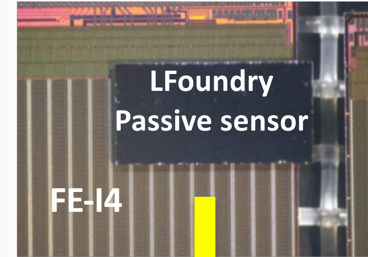
- Good radiation hardness of large electrode sensor proven in various prototypes

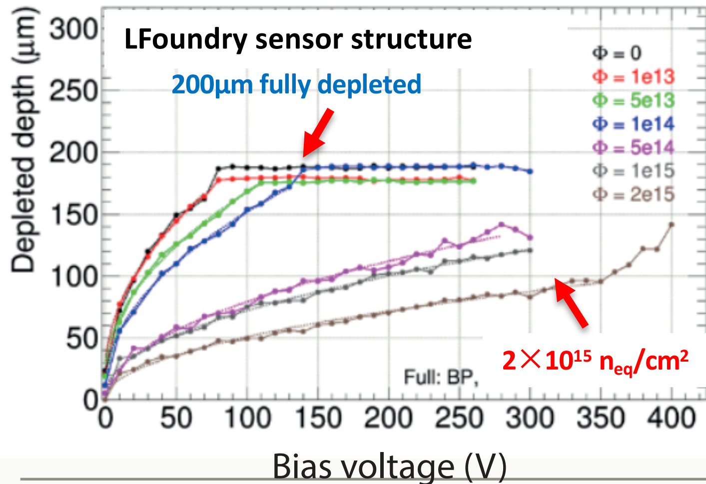
LFoundry 150 nm CMOS
P-substrate > 2 kΩ·cm
Bias 100 - 400 V
7 metal layers

Passive sensor





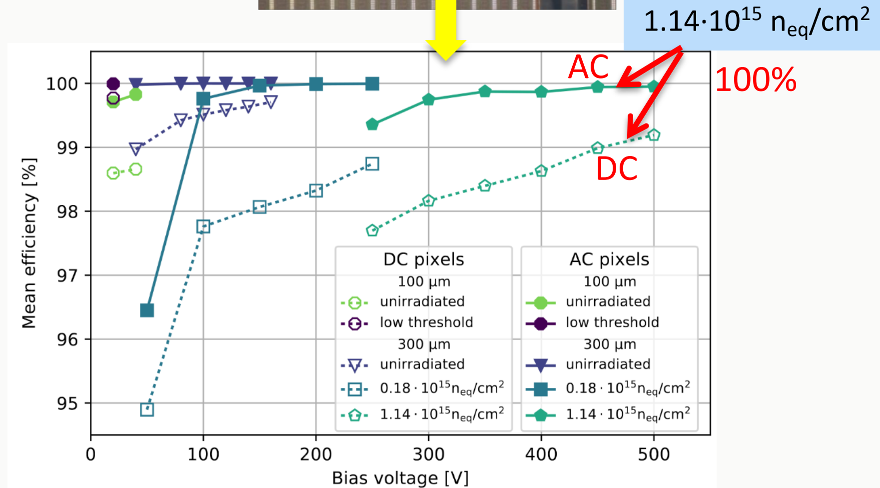
T. Hirono et al., DOI: 10.1016/j.nima.2016.01.088
P. Rymaszewski et al., DOI: 10.1088/1748-0221/11/02/C02045



Bias voltage (V)

I.Mandić, et al., DOI: 10.1016/j.nima.2018.06.062

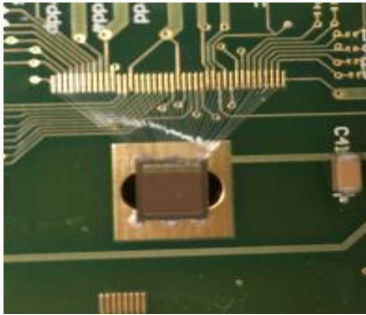
$1.14\cdot10^{15}$ n_{eq}/cm^2



D.-L. Pohl, et al., DOI: 10.1088/1748-0221/12/06/P06020

DEVELOPMENT SERIES

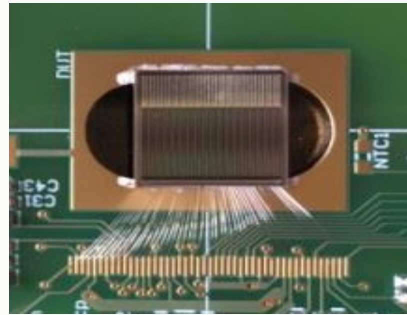
- ❑ CCPD_LF
- ❑ LF-CPIX
- ❑ LF-MonoPix (Fully Monolithic)



Sensor + Analog (Disc.)

- Pixel size: 33 µm x 125 µm
- Chip size: 5 mm x 5 mm
- Fast R/O with FE-I4
- Thickness: 750, 300, 100 µm
- Bonn/CPPM/KIT

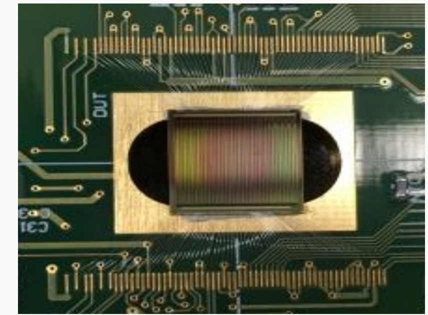
→



Sensor + Analog

- Pixel size: 50 µm x 250 µm
- Chip size: 10 mm x 10 mm
- Fast R/O with FE-I4
- Thickness: 750, 200, 100 µm
- Bonn/CPPM/IRFU

→

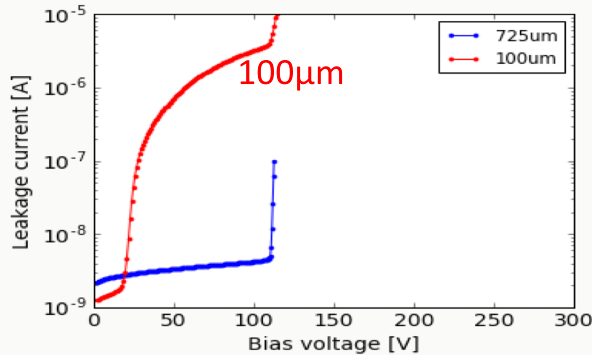


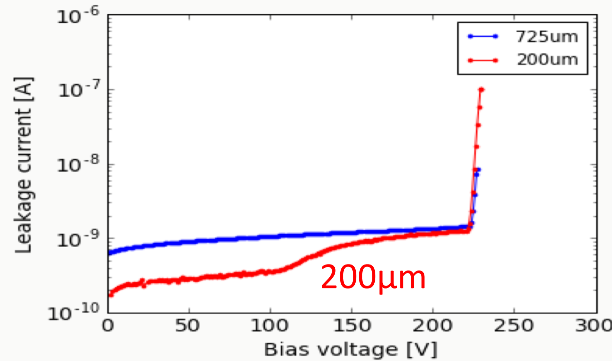
Sensor + Analog + Digital

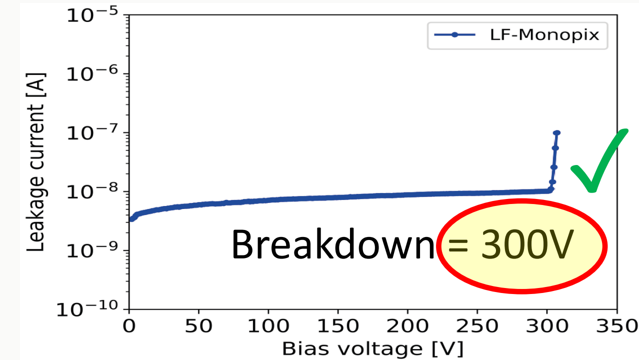
- Pixel size: 50 µm x 250 µm
- Chip size: 10 mm x 10 mm
- Column drain R/O architecture (sufficient for outer layer rates)
- Thickness: 750, 200, 100 µm
- Bonn/CPPM/IRFU

BIAS VOLTAGE (I-V CURVES)

- CCPD_LF
- LF-CPIX
- LF-MonoPix







- Guard rings have been improved to increase the breakdown voltage
- Leakage current performance @ full depletion improved by better backside processing (polishing)
- Full depletion voltage **@ 100 µm:** unirr. V_{dep} = **7 V**, irradiated V_{dep} = **130 V**

PIXEL DESIGN AND CROSS TALK MITIGATION

Preamp + Discriminator

R/O Logic

C_f 4 bit DAC Thres. Tuning

vddaBias Bias Preamp Vinj -HV BL TH HIT

EN TE HIT LE

S Q R $\bar{Q}$ 1st latch ReadInt

Token in (from previous pixel)

S Q R $\bar{Q}$ HIT flag

D Q EN $\bar{Q}$

LE TE ReadInt LE RAM TE RAM Addr. ROM

Token out (to next pixel)

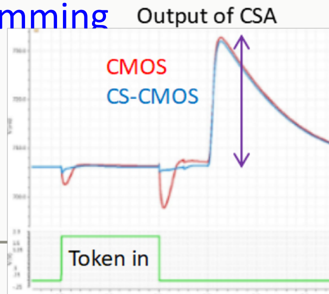
Freeze Read Time stamp (8-bit) Column bus (24 bit)

CCPD_LF, LF-CPIX

LF-Monopix

- Charge sensitive amplifier
- In-pixel 4-bit DAC for threshold trimming
- Hit register (1-bit counter)
- 8-bit time stamp @ 40 MHz
  - *Time, charge of signal*

Output of CSA



- Full-custom dig. circuit
  - *Minimized area => for less C_d*
  - *Low noise circuit design for critical dig. blocks*

eg. current steering logic, Source follower readout of SRAMs

mitigation works

RADIATION HARDNESS (TID)

The prototype chips (CSA+Discr.) were irradiated with X-rays up to 50 Mrad

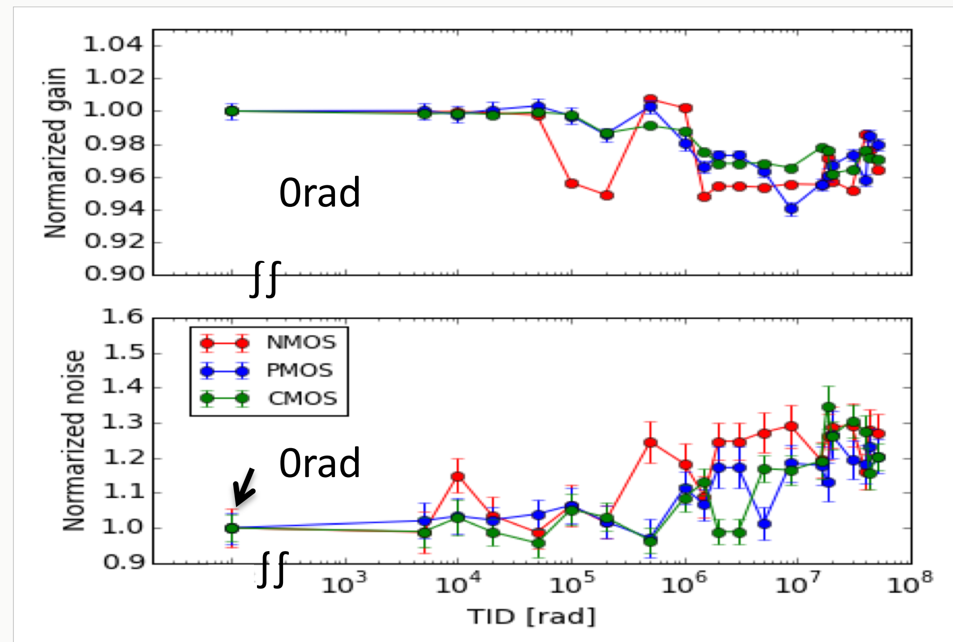
- Input transistor of CSA
  - NMOS
  - PMOS
  - CMOS
- Bias voltage: -100V

- **Gain degradation: <5%**
- **Noise increase: ~30%** ✓

- No significant difference between the 3 flavors observed

- Thresholds still tunable after 50 Mrad

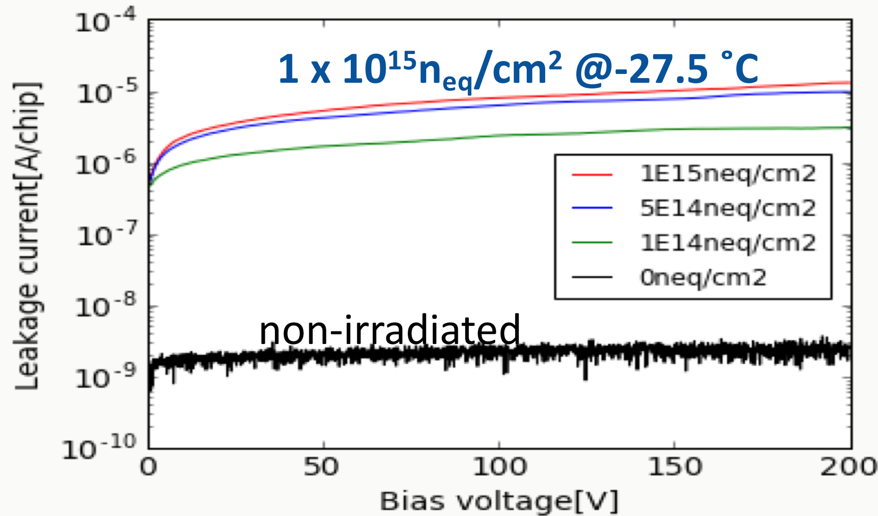
<u>Normalized gain and noise of LF-CPIX</u>



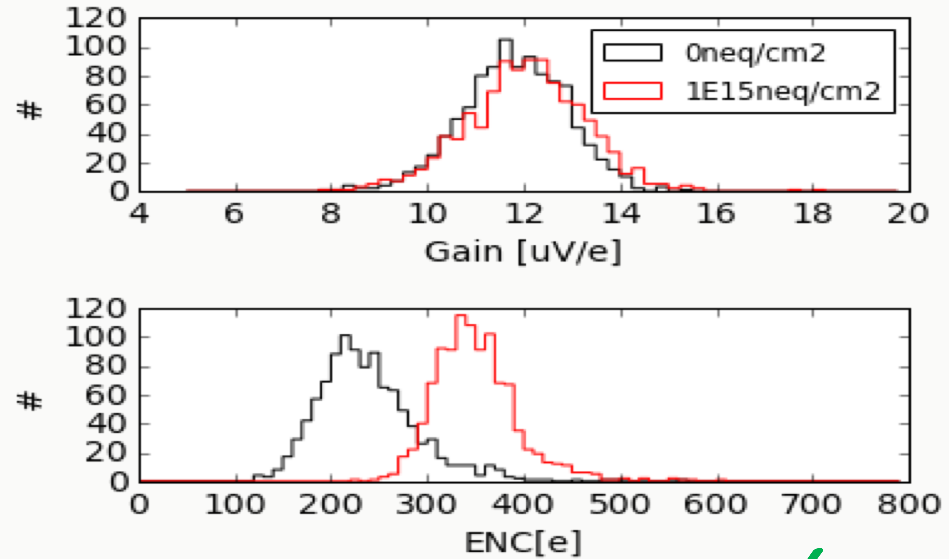
T. Hirono, et al., DOI: 10.1016/j.nima.2018.10.059

RADIATION HARDNESS OF FULL CHIP (NIEL)

- **I-V curve of MonoPix**



- **Gain and noise**



- Breakdown voltage is higher than 200V

RESULTS – LF-MONOPIX

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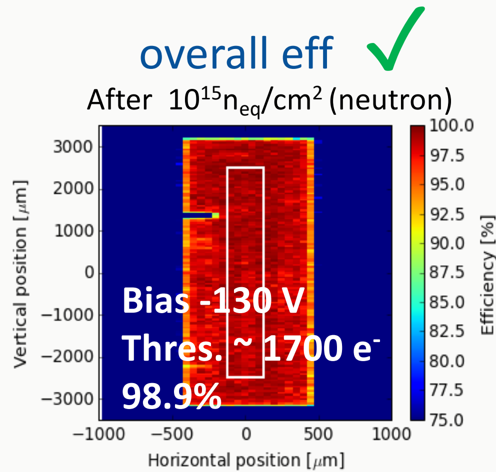
- High BV ~280 V => large depletion + high field
- High and uniform efficiency even after irradiation
  - Achieved @ very low noise occupancy < 10^{-7}/25ns/pixel
- Promising timing which can still be improved by

(a) optimization of FE biasing, (b) thinning + HV backbias

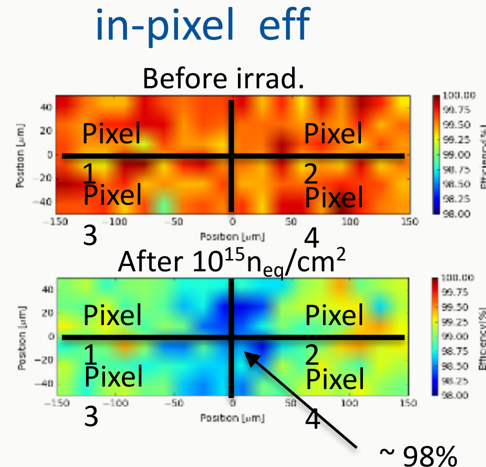
overall eff ✓



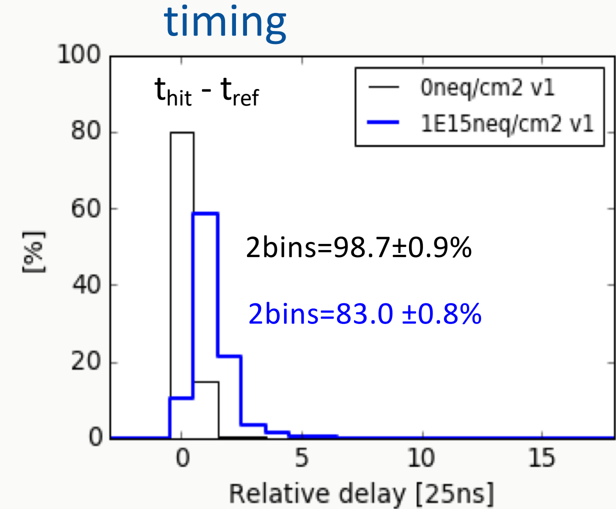
@ Noise occ. < 10^{-8}, thr~1700e-

T. Hirono, et. al, DOI: 10.1016/j.nima.2018.10.059

in-pixel eff



timing



Uni-Bonn (Preliminary)

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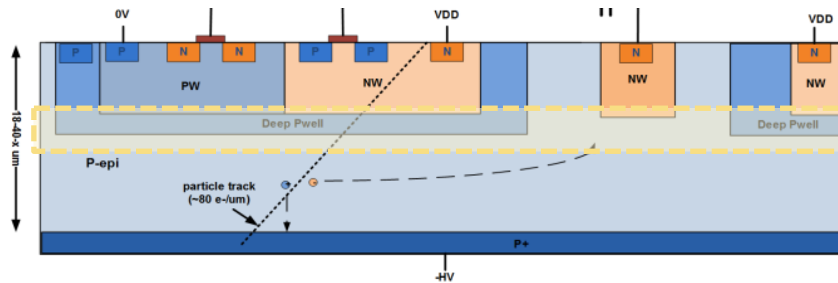
RESULTS ON
TOWERJAZZ 180 NM DESIGNS

TJ – MALTA & MONOPIX



- **TowerJazz** 180 nm CMOS CIS
- Deep Pwell allows full CMOS in pixel
- Gate oxide 3 nm good for TID
- Thickness: 18 – 40 µm
- High resistivity: 1 – 8 k Ohm-cm
- Reverse substrate bias
- **Modified process** to improve lateral depletion
- Derived from ALICE development (CERN)

Design: CERN (MALTA), Bonn (MONOPIX)

Collaboration: M.Barbero[3], I. Berdalovic[2], C. Bespin[1], P. Breugnon[3], I. Caicedo[1], R. Cardella[2], Y. Degerli[4], S.Godiot[3], F. Guilloux[4], T. Hemperek[1], T. Hirono[1], T. Kugathasan[2], C. A. Marin Tobon[2], K. Moustakas[1], P. Pangaud[3], H.Pernegger[2], P. Riedler[2], P. Rymaszeweski[1], E. J. Schioppa[2], P. Schwemling[4], W. Snoeys[2], M. Vandenbroucke[3], T. Wang[1], N. Wermes[1]

[1]Bonn, [2]CERN, [3]CPPM, [4]CEA/IRFU

SMALL ELECTRODE AND RADIATION TOLERANCE

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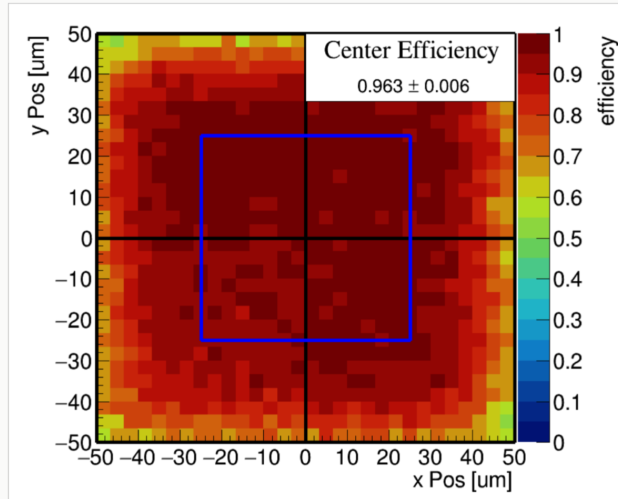
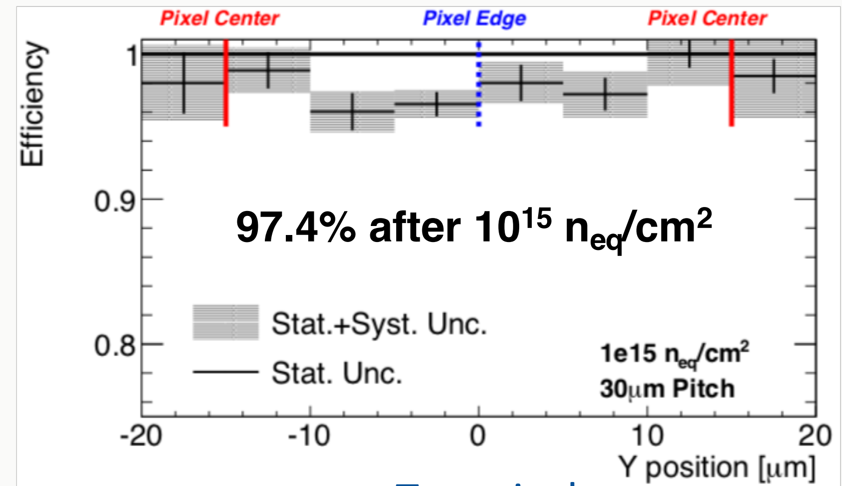
"Investigator" chip to investigate modified technology

JINST 12 (2017) no.06, P06008

50x50µm pixel pitch,
3µm electrode,
40µm opening



30x30µm pixel pitch,
3µm electrode
9µm opening

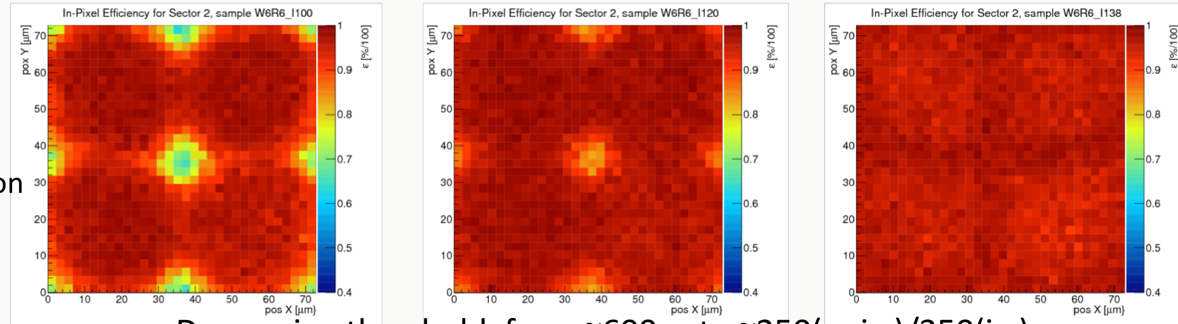


Two pixels

RESULTS – MALTA & TJ-MONOPIX

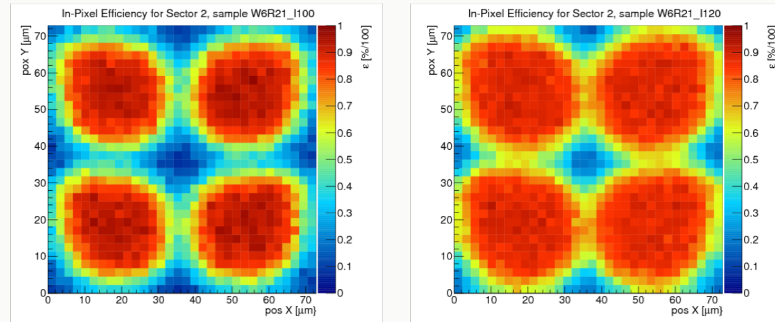
- Low corner efficiency, especially after irradiation

MALTA
Before irradiation



Decreasing threshold, from ~600 e^- to ~250(unirr)/350(irr) e^-

MALTA
Irradiated
5 $x10^{14}$ n_{eq}/cm^2



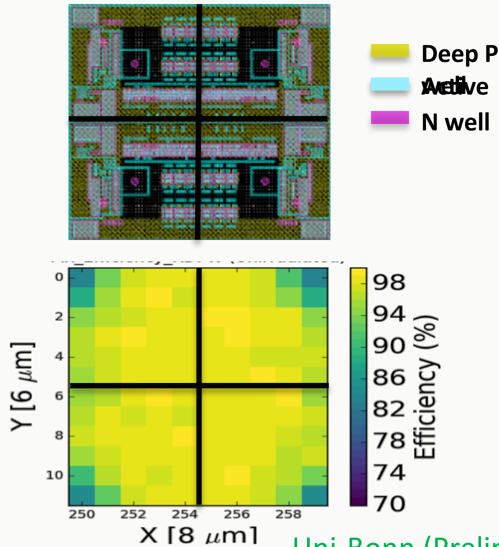
Couldn't reach lower threshold

A. Sharma, et al., Vertex 2018

RESULTS – MALTA & TJ-MONOPIX

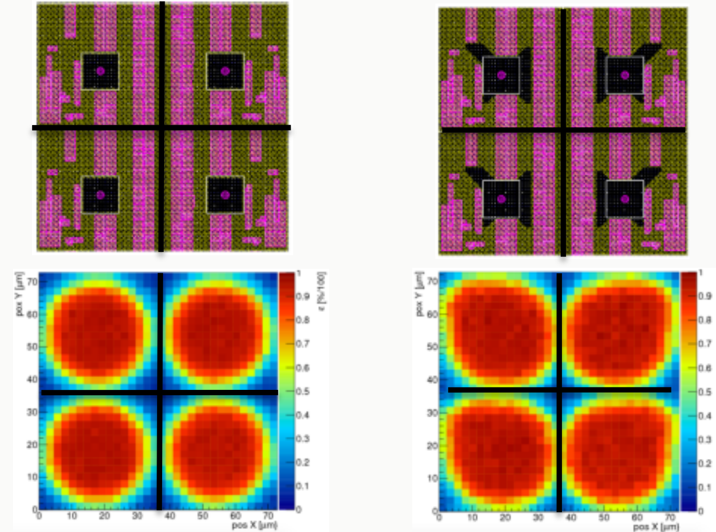
- Lateral field configuration under deep pwell at pixel corner is critical

TJ-Monopix, before irradiation

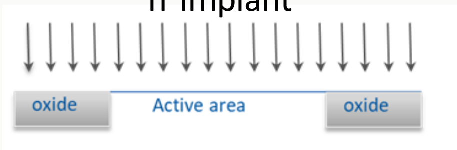


Uni-Bonn (Preliminary)

MALTA, **after irradiation**

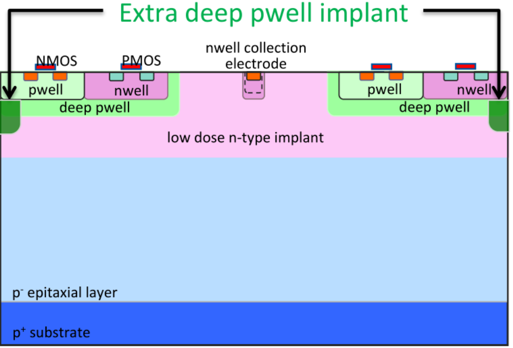


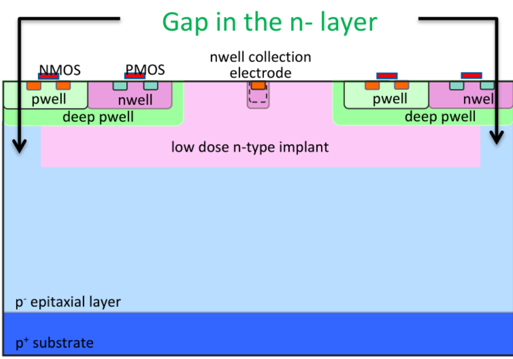
A. Sharma, et al., VERTEX 2018



- TJ-Monopix: low efficiency corners coincide with large active area
- MALTA: efficiency depends on deep pwell configuration
- Modifications inspired and verified by TCAD (next slide)

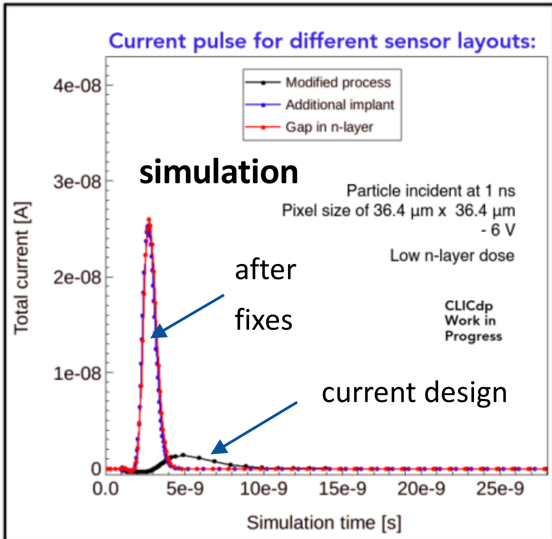
FIXES TO IMPROVE EFFICIENCY AFTER IRRADIATION

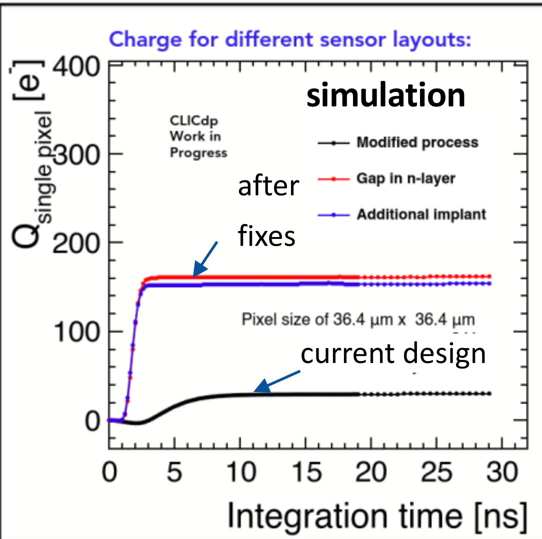




T. Kugathasan et al., VERTEX 2018

TCAD simulation after irradiation ($10^{15} n_{eq}/cm^2$) Preliminary, M. Munker





Note: simulation is for "worst case" = particle impinging at pixel corner

- Simulation shows significantly improved charge collection time and less charge loss after irradiation with both proposed fixes
- New design with both fixes submitted in August 2018

POWER ESTIMATES

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Design	pixel size (μm^2)	pixels/chip	pixels/cm2	analog/chip	digital/chip	periphery	Power/chip	Total Power density /cm^2	Power/pixel
AMS ALTASpix3	50 x 130	57288	13500	0.410 W	0.42 W	0.514 W	1.344 W	305 mW	23 µW
LF Monopix1	50 x 250	30720	8000	1.106 W	0.24 W	0.369 W	1.715 W	390 mW	55 µW
LF Monopix2	50 x 150	51200	13333	1 W	0.12 W	0.125 W	1.275 W	290 mW	25 µW
TJ Monopix	36 x 40	266667	69444	0.238 W	0.24 W	0.225 W	0.703 W	160 mW	3 µW
TJ Malta	36.5 x 36.5	288234	75061	0.238 W	0.012 W	0.264 W	0.514 W	115 mW	2 µW

THE SITUATION (MY VIEW)

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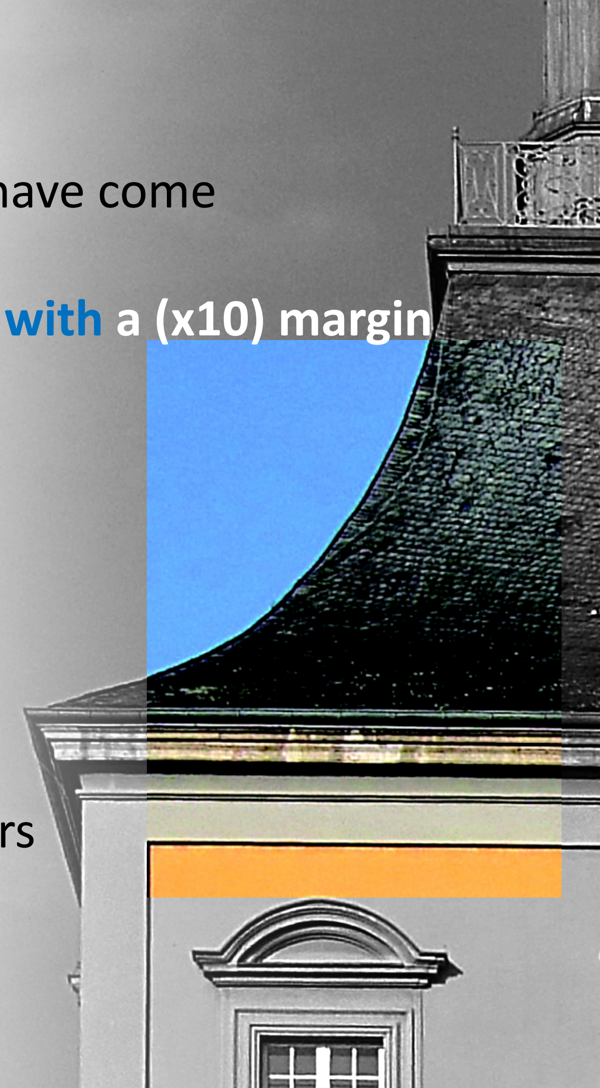
	AMS/TSI 180 nm Large FF	LFoundry 150 nm Large FF	TowerJazz Small FF
radiation hardness @ 10^{15} n_{eq}/cm^2	✓	✓	needs to be fixed
rate capability @ 5th layer	✓	✓	✓
timing	needs (small) improvement	needs (small) improvement	✓
power	😐	😐	😀
Technology/Vendor	TSI is new for HEP	established	work relationship w/ CERN (ALICE)

CONCLUSIONS

- Depleted CMOS pixels (DMAPS) combining HV and HR have come a big step forward towards usage @ HL-LHC
- Simulation: Col-drain architecture **meets 5th layer rates with a (x10) margin**
- Large FF (AMS & LFoundry):
  - high beak down voltage
  - large signal
  - high efficiency after 10^{15} n_{eq}/cm^2
- Small FF (TJ) features (MALTA / Monopix)
  - low capacitance, low noise
  - low power, large Q/C
  - issue: radiation hardness, low efficiency at pixel corners
    → ideas submitted → stay tuned



Norbert Wermes

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BACKUP

PASSIVE CMOS PIXEL SENSORS

PASSIVE CMOS SENSORS

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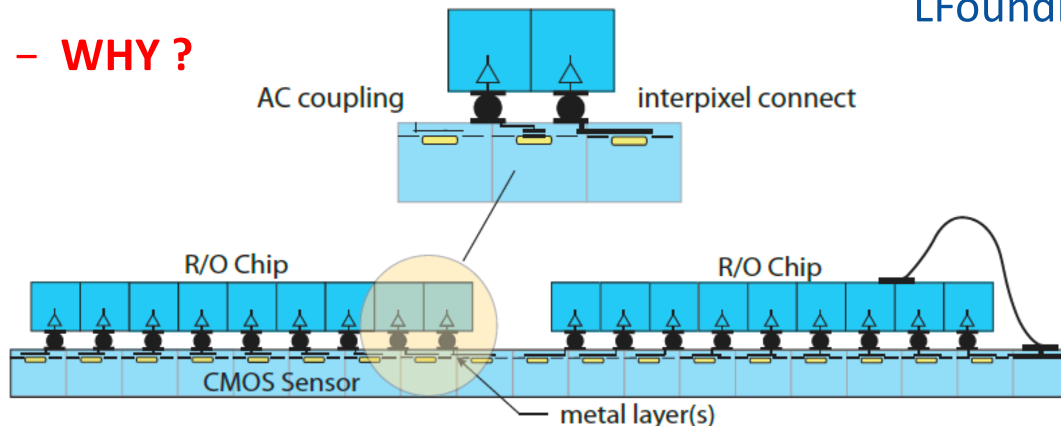
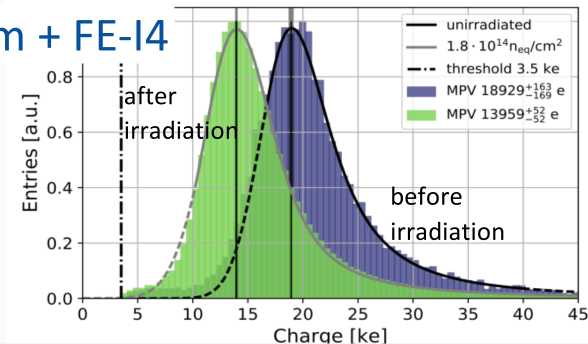
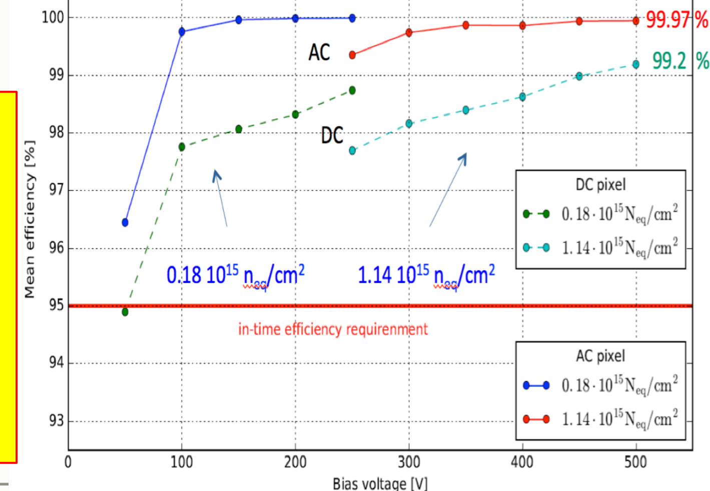
– **WHY ?**

LFoundry 150 nm + FE-I4







– Cheaper

– High wafer throughput

– Exploit metal layers for AC coupling and rerouting

Results

- **bias 120 V** -> 500 V
- **~220 µm** depletion depth
- same as standard sensors in i_{leak} and noise
- **high eff. after** ($1x10^{15} n_{eq}/cm^2$)

D.-L. Pohl et al., JINST 12 (2017) no.06, P06020

ANOTHER INTERESTING TECHNOLOGY

DMAPS ON SOI

SOI MONOLITHIC PIXELS

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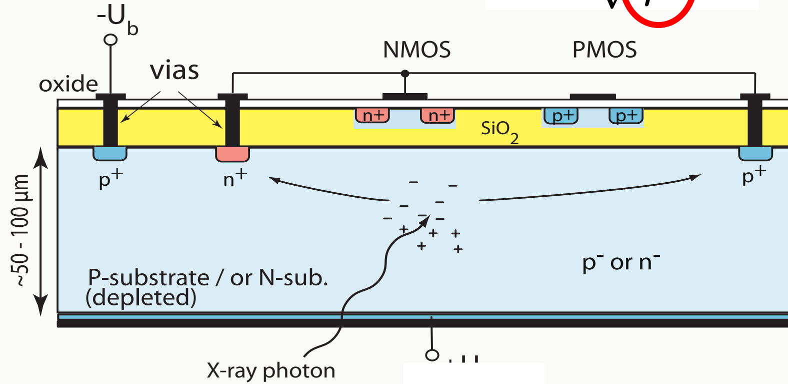
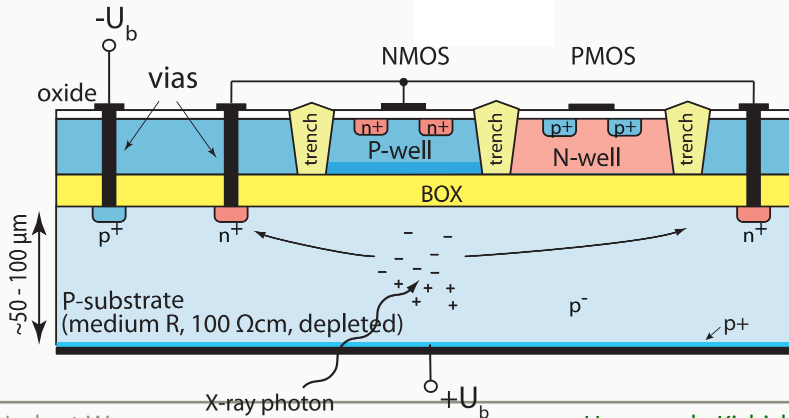
FD CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$





- **fully depleted SOI (thin film)** @ Lapis/KEK
- issues
  - back gate effect
  - coupling of sensor to circuit
  - radiation (TID) issues due to BOX
- cures developed in recent years
  - buried p-well, nested wells
  - "double SOI" structures

- **HV-SOI (thick film)**
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

Hemperek, Kishishita, Krüger, Wermes, NIM A796 (2015) 8-12

LFOUNDRY

LF – MONOPIX IN TESTBEAM

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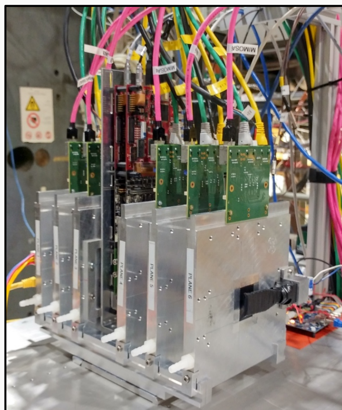
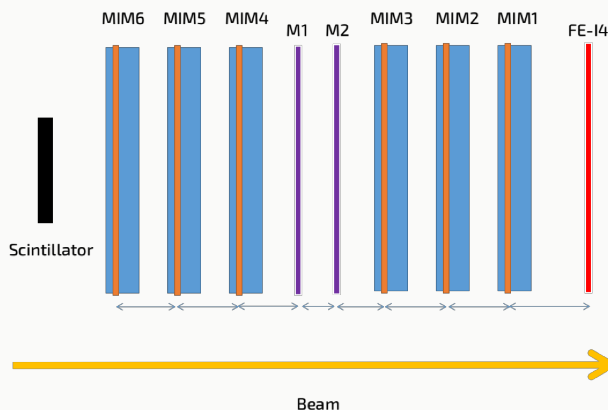
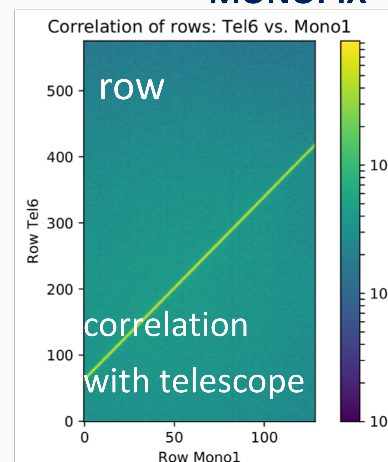


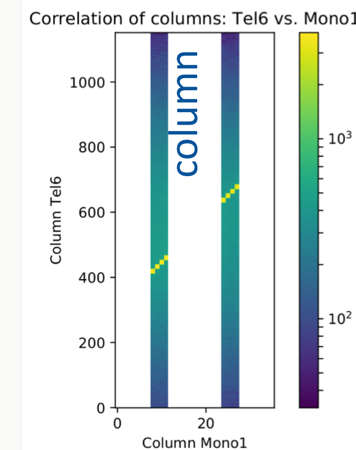


LF-MONOPIX (unirradiated and n-irradiated)

ELSA (2.5 GeV e-) CERN SPS H18 (180 GeV π)

Sample of event correlation (@SPS)
MONOPIX <-> MIM26 (6)

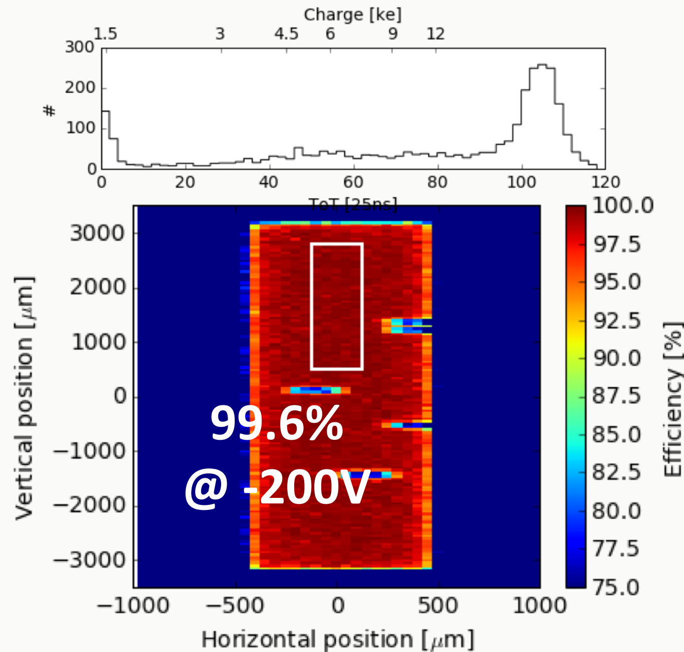




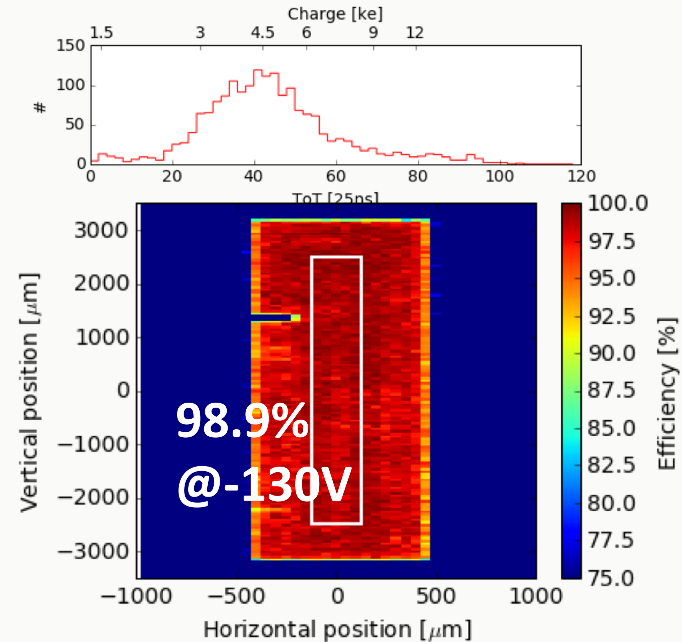
- **MIMOSA26 x 6**
  - Pixel size: 18.2 μm x 18.2μm
  - 1152 μs/frame (rolling shutter)
- **FE-I4 x 1**
  - Pixel size: 250 μm x 50 μm
  - Timing resolution: 25ns (trig. by scintillator + TLU)

TESTBEAM RESULTS -> EFFICIENCIES

- **un-irradiated**
  - Hit efficiency **@ Noise occ. << 10^{-7} , thr~1700e- (<10^{-7} @ 1400e-)**
  - 1% masked pixels from noise tuning



- **Neutron irradiated (1 x $10^{15} n_{eq}/cm^2$)**
  - Hit efficiency **@ Noise occ. < 10^{-8}, thr~1700e-**
  - < 0.2% masked pixels from noise tuning.

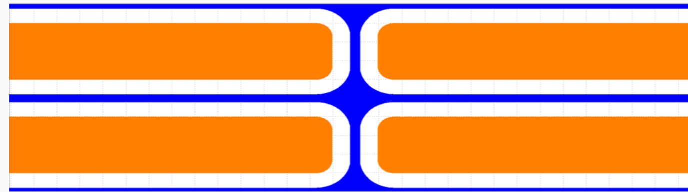


✓

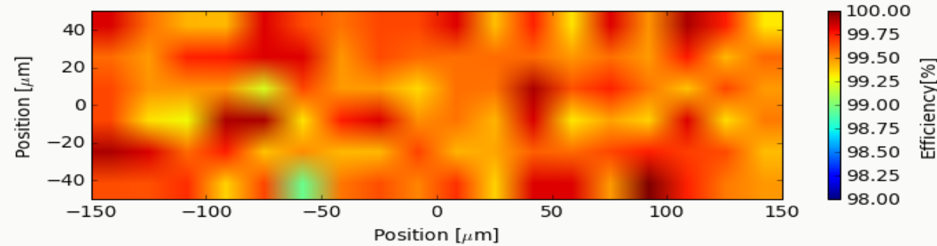
IN-PIXEL EFFICIENCY

N-well (collection well)

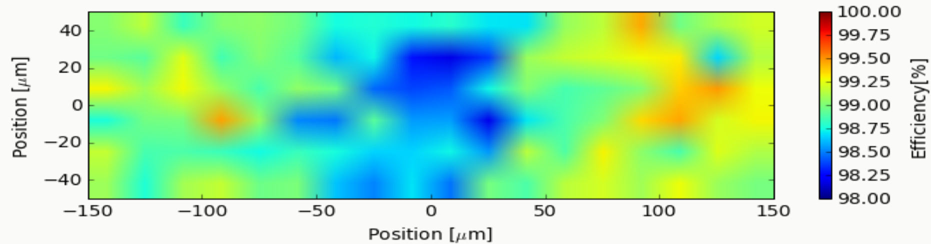
P-well



Un-irradiated



$1 \times 10^{15} n_{eq}/cm^2$



✓

In the irradiated sample, the degradation of the efficiency is observed not only at the corner of pixels but also in the middle of the pixel => normal degradation

TIMING PERFORMANCE

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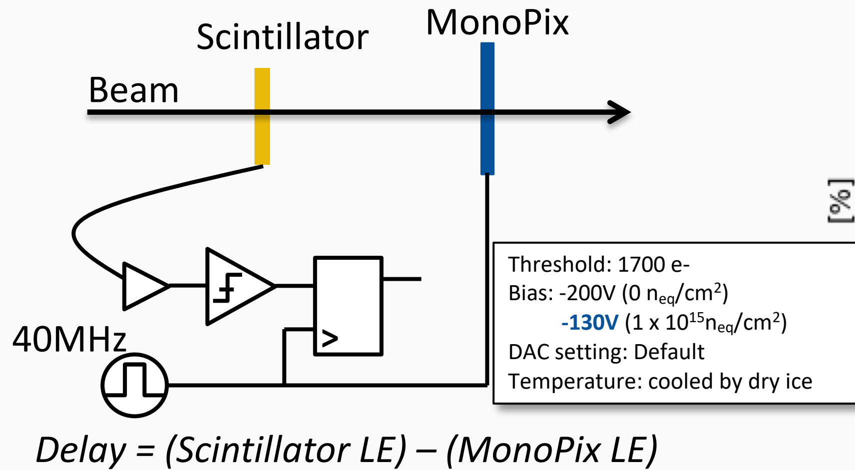
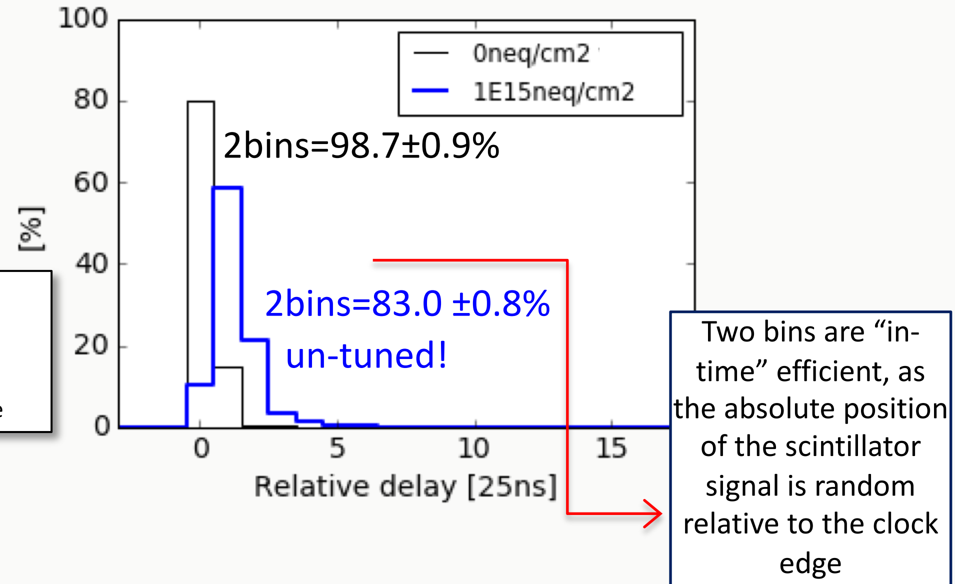


Delay = (Scintillator LE) – (MonoPix LE)

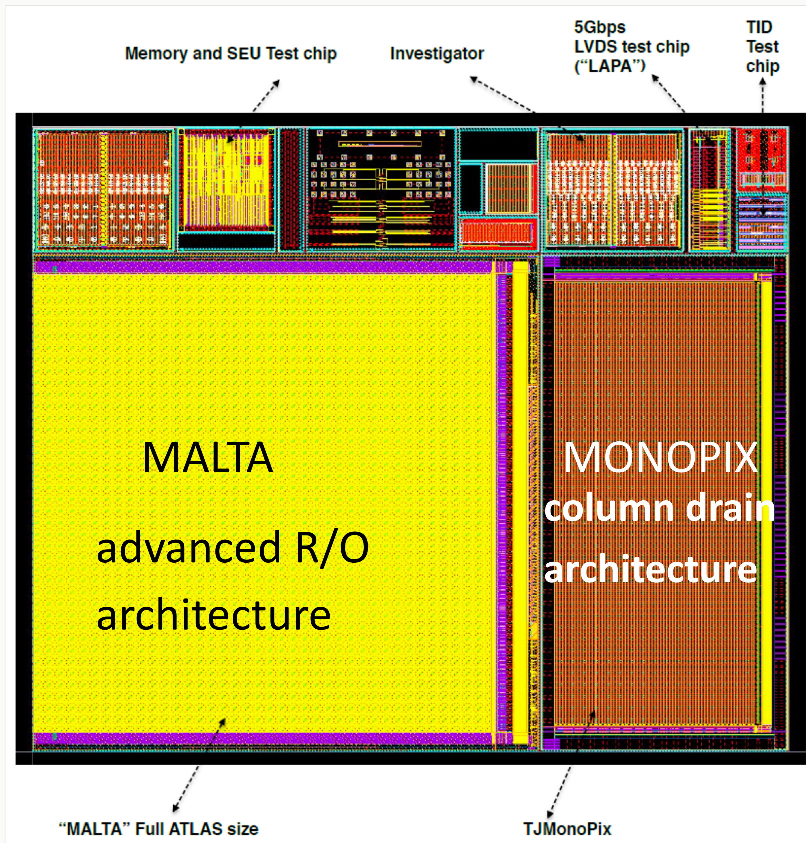


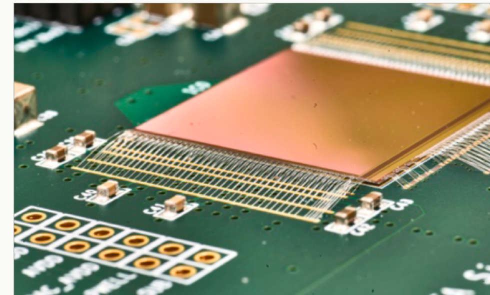
- **>80% in-time efficient after** 1 x $10^{15} n_{eq}/cm^2$.
  Remarkable for C_D ~ 400fF and promising for new design with smaller C_D (Optimized FF)
- **There is still room for improvement by tuning:**
  Optimize: CSA, discriminator currents, etc., higher bias voltage, back side process.

ANOTHER INTERESTING TECHNOLOGY

TOWERJAZZ (MONOPIX & MALTA)

TJ – MALTA AND TJ - MONOPIX





- Sensor design is identical
- Front ends similar (different biasing schemes)
- R/O architectures very different

MALTA:

- Hits are stored using in-pixel flipflops and are transmitted asynchronously over high-speed buses to the end-of-column logic.
- No clock distribution over the active matrix – reduces power consumption!

TJ MODIFIED PROCESS: SENSOR DESIGN

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- **Modified TJ-180 process:**
  Full depletion radiation tolerant to bulk damage
- **Small n-well collection electrode,**
- **Small electrode to electrode distance (small pixel size)**
  ↑ efficiency
- **Low analog power**

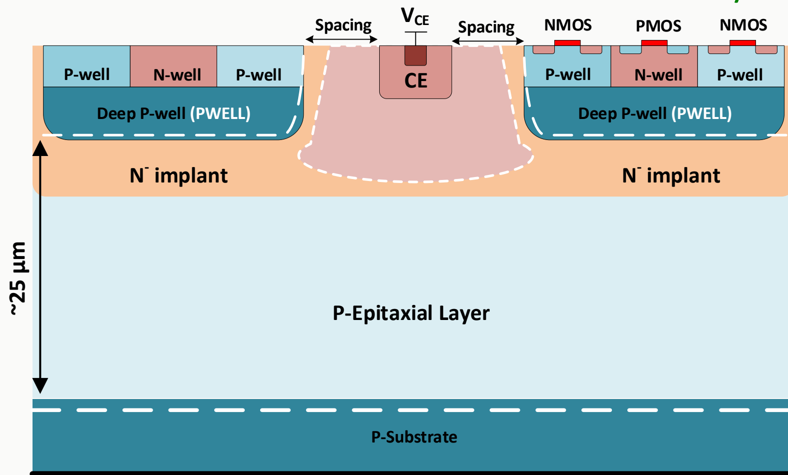
$$\frac{S}{N} \approx \frac{Q/C}{\sqrt{g_m}} \sim \frac{Q/C}{\sqrt[m]{P}} \Rightarrow P \sim \left(\frac{Q}{C}\right)^{-m}$$

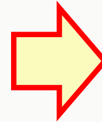
- **Biasing potentials: PWELL, PSUB, V_{CE}**
- **Reverse biasing will increase depletion and input signal amplitude**
- **High frontside bias possible with the TJ-Monopix HV flavour**
- **0 PWELL -6V, 0 PSUB -20V (after full depletion)**
- **0 HV +50V 2V/μm (including PSUB)**

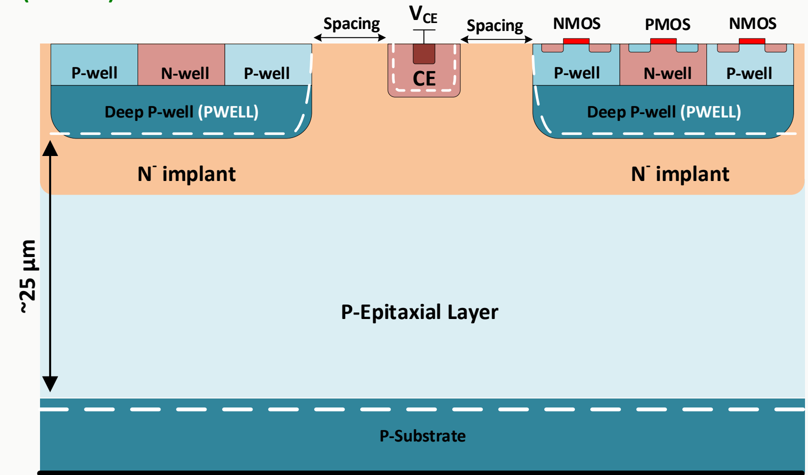
No reverse bias

W. Snoeys et al., NIM A871 (2017) 90 – 96.

High reverse bias







TJ-Monopix: Electronics Design

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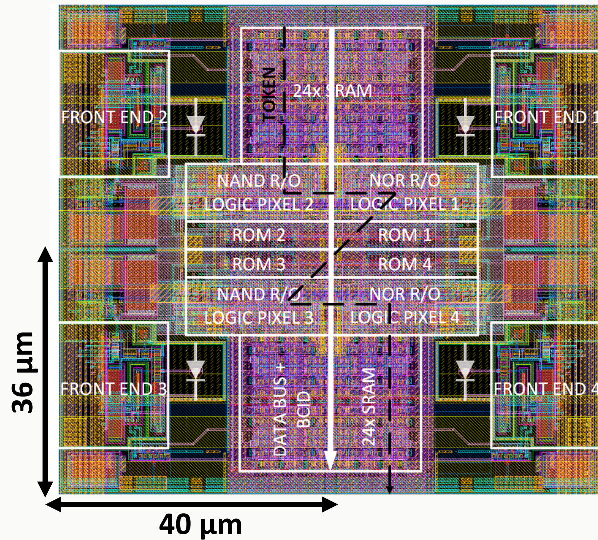
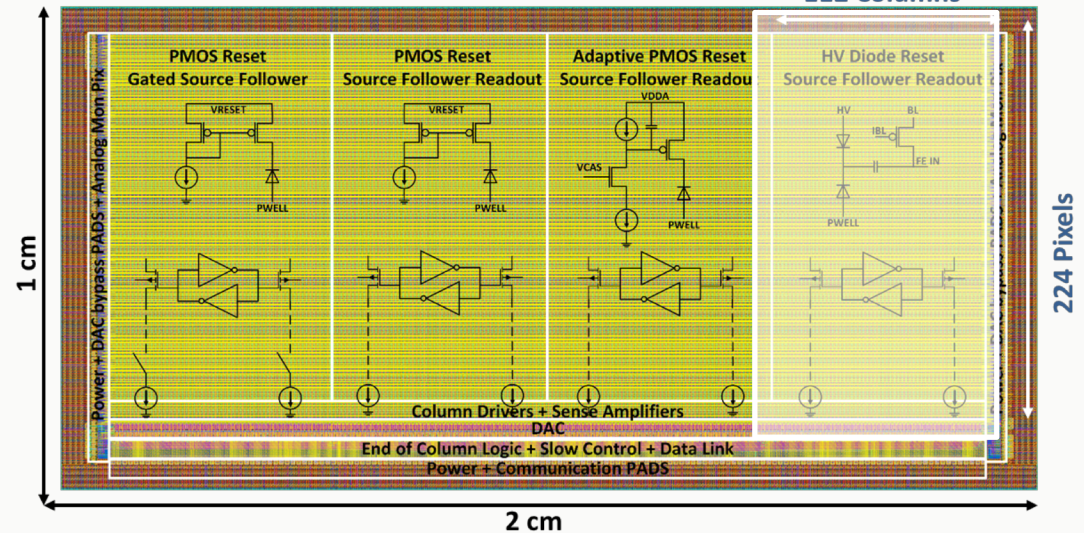
2x2 Pixel Layout



Full chip layout



- Non-conventional front-end design to take advantage of the low capacitance (voltage amplifier with LF feedback)
- **Low power:** 110 mW/cm²
- **High gain:** 0.3 - 0.6 mV/e^- (due to the small C_d)
- Optimized for **fast timing response**
- **Low threshold dispersion**, no in-pixel tuning

- 1x2cm² (1/2 of final size)
- 36x40µm² pixel size, 224x448 pixels
- 6-bit analog (charge) ToT information
- 4 different flavors implemented
- 160 MHz total data output

SOME TYPICAL CHARACTERISTICS (4 FLAVOURS)

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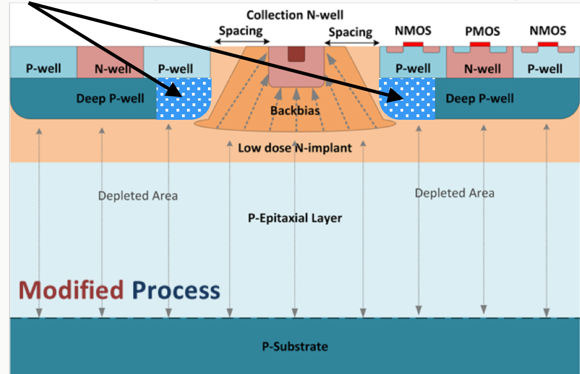
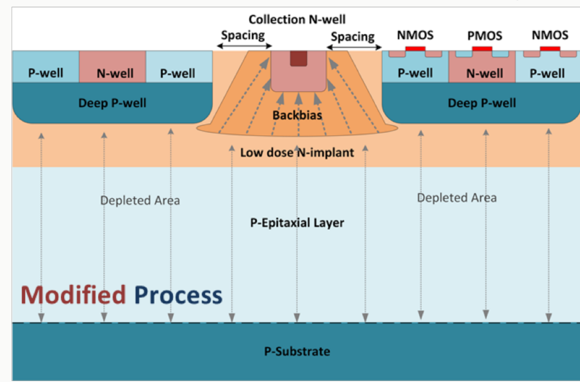
- All flavours working as expected: **thresholds (230 – 370) e-**
- ~ 0.1% masked pixels and **noise occupancy << 10^{-6} hits/BX**
- **ENC = (9 – 12) e-** and **σ_{thr} = (15 – 38) e-**
- Best results with front side diode **HV biasing (incr. signal)** -> can decrease C_{in} to < 1 fF ✓

REM DPW – top half of each column (112 pixels)



FULL DPW – bot half of each column (112 pixels)



threshold distribution (full DPW)