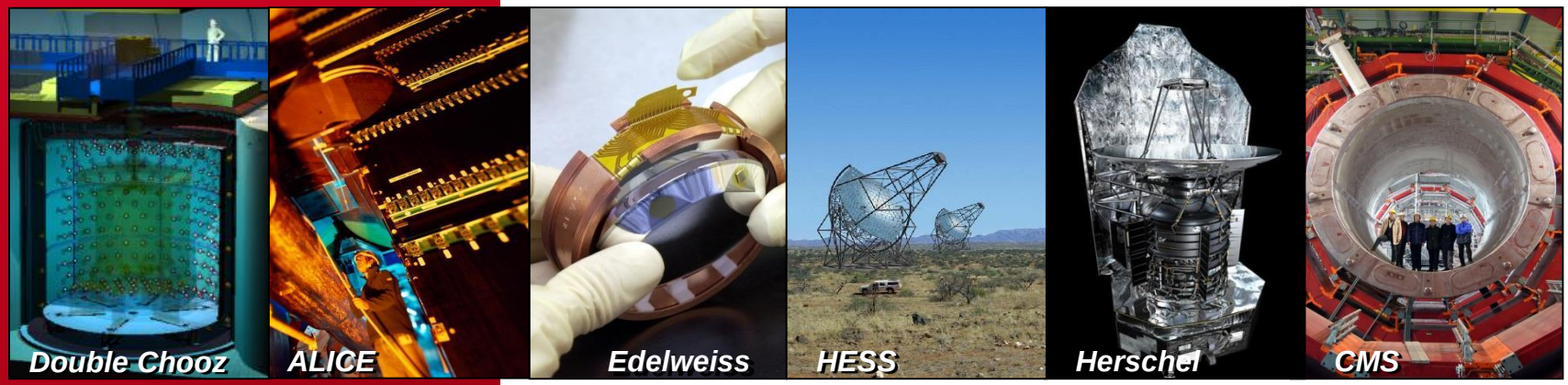
DE LA RECHERCHE À L'INDUSTRIE

DoTPiX , nouveau concept de détecteur pixel pour la physique des particules



Déchiffrer les rayons de l'Univers

Nicolas Fourches , IRFU, Charles Renard, C2N, Geraldine Hallais,C2N, Eric Imbernon, LAAS, Antoine Barbier, IRAMIS

Centre DE Nanosciences & DE Nanotechnologies

11th October 2022

DoTPiX , NOUVEAU CONCEPT DE DÉTECTEUR PIXEL POUR LA PHYSIQUE DES PARTICULES

- **FOREWORD:**
- **The principle of detection of photons using self-assembled Quantum Dots and a sensing transistor was first proposed by A. J. Shields et al. in 2000, Applied Physics Letters Vol 76, N°25,3673 although at low temperatures (4 K), next slide**
- **Quantum-Dot based detectors for single low energy photon counting were analyzed in 2005 , C. Blakesley, et al., Phys.Rev.Lett. 94,067401 52005) (Resonant tunneling structures)**
- **See also G. Yusaa and H. Sakaki , Appl. Phys. Lett. 70 (3), 20 January 1997, 345, at relatively low temperature (LN_2=77 K) and with III-V materials**

We will focus on pixel detectors as nuclear and particle physics detectors. We wish to operate them near room temperature. The aim is to detect high energy charged particles

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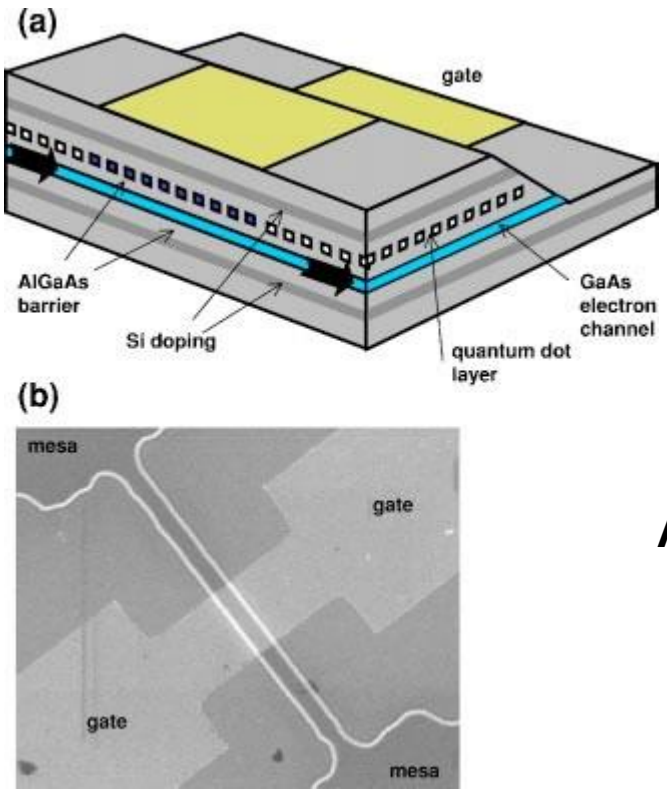


At 4 K

FIG. 1. (a) Schematic of the quantum-dot FET structure. Application of a positive bias to the gate charges the underlying dots with electrons, which limits the mobility of the adjacent electron channel. Single photons liberate a trapped electron, via capture of a photoexcited hole, resulting in a detectable increase in the conductance of the electron channel. (b) Scanning electron microscope image of the gate region for a FET with a 2-µm-wide mesa and 4-µm-long gate.

Detection of single photons using a field-effect transistor gated by a layer of quantum dots

A. J. Shields[a] and M. P. O'Sullivan[b]
Toshiba Research Europe Limited, 260 Cambridge Science Park, Milton Road, Cambridge CB4 0WE, United Kingdom

I. Farrer and D. A. Ritchie
Cavendish Laboratory, University of Cambridge, Madingley Road, Cambridge CB3 0HE, United Kingdom

R. A. Hogg, M. L. Leadbeater, C. E. Norman, and M. Pepper[b]
Toshiba Research Europe Limited, 260 Cambridge Science Park, Milton Road, Cambridge CB4 0WE, Uinited Kingdom

Received 13 March 2000; accepted for publication 26 April 2000

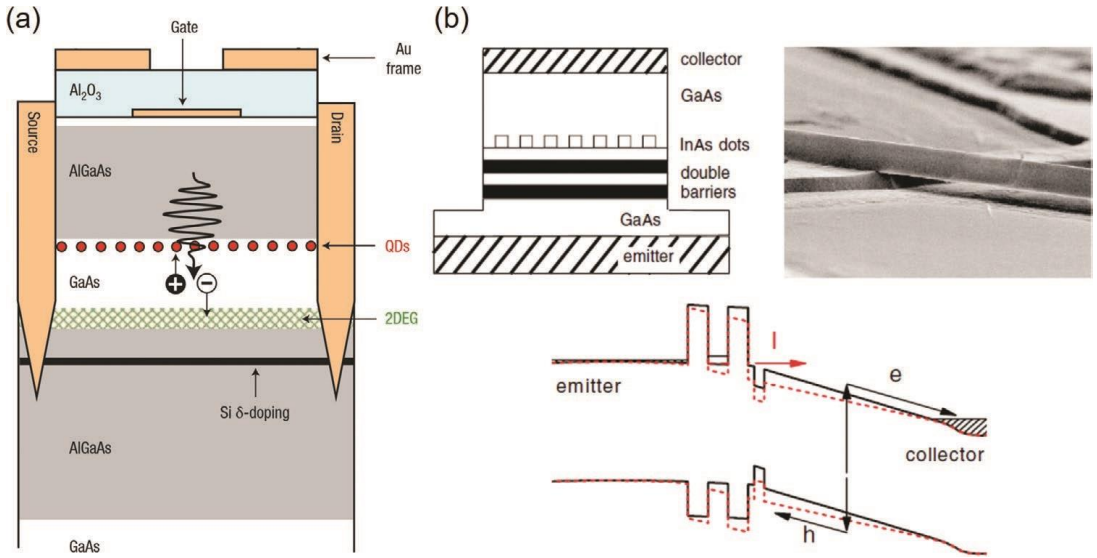
We demonstrate that the conductance of a field-effect transistor FET. gated by a layer of nanometer-sized quantum dots is sensitive to the absorption of single photons. Rather than relying upon an avalanche process, as in conventional semiconductor single-photon detectors, the gain in this device derives from the fact that the conductivity of the FET channel is very sensitive to the photoexcited charge trapped in the dots. This phenomenon may allow a type of three-terminal single-photon detector to be developed based upon FET technology. © *2000 American Institute of Physics.* @S0003-6951~00!01525-4#

Emerging Single-Photon Detectors Based on Low-Dimensional Materials

DOI: 10.1002/smll.202103963

http://www.small-journal.com/

Hailu Wang, Jiaxiang Guo, Jinshui Miao, Wenjin Luo, Yue Gu, Runzhang Xie, Fang Wang, Lili Zhang, Peng Wang, and Weida Hu**



Resonant tunneling structures

Figure 5. 0D quantum dot-based SPDs. a) 0D QDFETs for single-photon detection. Reproduced with permission.[16] Copyright 2007, Nature Publishing Group. b) 0D quantum dot-based SPDs dominated by resonant tunneling current. Reproduced with permission.[15] Copyright 2005, American Physics Society

1. What are pixel detectors , for particle and nuclear physics ?
2. What are they meant for ?
3. Which technologies are used up to now
4. Particle detection : the sensing element and the readout
5. Physical principles (ionizing and generation of carriers, light detection : scintillators)
6. Where are the challenges for the materials used ?

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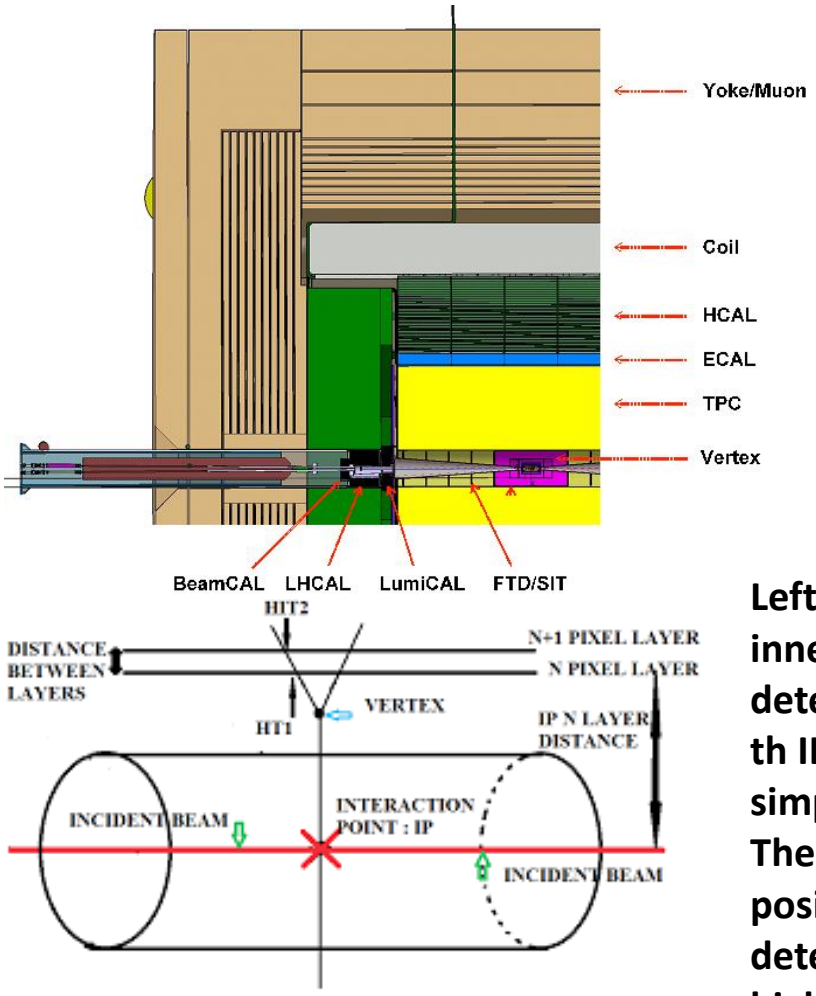
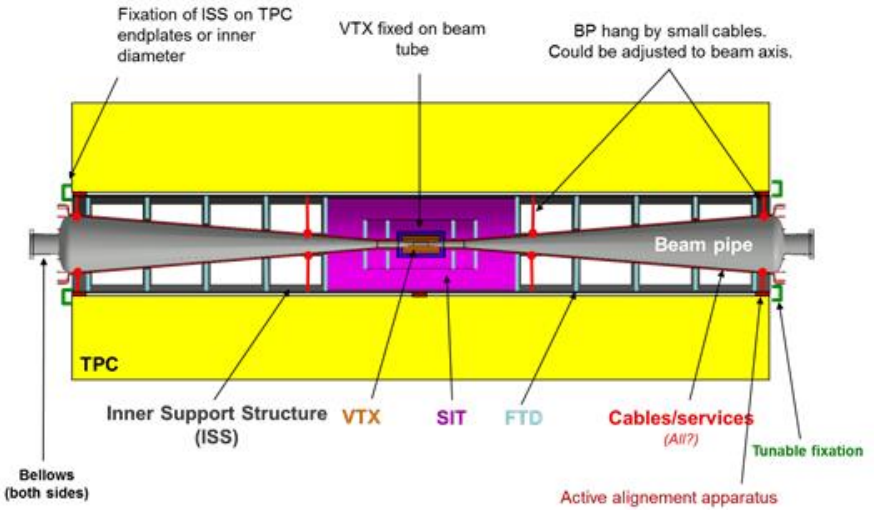
ILD INTERIM DESIGN REPORT





Left : outline of the inner pixel (Vertex) detector planned for th ILC. On the right simplified operation. The pixel detector is a position sensitive detector with a very high granularity of sensing elements

View of the proposed ILD (International Large Detector) , the vertex and the silicon tracker are a tiny par of the detector ensemble (up left , cut view of the whole detector and up right , zoom on the inner detector

DoTPiX , NOUVEAU CONCEPT DE DÉTECTEUR PIXEL POUR LA PHYSIQUE DES PARTICULES

- **Future accelerator based experiments**
- **ILC (e+e-)with two detectors : ILD and SiD**
- **FCC and CEPC with their detectors these are circular concepts and all are e+e- colliders**
- **Most are oriented towards the Higgs or Z-W factories concept**
- **Other include LHC developments and Electron-Ion colliders**

- **For the long-standing ILC project : the detectors should comply with the time structure of the beam**

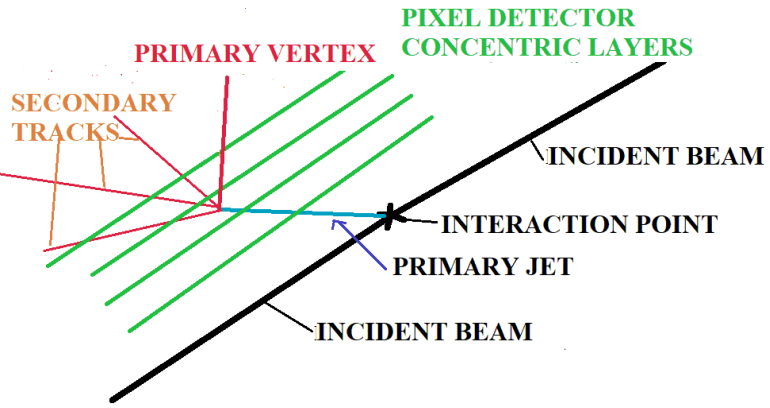
➢ **200 ms period with 1 ms of particle bunch. The bunches are separated by 199 ms**

➢ **Specific design of the detector and readout (see the following review : "Vertex detector R&D status" , Akimasa Ishikawa, Marcel Vos, Auguste Besson ,ILD group meeting 2020)**

Pixel Detector

a few cm

Giacomo Contin et al. https://doi.org/10.1016/j.nima.2018.03.003 This is the STAR VTX detector at RHIC (Relativistic Heavy Ion Collider) , CMOS maps sensors



IP is the point where the two beams collide, with a huge number of particles created per unit time

For newcomers: the pixel detector is used for the detection of primary charged particle very close to the interaction point.

- For this purpose the detector is made of concentric detecting layers (cylinders)
- The closest layer distant of a few centimeters from the interaction point
- As shown on your left the primary particle can decay into other particles (charged or not)
- With several concentric layers it is possible to detect the point where the particles imping and then then to reconstruct their trajectories and hence the vertices (as shown on the left).We need a dense array of pixel for precision.
- We have to implement a detector with many layers of a length large enough to cover the angular dependence of the primary particle momentum (azimuth)

INNER PIXEL DETECTOR (VERTEX DETECTOR)

Retrospect : pixel detector instead of strip detectors (xy strips)

Up to now the LHC has implemented a pixel detector in the ATLAS , CMS and other experiments:

- **There are based on hybrid silicon pixels with a silicon chip readout linked by a bump-bonding technique**
- **The other technologies are DEPFET (Depleted Field Effect Transistor, implemented on BELLE II experiment , 2020) and CMOS (still based on silicon) that is monolithic.**
- **Usually the pixels had a 100 µm x 50 µm) size in mature experiments**

Silicon is dominant : however there are some alternative materials

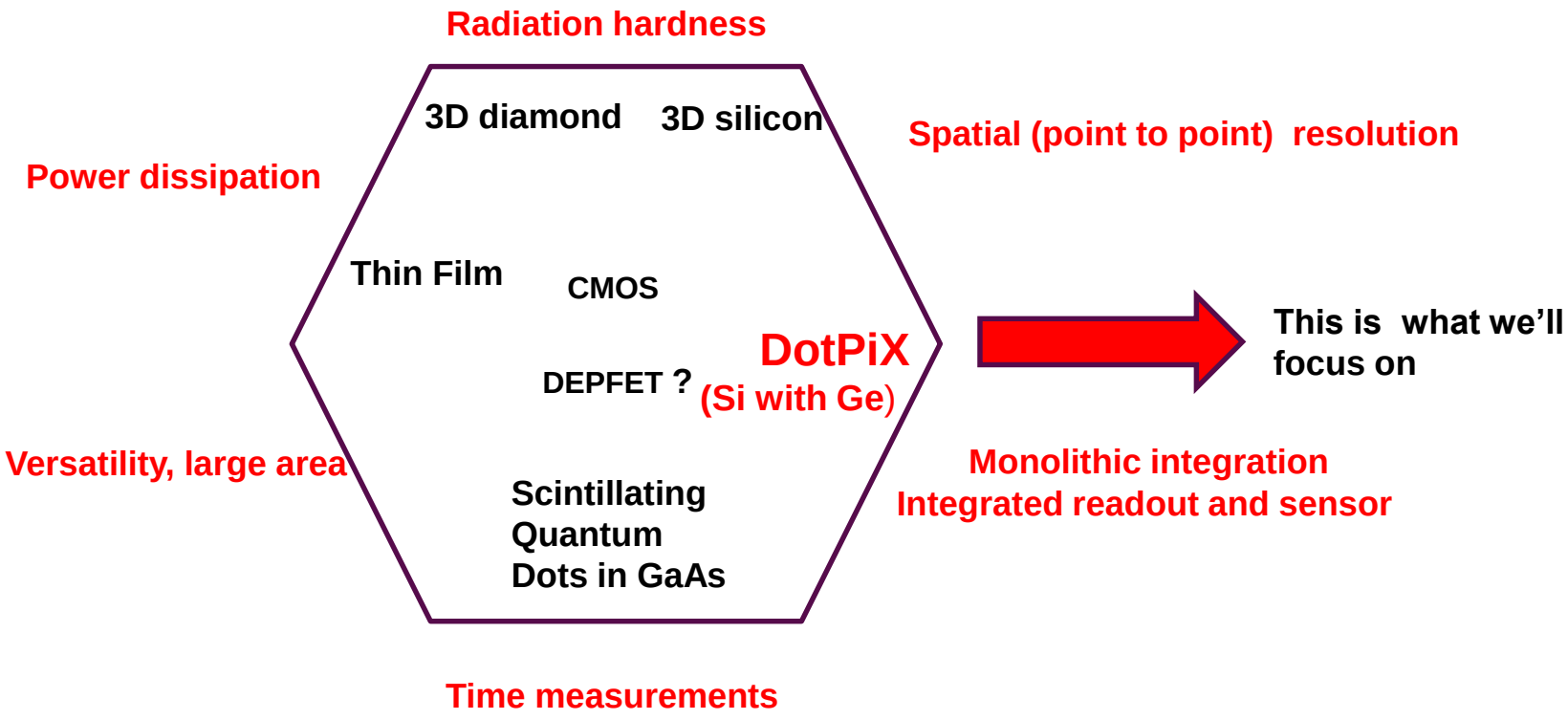
Constraints imposed on these detectors and the electronic readout :

1. **Low power per unit surface, to limit the operation temperature**
2. **High detection yield**
3. **High readout and detection speed (timing measurements)**
4. **Excellent (pointwise) spatial resolution, the size of the pixel should be small**
5. **High radiation hardness**

1. **High resistivity detector material, high bandgap**
2. **Significant number of e-h pairs created by unit length : n-h ~ (dE/dx)/e high**
3. **High electron and hole mobility for the detector material and readout**
4. **Small size means excellent material processing**
5. **Reduced defect introduction rate (defect concentration/integrated flux), low leakage current, use of adequate small pitch electrodes , deep submicron photolithography**

DoTPiX , nouveau concept de détecteur pixel pour la physique des particules

- Among others : 5 technologies identified (Snowmass 2021) for R&D : Novel Sensors for Particle Tracking: a Contribution to the Snowmass Community Planning Exercise of 2021, arXiv preprint arXiv:2202.11828
- The readout is also critical…
- Attempt to classify …

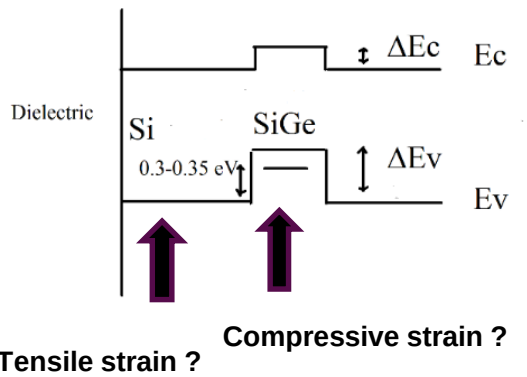


- The readout: electronic that reads out the signal from the pixel detectors.
- The signals from the pixel detectors are now mostly read out by µelectronic chips (ROC). One ROC for a few pixels is often the case. Front end readouts are necessary for hybrid-pixel detectors.
- Radiation hardness are prerequisites in all cases
- Power consumption is always , thermal dissipation
- Some key figures : ~ 10^{15} 1MeV neutron equivalent per cm2 for the LHC in term of Non Ionizing Energy loss.
- And 1 MGy for ionizing irradiation
- E.g. use of SOI (DMILL , 1990's) and small feature size rad-tolerant CMOS processes
- A lot of functionalities per ROC a sought, now timing measurements are in the pipeline
- But as with pixels optimizing is not possible when all requirements are to be met. This is true for the ROC , in order to limit complexity
- Specifications split between :

1. High granularity , low area pixels
2. High speed
3. And radiation hardness (constraints on the gate oxide , field oxide and the process depends on material and geometrical issues . Ionizing irradiation . See: Total Dose and Dose Rate Effects on Some Current Semiconducting Devices , Nicolas Fourches https://www.intechopen.com/chapters/32115
4. However trends to small transistors helps (Deep Submicron) change the landscape favorably

DoTPiX , NOUVEAU CONCEPT DE DÉTECTEUR PIXEL POUR LA PHYSIQUE DES PARTICULES

- For improved spatial resolution and monolithic integration we propose the DoTPiX (CEA-IRFU)
- The device finds its origins in the DEPFET and CMOS (MAPS) pixels
- It is designed to be fully CMOS compatible, and the pixel itself can be reduced to one MOS equivalent device, this means ultimate size reduction
- The name DoTPiX is chosen so that it may reduce its buried gate to a single quantum dot
- For the time being we'll consider a quantum BOX (3D instead) , it then be a quantum well based device (we use a GeSi buried layer with Ge concentration higher than 75%)

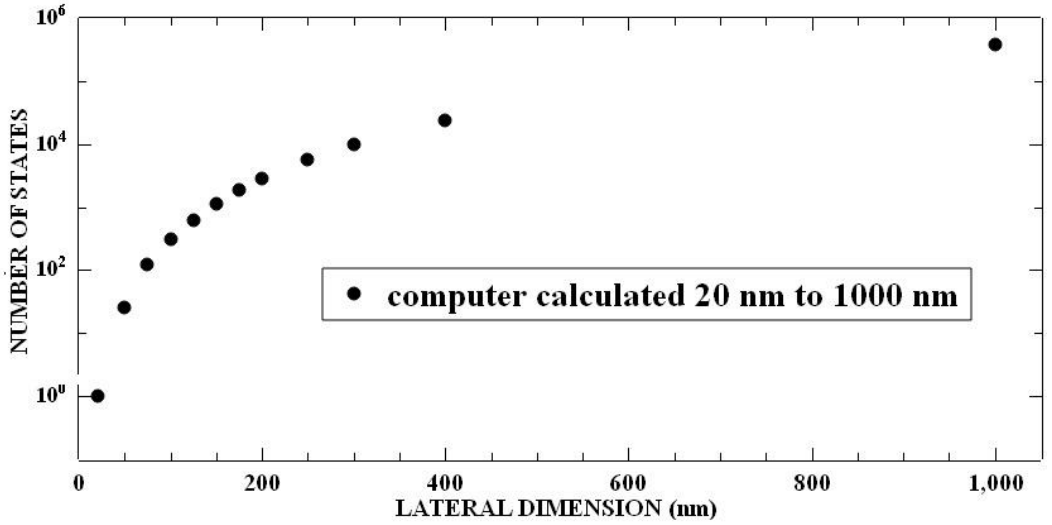


- In the conditions where the SiGe is in compressive strain or relaxed
- A quantum well for holes is present. It is better to have a compressively strained SiGe layer than an relaxed one (See D.J. Paul paper 2004)

Number of bound states in the well : $n=2\pi \frac{l_w}{h}\sqrt{\frac{(m^*V)}{2}}$

l_w is the length of the well m* the effective mass (Ge ,Si) V the potential depth

In a cubic box it could be approximated by : $n=\left((2\pi)^3 \frac{V_w}{h^3}\sqrt{\frac{(m^*V)}{2}}^3\right)$ the volume is V_w



- Number of bound states for a given trial solution , for a cubic quantum box , note that for a=20 nm there is only one bound state
- This was done with a home made computer program in Scilab
- Improvement with respect to the previous formulas for a 0.5 eV deep Quantum Box

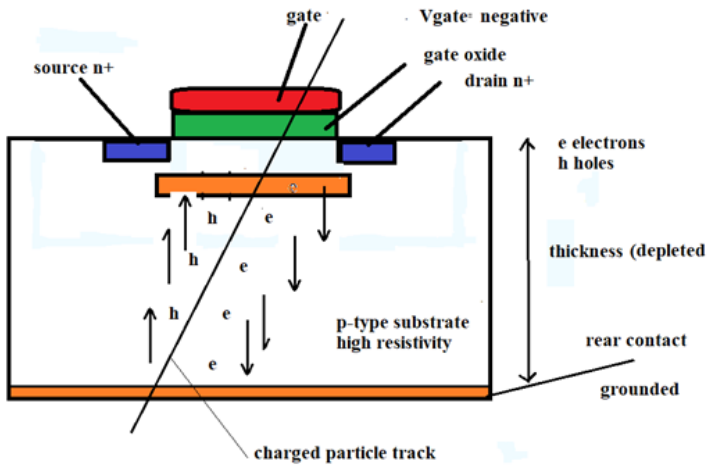
For a parallelepiped (cuboid) structure we obtain with a modified computer program, with a 0.5 V deep quantum box , for one solution family

1. a= 20 nm , b =100 nm and c =1000 nm , 819 states (without degeneracy)
2. a=20 nm , b=400 nm and c=1000 nm , 3276 states (without degeneracy)

- There are other solutions to be accounted for but this is still satisfactory.
- The number of electron-hole pairs created by a MIP is of the order of 800 if we assume a 10 µm active depth (in which all the holes drift towards the buried gate

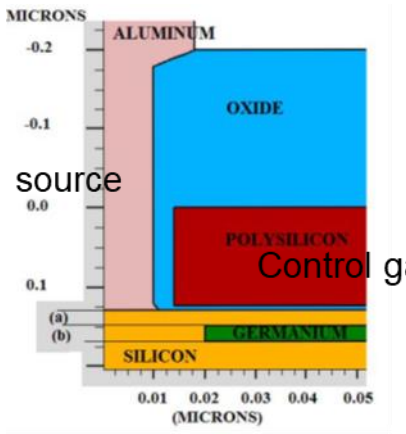
DoTPiX , NOUVEAU CONCEPT DE DÉTECTEUR PIXEL POUR LA PHYSIQUE DES PARTICULES

- Device simulations , general simulations



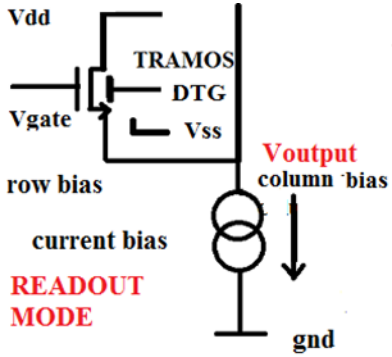
The device is based on :

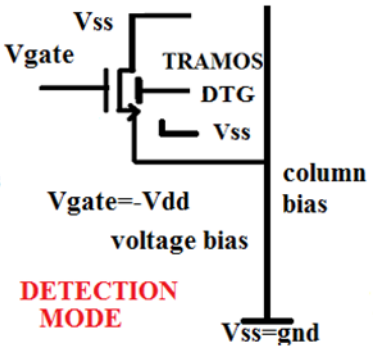
1. **A n-channel MOS structure**
2. **With drain source and an uppercontrol gate**
3. **A buried sensing gate that can trap and localise holes and modulate the source to drain current**

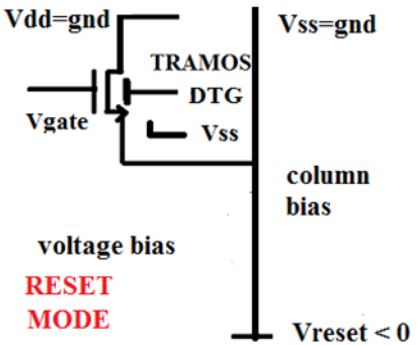


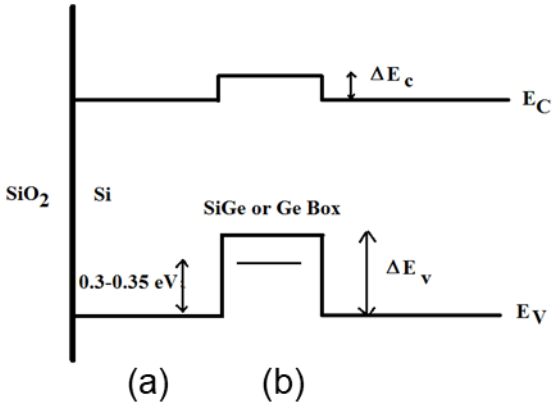
Bulk thickness ~ 2 µm for simulations

- The buried Ge gate is 20 nm thick for a 1 micrometer width



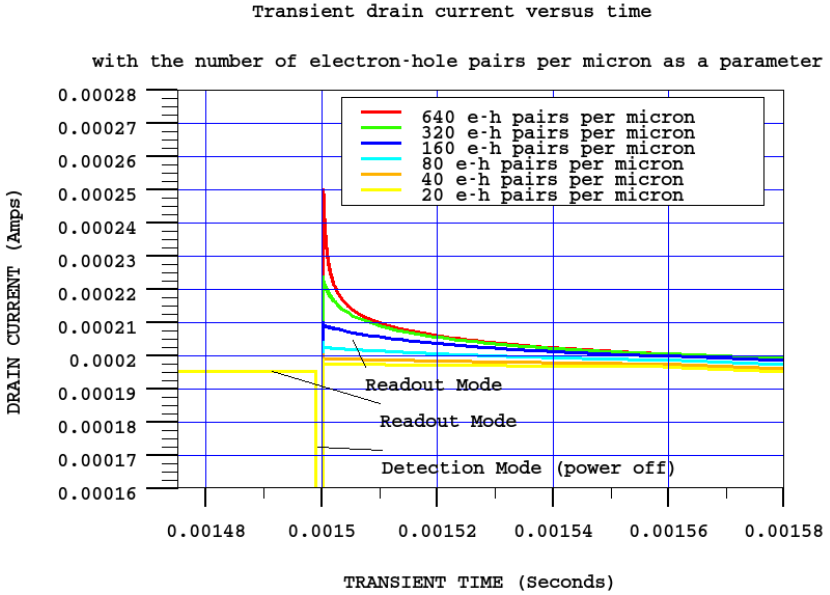


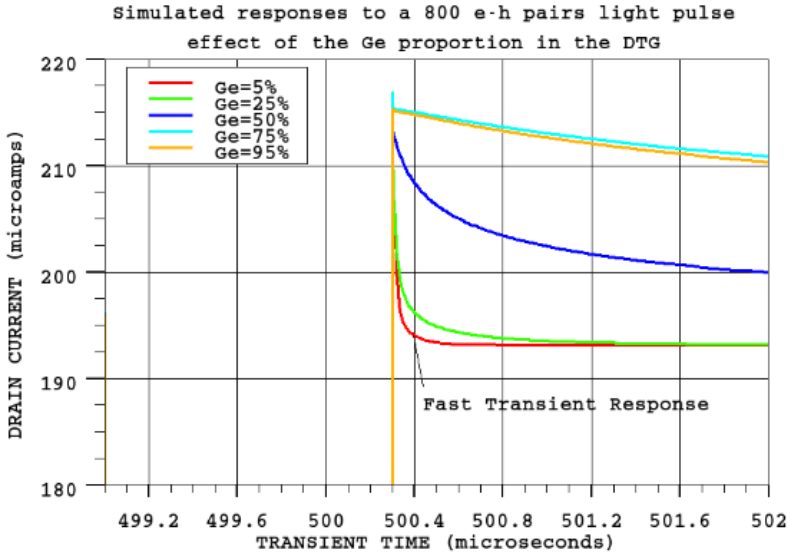




Description of the DoTPiX

- Proposed in 2017, derived from another structure (TRAMOS 2010) : goal ultimate point to point spatial resolution (~ 1µm) , See : N. T. Fourches, "Ultimate Pixel Based on a Single Transistor With Deep Trapping Gate", IEEE Trans. on Electron Devices 64, pp. 1619-1623 (2017). https://doi.org-98/10.1109/TED.2017.2670681
- We have a 100 nm x 20 nm x 1000 nm volume quantum box (Carrier lifetime < 1ns , high readout drain current)
- The device operates adequately with device simulation software when ionizing tracks are introduced. The quantum effect are introduce simply with density gradient model.





Proof of the principle is validated as far as we can trust simulation…

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L (µm) Gate Length	Buried Gate transconductance (µA/V)	Buried Gate-Upper Gate capacitance	ΔV (buried gate) for 80 e charge deposited	ΔV (source) for 80 e charge deposited and a 5 kohms source resistance	Conversion Factor in µV/e (source of the transistor) 5 kohms source resistance
1 µm	52	5.31 fF	3.01 mV	785 µV	9 µV/e
0.5 µm	60	2.65 fF	6.00 mV	1.56 mV	19.5 µV/e
0.25 µm	55	1.32 fF	12.0 mV	3.3 mV	41.25 µV/e
0.1 µm	60	0.531 fF	24.1 mV	7.23 mV	90.4 µV/e
Gate width 1µm	Simulated using Silvaco ATLAS	Gate width 1µm	Silvaco ATLAS	Silvaco ATLAS simulations	Silvaco ATLAS , Gate width 1µm simulations

Pixel Size (μm^2) X Thickness (µm)	E_{avg} (keV)	E_{MPV} (keV)	Ratio avg (%) (E_N/E_p)*	Efficiency (E_{Th}= 500eV)
1 * 1 *10	3.28	2.17	4.74	99.3
1 * 1 * 20	6.76	4.89	4.9	99.82
1 * 1 * 30	10.86	7.84	-	>99
1 * 1 * 40	14.36	9.68	-	>99
1 * 1 * 50	17.98	13.21	-	>99
10 * 10 * 10	3.26	2.15	0.994 1	99.9
10 * 10 * 50	16.68	13.17	2.08	>99
10 * 10 * 100	34.76	24.3	2.35	>99

Electrical characteristics forecast

https://arxiv.org/ftp/arxiv/papers/1602/1602.00263.pdf

See N. Fourches et al., "Limits in point to point resolution of MOS based pixels detector arrays," Journal of Instrumentation, vol. 13, pp. C01011, Jan. 2018.
and V. Kumar report 2016

➡ **Particle Detection characteristics**

The thickness can be reduced to 10 µm
See 2009 paper "Device simulations… :
https://ieeexplore.ieee.org/abstract/document/5341433

DoTPiX , NOUVEAU CONCEPT DE DÉTECTEUR PIXEL POUR LA PHYSIQUE DES PARTICULES

Size (lateral dimensions)	Resolution (first order binary)	Area	Number of pixels Np in an array	Number of hits per unit area and per second	Address length in bits N=log(Np)/log(2)	Data flow in bits/second
1x1 µm x µm	~ 1 µm	10 cm squared	10^9	N	30	30 x N
10x1 µm x µm	~ 3 µm	10 cm squared	10^8	N	27	27 x N
10x10 µm x µm	~ 10µm	10 cm squared	10^7	N	24	24 x N

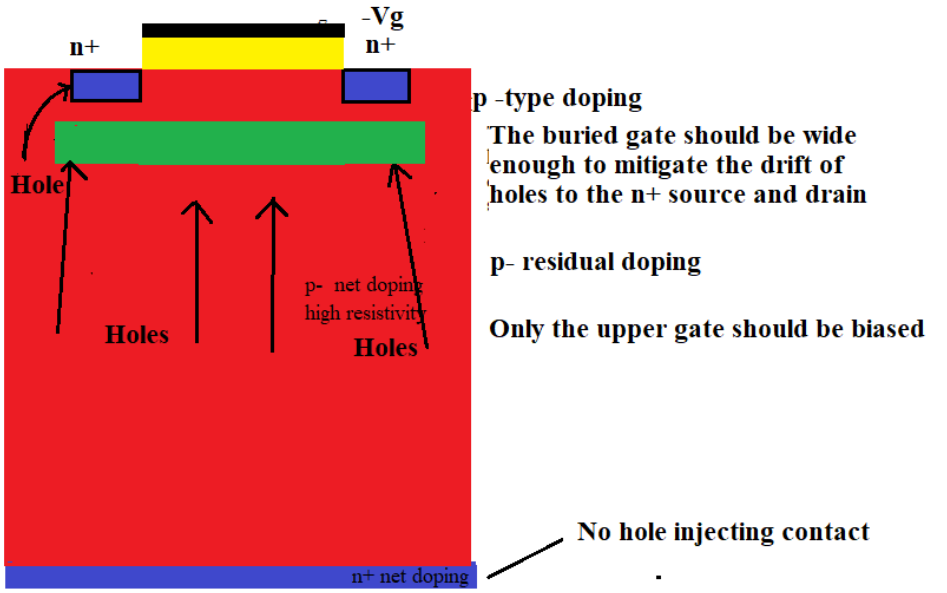
N. Fourches et al., "Limits in point to point resolution of MOS based pixels detector arrays," Journal of Instrumentation, vol. 13, pp. C01011--C01011, Jan. 2018.

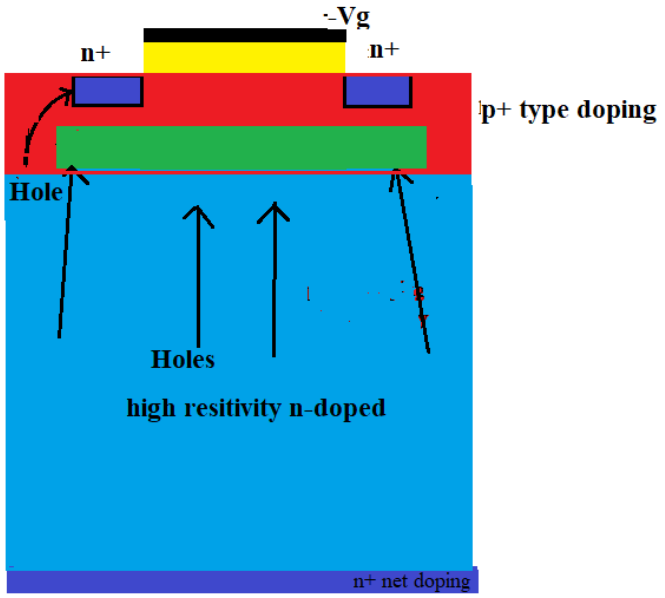
- **The data flow depends more on the event rate than on the density of pixels**
- **This will simplify the readout and transfer of the data by the on-chip CMOS electronic**

What can we expect from the DoTPiX

- High spatial resolution, due to the small size of the pixel
- No need to make pixel clustering and use center of gravity techniques
- Simpler offline analysis
- No power dissipation in detection mode. Only the upper control gate and the backside substrate are biased
- Leakage currents can be mitigated
- Ability to resolve hits from different particle tracks
- Thence, improved multiplicity rejection (reduced number of multiple hits in a single pixel
- Power dissipation can be mitigated by the adequate choice of array size and readout frequency
- The DoTPiX is CMOS process compatible !!!

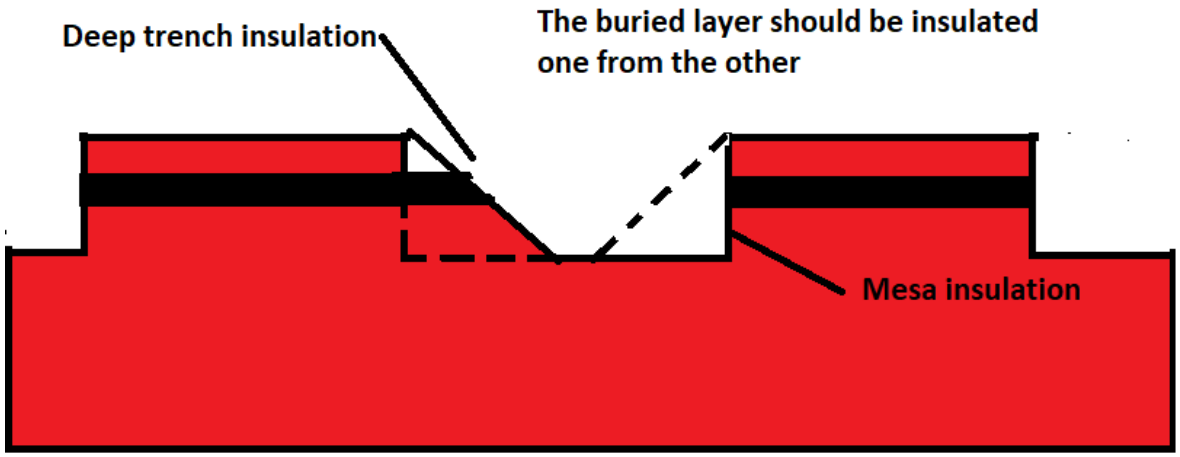
- **Issues in the operation of the DoTPiX :**





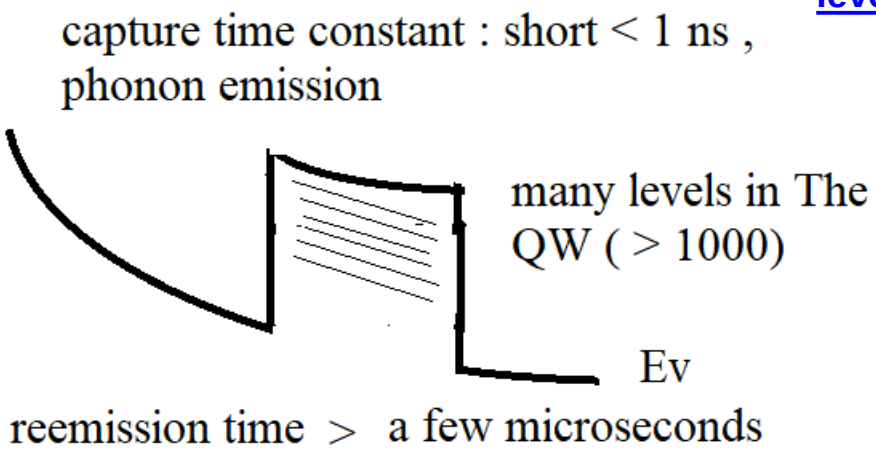
- **High resitivity substrates should be used for the DotPiX**
- **Best type (n or p) should be investigated**
- **Simulations show that it is ok for p-type slightly doped**

Possible issues :



Not to scale

- **Whatever is chosen the pixel should be set close to one other**
- **Field oxide with channel stop should be used between pixels**
- **This is necessary to prevent leakage current (source to drain)**
- **Insulation of buried layers one from the other**



- **We assume the holes behave like electrons**
- **The capture cross section should be calculated**
- **High spin orbit interaction**
- **Emission rates can be calculated**
- **Recent paper see right**

Deep-level spectroscopy studies of confinement levels in SiGe quantum wells

Irina V. Antonova,[1] Efim P. Neustroev,[2] Svetlana A. Smagulova,[2] Miron S. Kagan,[3,a]
Pavel S. Alekseev,[4] Samit K. Ray,[5] Nathan Sustersic,[6] and James Kolodzey[6]
[1] *Institute of Semiconductor Physics, SB RAS, 630090 Novosibirsk, Russia*
[2] *Yakutsk State University, 677000 Yakutsk, Russia*
[3] *Institute of Radio Engineering and Electronics, RAS, 125009 Moscow, Russia*
[4] *A.F. Ioffe Physico-Technical Institute, RAS, 194021 St. Petersburg, Russia*
[5] *Indian Institute of Technology, 721 302 Kharagpur, India*
[6] *University of Delaware, Newark, Delaware 19716, USA*

Received 24 April 2009; accepted 19 May 2009; published online 21 October 2009

The recharging of quantum confinement levels in SiGe quantum wells QWs was studied by charge deep-level transient spectroscopy Q-DLTS for Si/SiGe/Si structures with different Ge contents in the SiGe layer. The set of levels were observed as the different slopes in the Arrhenius plots for the same Q-DLTS peak in different temperature ranges. These activation energies were compared to the energies of quantum confinement levels in the QW calculated in frames of six-band model taking into account spin-orbit interaction and attributed to a thermally activated tunneling of holes from the SiGe QW. © *2009 American Institute of Physics*. doi:10.1063/1.3153974

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Up to now , simulations have shown the operational capabilities of the device.. but there are still issues.. (from material engineering and sciences)

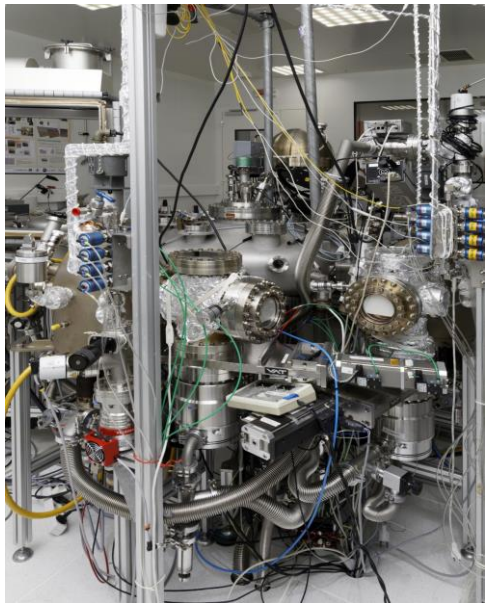
- **Modulation of the source-drain current in read mode. No power dissipated in detection mode (because of the device is operated in the off mode) . Accumulation of holes in the buried Ge layer …**
- **Depth of the quantum well (Ge inner layer)..**
- **Reemission time (charge retention in the buried gate ??)…**
- **Bulk leakage current (injection from backside substrate)…**
- **Influence of temperature..**
- **Crystal growth issues in the Ge buried layer, no defect , constraints …**
- **Dielectric used in the MOS structure, low defect concentration and adequate interface with the Silicon channel**

Methods :

- **Ultra High Vaccum Chemical vapor Deposition (UHV-CVD) is used for the growth of the Si (20nm)/Ge(20nm) epitaxial layers on silicon substrate (with a Cluster Tools UHV-CVD-CBE and in situ characterization at C2N laboratory (UMR 9001 CNRS/Université Paris-Saclay)**
- **Reduction of surface roughness**
- **Capacitance transient (versus temperature) methods for the characterization of the Ge layer**
- **Use of a blocking layer at the backside**
- **Reduction of thermal budget for the Ge buried layer as well as for the dielectric (ionizing radiation effects)**

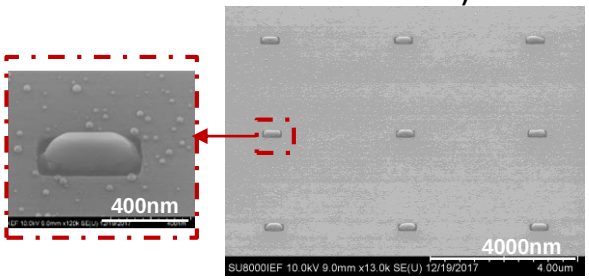
Growth epitaxial of the Si (20nm)/Ge(20nm) layers on silicon substrate by UHV-CVD : Preliminary results (credit C2N : internship R. Gourad)

➡ **Ge on Si integration challenge : High lattice mismatch between Si and Ge : 4.17% (threading dislocations formation and the Stranski-Krastanov 3D mode)**



Two solutions :

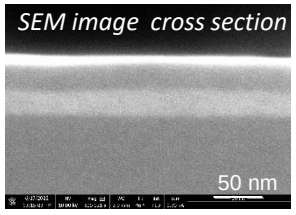
- **The Selective Epitaxial Growth (SEG) of localized Ge (GeH_4 gas used) layers on patterned bulk silicon wafer :** small nucleation area size enables the relaxation of the mismatched material without emission of misfit dislocations)

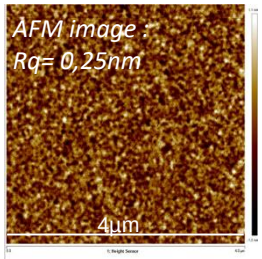


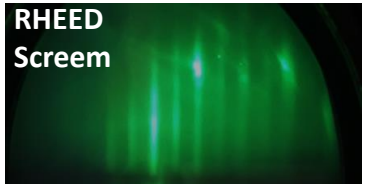
complete filling of Ge in openings of 300nmX100nm

- **The Full-wafer epitaxial Growth of Ge layer (GeH_4 gas used) at low temperature to avoid relaxation (~ 330 °C)**

➢ The roughness of the 2D Ge layer :
- ✓ during epitaxy with RHEED in situ
- ✓ ex-situ by SEM and AFM imaging.







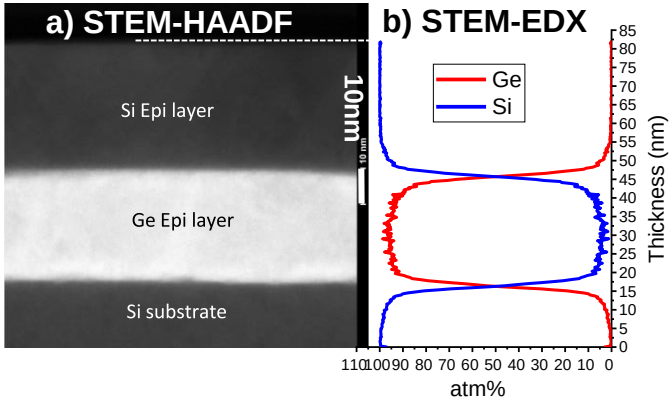
➡ **Epitaxial growth challenge of a Silicon capping layer on the top of the Ge layer**

- **low temperature epitaxial growth (SiH4 gas used) to avoid intermixing (~ 550 °C)**

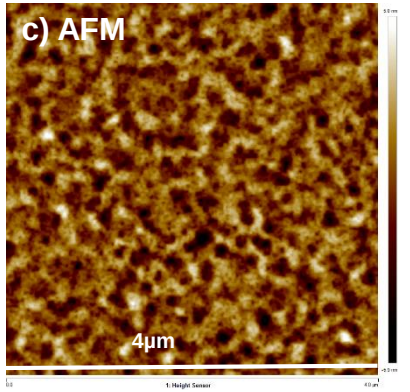
Successful growths epitaxial of the Si (25nm)/Ge(30nm) layers on silicon substrate by UHV-CVD

a) High Angle Annular Dark Field Imaging shows the epitaxial Ge layer (bright contrast) and the epitaxial Si layer (dark contrast)

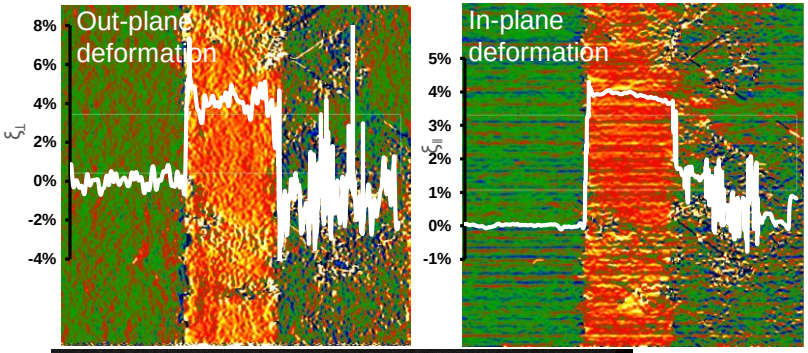
b) STEM-EDX profil shows a very high Ge concentration with abrupt interfaces



c) AFM image estimates the roughness at Rq=1,56nm

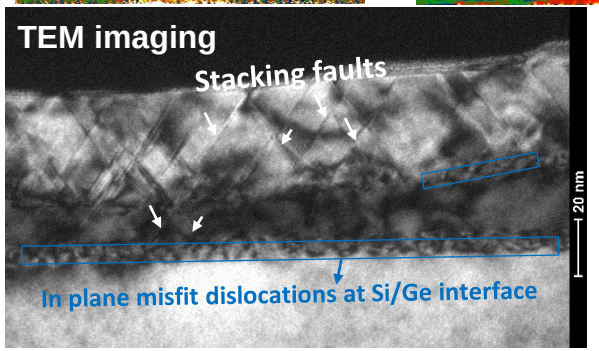


Geometrical Phase Analysis (GPA) shows :
-The Ge layer is fully relaxed out-of-plane and in-plane with about +4% (red area) deformation respect to silicon.
- The Si layer is slightly deformed out-of-plane in tension about -1% and decrease his in-plane compression deformation about +1%



Issues

- **We have to reduce the stacking faults (mainly in Si layer) due to out-plane dislocations in the Ge/Si interface (partial-not total crystal lattice relaxation)**



- **We have to estimate the effects of the thermal treatments post epitaxy → evaluate the intermixing**

- **We have a DLTS experiment set-up now, last checks and tests are under way**
- **Interface and defects studies (see picture below)**
- **The software was initially developed for EDELWEISS characterizations and was not fully used for this purpose.**
- **Other studies with the IRAMIS/SOLEIL : XRR X Ray Reflectometry with intense X ray source to investigate the evolution of the buried Ge layer with annealing temperature**

Gate dielectrics (from Gang He, Critical Reviews in Solid State and Materials Sciences, 37:131–157, 2012)

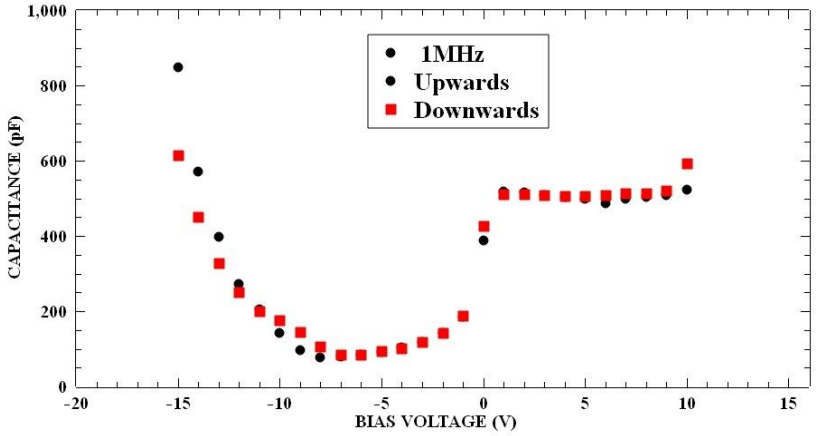
TABLE 1
Static dielectric constant, experimental band gap and conduction band offset on Si of the candidate gate dielectrics

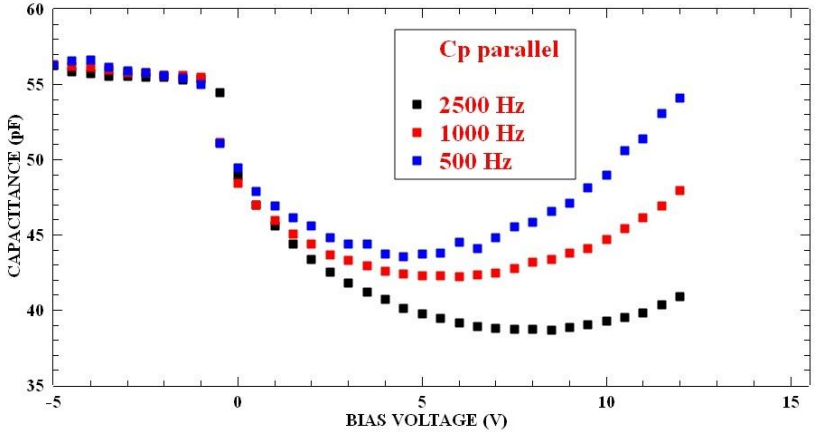
	K	Gap (eV)	CB offset (cV)
Si		1.1	
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8 (not ALD)
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8
La_2O_3	30	6	2.3
Y_2O_3	15	6	2.3
a-$LaAlO_3$	30	5.6	1.8

(Reprinted with permission from Robertson et al.[15] Copyright 2000: American Institute of Physics.)

. The importance of the low temperature for the epitaxial growth in order to have a good quality layer imposes limitations of the CMOS processing of the epi-substrate especially on upper gate dielectric

- So, alternatives to classical thermal oxides are investigated :
  1. Results from the analysis of the gate oxide (55 nm) for the [+5,-5] voltage range show that a thickness of 10 nm is optimal.
  2. For a thermal wet oxidization for instance at 800 °C, it is necessary to have a 24 minutes duration to reach a 10 nm oxide thickness → Rapid Thermal Oxidization is an alternative.
  3. HfO_2 is another possibility. It would reduce much of the thermal budget (hence there will be only some annealing at the last process step). It is deposited by Atomic Layer Deposition (ALD) at 300°C under water gases or plasma O_2





- Example of a C(V plot on a HfO capacitor (~10nm) on chemical silicon oxide (~2nm) and on n-type doped silicon at 1MHz.
- n-type doped silicon at 1MHz. We are in the low frequency regime in the p-type case
- The MOS structure does not breakdown at +/-10 Volts applied to the gate
- The structure may exhibit interface states
- The EOT (equivalent oxide thickness) is approximately < 5 nm , from the capacitance data assuming identical area samples

Modern technologies use very thin gate oxides (2 nm) ?

See Radiation Hardness by Design Techniques for 1 Grad TID Rad-Hard Systems in 65 nm Standard CMOS Technologies , Gabriel Carpi et al. International Conference on Applications in Electronics Pervading Industry, Environment and Society pp 269–276

Irradiation results:

- **A few published studies on HfO2 (basically Chinese-Indian-Turkish studies)**
- ➢ **The very best : flatband voltage shift of 0.5 V to 1 V at 1-5 Mrads**
- ➢ **High concentration of O vacancies**
- ➢ **Seems as difficult as with SiO2**
- ➢ **Low thicknesses 6 nm of HfO2 is good**

We are now investigating : Interface states : conductance method , DLTS, CV stretchout and other things on the HFO2 capacitors and effect of high temperature processing on the Ge layers

- **We'll implement a small n-channel transistor array on , first silicon substrates and on epitaxial substrates to test the process and devices (LAAS)**
- **We'll try to characterize the quantum box (valence band offsets) using DLTS,, other techniques can be considered**

WHAT ELSE :

- **R&D on this pixel design is running, but needs some support from all the communities**
- **Many bottlenecks have been overcome but much has still to be done**
- **Detection elements is one thing but we always have to consider the readout (especially in monolithic structures)**
- **The supporting mechanics is always an issue as the cooling**

Other R& D on pixels with quantum dots :

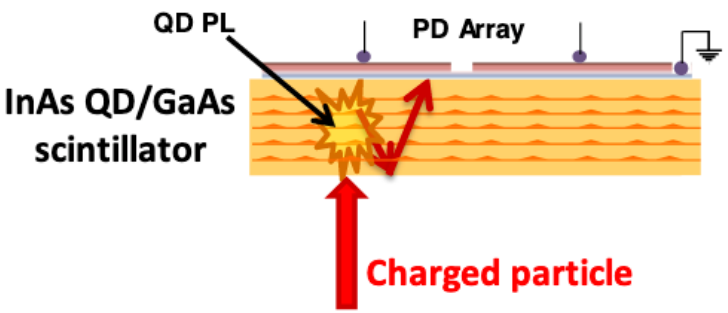
- **Use Qdots for they scintillation properties**
- **Fast pixel detectors**
- **The readout of the these detectors should be fast**
- **III-V detectors and readout**

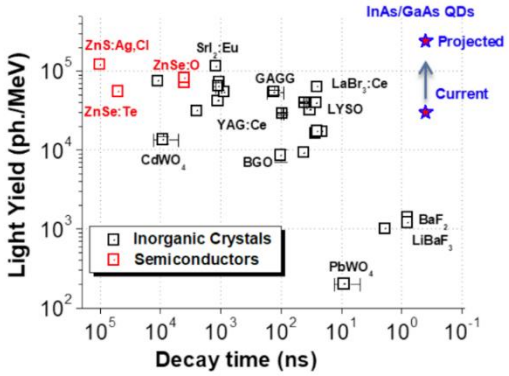
with input from some Snowmass 2022 Contributors :
Novel Sensors for Particle Tracking a Contribution to the Snowmass Community Planning Exercise of 2021

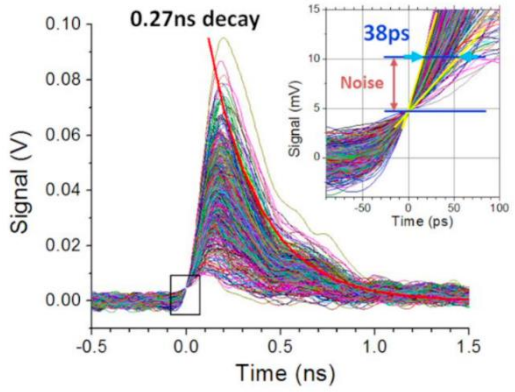
OTHER QD PROPOSED DETECTORS

Scintillating QD are in the pipeline

- Optimized for timing measurements (Credit to T. Mahajan, A. Minns, V. Tokranov, M. Yakimov, S. Oktyabrsky, SUNY College of Nanoscale Science and Engineering, Albany, NY, USA)
- High granularity and use of GaAs electronic on the same substrate…
- See : S. Oktyabrsky et al., Integrated semiconductor quantum dot scintillation detector: Ultimate limit for speed and light yield," IEEE Trans. Nucl. Sci. 63 (2016) 656-663
- K. Dropiewski et al , Ultrafast Waveguiding Quantum Dot Scintillation Detector, Nuclear Instruments and Methods in Phys. Res. Sec. A: Acc., Spectr., Det. and Ass.Equ. Vol. 954, 21 February 2020, 161472 https://doi.org/10.1016/j.nima.2018.10.150







- This talk is overview we have focused on a particular development
- Other designs may be considered for the future
- The improvements should always be driven , by spatial resolution and time measurements
- Benchmarking with other pixel/detector should be made (as for the DEPFET which is an ancestor of the DoTPiX)
- The radiation hardness is a common constraints on many on-accelerator experiments

Other applications for such pixel detectors:

- **Imaging in the medical field, high quality imaging due to the high granularity**
- **Low dose imaging due to the sensitivity**
- **Visible light and IR imaging for the same reasons**

Summary

- **Vast amount of development is still necessary for either field**
- **E.g. : Pixels detectors mechanics and power management data flow management**

Thank you for your attention

Contributors:
Nicolas Fourches , IRFU
Charles Renard ,C2N
Geraldine Hallais,C2N
Eric Imbernon, LAAS
Antoine Barbier,IRAMIS

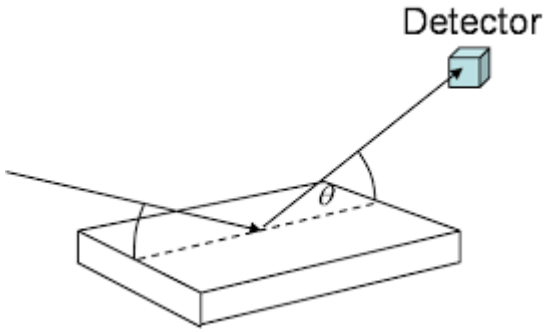
Commissariat à l'énergie atomique et aux énergies alternatives
Centre de Saclay | 91191 Gif-sur-Yvette Cedex

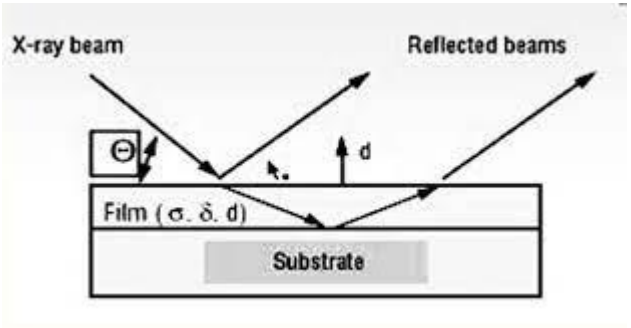
Etablissement public à caractère industriel et commercial | R.C.S Paris B 775 685 019

Tel : +33 1 69 08 xx xx – Fax : +33 1 69 08 xx xx

Direction de la Recherche Fondamentale
Institut de recherche
sur les lois fondamentales de l'Univers
Service

- The readout current : ~ 10 µA maximum ?
- The readout power : ~ 30 µW maximum ?
- The readout energy : ~ 30µW x 10 ns
- Equal to : 0.3 pJ per pixel
- Read every 10 µs >> 0.3 pJ/10 µs = 30 nW per pixel
- For 100 Mpixels per squared cm there is : 3 W this seems huge
- For the ILC there is the beam time structure :
- 1 ms/200ms =0.05 so the power is : 0.15 W/cm2
- There is margin and scope for improvements





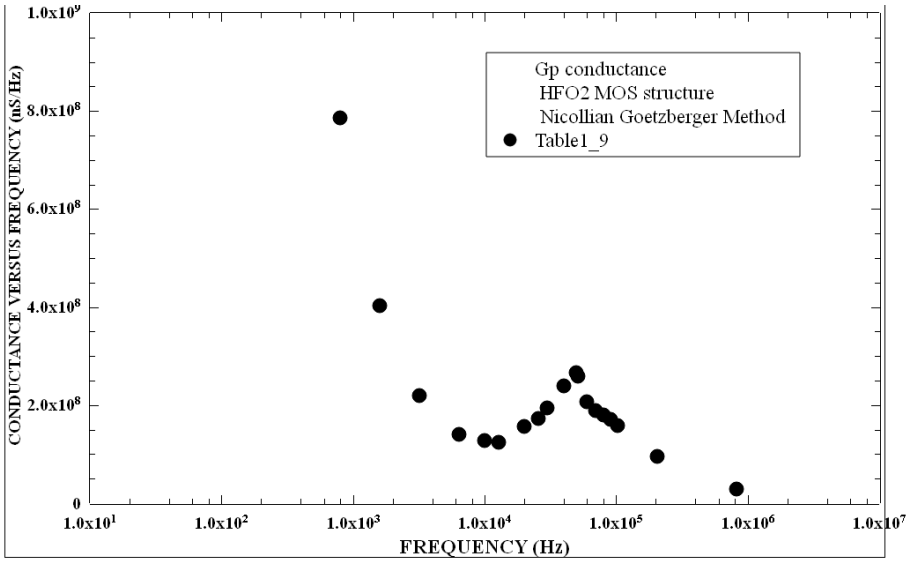
- XRR : X Ray Reflectometry
- Small incident angle X ray diffraction
- Bragg conditions for thin films
- Adequate for the study of very thin layers
- But needs high luminosity incident X ray beam (very low number of atomic planes)
- See above figures

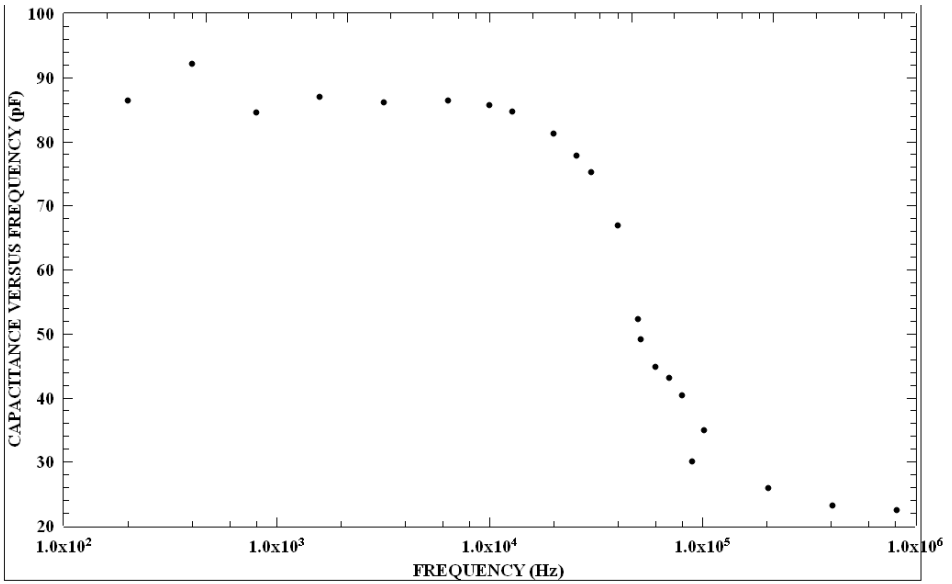
Layer	Radius in mm	Number of Bunchs Crossings and corresponding duration	Pixel Occupancy In brackets (25 x 25 µm x µm pixels)
0	16	83 (30 µs)	0.53 % (3.33 %)
1	17.9	83 (30 µs)	0.3 % (1.90 %)
2	37	333. (123 µs)	0.06% (0.40 %)
3	38.9	333 (123 µs)	0.053% (0.33 %)
0	//	2625 (1ms)	16.7%
1	//	2625	9.48%
2	//	2625	0.47%
3	//	2625	0.42%

Table 1: Updated from the letter of intent, International Large Detector, background improvements due to the reduction of the area of the pixel by a factor 625 [13] (page 32 ILD LOI). This occupancy value show that these pixels alleviate the need to have time stamping ability. We recall the time structure of the pixel. The LOI (Letter Of Intent) figures were based on a 25 µmx 25 µm sized pixel (MIMOSA 8 like) [14].

The operation of the pixel vertex detector at ILC strongly depends on the machine parameters. One should recall the beam parameters of the proposed ILC. The frequency is 5 Hz (200 ms period), with a pulse containing 2625 bunches separated by 369.2 ns, this gives a 0.969 ms beam pulse duration and a bunch length=300 µm. We have chosen to make a table similar to that of the Letter Of Intent [13] (Table 1).

LCWS 2021 , Beyond CMOS Sensors, N. Fourches et al.





- Gp/omega versus measurement signal frequency
- Interface states have a conductance behaviour
- Small resonance on HfO2